AN-1601 LM34917A Evaluation Board

1 Introduction

The LM34917A evaluation board, Figure 1, provides the design engineer with a fully functional buck regulator, employing the constant on-time (COT) operating principle. This evaluation board provides a 5V output over an input range of 8V to 33V. The circuit delivers load currents to 1A, with current limit set at ≅1.3A.

The board's specification are:

- Input Voltage: 8V to 33V
- Output Voltage: 5V
- Maximum load current: 1.0A
- Minimum load current: 0A
- Current Limit: ≅1.3A
- Measured Efficiency: 91.6% (V_{IN} = 8V, I_{OUT} = 400 mA)
- Nominal Switching Frequency: 1.5 MHz
- Size: 2.6 in. x 1.6 in. x 0.5 in

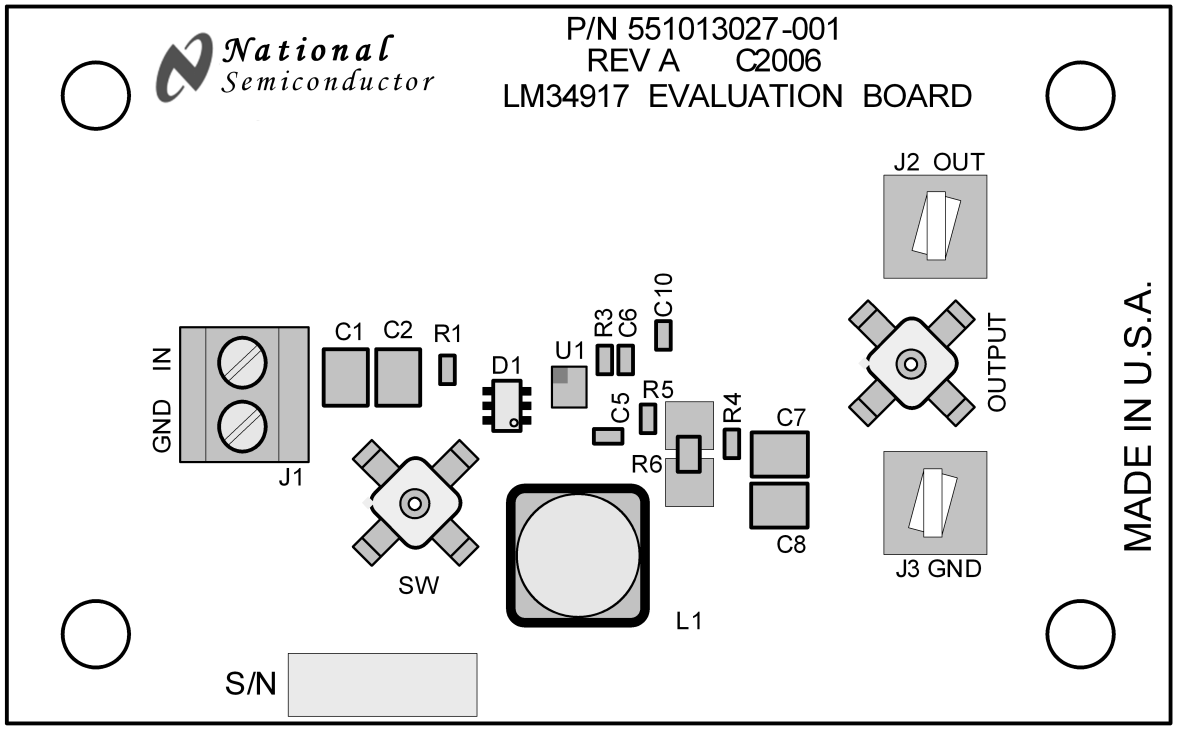

Figure 1. Evaluation Board - Top Side

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2 Theory of Operation

Refer to the evaluation board schematic in Figure 2, which contains a simplified block diagram of the LM34917A. When the circuit is in regulation, the buck switch is on each cycle for a time determined by R1 and VIN according to the equation:

$$t_{ON} = \frac{1.16 \times 10^{-10} \times (R1 + 1.4\ k\Omega)}{V_{IN} - 1.35V} + 100\ ns \quad (1)$$

The on-time of this evaluation board ranges from ≅510 ns at VIN = 8V, to ≅186 ns at VIN = 33V. The on-time varies inversely with VIN to maintain a nearly constant switching frequency. At the end of each on-time the Minimum Off-Timer ensures the buck switch is off for at least 90 ns. In normal operation, the off-time is much longer. During the off-time, the load current is supplied by the output capacitor (C7, C8). When the output voltage falls sufficiently that the voltage at FB is below 2.5V, the regulation comparator initiates a new on-time period. For stable, fixed frequency operation, a minimum of 25 mV of ripple is required at FB to switch the regulation comparator. The current limit threshold, which varies with Vin, is ≅1.4A at Vin = 8V, and ≅1.2A at Vin = 33V. Refer to the LM34917A data sheet for a more detailed block diagram, and a complete description of the various functional blocks.

3 Board Layout and Probing

Figure 1 shows the placement of the circuit components. The following should be kept in mind when the board is powered:

- When operating at high input voltage and high load current, forced air flow may be necessary.
- The LM34917A, and diode D1 may be hot to the touch when operating at high input voltage and high load current.
- Use CAUTION when probing the circuit at high input voltages to prevent injury, as well as possible damage to the circuit.
- At maximum load current (1A), the wire size and length used to connect the load becomes important. Ensure there is not a significant drop in the wires between this evaluation board and the load.

4 Board Connection/Start-Up

The input connections are made to the J1 connector. The load is connected to the J2 (OUT) and J3 (GND) terminals. Ensure the wires are adequately sized for the intended load current. Before start-up, a voltmeter should be connected to the input terminals and to the output terminals. The load current should be monitored with an ammeter or a current probe. It is recommended that the input voltage be increased gradually to 8V, at which time the output voltage should be 5V. If the output voltage is correct with 8V at VIN, then increase the input voltage as desired and proceed with evaluating the circuit. Do not exceed 50V at VIN.

5 Output Ripple Control

The LM34917A requires a minimum of 25 mVp-p ripple at the FB pin, in phase with the switching waveform at the SW pin, for proper operation. The required ripple can be supplied from ripple at V_{OUT}, through the feedback resistors, as described in options B and C below, or the ripple can be generated separately (using R5, C9, C10) keeping the ripple at V_{OUT} to a minimum as described in option A.

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A) **Minimum Output Ripple:** This evaluation board is supplied configured for minimum ripple at V_{OUT} by using components R5, C9 and C10. The output ripple, which ranges from ≅4mVp-p at V_{IN} = 8V to ≅14 mVp-p at V_{IN} = 33V, is determined primarily by the ESR of output capacitance, and the inductor's ripple current, which ranges from 105 mAp-p to 350 mAp-p over the input voltage range. The ripple voltage required by the FB pin is generated by R5, C9 and C10 since the SW pin switches from -1V to V_{IN}, and the right end of C10 is a virtual ground. The values for R5 and C10 are chosen to generate a 100 mVp-p triangle waveform at their junction. That triangle wave is then coupled to the FB pin through C9.

The following procedure is used to calculate values for R5, C9, and C10:

1) Calculate the voltage V_A:

$$V_A = V_{OUT} - (V_{SW} \times (1 - (V_{OUT}/V_{IN}))) \quad (2)$$

where V_{SW} is the absolute value of the voltage at the SW pin during the off-time (typically 1V), and V_{IN} is the minimum input voltage. For this circuit V_A calculates to 4.63V. This is the approximate DC voltage at the R5/C10 junction, and is used in the next equation.

2) Calculate the R5 × C10 product:

$$R5 \times C10 = \frac{(V_{IN} - V_A) \times t_{ON}}{\Delta V} \quad (3)$$

where t_{ON} is the maximum on-time (≅510 ns), V_{IN} is the minimum input voltage, and ΔV is the desired ripple amplitude at the R5/C10 junction, 100 mVp-p for this example.

$$R5 \times C10 = \frac{(8V - 4.63V) \times 510\ ns}{0.1V} = 0.172 \times 10^{-4} \quad (4)$$

R5 and C10 are then chosen from standard value components to satisfy the above product. For example, C10 can be 3300 pF requiring R5 to be ≅5.2 kΩ. C9 is chosen to be 0.1 µF, large compared to C10. The circuit as supplied on this EVB is shown in Figure 2.

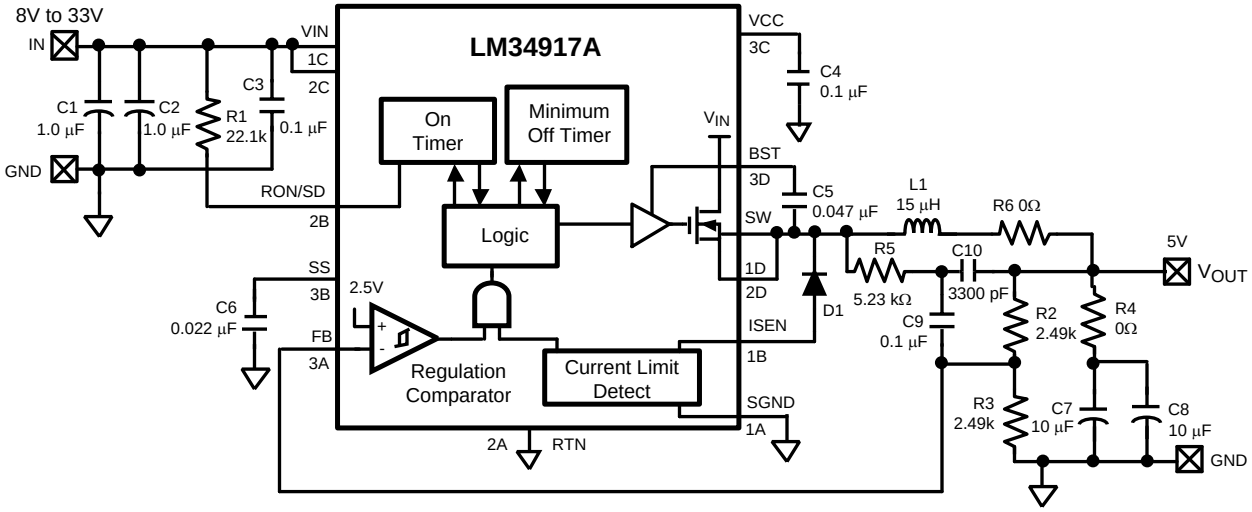

Figure 2. Minimum Output Ripple Configuration Using R5,C9,C10

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B) **Intermediate Ripple Level Configuration:** This configuration generates more ripple at V_{OUT} than the option A configuration, but uses one less capacitor. If some ripple can be tolerated in the application, this configuration is slightly more economical, and simpler. R5, C9 and C10 are removed. R4 and Cff are added as shown in Figure 3.

R4 is chosen to generate 25-30 mVp-p at V_{OUT} knowing that the minimum ripple current is 105 mAp-p at minimum V_{IN}. Cff couples that ripple to the FB pin without the attenuation of the feedback resistors. Cff's minimum value is calculated from:

$$Cff = \frac{t_{ON\ (max)}}{(R2//R3)} \tag{5}$$

where $t_{ON(max)}$ is the maximum on-time (at minimum V_{IN}), and R2//R3 is the equivalent parallel value of the feedback resistors. For this evaluation board $t_{ON(max)}$ is approximately 510 ns, and R2//R3 = 1.25 kΩ, and Cff calculates to a minimum of 408 pF. In the circuit of Figure 3 the ripple at V_{OUT} ranges from ≅32 mVp-p to ≅84 mVp-p over the input voltage range.

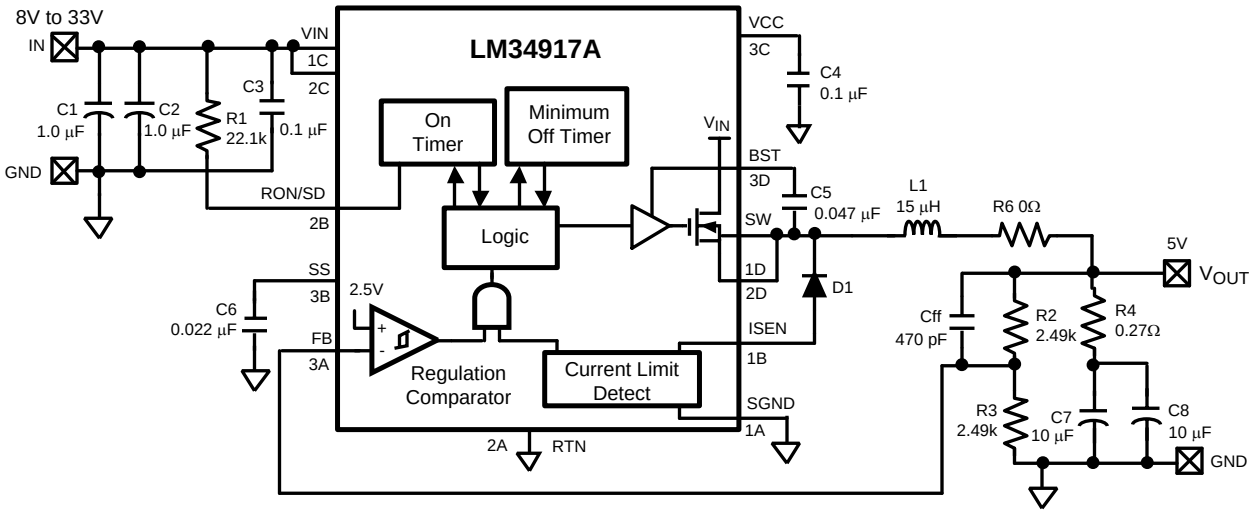

Figure 3. Intermediate Ripple Configuration Using Cff and R4

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C) **Lowest Cost Configuration:** This configuration is the same as option B, but without Cff. Since ≥25 mVp-p are required at the FB pin, R4 is chosen to generate ≥50 mV at V_{OUT}, knowing that the minimum ripple current in this circuit is 105 mAp-p at minimum V_{IN}. Using 0.5Ω for R4, the ripple at V_{OUT} ranges from ≅80 mVp-p to ≅150 mVp-p over the input voltage range. If the application can tolerate this ripple level, this is the most economical solution. The circuit is shown in Figure 4.

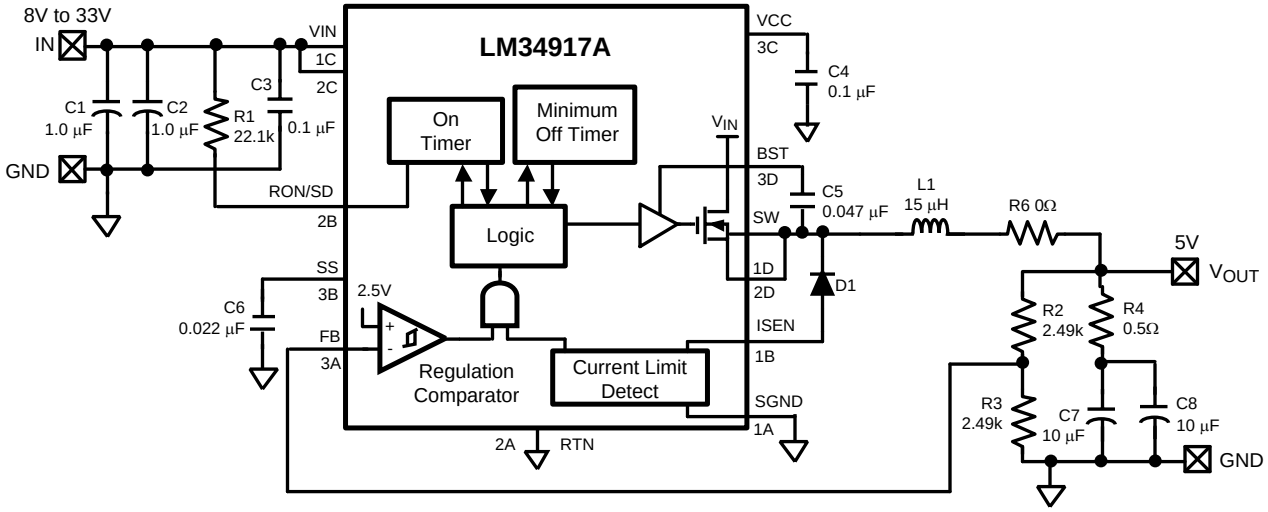

Figure 4. Lowest Cost Configuration

6 Monitor the Inductor Current

The inductor's current can be monitored or viewed on a scope with a current probe. Remove R6, and install an appropriate current loop across the two large pads where R6 was located. In this way the inductor's ripple current and peak current can be accurately determined.

7 Scope Probe Adapters

Scope probe adapters are provided on this evaluation board for monitoring the waveform at the SW pin, and at the circuit's output (V_{OUT}), without using the probe's ground lead which can pick up noise from the switching waveforms. The probe adapters are suitable for Tektronix P6137 or similar probes, with a 0.135" diameter.

8 Minimum Load Current

The LM34917A requires a minimum load current of ≅1 mA to ensure the boost capacitor (C5) is recharged sufficiently during each off-time. In this evaluation board, the minimum load current is provided by the feedback resistors allowing the board's minimum load current at V_{OUT} to be specified at zero.

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9 Bill of Materials

Table 1. Bill of Materials

Item	Description	Mfg., Part Number	Package	Value
C1,2	Ceramic Capacitor	TDK C3216X7R1H105M	1206	1.0 µF, 50V
C3	Ceramic Capacitor	TDK C1608X7R1H104K	0603	0.1 µF, 50V
C4	Ceramic Capacitor	TDK C1608X7R1H104K	0603	0.1 µF, 50V
C6	Ceramic Capacitor	TDK C1608X7R1H223K	0603	0.022 µF, 50V
C5	Ceramic Capacitor	TDK C1608X7R1H473K	0603	0.047 µF, 50V
C7, C8	Ceramic Capacitor	TDK C3216X7R1C106K	1206	10 µF, 16V
C9	Ceramic Capacitor	TDK C1608X7R1H104K	0603	0.1 µF, 50V
C10	Ceramic Capacitor	TDK C1608X7R1H332K	0603	3300 pF
D1	Schottky Diode	Zetex ZLLS2000	SOT23-6	40V, 2.2A
L1	Power Inductor	Bussman DR73-150	7.6 mm x 7.6 mm	15 µH, 1.8A
R1	Resistor	Vishay CRCW06032212F	0603	22.1 kΩ
R2, R3	Resistor	Vishay CRCW06032491F	0603	2.49 kΩ
R4	Resistor	Vishay CRCW06030000Z	0603	0Ω
R5	Resistor	Vishay CRCW06035231F	0603	5.23 kΩ
R6	Resistor	Vishay CRCW08050000Z	0805	0Ω Jumper
U1	Switching Regulator	LM34917	12 Bump DSBGA	

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10 Circuit Performance

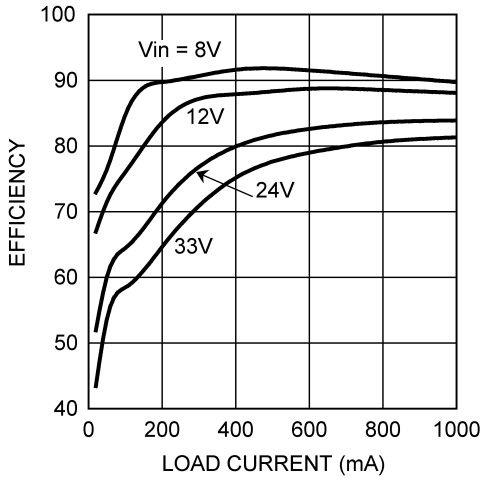

Figure 5. Efficiency vs Load Current

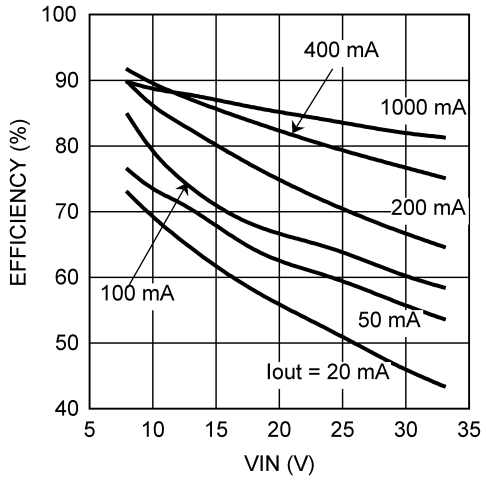

Figure 6. Efficiency vs Input Voltage

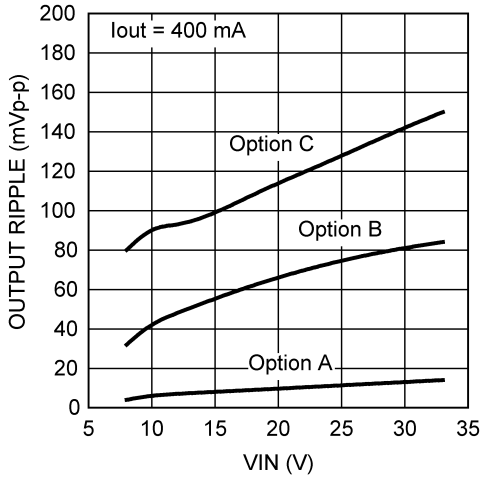

Figure 7. Output Voltage Ripple

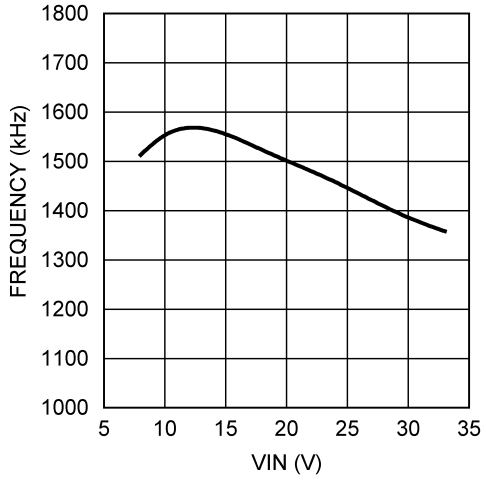

Figure 8. Switching Frequency vs. Input Voltage

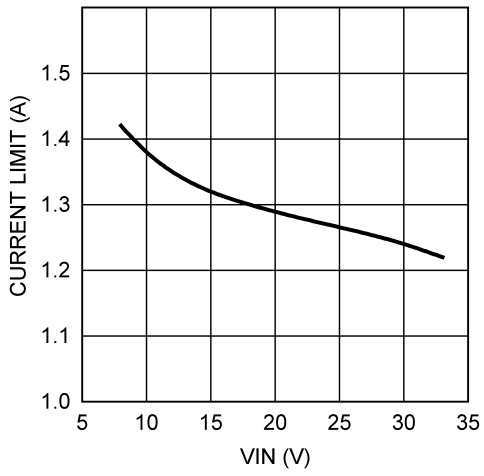

Figure 9. Current Limit vs Input Voltage

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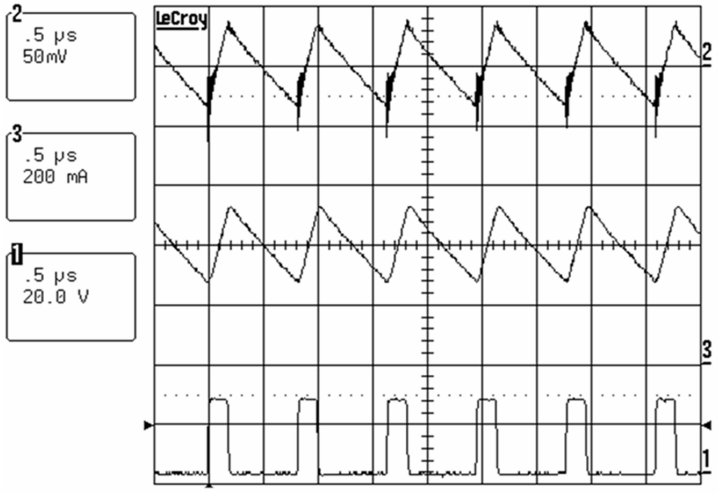
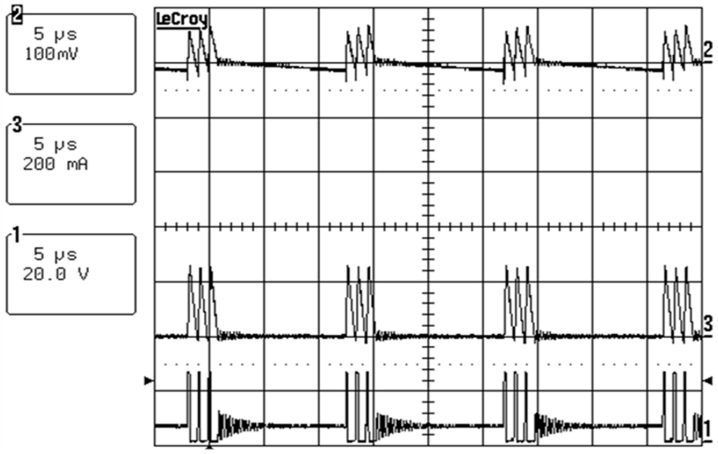
11 Typical Waveforms



Trace 2 = Vout
Trace 3 = Inductor Current
Trace 1 = SW Pin
Vin = 24V, Iout = 400 mA, Option B

Figure 10. Continuous Conduction Mode



Trace 2 = Vout
Trace 3 = Inductor Current
Trace 1 = SW Pin
Vin = 24V, Iout = 20 mA, Option B

Figure 11. Discontinuous Conduction Mode

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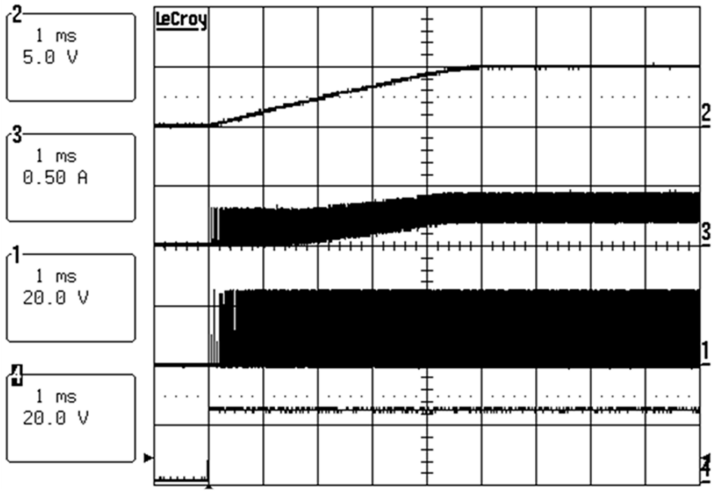

Trace 2 = Vout
Trace 3 = Inductor Current
Trace 1 = SW Pin
Trace 4 = Vin (0V to 24V)
Iout = 400 mA, Option B

Figure 12. Startup Waveforms

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12 PC Board Layout

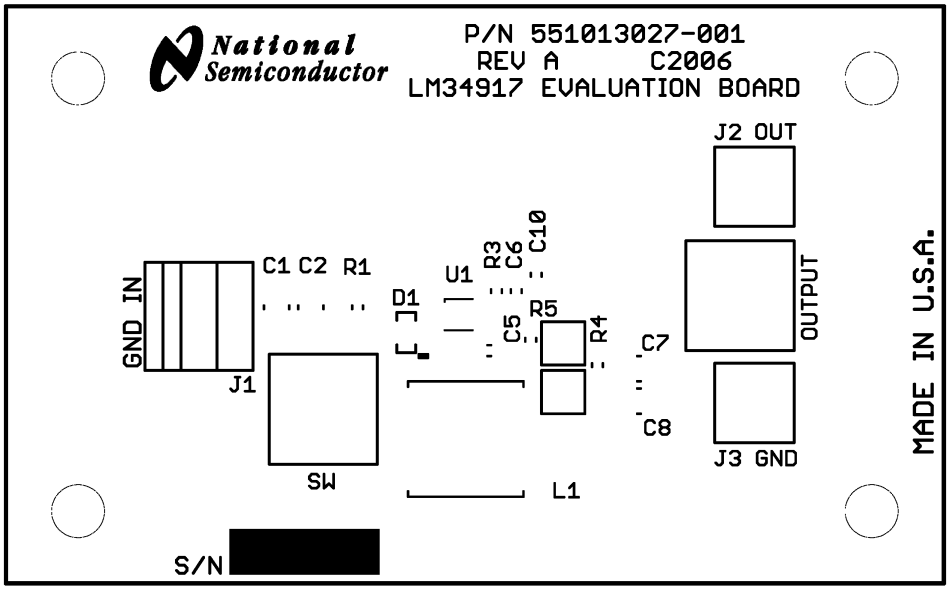

Figure 13. Board Silkscreen

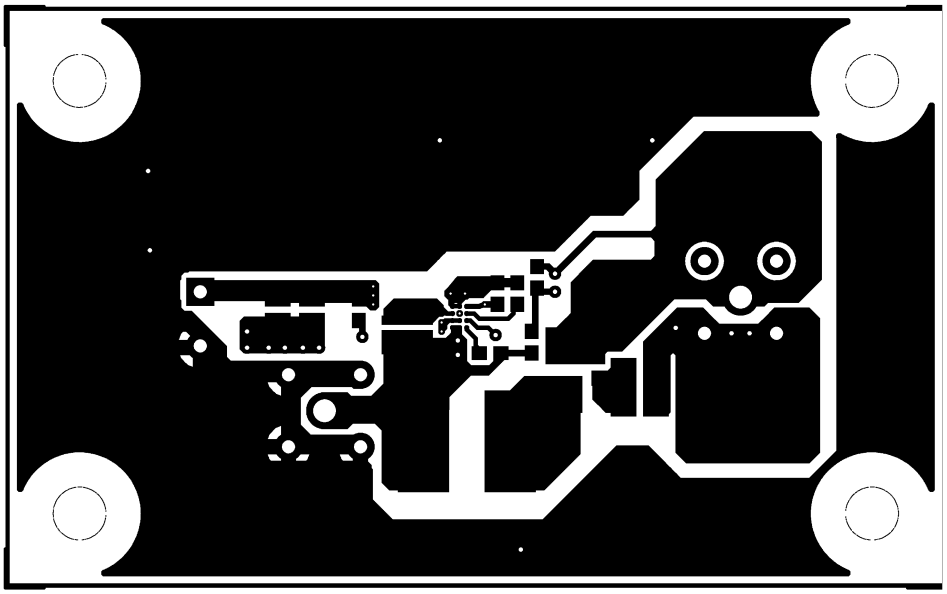

Figure 14. Board Top Layer

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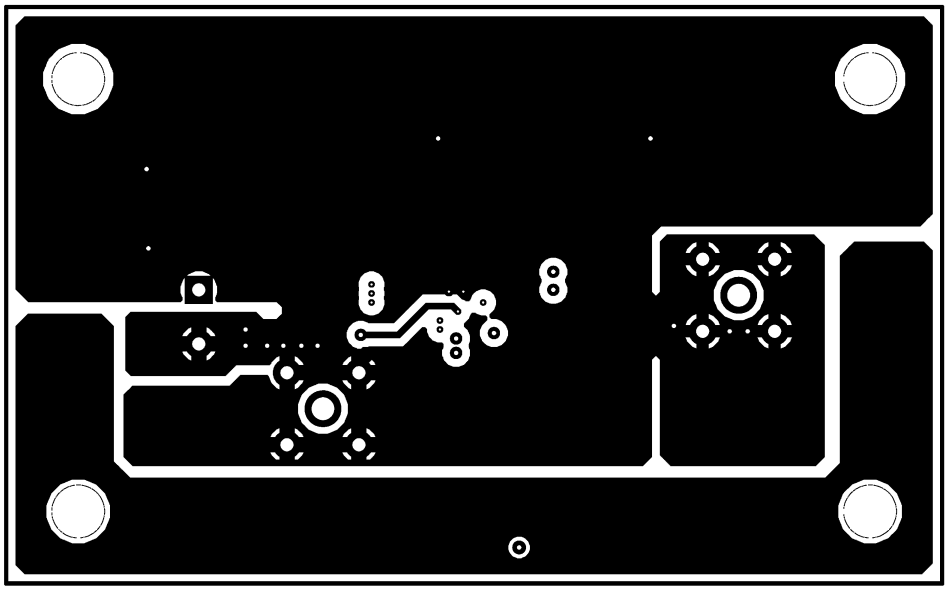

Figure 15. Board Second Layer (Viewed from Top)

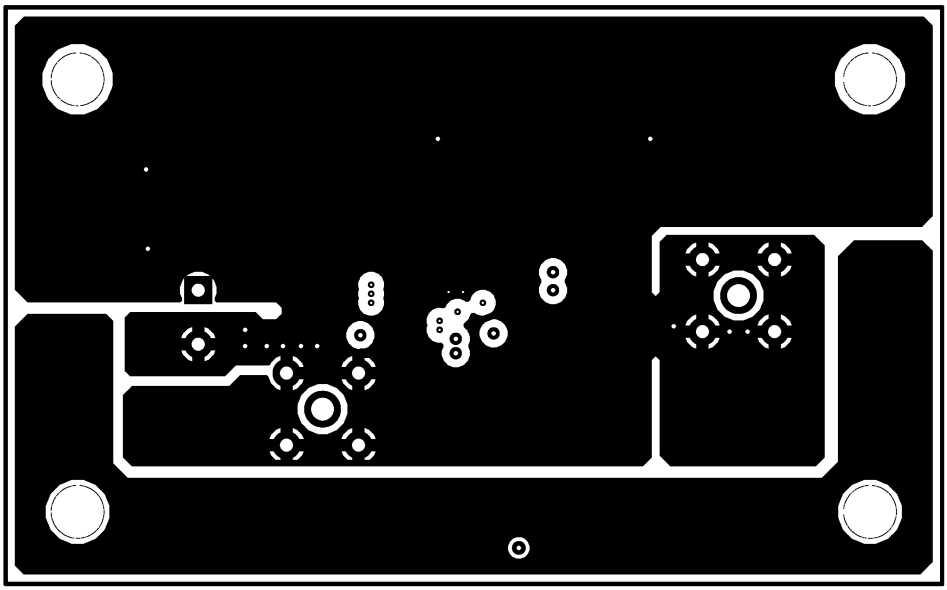

Figure 16. Board Third Layer (Viewed from Top)

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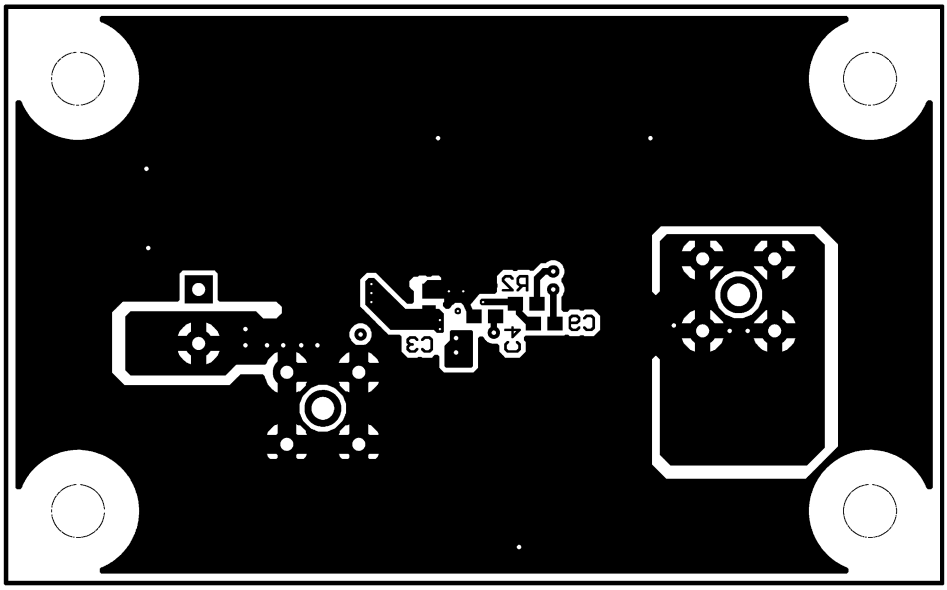

Figure 17. Board Bottom Layer (Viewed from Top)

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