FPC402 Quad Port Controller

1 Features

- Control Signal Management and I2C Aggregation Across Four Ports
- Combine Multiple FPC402s to Control 56 Total Ports Through a Single Host Interface
- Eliminate Need for Discrete I2C Muxes, LED Drivers, and High-Pin-Count FPGA/CPLD Control Devices
- Reduce PCB Routing Complexity by Handling All Low-Speed Control Signals Close to the Port
- Selectable I2C (up to 1 MHz) or SPI (up to 10 MHz) Host Control Interface
- Automatic Prefetching of Critical, User-Specified Data From the Modules
- Broadcast Mode Write to All Ports Simultaneously Across All FPC402 Controllers
- Advanced LED Features for Port Status Indication, Including Programmable Blinking and Dimming
- Customizable Interrupt Events
- Separate Host-Side I/O Voltage: 1.8 V to 3.3 V
- Small WQFN Package Enabling Placement on Bottom Side of PCB Underneath Ports

2 Applications

- ToR/Aggregation/Core Switch and Router
- Wireless Infrastructure Base Band Unit and Remote Radio Unit
- Video Switch and Router
- Storage Cards and Storage Racks
- SFP, QSFP, QSFP-DD, OSFP, Mini-SAS HD Port Management

3 Description

The FPC402 quad port controller serves as a low-speed signal aggregator for common port types such as SFP, QSFP, Mini-SAS HD, and others. The FPC402 aggregates all low-speed control and I2C signals across four ports and presents a single easy-to-use management interface to the host (I2C or SPI). Multiple FPC402s can be used in high-port-count applications with one common control interface to the host. The FPC402 is designed to allow placement on the bottom side of the PCB, underneath the press fit connector, to simplify routing. This localized control of the low-speed signals in the ports cuts system BOM costs by enabling the use of smaller IO count control devices (FPGAs, CPLDs, and MCUs) and by reducing routing layer congestion.

Device Information(1)

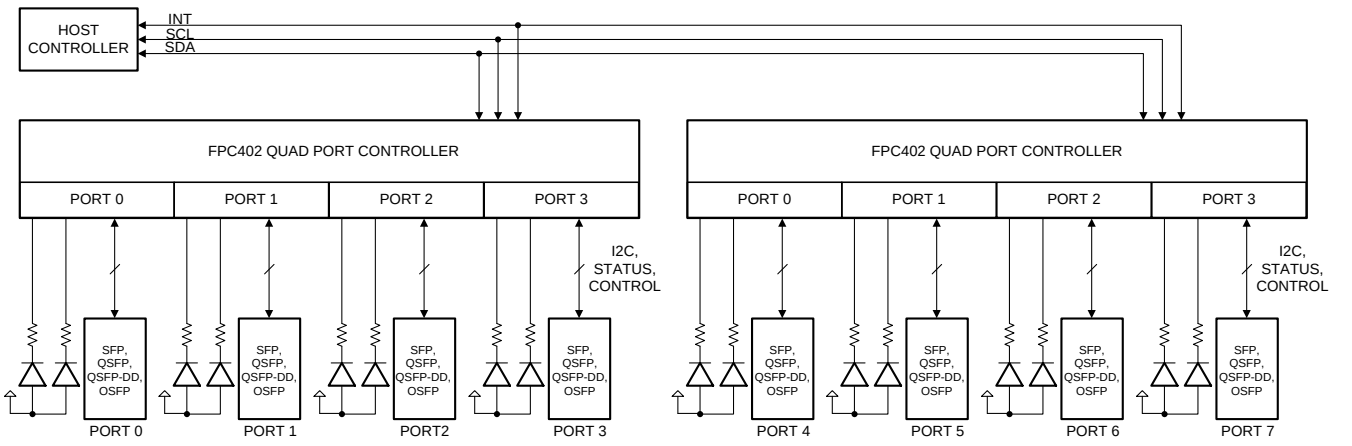
PART NUMBER	PACKAGE	BODY SIZE (NOM)
FPC402	WQFN (56)	5.00 mm × 11.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Device Comparison

PART NUMBER	ACCESSIBLE DOWNSTREAM ADDRESSES	PIN COMPATIBLE
FPC402	All valid I2C addreses	Yes
FPC401	MSA Addresses: 0xA0, 0xA2	Yes

Simplified Block Diagram



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4 Revision History

Changes from Original (June 2017) to Revision A	Page
• Changed Advance Information to Production Data	1

5 Description (continued)

The FPC402 is compatible with standard SFF-8431, SFF-8436, and SFF-8449 low-speed management interfaces, including a dedicated 100- or 400-kHz I2C interface to each port. Additional general-purpose pins are available to perform functions such as driving port status LEDs or controlling power switches. The LED drivers have convenience features such as programmable blinking and dimming. The interface to the host controller can operate on a separate supply voltage between 1.8 V and 3.3 V to support low-voltage I/Os.

The FPC402 can prefetch data from user-specified registers in each module, making the data readily accessible to the host through a fast I2C (up to 1 MHz) or SPI (up to 10 MHz) interface. In addition, the FPC402 can trigger an interrupt to the host whenever critical, user-configurable events occur associated with any of the ports the device controls. This eliminates the need to continuously poll the modules.

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6 Device and Documentation Support

6.1 Documentation Support

6.1.1 Related Documentation

For related documentation see the following:

- *FPC402 Programmer's Guide* (SNLU227)
- *FPC401 Evaluation Module (EVM) User's Guide* (SNLU222)

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.4 Trademarks

E2E is a trademark of Texas Instruments.
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6.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
FPC402RHUR	ACTIVE	WQFN	RHU	56	2000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 85	FPC402	Samples
FPC402RHUT	ACTIVE	WQFN	RHU	56	250	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 85	FPC402	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

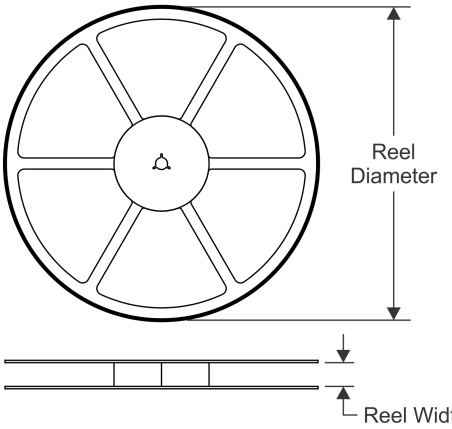
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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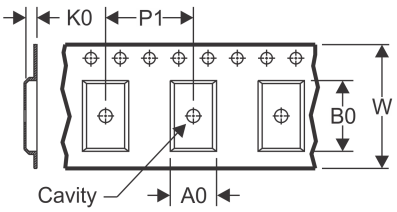
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

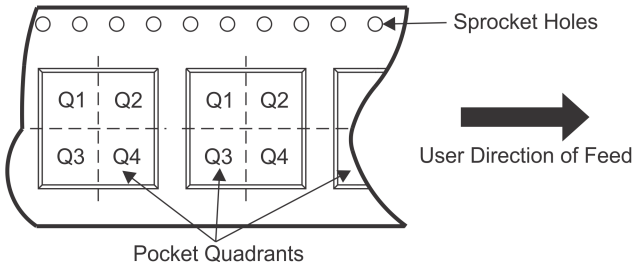


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

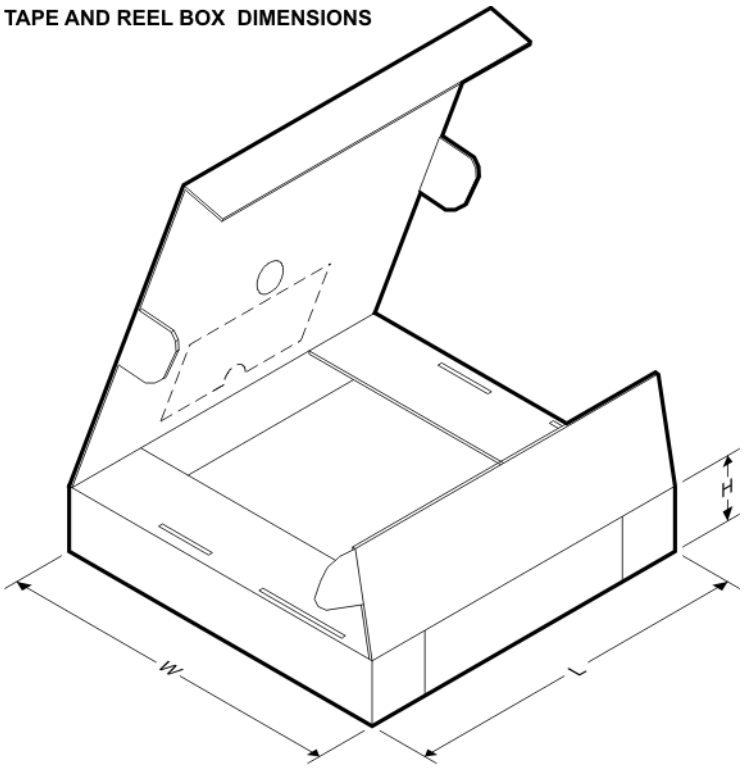
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
FPC402RHUR	WQFN	RHU	56	2000	330.0	24.4	5.3	11.3	1.0	8.0	24.0	Q1
FPC402RHUT	WQFN	RHU	56	250	178.0	24.4	5.3	11.3	1.0	8.0	24.0	Q1

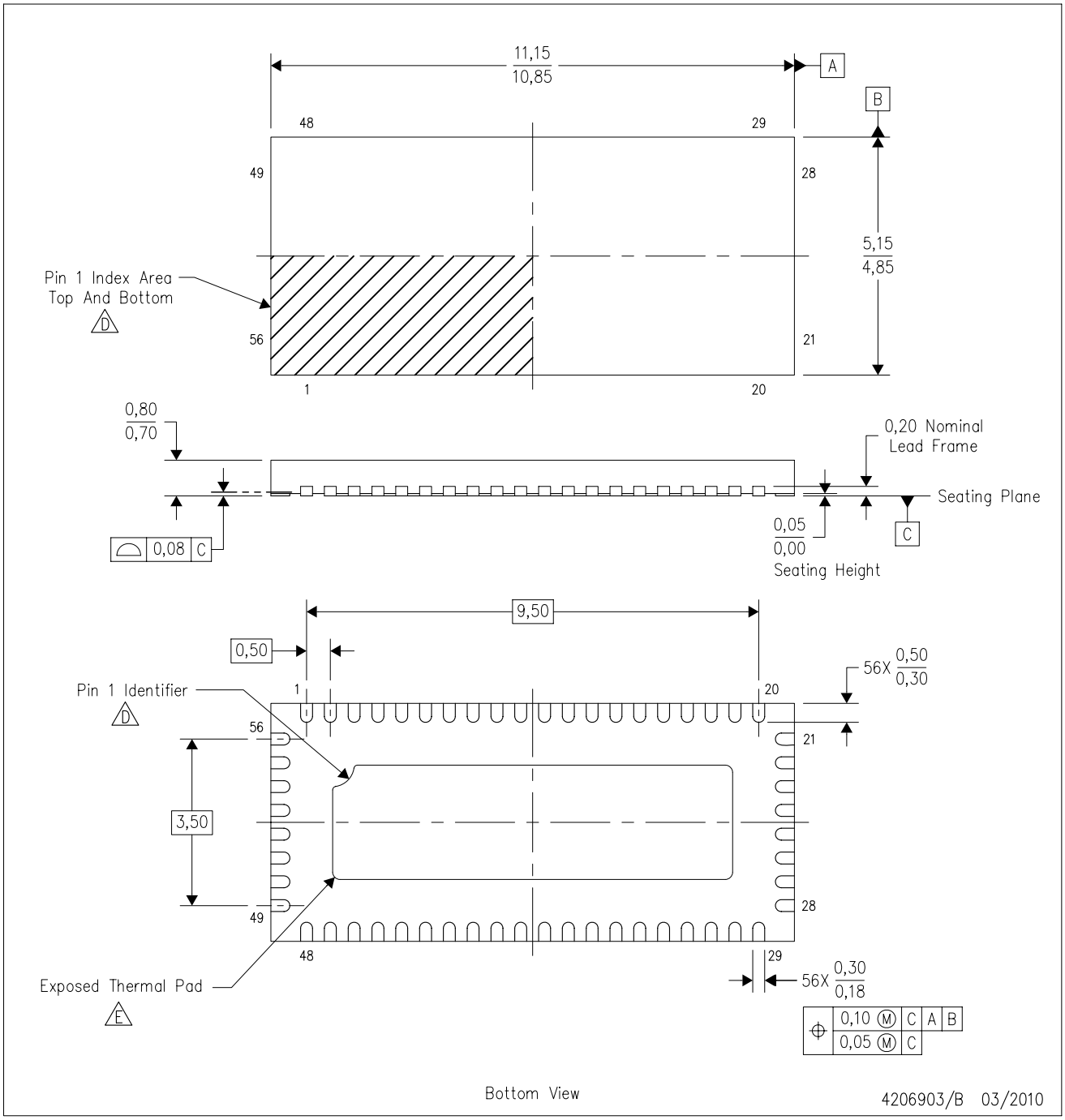
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
FPC402RHUR	WQFN	RHU	56	2000	367.0	367.0	45.0
FPC402RHUT	WQFN	RHU	56	250	213.0	191.0	55.0

RHU (R–PWQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



Notes:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
E. The package thermal pad must be soldered to the board for thermal and mechanical performance.
F. JEDEC MO–220 package registration is pending.

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