

# SN65LBC031, SN65LBC031Q, SN75LBC031 HIGH-SPEED CONTROLLER AREA NETWORK (CAN) TRANSCEIVERS

SLRS048A – MAY 1998 – REVISED APRIL 2000

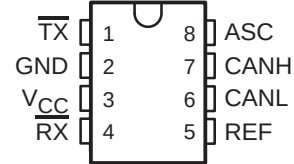
- SN75LBC031 Meets Standard ISO/DIS 11898 (up to 500 k Baud)
- Driver Output Capability at 50 mA
- Wide Positive and Negative Input/output Bus Voltage Range
- Bus Outputs Short-Circuit-Protected to Battery Voltage and Ground
- Thermal Shutdown
- Available in Q-Temp Automotive
  - HighRel Automotive Applications
  - Configuration Control/Print Support
  - Qualification to Automotive Standards

## description

The SN75LBC031 is a CAN transceiver used as an interface between a CAN controller and the physical bus for high speed applications of up to 500 kBaud. The device provides transmit capability to the differential bus and differential receive capability to the controller. The transmitter outputs (CANH and CANL), feature internal transition regulation to provide controlled symmetry resulting in low EMI emissions. Both transmitter outputs are fully protected against battery short circuits and electrical transients that can occur on the bus lines. In the event of excessive device power dissipation the output drivers are disabled by the thermal shutdown circuitry at a junction temperature of approximately 160°C. The inclusion of an internal pullup resistor on the transmitter input ensures a defined output during power up and protocol controller reset. For normal operation at 500 kBaud the ASC terminal is open or tied to GND. For slower speed operation at 125 kBaud the bus output transition times can be increased to reduce EMI by connecting the ASC terminal to  $V_{CC}$ . The receiver includes an integrated filter that suppresses the signal into pulses less than 30 ns wide.

The SN75LBC031 is characterized for operation from –40°C to 85°C. The SN65LBC031 is characterized for operation from –40°C to 125°C. The SN65LBC031Q is characterized for operation over the automotive temperature range of –40°C to 125°C.

D PACKAGE  
(TOP VIEW)



TERMINAL FUNCTIONS

| TERMINAL               | DESCRIPTION                 |
|------------------------|-----------------------------|
| $\overline{\text{TX}}$ | Transmitter input           |
| GND                    | Ground                      |
| $V_{CC}$               | Supply voltage              |
| $\overline{\text{RX}}$ | Receiver output             |
| REF                    | Reference output            |
| CANL                   | Low side bus output driver  |
| CANH                   | High side bus output driver |
| ASC                    | Adjustable slope control    |

FUNCTION TABLE

| $\overline{\text{TX}}$ | CANH     | CANL     | BUS STATE | $\overline{\text{RX}}$ |
|------------------------|----------|----------|-----------|------------------------|
| L                      | H        | L        | Dominant  | L                      |
| High or floating       | Floating | Floating | Recessive | H                      |

L = low, H = high



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

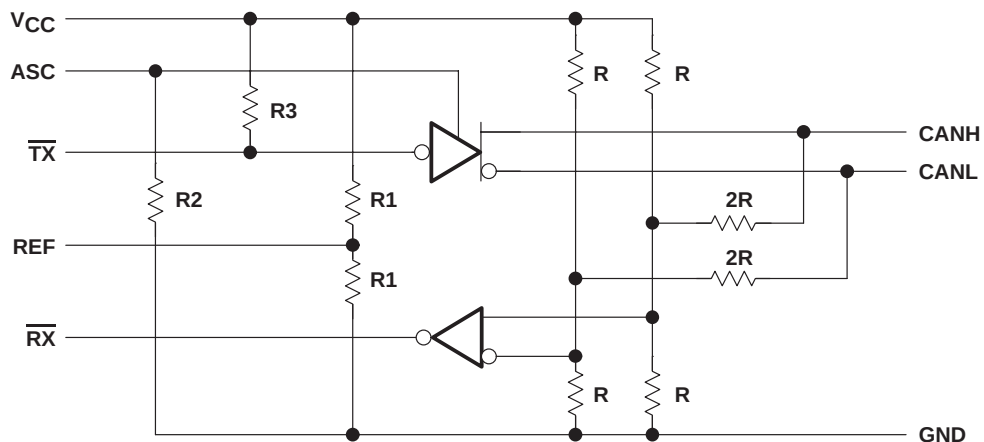
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# SN65LBC031, SN65LBC031Q, SN75LBC031 HIGH-SPEED CONTROLLER AREA NETWORK (CAN) TRANSCEIVERS

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## logic diagram



# SN65LBC031, SN65LBC031Q, SN75LBC031 HIGH-SPEED CONTROLLER AREA NETWORK (CAN) TRANSCEIVERS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                            |                              |
|----------------------------------------------------------------------------|------------------------------|
| Logic supply voltage, $V_{CC}$ (see Note 1)                                | 7 V                          |
| Bus terminal voltage                                                       | –5 V to 20 V                 |
| Input current at $\overline{TX}$ and ASC terminal, $I_I$                   | $\pm 10$ mA                  |
| Input voltage at $\overline{TX}$ and ASC terminal, $V_I$                   | $2 \times V_{CC}$            |
| Operating free-air temperature range, $T_A$ : SN65LBC031, SN65LBC031Q      | –40°C to 125°C               |
| SN75LBC031                                                                 | –40°C to 85°C                |
| Operating junction range, $T_J$                                            | –40°C to 150°C               |
| Continuous total power dissipation at (or below) 25°C free-air temperature | See Dissipation Rating Table |
| Storage temperature range, $T_{Stg}$                                       | –65°C to 150°C               |
| Case temperature for 10 sec $T_C$ , D package                              | 260°C                        |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential bus voltage, are measured with respect to GND.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$<br>POWER RATING | OPERATING FACTOR<br>ABOVE $T_C = 25^\circ\text{C}$ | $T_C = 125^\circ\text{C}$<br>POWER RATING |
|---------|---------------------------------------------|----------------------------------------------------|-------------------------------------------|
| D       | 725 mW                                      | 5.8 mW/°C                                          | 145 mW                                    |

DISSIPATION DERATING CURVE  
vs  
FREE-AIR TEMPERATURE

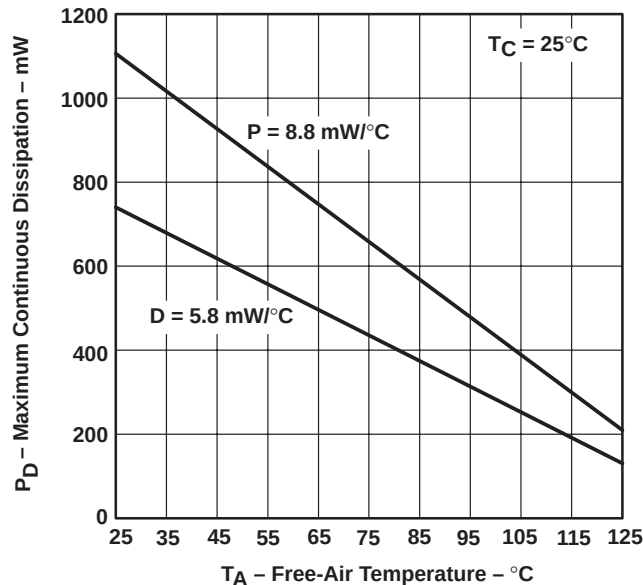


Figure 1

# SN65LBC031, SN65LBC031Q, SN75LBC031 HIGH-SPEED CONTROLLER AREA NETWORK (CAN) TRANSCEIVERS

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## recommended operating conditions

|                                                                                         |                         | MIN | NOM | MAX      | UNIT         |
|-----------------------------------------------------------------------------------------|-------------------------|-----|-----|----------|--------------|
| Logic supply voltage, $V_{CC}$                                                          |                         | 4.5 | 5   | 5.5      | V            |
| Voltage at any bus terminal (separately or common mode), $V_I$ or $V_{IC}$ (see Note 3) |                         | –2  |     | 7        | V            |
| High-level input voltage, $V_{IH}$                                                      | $\overline{TX}$         | 2   |     | $V_{CC}$ | V            |
| Low-level input voltage, $V_{IL}$                                                       | $\overline{TX}$         | 0   |     | 0.8      | V            |
| High-level output current, $I_{OH}$                                                     | Transmitter             |     |     | –50      | mA           |
|                                                                                         | Receiver                |     |     | –400     | $\mu$ A      |
| Low-level output current, $I_{OL}$                                                      | Transmitter             |     |     | 50       | mA           |
|                                                                                         | Receiver                |     |     | 1        |              |
| Operating free-air temperature, $T_A$                                                   | SN75LBC031              | –40 |     | 85       | $^{\circ}$ C |
|                                                                                         | SN65LBC031, SN65LBC031Q | –40 |     | 125      |              |

NOTES: 2. All voltage values, except differential bus voltage, are measured with respect to the ground terminal.

3. For bus voltages from –5 V to –2 V and 7 V to 20 V the receiver output is stable.

## SYMBOL DEFINITION

| DATA SHEET PARAMETER | DEFINITION                                        |
|----------------------|---------------------------------------------------|
| $V_{O(CANH R)}$      | CANH bus output voltage (recessive state)         |
| $V_{O(CANL R)}$      | CANL bus output voltage (recessive state)         |
| $V_{O(CANH D)}$      | CANH bus output voltage (dominant state)          |
| $V_{O(CANL D)}$      | CANL bus output voltage (dominant state)          |
| $V_{O(DIFF R)}$      | Bus differential output voltage (recessive state) |
| $V_{O(DIFF D)}$      | Bus differential output voltage (dominant state)  |
| $V_I(ASC)$           | Adjustable slope control input voltage            |

## electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                           | TEST CONDITIONS          | MIN           | TYP | MAX           | UNIT       |
|-----------------------------------------------------|--------------------------|---------------|-----|---------------|------------|
| $V_{O(REF)}$ Reference source output voltage        | $I_{REF} = \pm 20 \mu A$ | $0.45 V_{CC}$ |     | $0.55 V_{CC}$ | V          |
| $R_{O(REF)}$ Reference source output resistance     |                          | 5             |     | 10            | k $\Omega$ |
| $I_{CC(REC)}$ Logic supply current, recessive state | See Figure 2, S1 closed  |               | 12  | 20            | mA         |
| $I_{CC(DOM)}$ Logic supply current, dominant state  |                          |               | 55  | 80            |            |



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## HIGH-SPEED CONTROLLER AREA NETWORK (CAN) TRANSCEIVERS

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**transmitter electrical characteristics over recommended ranges of supply and operating free-air temperature (unless otherwise noted)**

| PARAMETER                        |                                                    | TEST CONDITIONS                            | MIN  | TYP         | MAX     | UNIT          |
|----------------------------------|----------------------------------------------------|--------------------------------------------|------|-------------|---------|---------------|
| $V_{O(CANHR)}$<br>$V_{O(CANLR)}$ | Output voltage (recessive state)                   | See Figure 2, S1 open                      | 2    | $0.5V_{CC}$ | 3       | V             |
| $V_{O(DIFFR)}$                   | Differential output voltage (recessive state)      |                                            | –500 | 0           | 50      | mV            |
| $V_{O(CANHD)}$                   | Output voltage (dominant state)                    | See Figure 2, S1 closed                    | 2.75 | 3.5         | 4.5     | V             |
| $V_{O(CANLD)}$                   | Output voltage (dominant state)                    |                                            | 0.5  | 1.5         | 2.25    |               |
| $V_{O(DIFFD)}$                   | Differential output voltage (dominant state)       |                                            | 1.5  | 2           | 3       |               |
| $I_{IH(TX)}$                     | High-level input current (TX)                      | $V_{IH} = 2.4\text{ V}$                    |      | –100        | –185    | $\mu\text{A}$ |
|                                  |                                                    | $V_{IH} = V_{CC}$                          |      |             | $\pm 2$ |               |
| $I_{IH(ASC)}$                    | High-level input current (ASC)                     | $V_{IH} = 2.4\text{ V}$                    |      | 100         | 165     | $\mu\text{A}$ |
|                                  |                                                    | $V_{IH} = V_{CC}$                          |      | 200         | 340     |               |
| $I_{IL(TX)}$                     | Low-level input current ( $\overline{\text{TX}}$ ) | $V_{IL} = 0.4\text{ V}$                    |      | –180        | –400    | $\mu\text{A}$ |
| $I_{IL(ASC)}$                    | Low-level input current (ASC)                      | $V_{IL} = 0.4\text{ V}$                    |      | 15          | 25      | $\mu\text{A}$ |
| $C_I(TX)$                        | $\overline{\text{TX}}$ input capacitance           |                                            |      | 8           |         | pF            |
| $I_{O(SSH)}$                     | CANH short circuit output current                  | $V_{O(CANH)} = -2\text{ V to }20\text{ V}$ |      | –95         | –200    | mA            |
| $I_{O(SSL)}$                     | CANL short circuit output current                  | $V_{O(CANL)} = 20\text{ V to }-2\text{ V}$ |      | 140         | 250     | mA            |

NOTE 2: All voltage values, except differential bus voltage, are measured with respect to the ground terminal.

**transceiver dynamic characteristics over recommended operating free-air temperature range and  $V_{CC} = 5\text{ V}$**

| PARAMETER              |                                                       | TEST CONDITIONS                                                                         | MIN | TYP | MAX | UNIT             |
|------------------------|-------------------------------------------------------|-----------------------------------------------------------------------------------------|-----|-----|-----|------------------|
| $t_{\text{loop}}$      | Loop time                                             | See Figures 2 and 3, S1 closed, $V_I(\text{ASC}) = 0\text{ V}$ or open circuit, S2 open |     |     | 280 | ns               |
|                        |                                                       | See Figures 2 and 3, S1 closed, $V_I(\text{ASC}) = V_{CC}$ , S2 closed                  |     |     | 400 | ns               |
| $SR(\text{RD})$        | Differential-output slew rate (recessive to dominant) | See Figures 2 and 4, S1 closed, $V_I(\text{ASC}) = 0$ or open circuit, S2 open          |     | 35  |     | V/ $\mu\text{s}$ |
|                        |                                                       | See Figures 2 and 4, S1 closed, $V_I(\text{ASC}) = V_{CC}$ , S2 closed                  |     | 10  |     | V/ $\mu\text{s}$ |
| $SR(\text{DR})$        | Differential-output slew rate (dominant to recessive) | See Figures 2 and 4, S1 closed, $V_I(\text{ASC}) = 0$ or open circuit, S2 open          |     | 10  |     | V/ $\mu\text{s}$ |
|                        |                                                       | See Figures 2 and 4, S1 closed, $V_I(\text{ASC}) = V_{CC}$ , S2 closed                  |     | 10  |     | V/ $\mu\text{s}$ |
| $t_{d(\text{RD})}$     | Differential-output delay time                        | See Figure 2, S1 closed                                                                 |     | 55  |     | ns               |
| $t_{d(\text{DR})}$     |                                                       |                                                                                         |     | 160 |     | ns               |
| $t_{pd(\text{RECRD})}$ | Receiver propagation delay time                       | See Figures 2 and 5                                                                     |     | 90  |     | ns               |
| $t_{pd(\text{RECDR})}$ |                                                       |                                                                                         |     | 55  |     | ns               |

NOTE 4: Receiver input pulse width should be >50 ns. Input pulses of <30 ns are suppressed.



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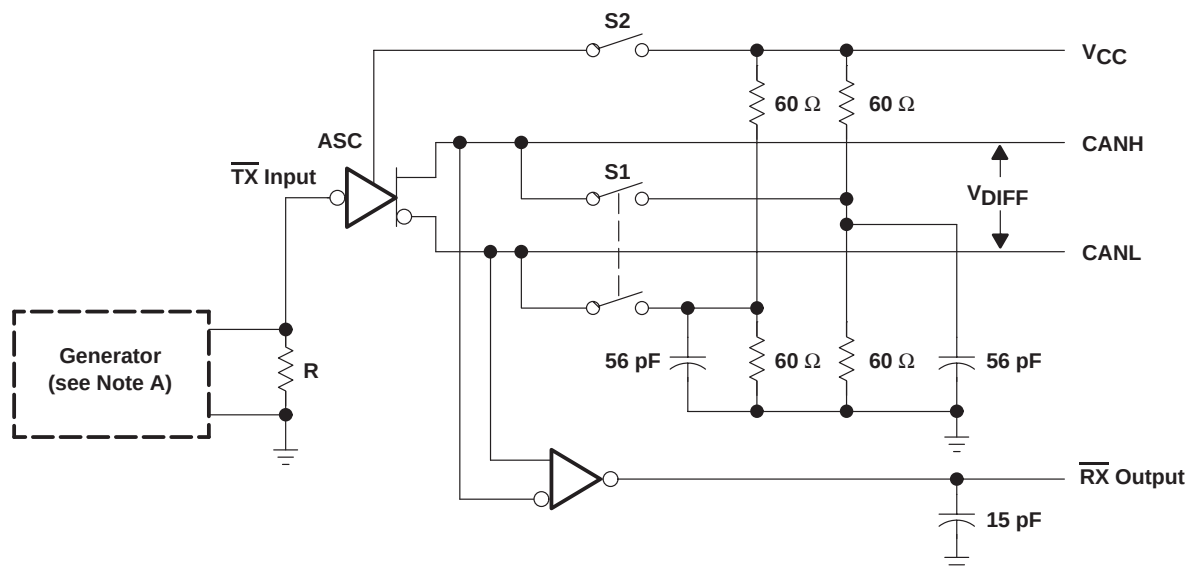
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receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                    | TEST CONDITIONS                                                       | MIN                     | TYP | MAX      | UNIT       |
|------------------------------------------------------------------------------|-----------------------------------------------------------------------|-------------------------|-----|----------|------------|
| $V_{IT(REC)}$ Differential input threshold voltage for recessive state       | $V_{IC} = -2\text{ V to } 7\text{ V}$                                 |                         |     | 500      | mV         |
| $V_{IT(DOM)}$ Differential input threshold voltage for dominant state        |                                                                       | 900                     |     |          |            |
| $V_{hys}$ Recessive-dominant input hysteresis                                |                                                                       | 100                     | 180 |          | mV         |
| $V_{OH(RX)}$ High-level output voltage                                       | $V_{O(DIFF)} = 500\text{ mV}$ ,<br>$I_{OH} = -400\text{ }\mu\text{A}$ | $V_{CC} - 0.5\text{ V}$ |     | $V_{CC}$ | V          |
| $V_{OL(RX)}$ Low-level output voltage                                        | $V_{O(DIFF)} = 900\text{ mV}$ ,<br>$I_{OL} = 1\text{ mA}$             | 0                       |     | 0.5      | V          |
| $r_{I(REC)}$ CANH and CANL input resistance in recessive state               | dc, no load                                                           | 5                       |     | 50       | k $\Omega$ |
| $r_{I(DIFF)}$ Differential CANH and CANL input resistance in recessive state | dc, no load                                                           | 10                      |     | 100      | k $\Omega$ |
| $C_i$ CANH and CANL input capacitance                                        |                                                                       |                         | 20  |          | pF         |
| $C_{i(DHL)}$ Differential CANH and CANL input capacitance                    |                                                                       |                         | 10  |          | pF         |

NOTE 2: All voltage values, except differential bus voltage, are measured with respect to the ground terminal.

## PARAMETER MEASUREMENT INFORMATION



NOTE A: The input pulse is supplied to  $\overline{TX}$  by a generator having a  $t_r$  and  $t_f = 5\text{ ns}$ .

Figure 2. Test Circuit

## PARAMETER MEASUREMENT INFORMATION

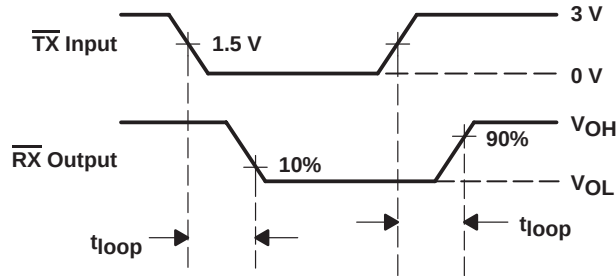


Figure 3. Loop Time

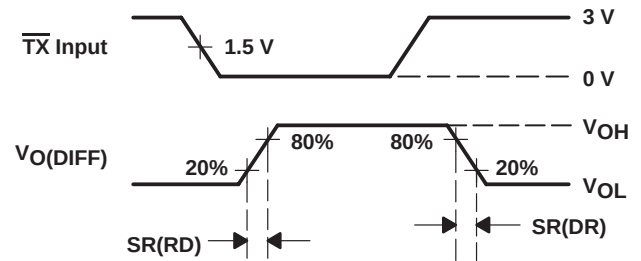
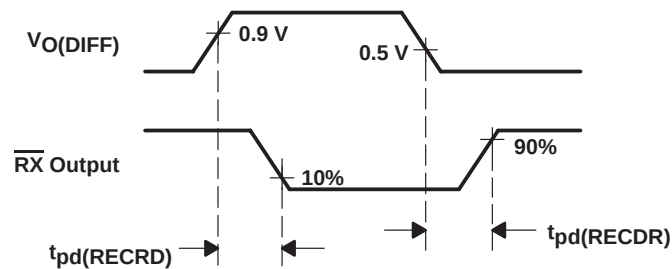


Figure 4. Slew Rate

NOTE A: The input pulse is supplied to  $\overline{TX}$  by a generator having a  $t_r$  and  $t_f = 5$  ns.



NOTE A: The input pulse is supplied as  $V_{DIFF}$  using CANH and CANL respectively by a generator having a  $t_r$  and  $t_f = 5$  ns.

Figure 5. Receiver Delay Times

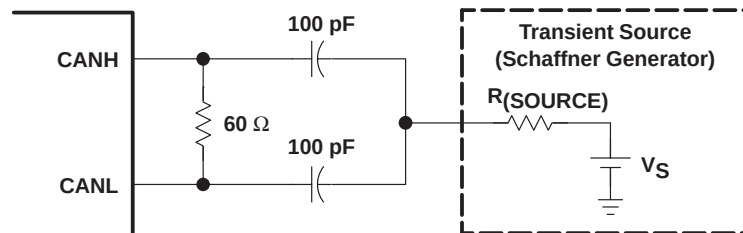


Figure 6. Transient Stress Capability Test Circuit

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PARAMETER MEASUREMENT INFORMATION

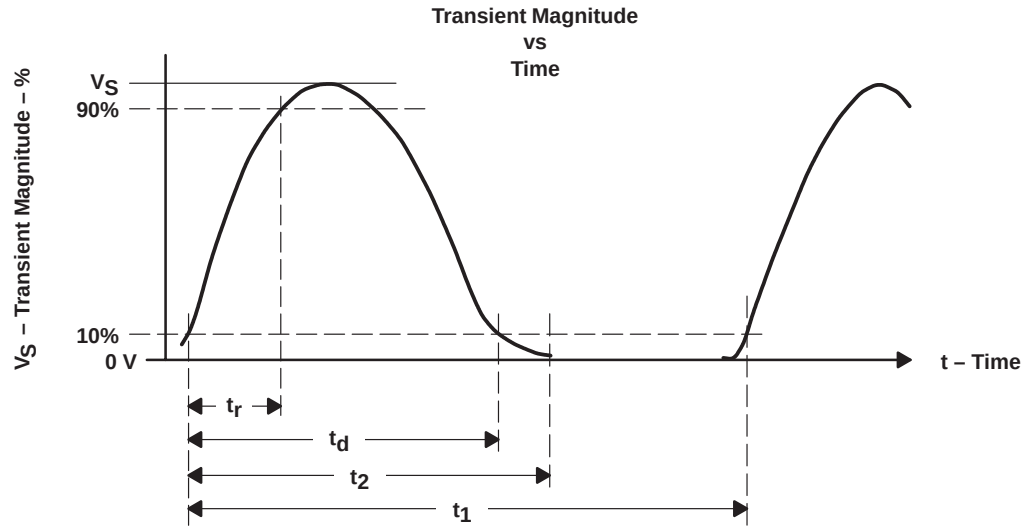


Figure 7. Transient Stress Capability Waveform

Table 1. Test Circuit Results According to DIN 40839

| TEST PULSE | TRANSIENT MAGNITUDE V <sub>S</sub> | SOURCE IMPEDANCE R <sub>SOURCE</sub> | PULSE WIDTH t <sub>d</sub> (see Note 5) | PULSE RISE TIME, t <sub>r</sub> (see Note 6) | PULSE TIME, t <sub>2</sub> (see Figure 7) | REPETITION PERIOD, t <sub>1</sub> (see Figure 7) | NUMBER OF PULSES |
|------------|------------------------------------|--------------------------------------|-----------------------------------------|----------------------------------------------|-------------------------------------------|--------------------------------------------------|------------------|
| 1          | −100 V                             | 10 Ω                                 | 2 ms                                    | 1 μs                                         | 200 ms                                    | 5 s                                              | 5000             |
| 2          | 100 V                              | 10 Ω                                 | 50 μs                                   | 1 μs                                         | 200 ms                                    | 5 s                                              | 5000             |
| 3a         | −150 V                             | 50 Ω                                 | 0.1 μs                                  | 5 ns                                         | 100 μs                                    | 100 μs                                           | See Note 7       |
| 3b         | 100 V                              | 50 Ω                                 | 0.1 μs                                  | 5 ns                                         | 100 μs                                    | 100 μs                                           | See Note 7       |
| 5          | 60 V                               | 1 Ω                                  | 400 ms                                  | 5 ms                                         | —                                         | —                                                | 1                |

NOTES: 5. Measured from 10% on rising edge to 10% on falling edge  
6. Measured from 10% to 90% of pulse  
7. Pulse package for a period of 3600 s, 10 ms pulse time, 90 ms stop time



# SN65LBC031, SN65LBC031Q, SN75LBC031 HIGH-SPEED CONTROLLER AREA NETWORK (CAN) TRANSCEIVERS

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## APPLICATION INFORMATION

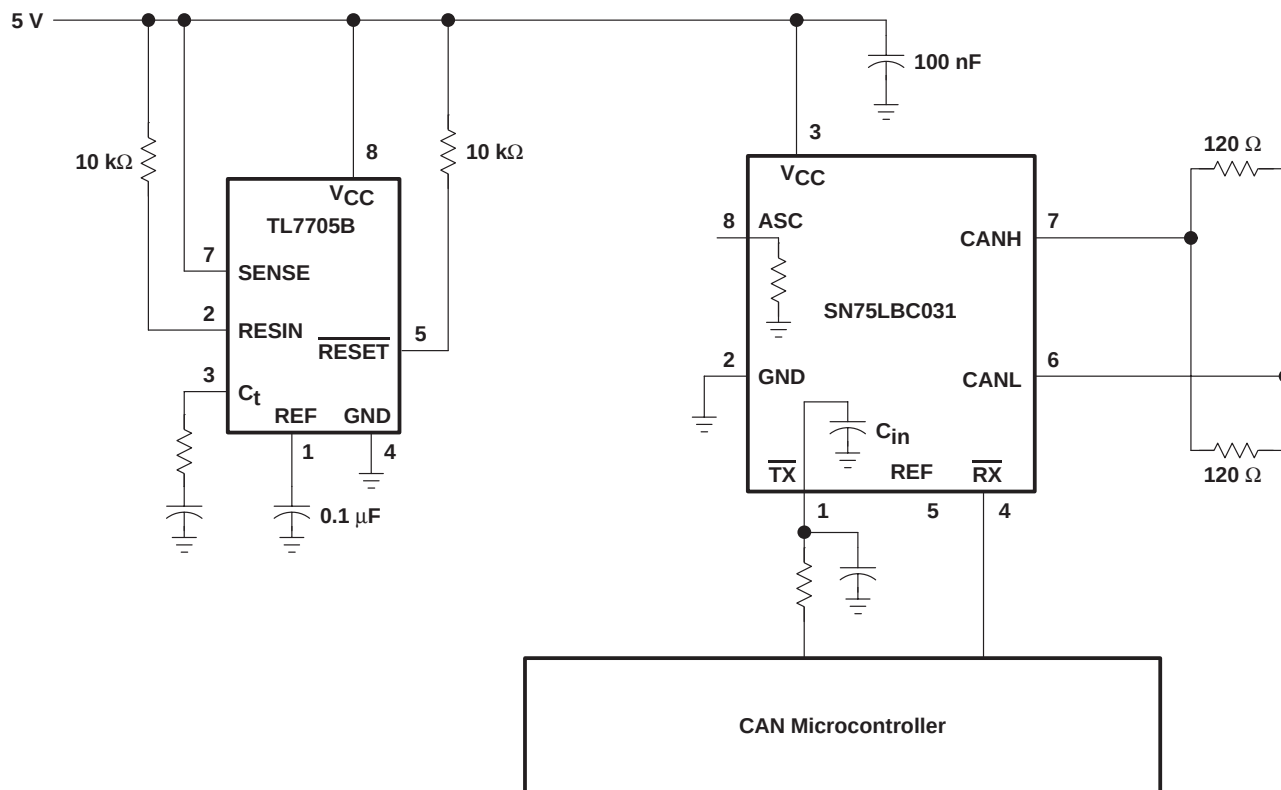


Figure 8. Typical SN75LBC031 Application

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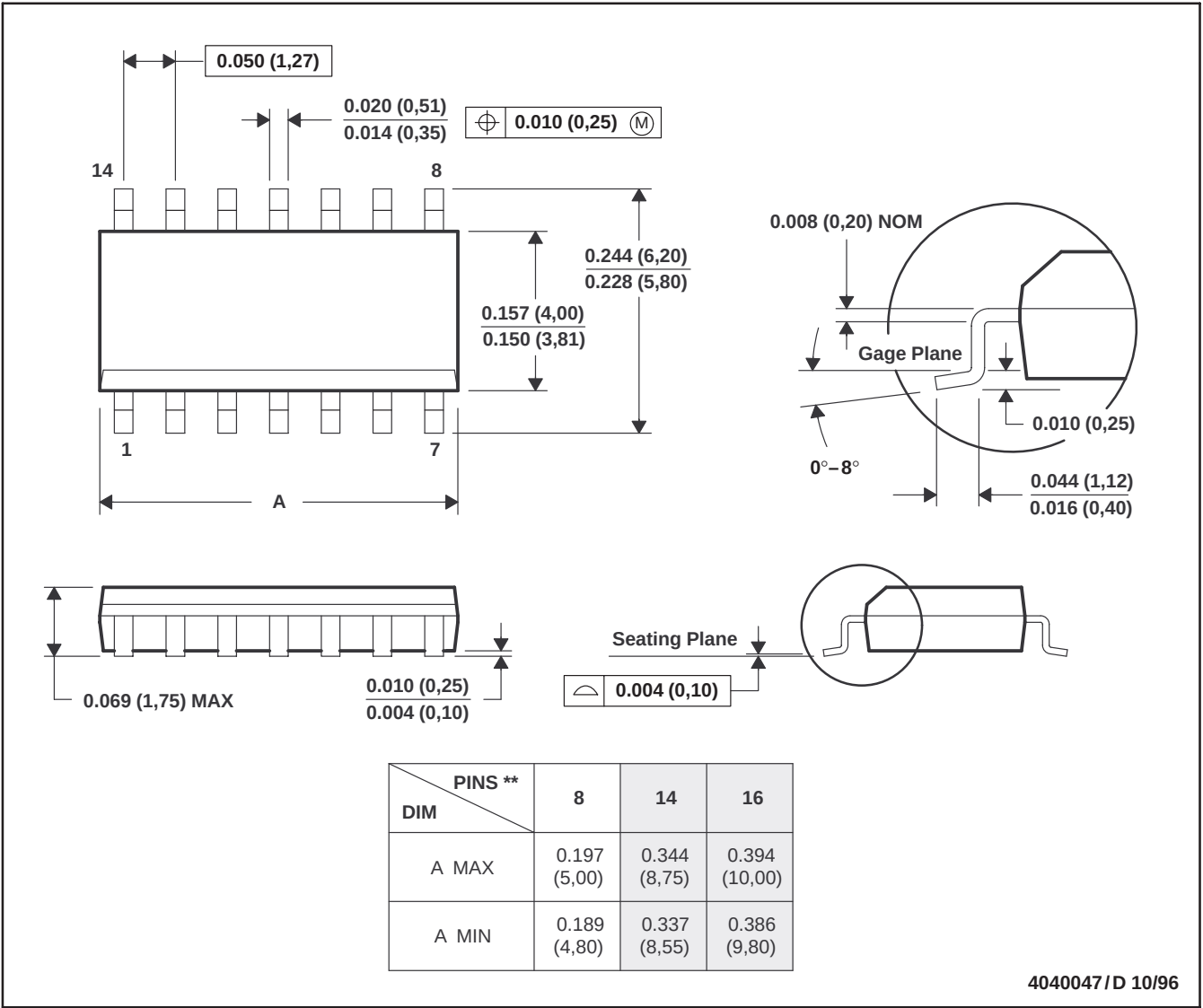
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MECHANICAL DATA

D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
D. Falls within JEDEC MS-012

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN65LBC031D      | ACTIVE        | SOIC         | D                  | 8    | 75             | TBD                        | NIPDAU                  | Level-1-220C-UNLIM   | -40 to 85    | 6LB031                  | <a href="#">Samples</a> |
| SN65LBC031DG4    | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 85    | 6LB031                  | <a href="#">Samples</a> |
| SN65LBC031DRG4   | ACTIVE        | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   |              | 6LB031                  | <a href="#">Samples</a> |
| SN65LBC031QD     | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | 6LB031Q                 | <a href="#">Samples</a> |
| SN65LBC031QDG4   | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | 6LB031Q                 | <a href="#">Samples</a> |
| SN65LBC031QDR    | ACTIVE        | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | LB031Q                  | <a href="#">Samples</a> |
| SN65LBC031QDRG4  | ACTIVE        | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -40 to 125   | LB031Q                  | <a href="#">Samples</a> |
| SN75LBC031D      | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | 7LB031                  | <a href="#">Samples</a> |
| SN75LBC031DR     | ACTIVE        | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | 7LB031                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

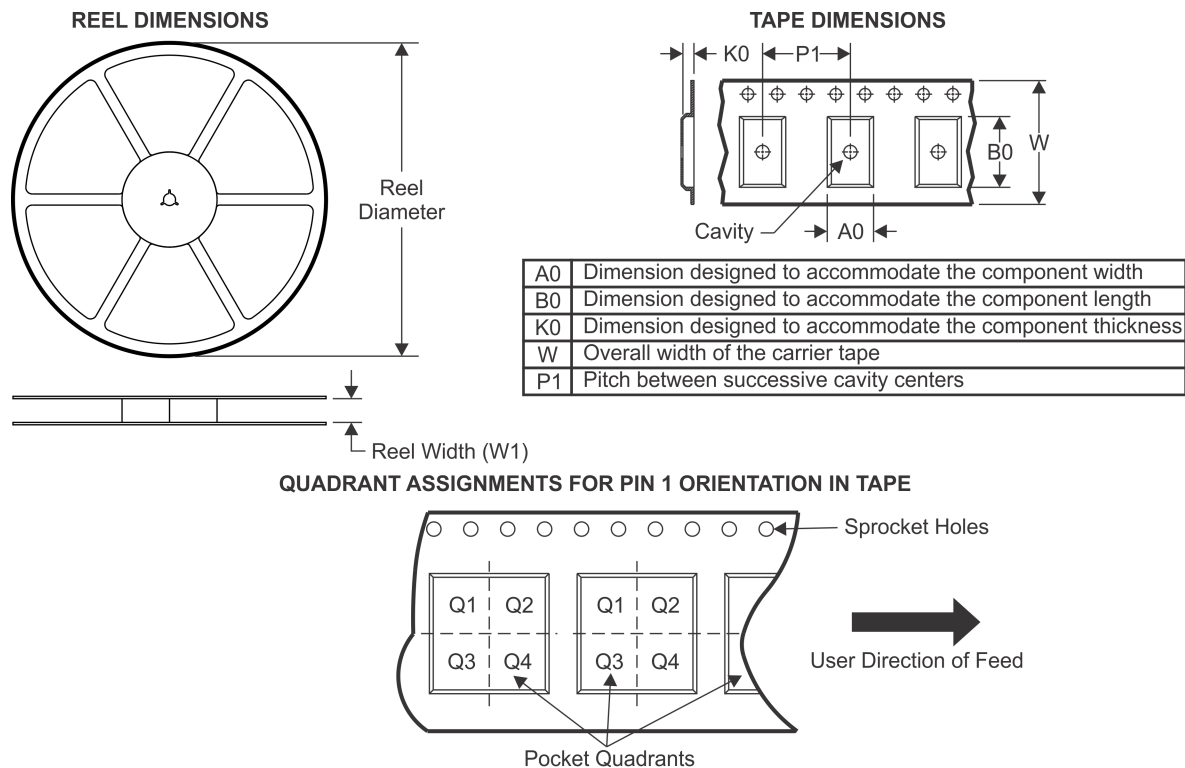
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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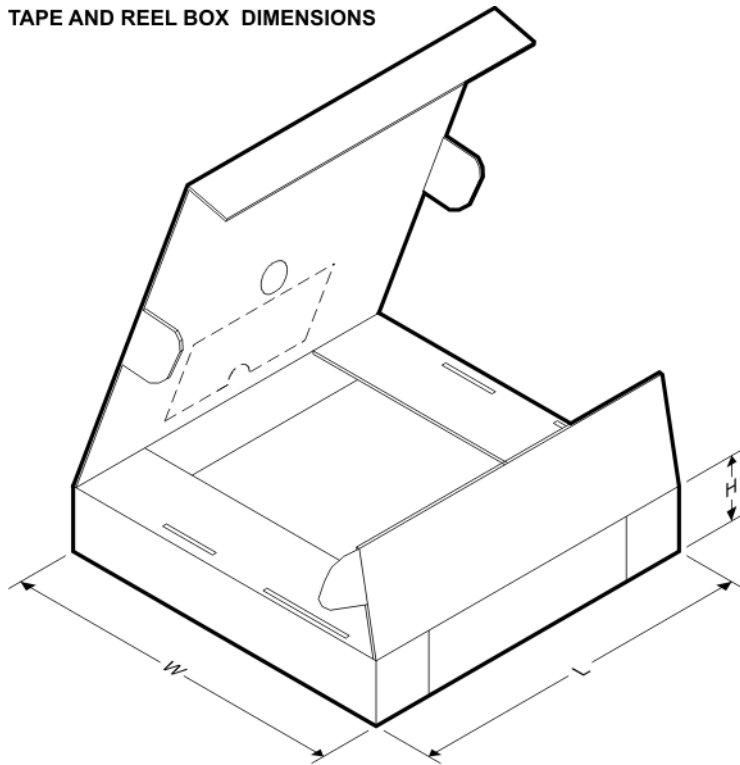
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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

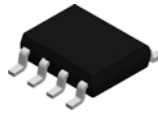
| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65LBC031QDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN65LBC031QDRG4 | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN75LBC031DR    | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65LBC031QDR   | SOIC         | D               | 8    | 2500 | 350.0       | 350.0      | 43.0        |
| SN65LBC031QDRG4 | SOIC         | D               | 8    | 2500 | 350.0       | 350.0      | 43.0        |
| SN75LBC031DR    | SOIC         | D               | 8    | 2500 | 350.0       | 350.0      | 43.0        |

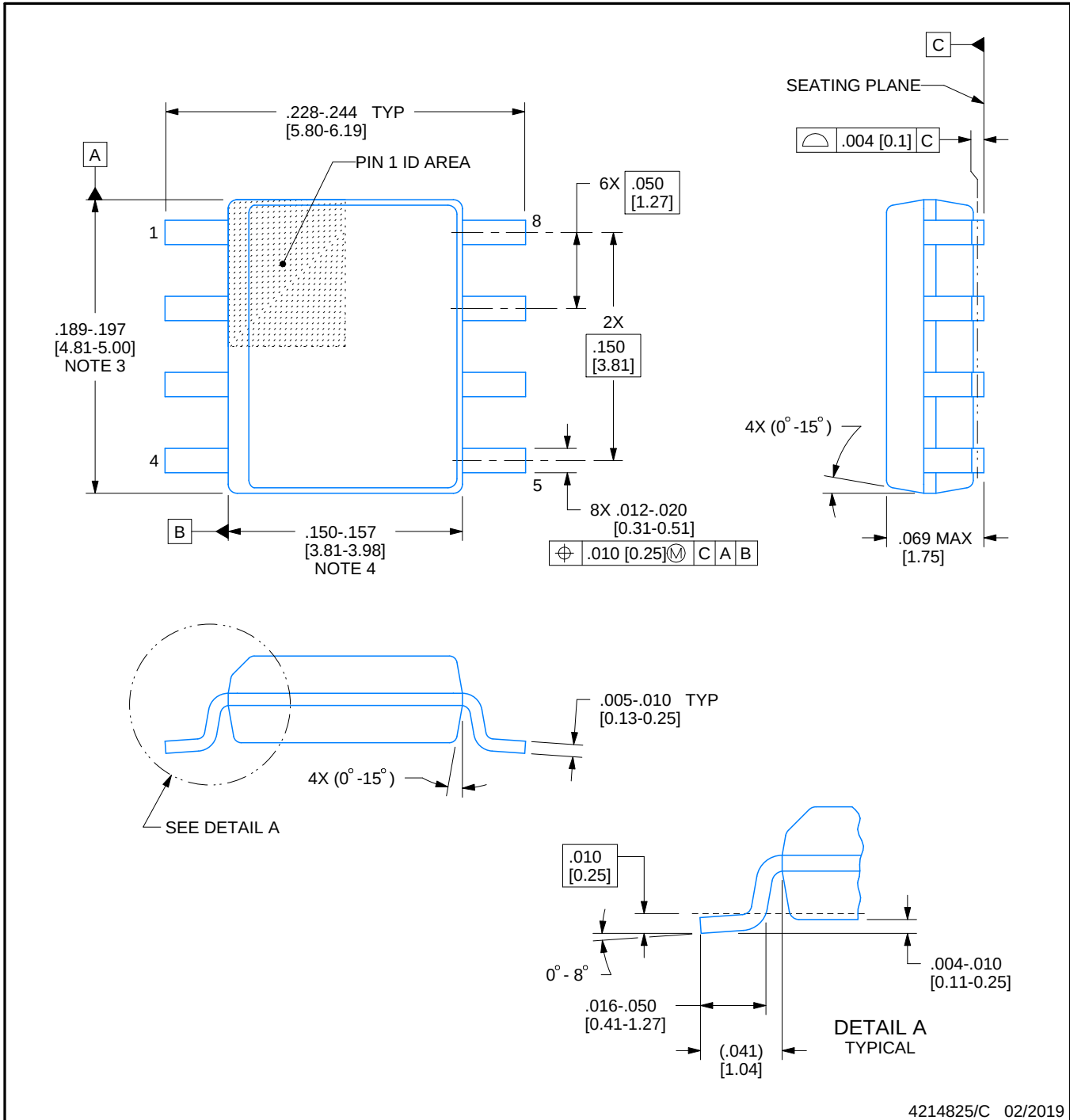


**D0008A**

# PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



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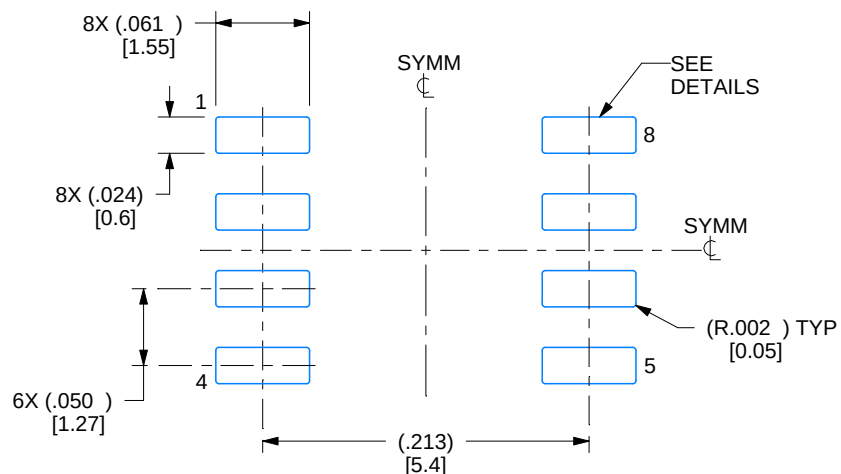
## NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

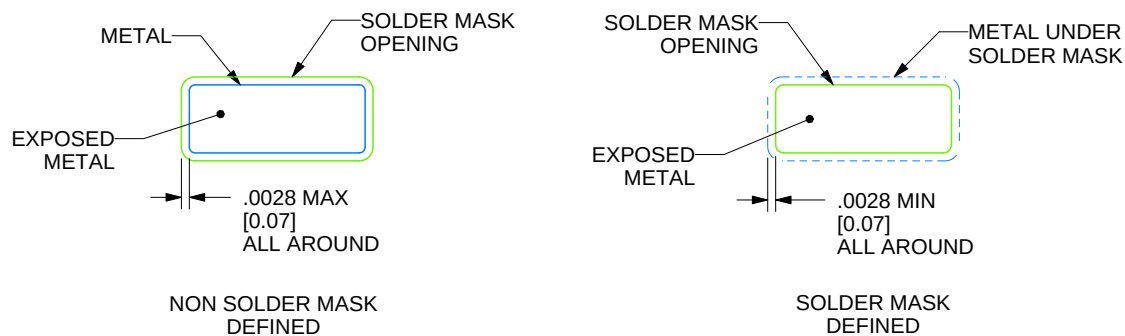
**D0008A**

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



## SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

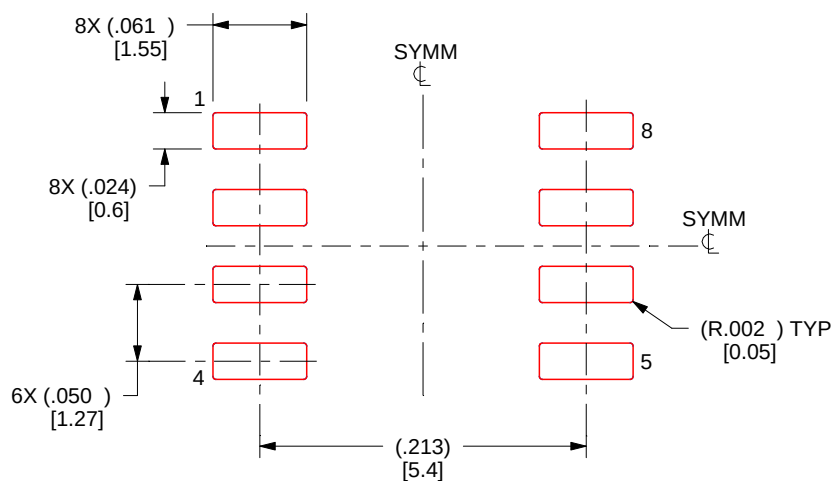


## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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