

### Features

- True and Complementary Outputs
- Buffered Inputs and Outputs
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The 'HC75 and 'HCT75 are dual 2-bit bistable transparent latches. Each one of the 2-bit latches is controlled by separate Enable inputs ( $\overline{1E}$  and  $\overline{2E}$ ) which are active LOW. When the Enable input is HIGH data enters the latch and appears at the Q output. When the Enable input ( $\overline{1E}$  and  $\overline{2E}$ ) is LOW the output is not affected.

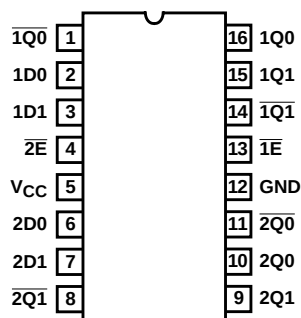
### Ordering Information

| PART NUMBER  | TEMP. RANGE (°C) | PACKAGE      |
|--------------|------------------|--------------|
| CD54HC75F3A  | -55 to 125       | 16 Ld CERDIP |
| CD54HCT75F3A | -55 to 125       | 16 Ld CERDIP |
| CD74HC75E    | -55 to 125       | 16 Ld PDIP   |
| CD74HC75M    | -55 to 125       | 16 Ld SOIC   |
| CD74HC75MT   | -55 to 125       | 16 Ld SOIC   |
| CD74HC75M96  | -55 to 125       | 16 Ld SOIC   |
| CD74HC75NSR  | -55 to 125       | 16 Ld SOP    |
| CD74HC75PW   | -55 to 125       | 16 Ld TSSOP  |
| CD74HC75PWR  | -55 to 125       | 16 Ld TSSOP  |
| CD74HCT75E   | -55 to 125       | 16 Ld PDIP   |
| CD74HCT75M   | -55 to 125       | 16 Ld SOIC   |
| CD74HCT75PWT | -55 to 125       | 16 Ld TSSOP  |

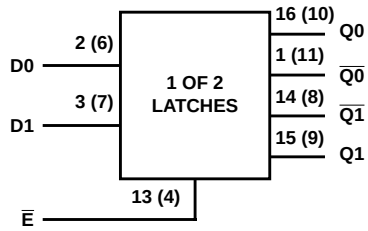
NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

### Pinout

CD54HC75, CD54HCT75 (CERDIP)  
CD74HC75 (PDIP, SOIC, SOP, TSSOP)  
CD74HCT75 (PDIP, SOIC, TSSOP)  
TOP VIEW



## Functional Diagram



TRUTH TABLE

| INPUTS |           | OUTPUTS |            |
|--------|-----------|---------|------------|
| D      | $\bar{E}$ | Q       | $\bar{Q}$  |
| L      | H         | L       | H          |
| H      | H         | H       | L          |
| X      | L         | Q0      | $\bar{Q}0$ |

H= High Level

L= Low Level

X= Don't Care

Q0 = The level of Q before the transition of  $\bar{E}$ .

## Logic Diagram

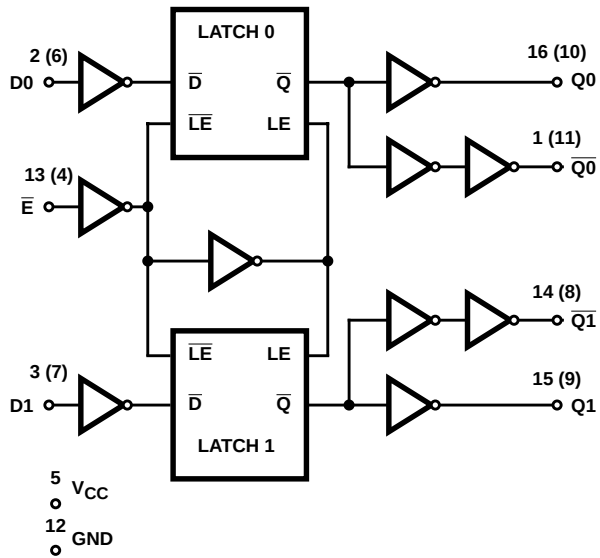


FIGURE 1. LOGIC DIAGRAM

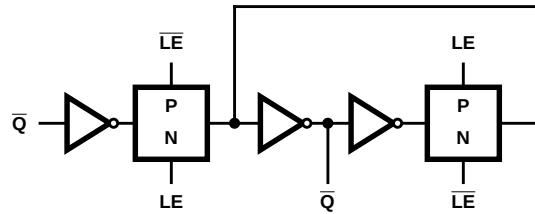


FIGURE 2. LATCH DETAIL

# CD54HC75, CD74HC75, CD54HCT75, CD74HCT75

## Absolute Maximum Ratings

|                                                        |             |
|--------------------------------------------------------|-------------|
| DC Supply Voltage, $V_{CC}$                            | -0.5V to 7V |
| DC Input Diode Current, $I_{IK}$                       |             |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$             | $\pm 20mA$  |
| DC Drain Current, per Output, $I_O$                    |             |
| For $-0.5V < V_O < V_{CC} + 0.5V$                      | $\pm 25mA$  |
| DC Output Diode Current, $I_{OK}$                      |             |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$             | $\pm 20mA$  |
| DC Output Source or Sink Current per Output Pin, $I_O$ |             |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$             | $\pm 25mA$  |
| DC $V_{CC}$ or Ground Current, $I_{CC}$                | $\pm 50mA$  |

## Thermal Information

|                                                        |                |
|--------------------------------------------------------|----------------|
| Package Thermal Impedance, $\theta_{JA}$ (see Note 1)  |                |
| E (PDIP) package                                       | 67°C/W         |
| M (SOIC) package                                       | 73°C/W         |
| NS (SOP) package                                       | 64°C/W         |
| PW (TSSOP) package                                     | 108°C/W        |
| Maximum Junction Temperature (Hermetic Package or Die) | 175°C          |
| Maximum Junction Temperature (Plastic Package)         | 150°C          |
| Maximum Storage Temperature Range                      | -65°C to 150°C |
| Maximum Lead Temperature (Soldering 10s)               | 300°C          |
| (SOIC - Lead Tips Only)                                |                |

## Operating Conditions

|                                        |                |
|----------------------------------------|----------------|
| Temperature Range, $T_A$               | -55°C to 125°C |
| Supply Voltage Range, $V_{CC}$         |                |
| HC Types                               | 2V to 6V       |
| HCT Types                              | 4.5V to 5.5V   |
| DC Input or Output Voltage, $V_I, V_O$ | 0V to $V_{CC}$ |
| Input Rise and Fall Time               |                |
| 2V                                     | 1000ns (Max)   |
| 4.5V                                   | 500ns (Max)    |
| 6V                                     | 400ns (Max)    |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER                               | SYMBOL          | TEST CONDITIONS                       |                     | V <sub>CC</sub> (V) | 25°C |     |      | -40°C TO 85°C |      | -55°C TO 125°C |      | UNITS |
|-----------------------------------------|-----------------|---------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|------|-------|
|                                         |                 | V <sub>I</sub> (V)                    | I <sub>O</sub> (mA) |                     | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX  |       |
| HC TYPES                                |                 |                                       |                     |                     |      |     |      |               |      |                |      |       |
| High Level Input Voltage                | V <sub>IH</sub> | -                                     | -                   | 2                   | 1.5  | -   | -    | 1.5           | -    | 1.5            | -    | V     |
|                                         |                 |                                       |                     | 4.5                 | 3.15 | -   | -    | 3.15          | -    | 3.15           | -    | V     |
|                                         |                 |                                       |                     | 6                   | 4.2  | -   | -    | 4.2           | -    | 4.2            | -    | V     |
| Low Level Input Voltage                 | V <sub>IL</sub> | -                                     | -                   | 2                   | -    | -   | 0.5  | -             | 0.5  | -              | 0.5  | V     |
|                                         |                 |                                       |                     | 4.5                 | -    | -   | 1.35 | -             | 1.35 | -              | 1.35 | V     |
|                                         |                 |                                       |                     | 6                   | -    | -   | 1.8  | -             | 1.8  | -              | 1.8  | V     |
| High Level Output Voltage<br>CMOS Loads | V <sub>OH</sub> | V <sub>IH</sub> or<br>V <sub>IL</sub> | -0.02               | 2                   | 1.9  | -   | -    | 1.9           | -    | 1.9            | -    | V     |
|                                         |                 |                                       |                     | 4.5                 | 4.4  | -   | -    | 4.4           | -    | 4.4            | -    | V     |
|                                         |                 |                                       |                     | 6                   | 5.9  | -   | -    | 5.9           | -    | 5.9            | -    | V     |
| High Level Output Voltage<br>TTL Loads  |                 |                                       | -                   | -                   | -    | -   | -    | -             | -    | -              | -    | V     |
|                                         |                 |                                       | -4                  | 4.5                 | 3.98 | -   | -    | 3.84          | -    | 3.7            | -    | V     |
|                                         |                 |                                       | -5.2                | 6                   | 5.48 | -   | -    | 5.34          | -    | 5.2            | -    | V     |
| Low Level Output Voltage<br>CMOS Loads  | V <sub>OL</sub> | V <sub>IH</sub> or<br>V <sub>IL</sub> | 0.02                | 2                   | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                       |                     | 4.5                 | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                       |                     | 6                   | -    | -   | 0.1  | -             | 0.1  | -              | 0.1  | V     |
| Low Level Output Voltage<br>TTL Loads   |                 |                                       | -                   | -                   | -    | -   | -    | -             | -    | -              | -    | V     |
|                                         |                 |                                       | 4                   | 4.5                 | -    | -   | 0.26 | -             | 0.33 | -              | 0.4  | V     |
|                                         |                 |                                       | 5.2                 | 6                   | -    | -   | 0.26 | -             | 0.33 | -              | 0.4  | V     |
| Input Leakage Current                   | I <sub>I</sub>  | V <sub>CC</sub> or<br>GND             | -                   | 6                   | -    | -   | ±0.1 | -             | ±1   | -              | ±1   | μA    |

# CD54HC75, CD74HC75, CD54HCT75, CD74HCT75

## DC Electrical Specifications (Continued)

| PARAMETER                                                      | SYMBOL                    | TEST CONDITIONS                    |                     | V <sub>CC</sub> (V) | 25°C |     |      | -40°C TO 85°C |      | -55°C TO 125°C |     | UNITS |
|----------------------------------------------------------------|---------------------------|------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
|                                                                |                           | V <sub>I</sub> (V)                 | I <sub>O</sub> (mA) |                     | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX |       |
| Quiescent Device Current                                       | I <sub>CC</sub>           | V <sub>CC</sub> or GND             | 0                   | 6                   | -    | -   | 4    | -             | 40   | -              | 80  | μA    |
| <b>HCT TYPES</b>                                               |                           |                                    |                     |                     |      |     |      |               |      |                |     |       |
| High Level Input Voltage                                       | V <sub>IH</sub>           | -                                  | -                   | 4.5 to 5.5          | 2    | -   | -    | 2             | -    | 2              | -   | V     |
| Low Level Input Voltage                                        | V <sub>IL</sub>           | -                                  | -                   | 4.5 to 5.5          | -    | -   | 0.8  | -             | 0.8  | -              | 0.8 | V     |
| High Level Output Voltage<br>CMOS Loads                        | V <sub>OH</sub>           | V <sub>IH</sub> or V <sub>IL</sub> | - 0.02              | 4.5                 | 4.4  | -   | -    | 4.4           | -    | 4.4            | -   | V     |
| High Level Output Voltage<br>TTL Loads                         |                           |                                    | -4                  | 4.5                 | 3.98 | -   | -    | 3.84          | -    | 3.7            | -   | V     |
| Low Level Output Voltage CMOS Loads                            | V <sub>OL</sub>           | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 4.5                 | -    | -   | 0.1  | -             | 0.1  | -              | 0.1 | V     |
| Low Level Output Voltage<br>TTL Loads                          |                           |                                    | 4                   | 4.5                 | -    | -   | 0.26 | -             | 0.33 | -              | 0.4 | V     |
| Input Leakage Current                                          | I <sub>I</sub>            | V <sub>CC</sub> and GND            | -                   | 5.5                 | -    |     | ±0.1 | -             | ±1   | -              | ±1  | μA    |
| Quiescent Device Current                                       | I <sub>CC</sub>           | V <sub>CC</sub> or GND             | 0                   | 5.5                 | -    | -   | 4    | -             | 40   | -              | 80  | μA    |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ΔI <sub>CC</sub> (Note 2) | V <sub>CC</sub> - 2.1              | -                   | 4.5 to 5.5          | -    | 100 | 360  | -             | 450  | -              | 490 | μA    |

NOTE:

- For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

## HCT Input Loading Table

| INPUT  | UNIT LOADS |
|--------|------------|
| D0, D1 | 0.8        |
| 1E, 2E | 1.2        |

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Specifications table, e.g., 360μA max at 25°C.

## Prerequisite For Switching Specifications

| PARAMETER                | SYMBOL          | TEST CONDITIONS | V <sub>CC</sub> (V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|--------------------------|-----------------|-----------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                          |                 |                 |                     | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| HC TYPES                 |                 |                 |                     |      |     |     |               |     |                |     |       |
| Pulse Width Enable Input | t <sub>W</sub>  | -               | 2                   | 80   | -   | -   | 100           | -   | 120            | -   | ns    |
|                          |                 |                 | 4.5                 | 16   | -   | -   | 20            | -   | 24             | -   | ns    |
|                          |                 |                 | 6                   | 14   | -   | -   | 17            | -   | 20             | -   | ns    |
| Setup Time D to Enable   | t <sub>SU</sub> | -               | 2                   | 60   | -   | -   | 75            | -   | 90             | -   | ns    |
|                          |                 |                 | 4.5                 | 12   | -   | -   | 15            | -   | 18             | -   | ns    |
|                          |                 |                 | 6                   | 10   | -   | -   | 13            | -   | 15             | -   | ns    |

# CD54HC75, CD74HC75, CD54HCT75, CD74HCT75

## Prerequisite For Switching Specifications (Continued)

| PARAMETER                | SYMBOL          | TEST CONDITIONS | V <sub>CC</sub> (V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|--------------------------|-----------------|-----------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                          |                 |                 |                     | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| Hold Time Enable to D    | t <sub>H</sub>  | -               | 2                   | 3    | -   | -   | 3             | -   | 3              | -   | ns    |
|                          |                 |                 | 4.5                 | 3    | -   | -   | 3             | -   | 3              | -   | ns    |
|                          |                 |                 | 6                   | 3    | -   | -   | 3             | -   | 3              | -   | ns    |
| HCT TYPES                |                 |                 |                     |      |     |     |               |     |                |     |       |
| Pulse Width Enable Input | t <sub>W</sub>  | -               | 4.5                 | 16   | -   | -   | 20            | -   | 24             | -   | ns    |
| Setup Time D to Enable   | t <sub>SU</sub> | -               | 4.5                 | 12   | -   | -   | 15            | -   | 18             | -   | ns    |
| Hold Time Enable to D    | t <sub>H</sub>  | -               | 4.5                 | 3    | -   | -   | 3             | -   | 3              | -   | ns    |

## Switching Specifications Input t<sub>r</sub>, t<sub>f</sub> = 6ns

| PARAMETER                                  | SYMBOL                              | TEST CONDITIONS       | V <sub>CC</sub> (V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|--------------------------------------------|-------------------------------------|-----------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                                            |                                     |                       |                     | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| HC TYPES                                   |                                     |                       |                     |      |     |     |               |     |                |     |       |
| Propagation Delay, Data to Q               | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 110 | -             | 140 | -              | 165 | ns    |
|                                            |                                     | C <sub>L</sub> = 50pF | 4.5                 | -    | -   | 22  | -             | 28  | -              | 33  | ns    |
|                                            |                                     | C <sub>L</sub> = 15pF | 5                   | -    | 9   | -   | -             | -   | -              | -   | ns    |
|                                            |                                     | C <sub>L</sub> = 50pF | 6                   | -    | -   | 19  | -             | 24  | -              | 28  | ns    |
| Propagation Delay, Data to Q̄              | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 130 | -             | 165 | -              | 195 | ns    |
|                                            |                                     | C <sub>L</sub> = 50pF | 4.5                 | -    | -   | 26  | -             | 33  | -              | 39  | ns    |
|                                            |                                     | C <sub>L</sub> = 15pF | 5                   | -    | 10  | -   | -             | -   | -              | -   | ns    |
|                                            |                                     | C <sub>L</sub> = 50pF | 6                   | -    | -   | 22  | -             | 28  | -              | 33  | ns    |
| Propagation Delay, Enable to Q             | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 130 | -             | 165 | -              | 195 | ns    |
|                                            |                                     | C <sub>L</sub> = 50pF | 4.5                 | -    | -   | 26  | -             | 33  | -              | 39  | ns    |
|                                            |                                     | C <sub>L</sub> = 15pF | 5                   | -    | 10  | -   | -             | -   | -              | -   | ns    |
|                                            |                                     | C <sub>L</sub> = 50pF | 6                   | -    | -   | 22  | -             | 28  | -              | 33  | ns    |
| Propagation Delay, Enable to Q̄            | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 130 | -             | 165 | -              | 195 | ns    |
|                                            |                                     | C <sub>L</sub> = 50pF | 4.5                 | -    | -   | 26  | -             | 33  | -              | 39  | ns    |
|                                            |                                     | C <sub>L</sub> = 15pF | 5                   | -    | 11  | -   | -             | -   | -              | -   | ns    |
|                                            |                                     | C <sub>L</sub> = 50pF | 6                   | -    | -   | 22  | -             | 28  | -              | 33  | ns    |
| Output Transition Time                     | t <sub>TLH</sub> , t <sub>THL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 75  | -             | 95  | -              | 110 | ns    |
|                                            |                                     | C <sub>L</sub> = 50pF | 4.5                 | -    | -   | 15  | -             | 19  | -              | 22  | ns    |
|                                            |                                     | C <sub>L</sub> = 50pF | 6                   | -    | -   | 13  | -             | 16  | -              | 19  | ns    |
| Input Capacitance                          | C <sub>I</sub>                      | -                     | -                   | -    | -   | 10  | -             | 10  | -              | 10  | pF    |
| Power Dissipation Capacitance (Notes 3, 4) | C <sub>PD</sub>                     | -                     | 5                   | -    | 46  | -   | -             | -   | -              | -   | pF    |
| HCT TYPES                                  |                                     |                       |                     |      |     |     |               |     |                |     |       |
| Propagation Delay, Data to Q               | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 4.5                 | -    | -   | 28  | -             | 35  | -              | 42  | ns    |
|                                            |                                     | C <sub>L</sub> = 15pF | 5                   | -    | 11  | -   | -             | -   | -              | -   | ns    |
| Propagation Delay, Data to Q̄              | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 4.5                 | -    | -   | 28  | -             | 35  | -              | 42  | ns    |
|                                            |                                     | C <sub>L</sub> = 15pF | 5                   | -    | 11  | -   | -             | -   | -              | -   | ns    |
| Propagation Delay, Enable to Q             | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 4.5                 | -    | -   | 28  | -             | 35  | -              | 42  | ns    |
|                                            |                                     | C <sub>L</sub> = 15pF | 5                   |      | 11  | -   | -             | -   | -              | -   | ns    |

# CD54HC75, CD74HC75, CD54HCT75, CD74HCT75

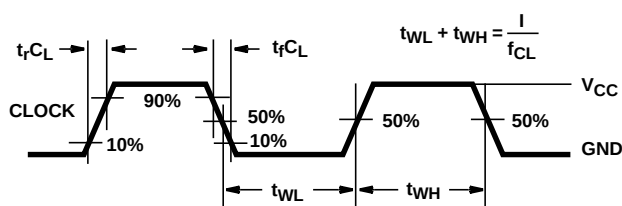
## Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

| PARAMETER                                     | SYMBOL             | TEST CONDITIONS     | $V_{CC}$<br>(V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|-----------------------------------------------|--------------------|---------------------|-----------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                                               |                    |                     |                 | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| Propagation Delay,<br>Enable to $\bar{Q}$     | $t_{PLH}, t_{PHL}$ | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 30  | -             | 38  | -              | 45  | ns    |
|                                               |                    | $C_L = 15\text{pF}$ | 5               | -    | 12  | -   | -             | -   | -              | -   | ns    |
| Output Transition Time                        | $t_{TLH}, t_{THL}$ | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 15  | -             | 19  | -              | 22  | ns    |
| Input Capacitance                             | $C_I$              | -                   | -               | -    | -   | 10  | -             | 10  | -              | 10  | pF    |
| Power Dissipation Capacitance<br>(Notes 3, 4) | $C_{PD}$           | -                   | 5               | -    | 46  | -   | -             | -   | -              | -   | pF    |

### NOTES:

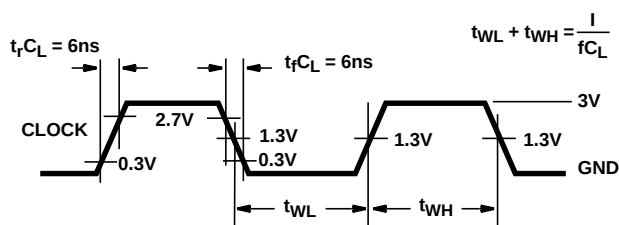
- $C_{PD}$  is used to determine the dynamic power consumption, per latch.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

## Test Circuits and Waveforms



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

FIGURE 3. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

FIGURE 4. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

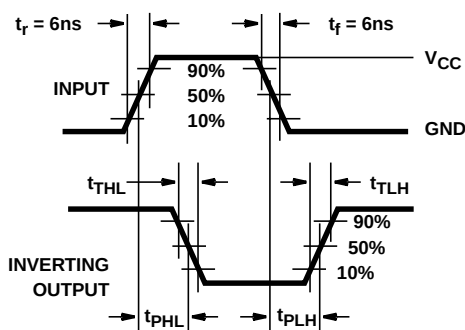


FIGURE 5. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

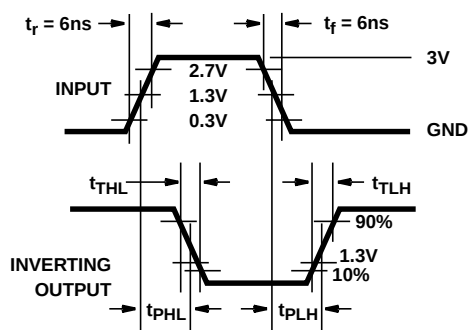


FIGURE 6. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

**Test Circuits and Waveforms (Continued)**

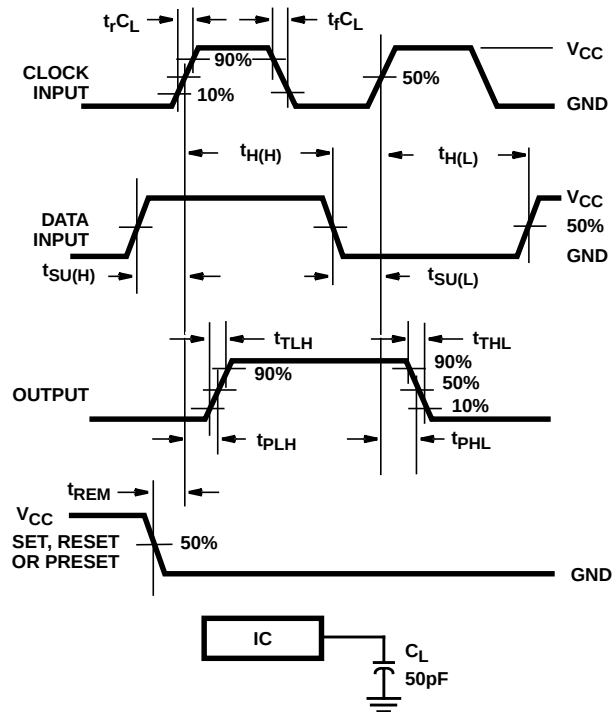


FIGURE 7. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

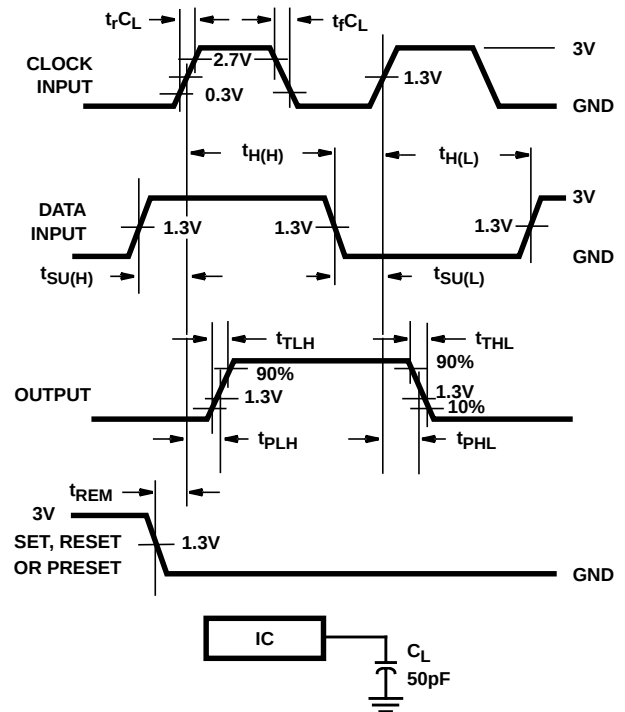


FIGURE 8. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)             | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------------------|-------------------------|
| 5962-9075801MEA  | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 5962-9075801ME<br>A<br>CD54HCT75F3A | <a href="#">Samples</a> |
| 8407001EA        | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 8407001EA<br>CD54HC75F3A            | <a href="#">Samples</a> |
| CD54HC75F3A      | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 8407001EA<br>CD54HC75F3A            | <a href="#">Samples</a> |
| CD54HCT75F3A     | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 5962-9075801ME<br>A<br>CD54HCT75F3A | <a href="#">Samples</a> |
| CD74HC75E        | ACTIVE        | PDIP         | N                  | 16   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | N / A for Pkg Type   | -55 to 125   | CD74HC75E                           | <a href="#">Samples</a> |
| CD74HC75M        | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HC75M                               | <a href="#">Samples</a> |
| CD74HC75M96      | ACTIVE        | SOIC         | D                  | 16   | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HC75M                               | <a href="#">Samples</a> |
| CD74HC75MT       | ACTIVE        | SOIC         | D                  | 16   | 250            | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HC75M                               | <a href="#">Samples</a> |
| CD74HC75PW       | ACTIVE        | TSSOP        | PW                 | 16   | 90             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HJ75                                | <a href="#">Samples</a> |
| CD74HC75PWR      | ACTIVE        | TSSOP        | PW                 | 16   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HJ75                                | <a href="#">Samples</a> |
| CD74HC75PWRG4    | ACTIVE        | TSSOP        | PW                 | 16   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HJ75                                | <a href="#">Samples</a> |
| CD74HC75PWT      | ACTIVE        | TSSOP        | PW                 | 16   | 250            | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HJ75                                | <a href="#">Samples</a> |
| CD74HCT75E       | ACTIVE        | PDIP         | N                  | 16   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | N / A for Pkg Type   | -55 to 125   | CD74HCT75E                          | <a href="#">Samples</a> |
| CD74HCT75EE4     | ACTIVE        | PDIP         | N                  | 16   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | N / A for Pkg Type   | -55 to 125   | CD74HCT75E                          | <a href="#">Samples</a> |
| CD74HCT75M       | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | -55 to 125   | HCT75M                              | <a href="#">Samples</a> |

<sup>(1)</sup> The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.



**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD54HC75, CD54HCT75, CD74HC75, CD74HCT75 :**

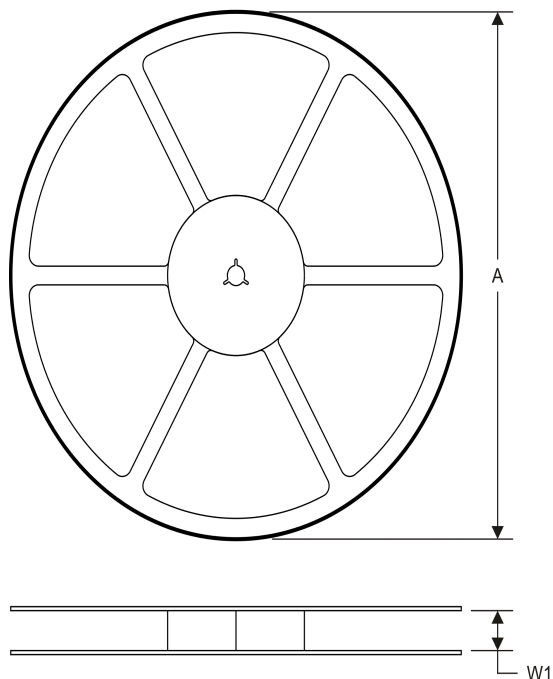
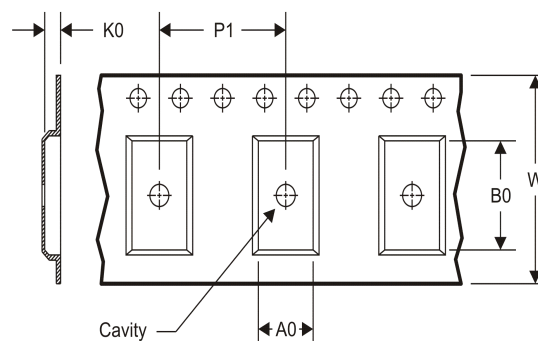
• Catalog: [CD74HC75](#), [CD74HCT75](#)

• Military: [CD54HC75](#), [CD54HCT75](#)

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

- 
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


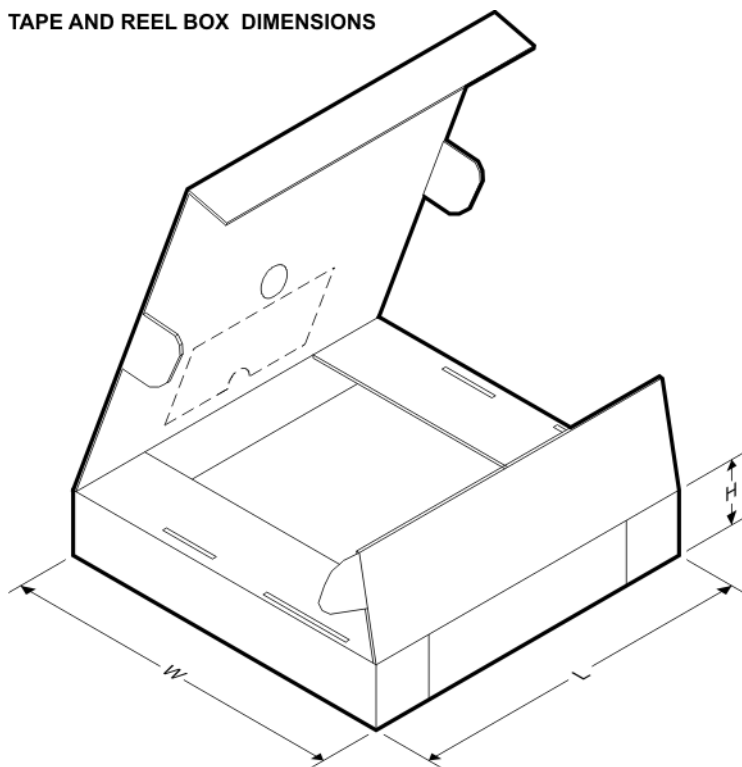
|    |                                                           |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC75M96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HC75PWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| CD74HC75PWT | TSSOP        | PW              | 16   | 250  | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



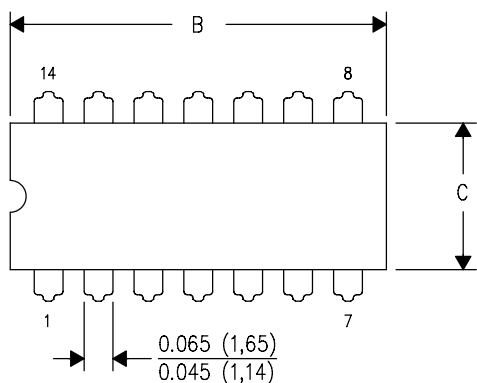
\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC75M96 | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| CD74HC75PWR | TSSOP        | PW              | 16   | 2000 | 367.0       | 367.0      | 35.0        |
| CD74HC75PWT | TSSOP        | PW              | 16   | 250  | 367.0       | 367.0      | 35.0        |

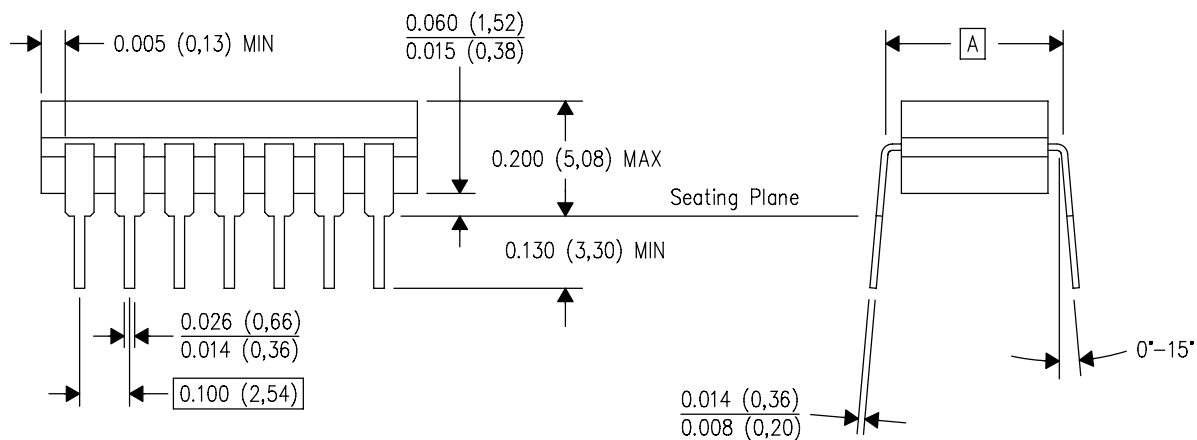
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



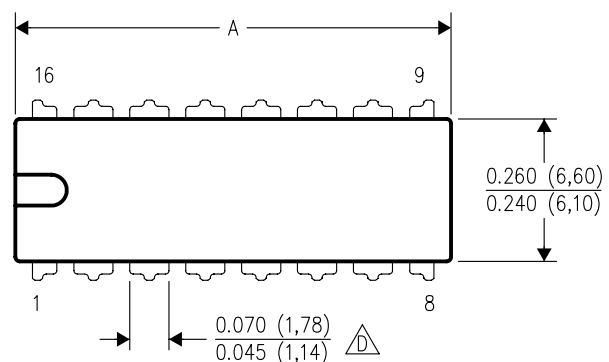
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

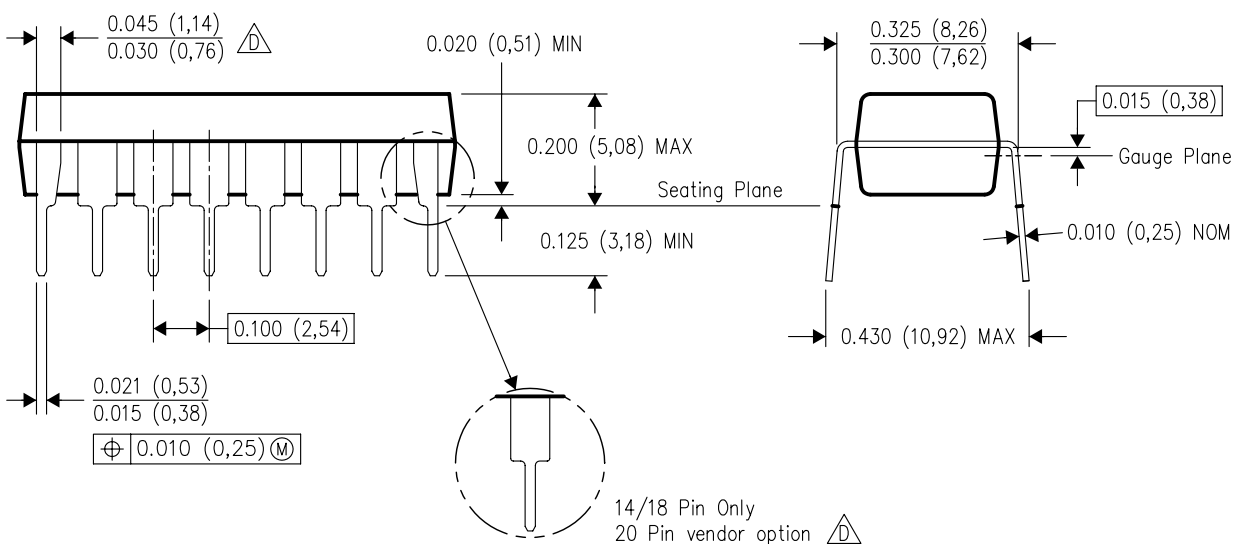
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



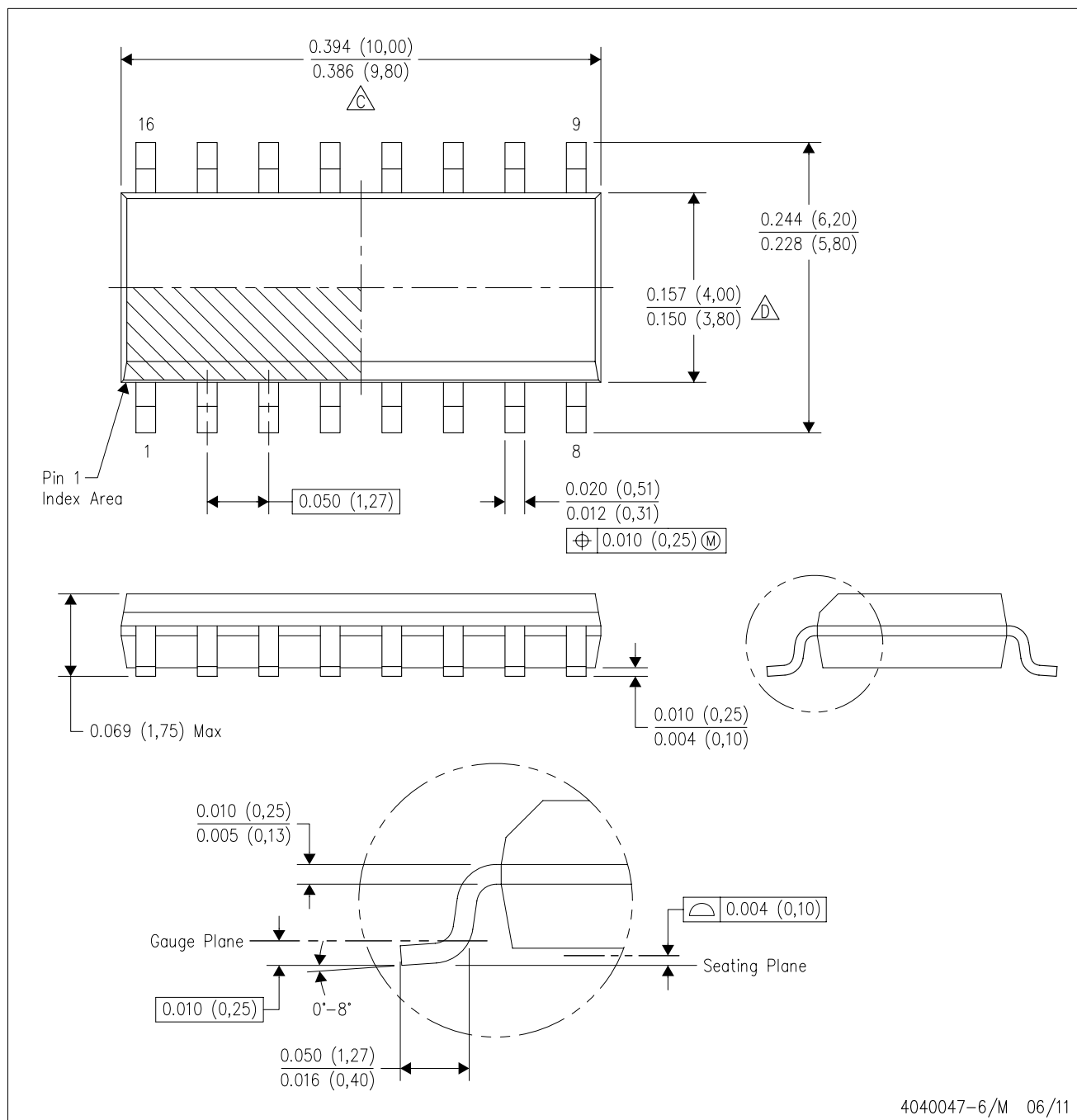
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



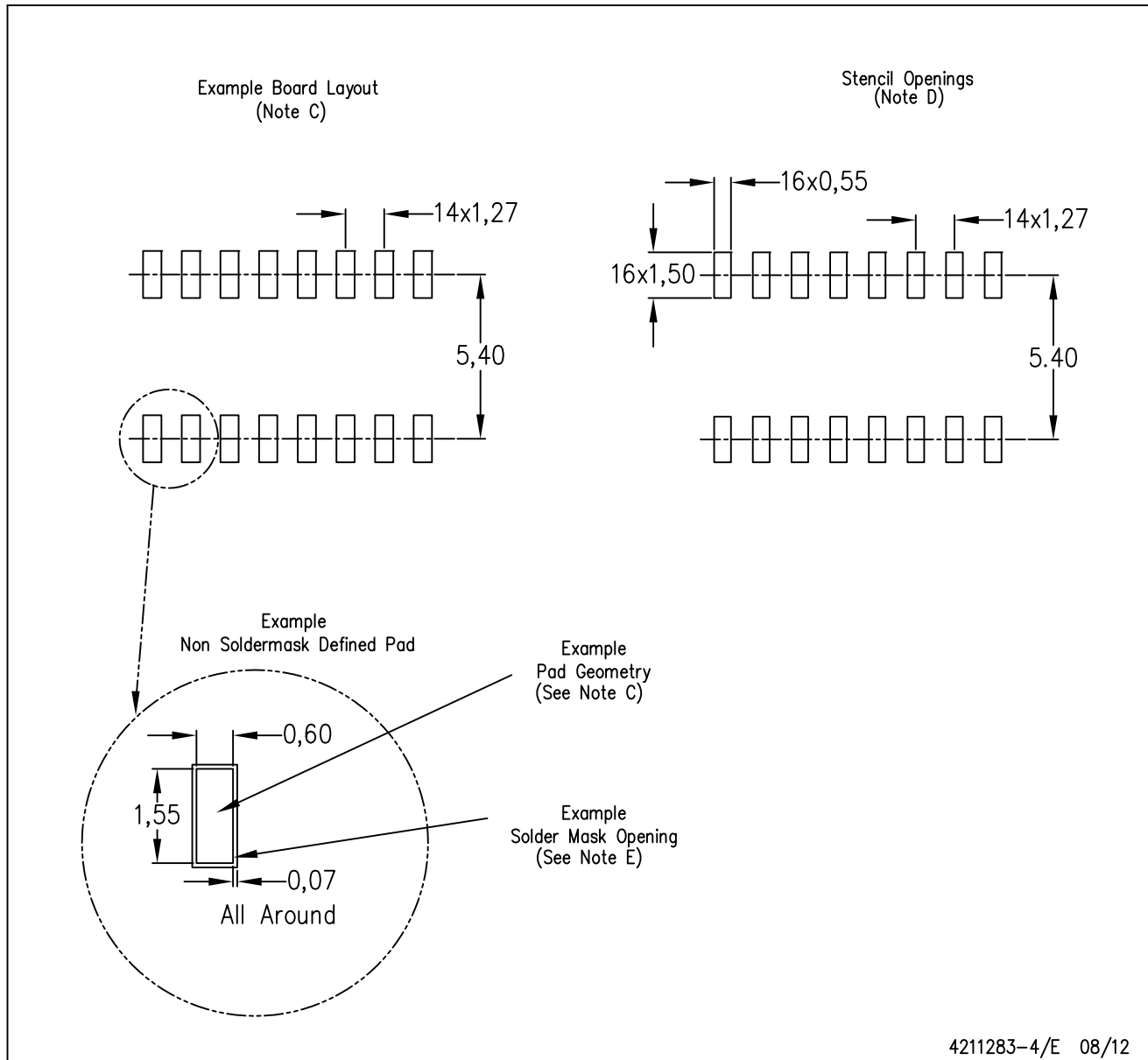
4040047-6/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.





## PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



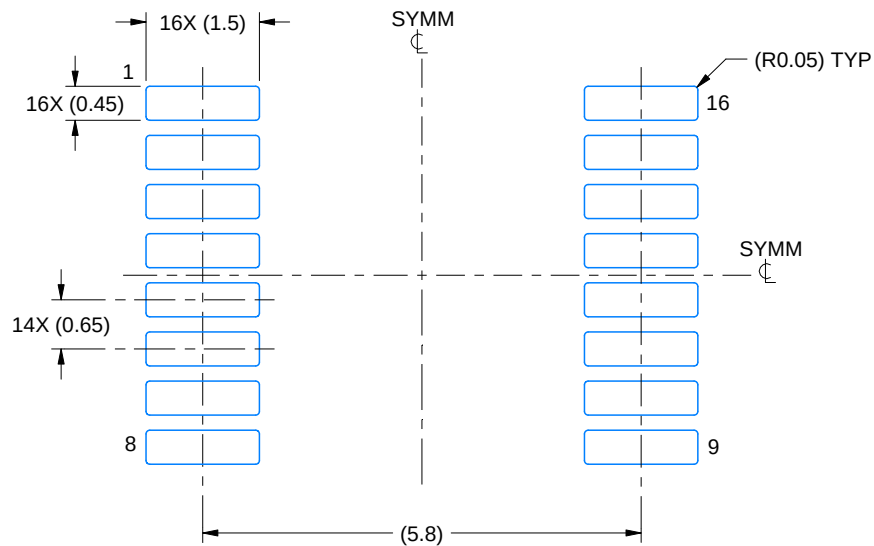
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

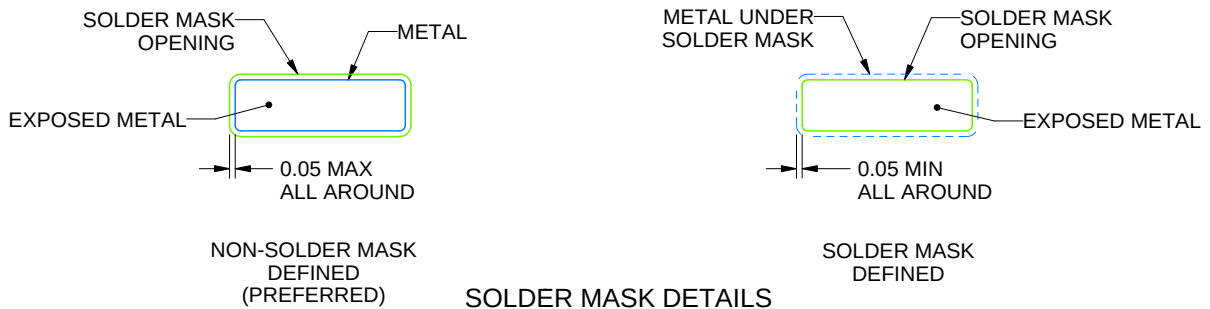
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

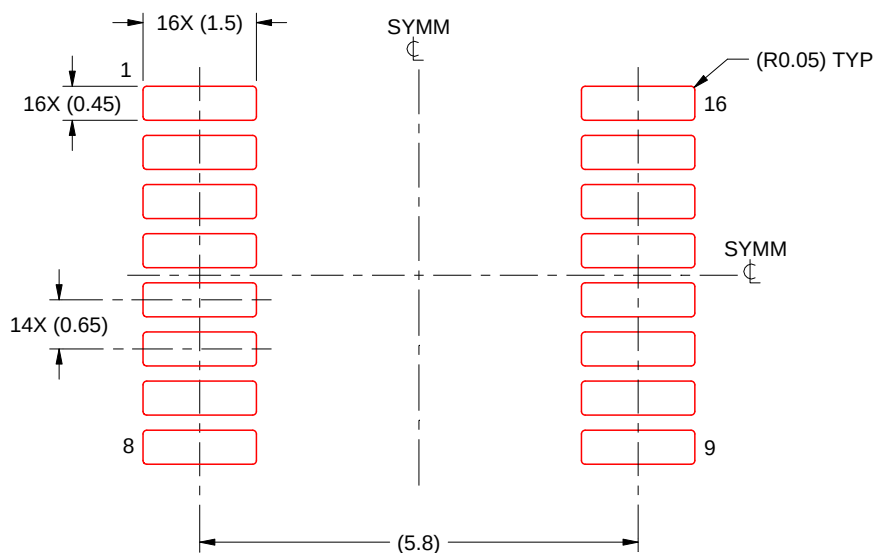
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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