KSZ8863RLL Reference Design Revision 1.0

REVISION HISTORY

DATE:	DESCRIPTION	REVISION
05/30/2009	Initial Draft	1.0

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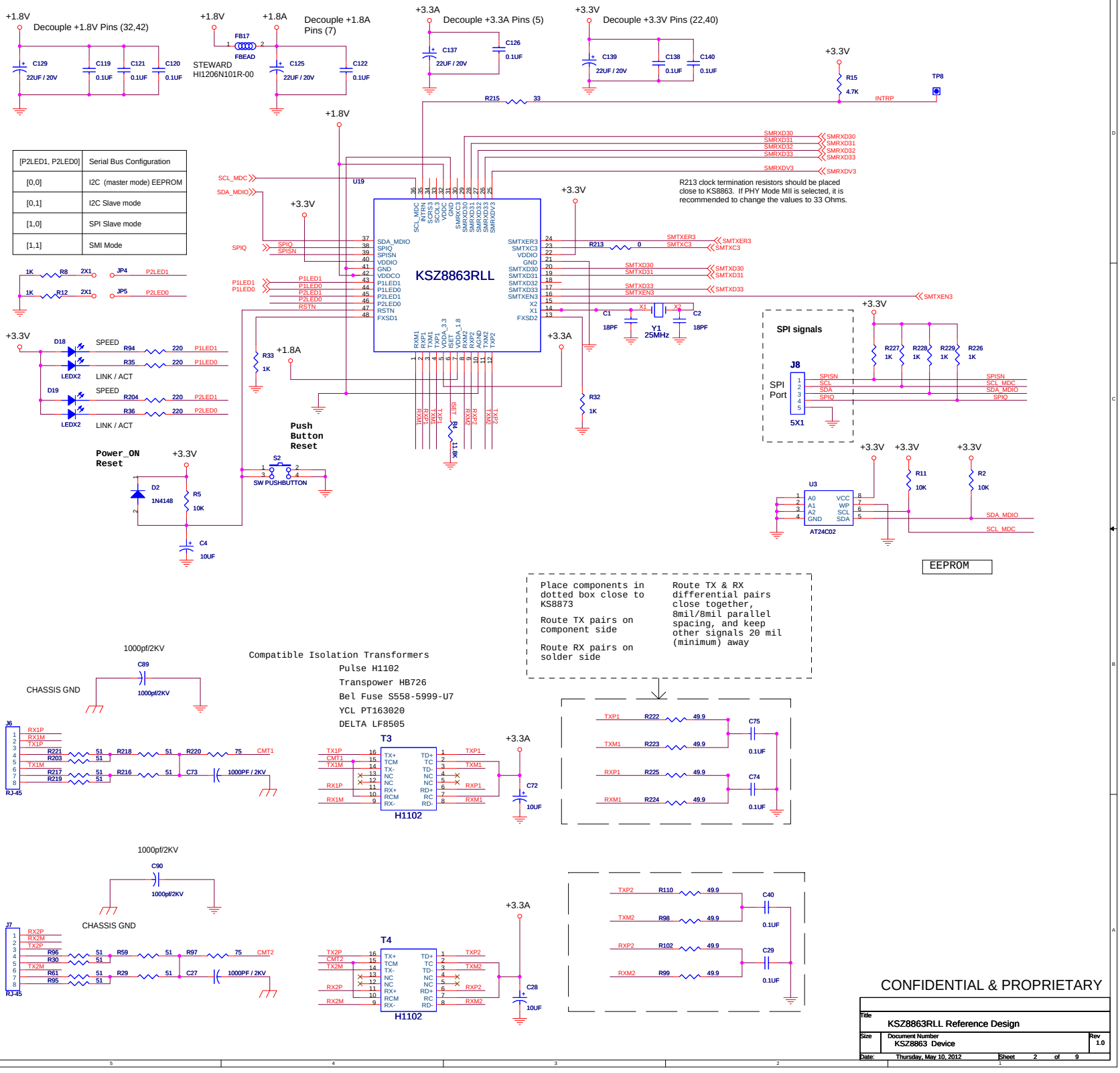

[P2LED1, P2LED0]	Serial Bus Configuration
[0,0]	I2C (master mode) EEPROM
[0,1]	I2C Slave mode
[1,0]	SPI Slave mode
[1,1]	SMI Mode

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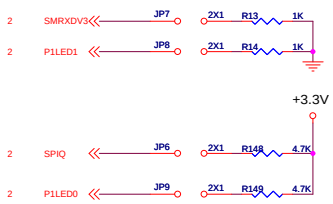
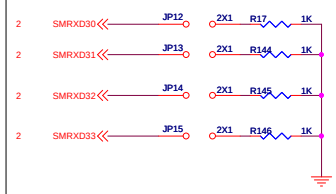
PORT 1



JP6	Force Flow Control High = Enable Off (default) = Disable
JP7	Force Full/Half Off = Full Duplex Low = Half Duplex
JP8	Force Speed Off = 100BaseTX Low = 10BaseT
JP9	Auto-negotiation High = Enable Off(default) = Disable

PORT 2



JP12	Force Flow Control Off = ENABLE Low = DISABLE
JP13	Force Full/Half Off = Full Duplex Low = Half Duplex
JP14	Force Speed Off = 100BaseTX Low = 10BaseT
JP15	Auto-negotiation Off = ENABLE Low = DISABLE

RMII option

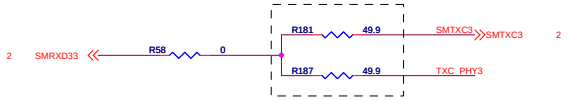
KS8863RLL provides RMII signals with respect to both PHY and MAC sides.

For this board, the KS8863RLL provides RMII signals with respect to MAC side only. The RMII signal connections between KS8863RLL and external PHY are shown in the table to the right.

The KSZ8863RLL can provide the 50MHz reference clock by disconnect JP19 to enable REFCLKO.

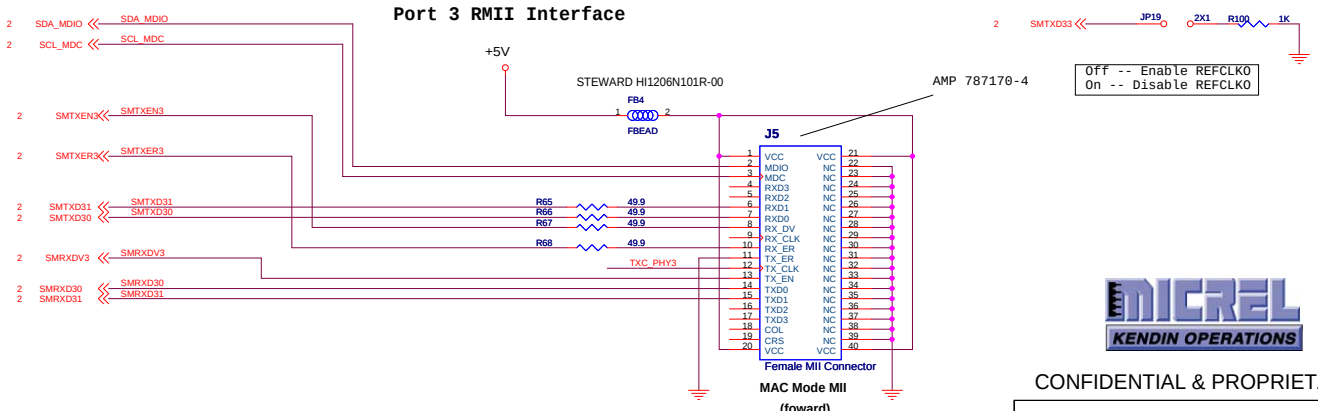
The KSZ8863RLL can use internal or external reference clock which is selected by register 198 bit 3.
For external, it is set to 0, vice reverse.

External PHY RMII (with respect to PHY)		KSZ8863RLL RMII (with respect to MAC)		
Signal	**Type**	**Signal**	**Pin #**	**Type**
REF_CLK	Input	SMTXC3	23	Input
CRS_DV	Output	SMTXEN3	16	Input
RXD[1]	Output	SMTXD31	19	Input
RXD[0]	Output	SMTXD30	20	Input
TX_EN	Input	SMRXDV3	25	Output
TXD[1]	Input	SMRXD31	28	Output
TXD[0]	Input	SMRXD30	29	Output
RX_ER	Output	SMTXER3	24	Input



If 50MHz comes from Internal KSZ8873RLL.

Port 3 RMII Interface



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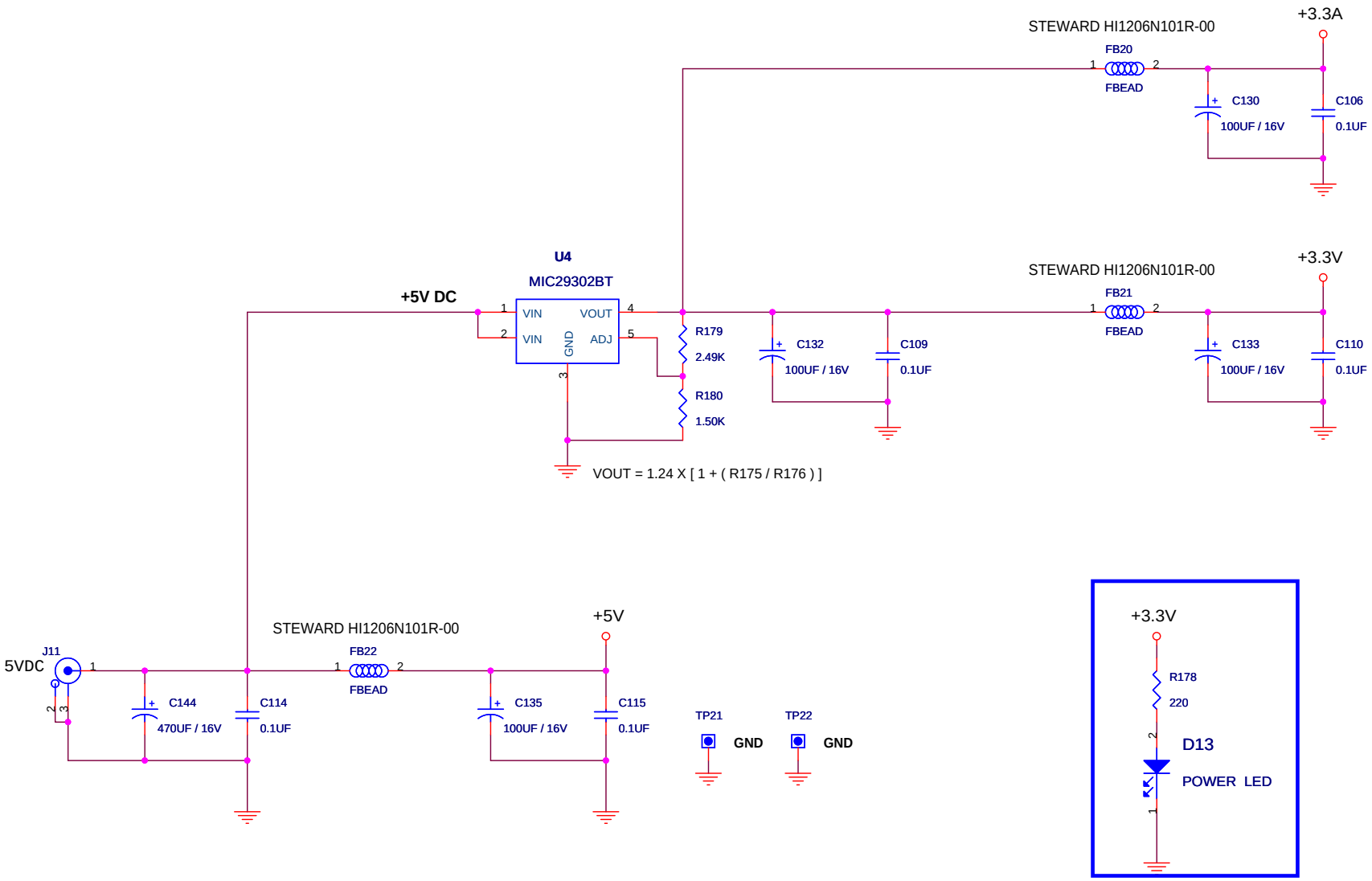

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