

KSZ8863FLL/MLL/RLL_LQFP Demo Board Revision 1.0

REVISION HISTORY

DATE:	DESCRIPTION	REVISION
04/08/2009	Initial Draft	1.0

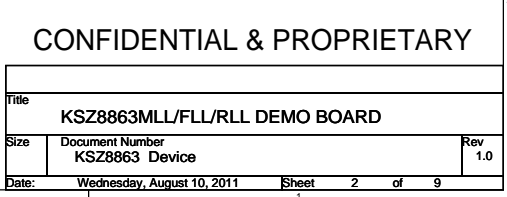
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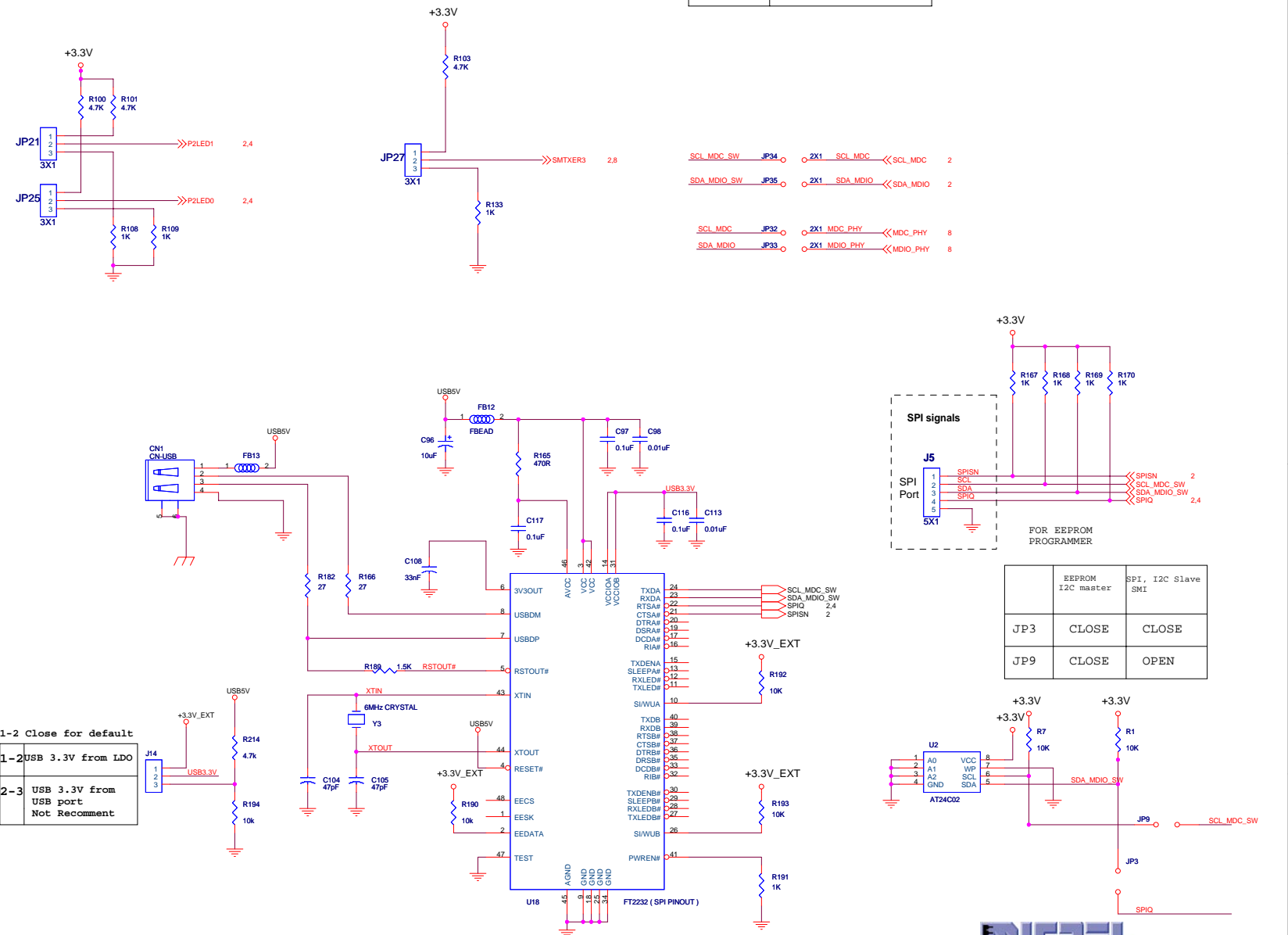
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[P2LED1, P2LED0]	Serial Bus Configuration
[0,0]	I2C (master mode) EEPROM
[0,1]	I2C Slave mode
[1,0]	SPI Slave mode
[1,1]	SMI Mode

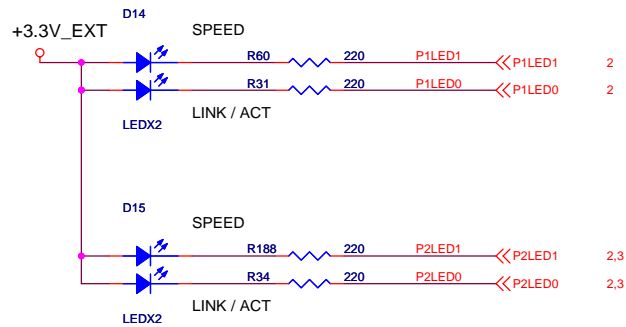
SMTXER3	SWITCH MII Configuration (For Test Only)
1	MI no link in PHY mode
0	Tie to GND in RMII mode

Bus Selection	Jumper Setting
SMI / MIIM (SW)	open JP32 and JP33. close JP34 and JP35.
I2C Master / I2C Slave / SPI Slave	open JP32 and JP33 close JP34 and JP35.
MIIM (PHY only)	close JP32 and JP33 open JP34 and JP35.

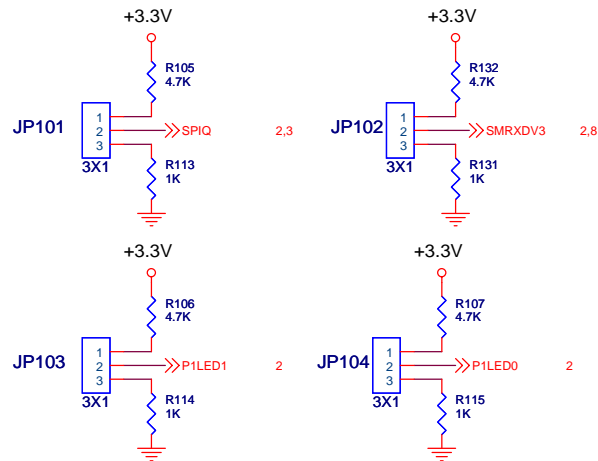


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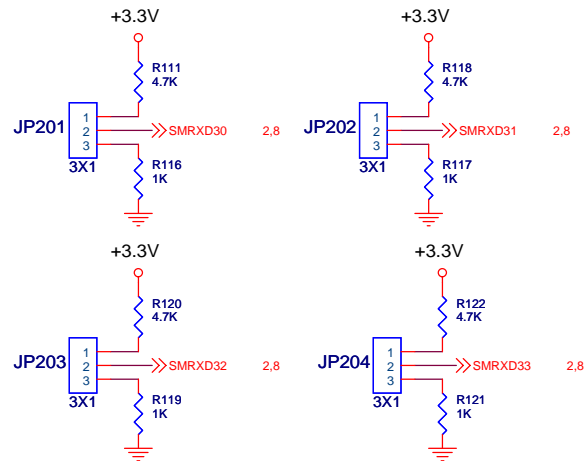
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PORT 1



PORT 2



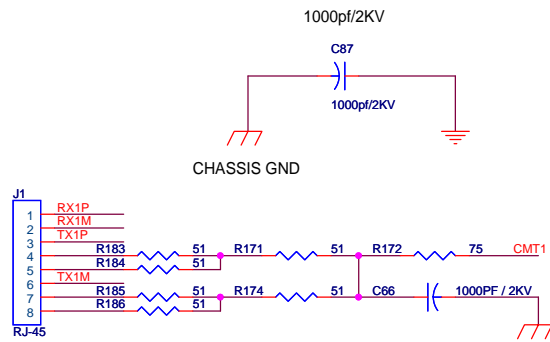
JP101	Force Flow Control Pull Up = ENABLE Pull Down = DISABLE
JP102	Force Full/Half Pull Up = Full Duplex Pull Down = Half Duplex
JP103	Force Speed Pull Up = 100BaseTX Pull Down = 10BaseT
JP104	Auto-negotiation Pull Up = ENABLE Pull Down = DISABLE(default)

JP201	Force Flow Control Pull Up = ENABLE Pull Down = DISABLE
JP202	Force Full/Half Pull Up = Full Duplex Pull Down = Half Duplex
JP203	Force Speed Pull Up = 100BaseTX Pull Down = 10BaseT
JP204	Auto-negotiation Pull Up = ENABLE Pull Down = DISABLE

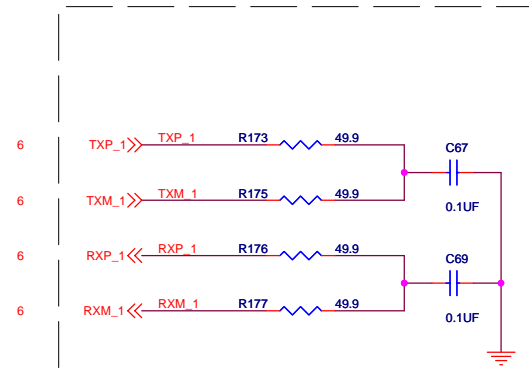
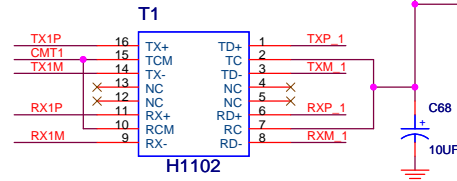


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Compatible Isolation Transformers
 Pulse H1102
 Transpower HB726
 Bel Fuse S558-5999-U7
 YCL PT163020
 DELTA LF8505



Place components in dotted box close to KS8863

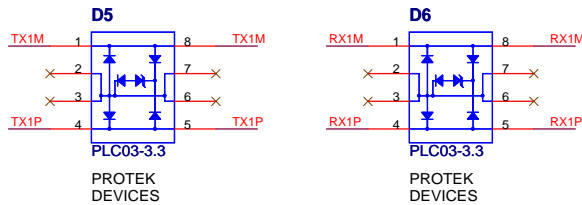
Route TX pairs on component side

Route RX pairs on solder side

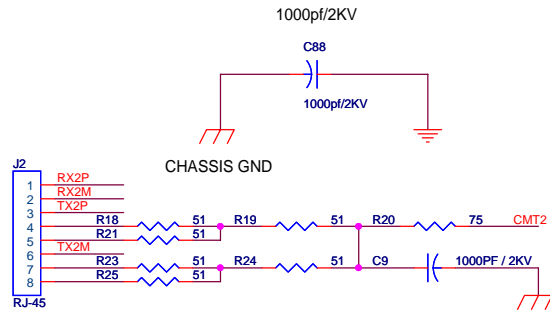
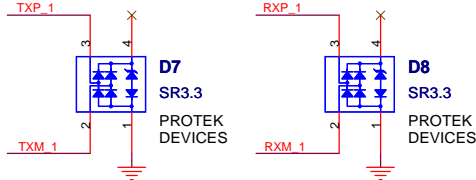
Route TX & RX differential pairs close together, 8mil/8mil parallel spacing, and keep other signals 20 mil (minimum) away

Line Side Protection (test option)

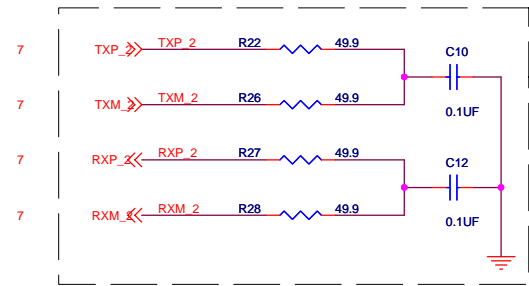
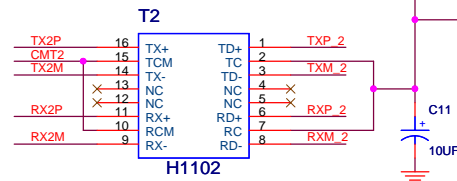
Place near RJ-45 connector



Chip Side Protection (test option)



Compatible Isolation Transformers
 Pulse H1102
 Transpower HB726
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Place components in dotted box close to KSZ8863

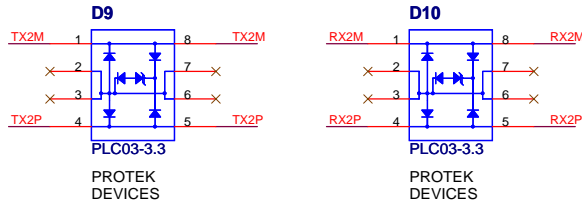
Route TX pairs on component side

Route RX pairs on solder side

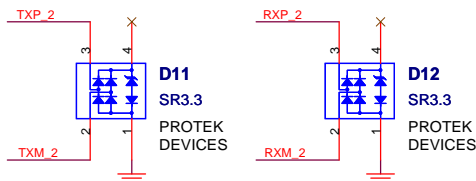
Route TX & RX differential pairs close together, 8mil/8mil parallel spacing, and keep other signals 20 mil (minimum) away

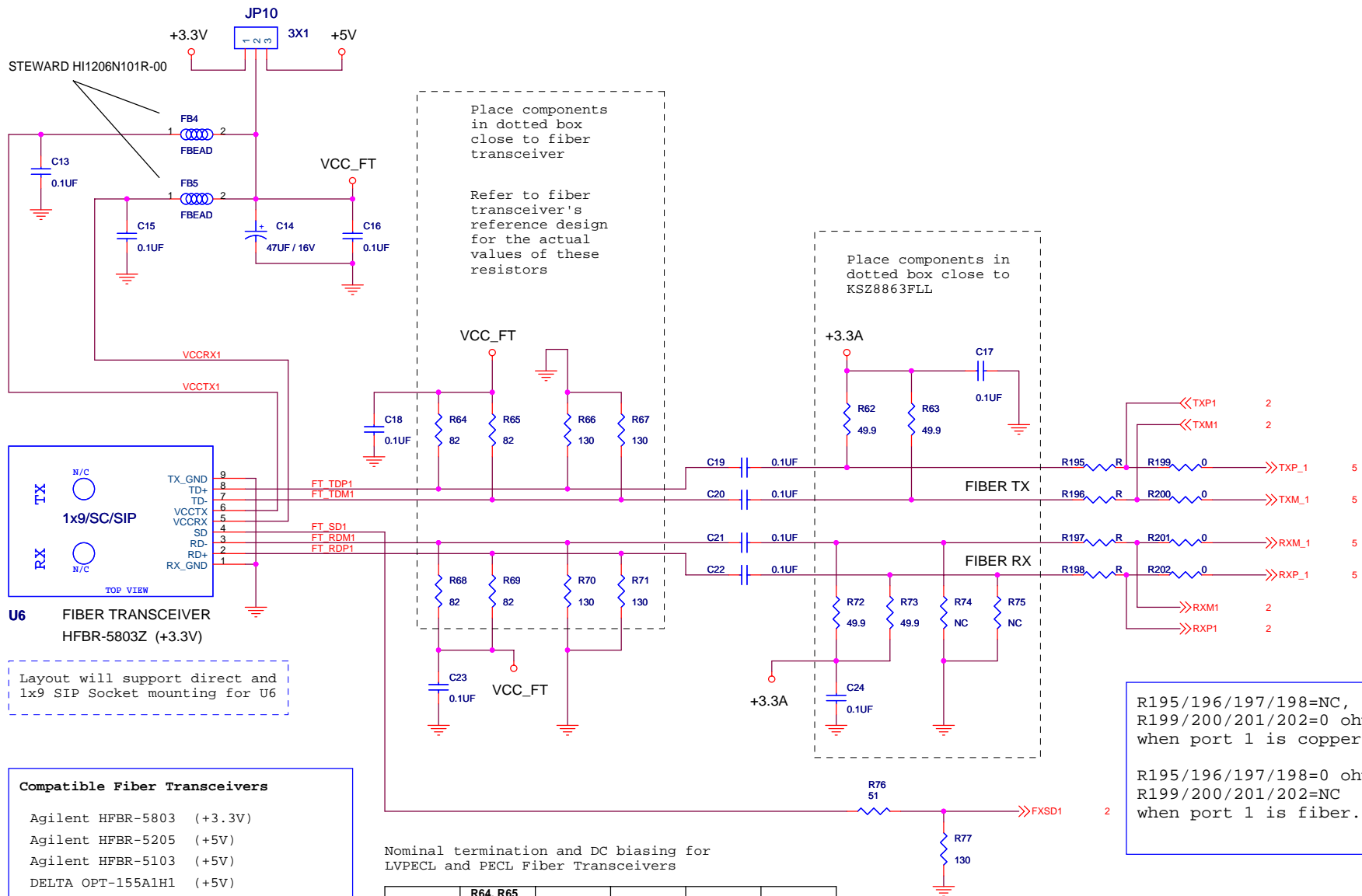
Line Side Protection (test option)

Place near RJ-45 connector



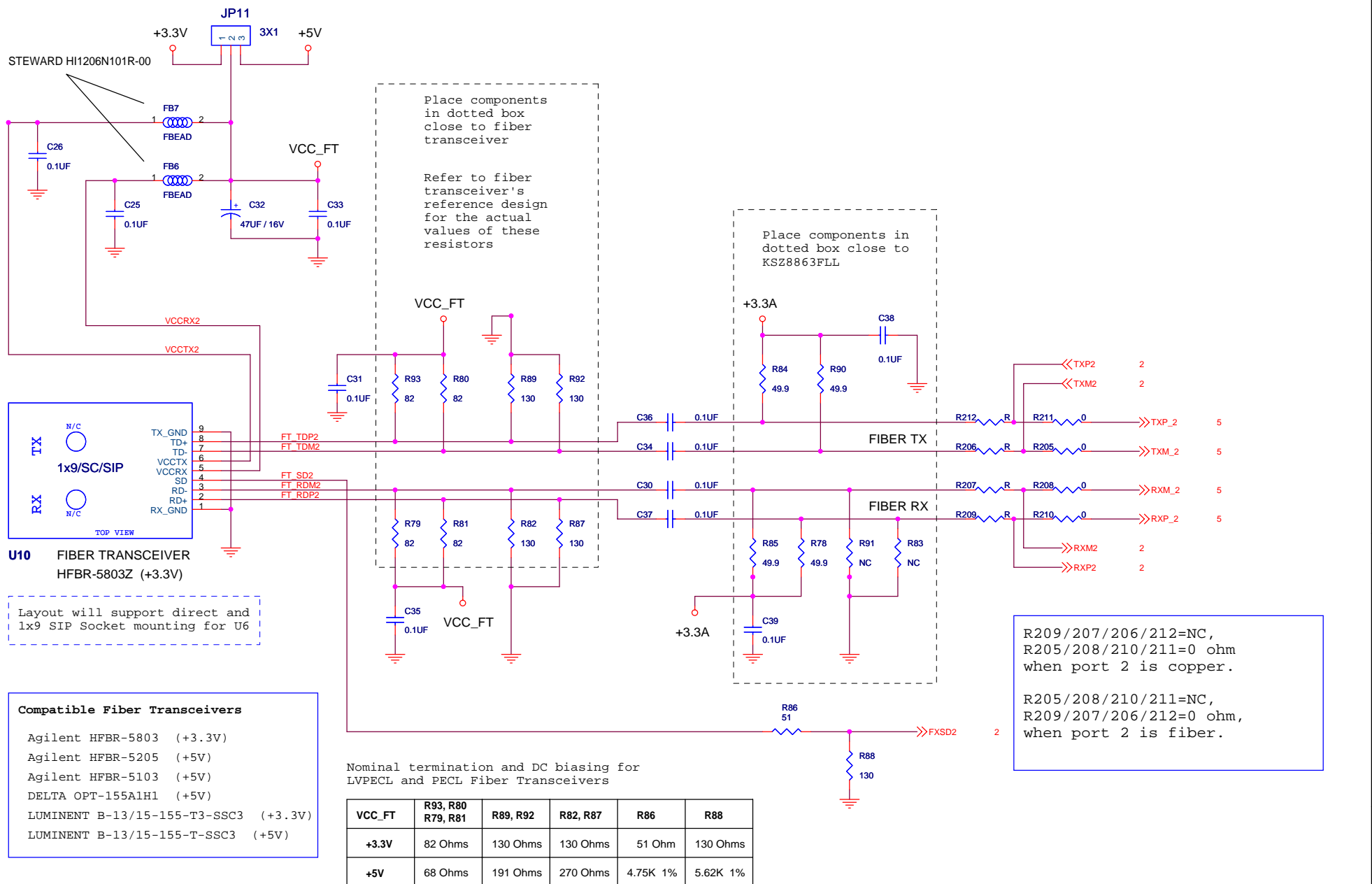
Chip Side Protection (test option)





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RMII option

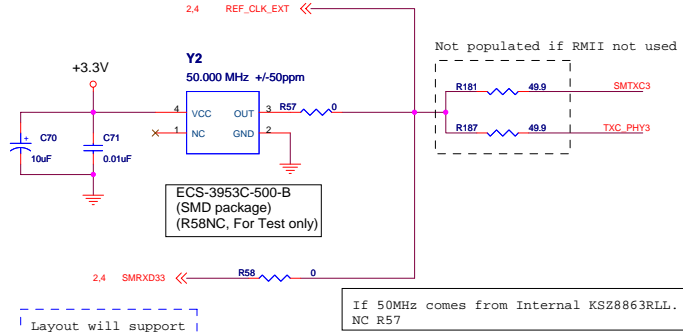
KS8863RLL provides RMII signals with respect to both PHY and MAC sides.

For this board, the KS8863RLL provides RMII signals with respect to MAC side only. The RMII signal connections between KS8863RLL and external PHY are shown in the table to the right.

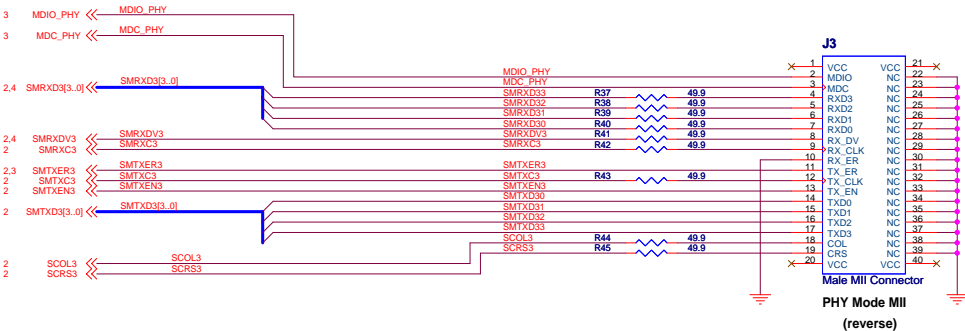
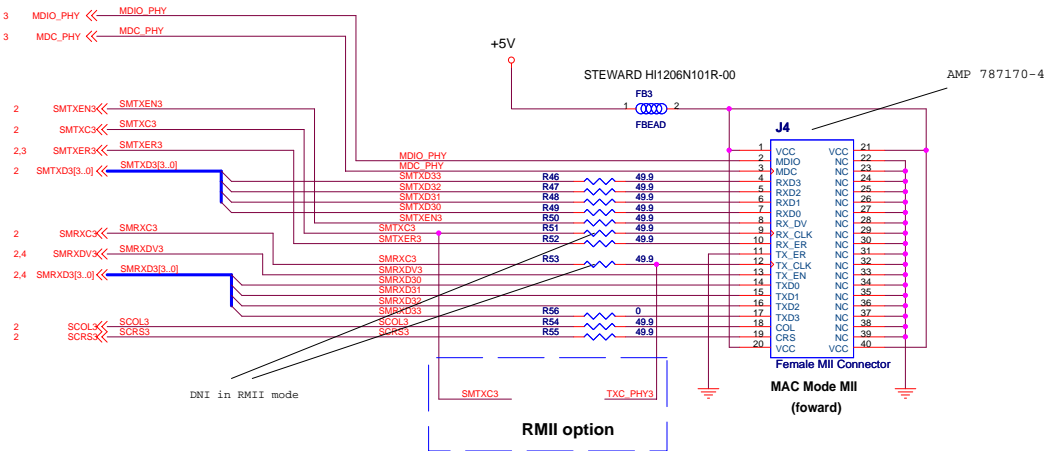
The KSZ8863RLL can provide the 50MHz reference clock by disconnect JP19 to enable REFCLKO. Remove R51 and R53.

The KSZ8863RLL can use internal or external reference clock which is selected by register 198 bit 3. For external, it is set to 1, vice reverse.

External PHY RMII (with respect to PHY)		KSZ8863RLL RMII (with respect to MAC)		
Signal	Type	Signal	Pin #	Type
REF_CLK	Input	SMTXC3	23	Input
CRS_DV	Output	SMTXEN3	16	Input
RXD[1]	Output	SMTXD31	19	Input
RXD[0]	Output	SMTXD30	20	Input
TX_EN	Input	SMRXDV3	25	Output
TXD[1]	Input	SMRXD31	28	Output
TXD[0]	Input	SMRXD30	29	Output
RX_ER	Output	SMTXER3	24	Input



SMTXD33	Reference Clock selection Port 3 RMII
1	Enable REFCLKO Output
0	Disable REFCLKO





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