



Introduction

This application note is intended to assist customers in designing products that comply with both EMI and ESD standards using Micrel's 10/100 family of Ethernet products.

The printed circuit board (PCB) is the single most important factor that affects EMI, ESD and overall performance. In order to meet these requirements depend on good design practices. The goal here is to minimize digital and common mode noise as well as to provide shielding between the PCB's internal circuitry and the external environment. These PCB design practices should apply to the entire PCB design, not just to Micrel Ethernet products.

All datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

General Rules

- Place components so as to avoid long loop traces.
- Choose a metal box to shield the printed circuit board.
- Use a ferrite core on the DC power cord to reduce EMI.
- Follow the guidelines to layout differential pairs, the ground plane, and high-speed signals.
- Provide controlled impedance on all clock lines and high-speed digital signals traces with right termination schemes to prevent reflection and ringing.
- Ensure that the power supply is rated for the application and optimized with decoupling capacitors.
- Keep power and ground noise under 50mV peak-to-peak.
- Ensure that the switching DC-DC converter is filtered and properly shielded as the DC-DC power converter can produce a great deal of EMI noise.
- Avoid via and pad in the path on any critical signal as via and pad will induce unwanted capacitance and inductance which can cause reflection and distortion.

Power Ground Rules

- Do not split the ground plane into separate planes for analog, digital, power pins. A single and contiguous ground plane is recommended.
- Route high-speed signals above a solid and unbroken ground plane.
- Fill copper in the unused area of signal planes and connect these coppers to the ground plane through vias.
- Stagger the placement of vias to avoid creating long gap in the plane due to via voids.

Analog VCC Plane

Place and route analog components within the Analog VCC plane.

Digital VCC plane

Place and route digital components within the Digital VCC plane.

Signal Ground

The signal ground region should be one continuous and unbroken plane. Both analog (AGND) and digital (DGND) grounds should be directly connected to the signal ground plane.

Chassis Ground

The chassis ground and magnetics serve two purposes: they help to reduce EMI noise emissions from the signal ground plane to the PCB's external environment and also act as a shield to protect the PCB components from ESD.

Place the chassis ground on all PCB layers and use connection mounting holes to join the chassis ground on different PCB layers

This chassis ground on the PCB is directly connected to the metal shield of equipment through the connection mounting holes.

Use a trench/moat to isolate the chassis ground plane from the signal ground plane.

The chassis ground region extends from the front edge of the PCB board (RJ45 connectors) to the magnetics and around the edge of the board as shown in Figure 1.

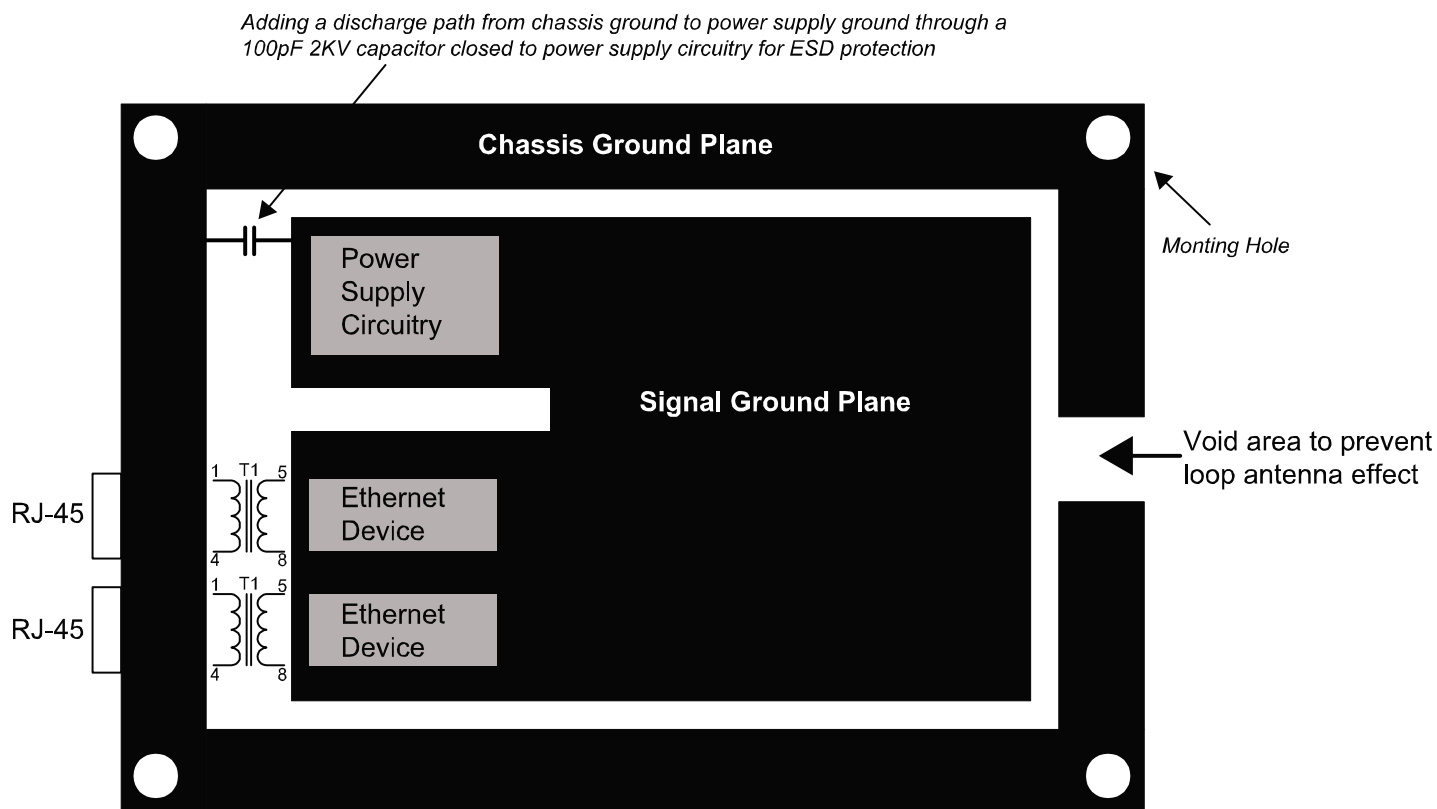


Figure 1. Signal and Ground Planes

Magnetic Noise Zone

- Void both power and ground planes on all PCB layers directly under the magnetics.
- Chassis ground should extend from the magnetics to the RJ45 connector.
- Do not route any digital signals between the PHY and RJ45 connector.

Differential Signal Layout

- Differential pair (TX+/- or RX+/-) should be routed away from all other signals and close together to use 5-mil trace width and 5-mil trace space in same length as possible with 100 ohms controlled trace.
- Keep both traces of each differential pair as identical to each other as possible.
- Route each differential pair on the same PCB layer.
- Route both TX+/- and RX+/- pairs as far as away from each other at least four times of 5-mil trace space as shown in Figure 2.

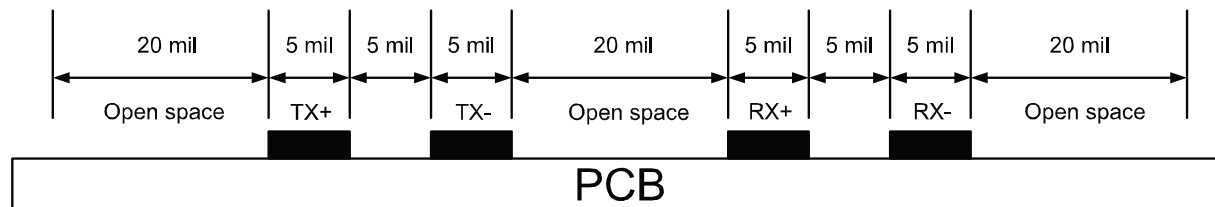


Figure 2. Transmit/Receive Differential Pair Routing

PCB Layer Stacking

6-Layer Example:

- Layer 1 component + signal side (short traces)
- Layer 2 ground plane
- Layer 3 signal
- Layer 4 signal
- Layer 5 power plane
- Layer 6 signal

4-Layer Example:

- Layer 1 component + signal side (short traces)
- Layer 2 ground plane
- Layer 3 power plane
- Layer 4 signal

Clock Layout Guidelines

- Keep clock traces as short as possible.
- Ensure that all clock traces should have an unbroken reference ground plane.
- Use a clock driver when driving multiple loads from a single oscillator.
- All clock signals should be terminated. For example, place a 33-50 ohm series resistor close to the clock source.

ESD Protection

Various ESD protection methods and devices can be used. The level of ESD protection provided by each method varies and depends on the type of protection device used. Consult the specific manufacture's data sheet to determine the level of ESD protection and proper connection. Figure 3 and 4 show example of two ESD protection methods.

The most important issue for designing PCBs with ESD compliance is to carefully consider how the ESD currents will flow to earth and where the ESD voltages will appear, to avoid other circuitry malfunctioning or even being destroyed.

- Place transient voltage suppressor (TVS) devices on the TX +/- and RX +/- differential pairs to help increase ESD protection. These devices are connected in parallel with the I/O lines to be protected.
- Connect all unused inputs to either ground with a 1K resistor or power with a 10K resistor, depending on the desired strap-in setting of the chip.
- Place termination resistors for the TX +/- and RX +/- differential pairs close to the Micrel chip as shown in Figure 5.
- During FCC or ESD tests, remove all unused header pins, jumpers, test point pins, etc. These parts act as antenna and can degrade test results.

For additional support, contact your local Micrel Field Application Engineer or Salesperson.

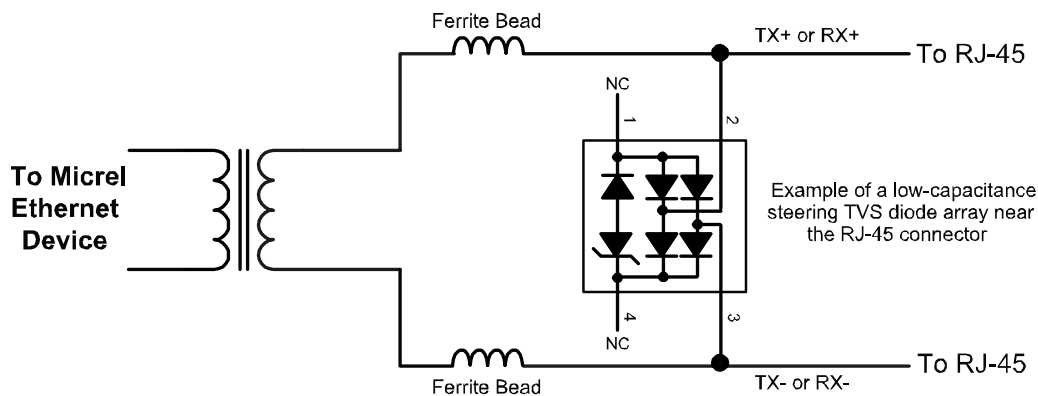


Figure 3. ESD Protection on the RJ-45 Side

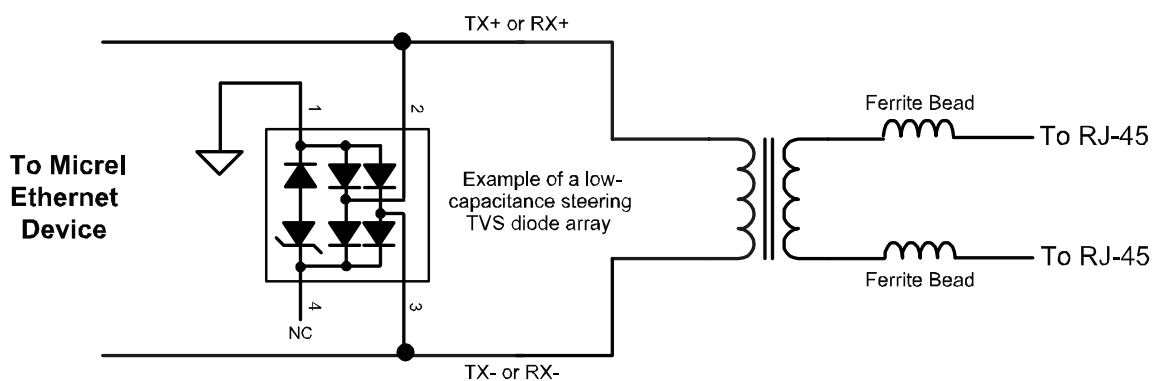


Figure 4. ESD Protection on Micrel's Ethernet Device Side

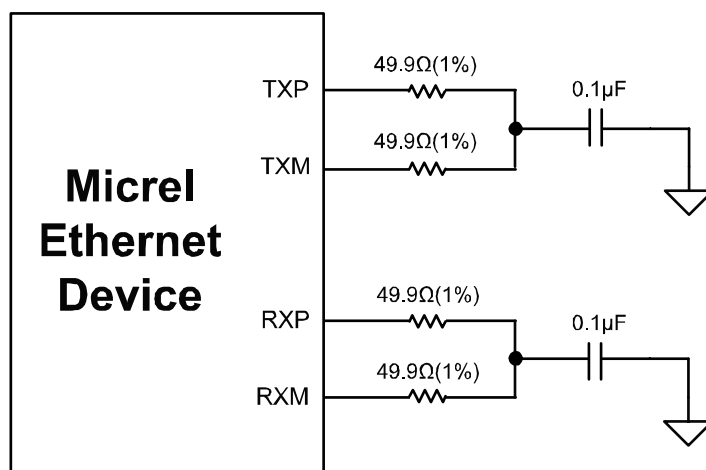


Figure 5. Terminator of TX+/- and RX+/- Differential Pairs

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USATEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB <http://www.micrel.com>

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