

KSZ8863MLL Reference Design Revision 1.0

REVISION HISTORY

DATE:	DESCRIPTION	REVISION
05/30/2009	Initial Draft	1.0

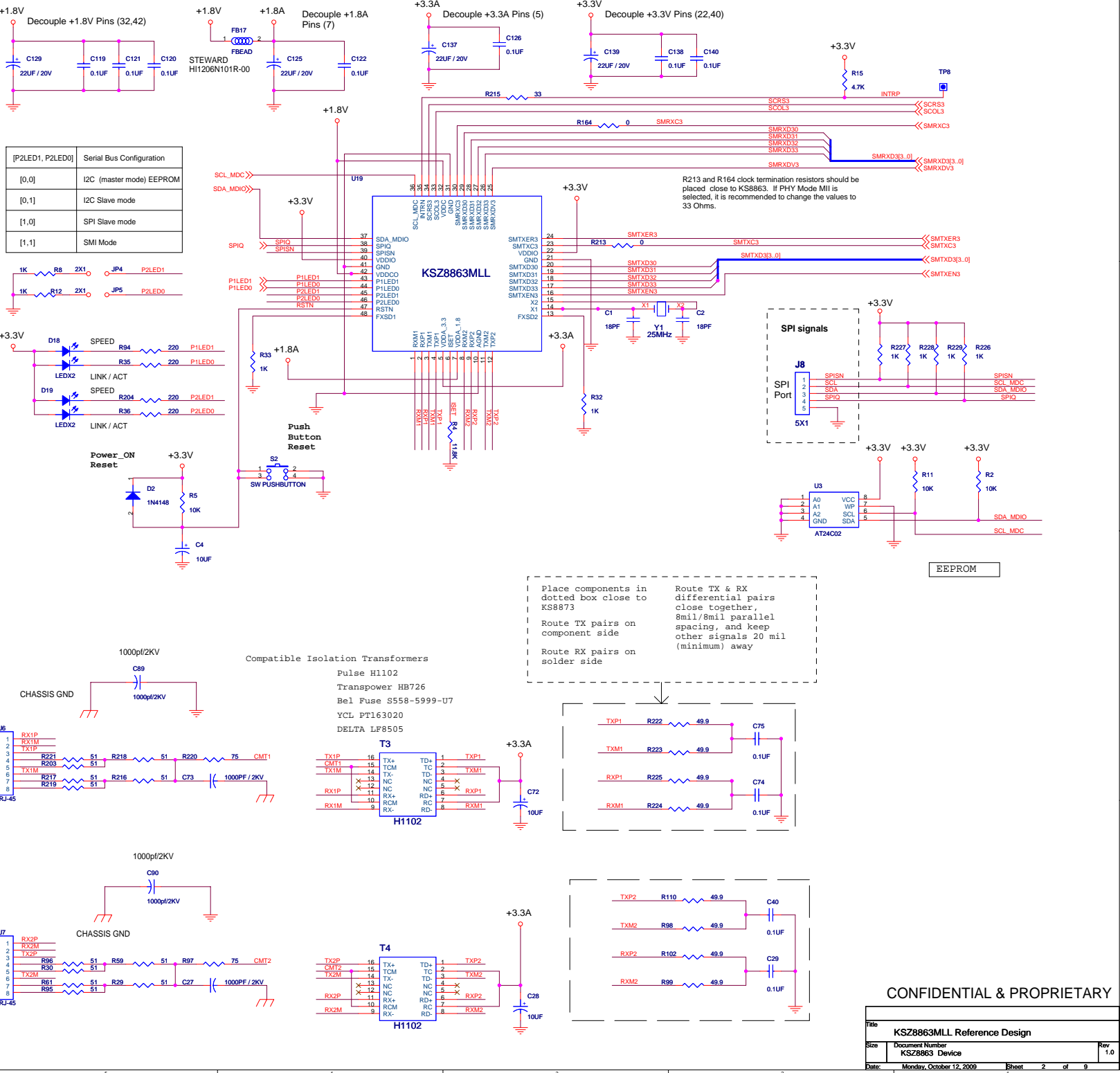
Table of Contents

PAGE 01: Revision History
PAGE 02: KSZ8863MLL_48LQFP Device
PAGE 03: Device Configuration / Strap and MII Interface
PAGE 04: Power



CONFIDENTIAL & PROPRIETARY

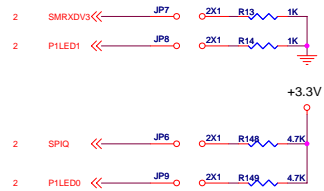
Title		
KSZ8863MLL Reference Design		
Size	Document Number Revision History	Rev 1.0
Date:	Monday, October 12, 2009	Sheet 1 of 9



CONFIDENTIAL & PROPRIETARY

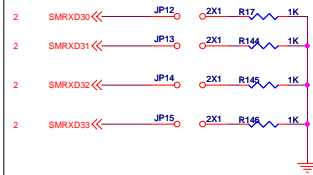
Title		
KSZ8863MLL Reference Design		
Size	Document Number	Rev
	KSZ8863 Device	1.0
Date:	Monday, October 12, 2009	Sheet 2 of 9

PORT 1



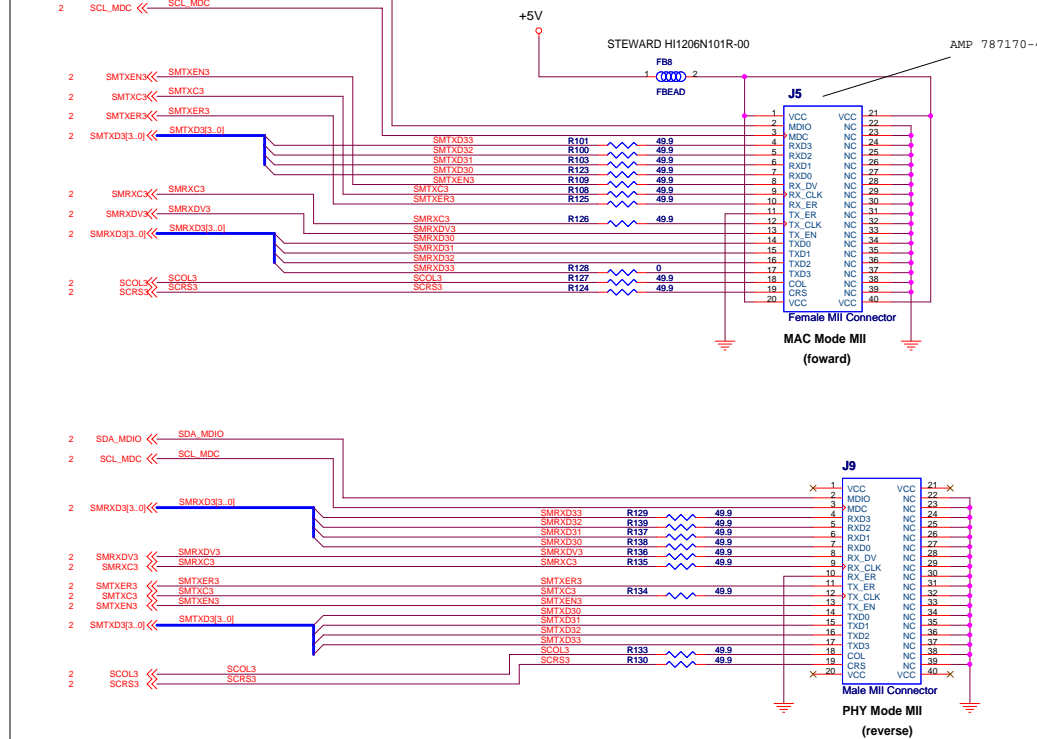
JP6	Force Flow Control High = Enable Off (default) = Disable
JP7	Force Full/Half Off = Full Duplex Low = Half Duplex
JP8	Force Speed Off = 100BaseTX Low = 10BaseT
JP9	Auto-negotiation High = Enable Off(default) = Disable

PORT 2



JP12	Force Flow Control Off = ENABLE Low = DISABLE
JP13	Force Full/Half Off = Full Duplex Low = Half Duplex
JP14	Force Speed Off = 100BaseTX Low = 10BaseT
JP15	Auto-negotiation Off = ENABLE Low = DISABLE

Port 3 MII Interface



CONFIDENTIAL & PROPRIETARY

File	KSZ8863MLL Reference Design		
Size	Document Number	Device Config/Strap and MII Interface	Rev 1.0
Date	Monday, October 12, 2009	Sheet 3 of 4	

