TEXAS INSTRUMENTS

UCC28063A

SNVSA88C – DECEMBER 2014 – REVISED NOVEMBER 2016

UCC28063A Natural Interleaving™ Transition-Mode PFC Controller With Improved Audible and Input Surge Noise Immunity

1 Features

- Input Filter and Output Capacitor Ripple-Current Cancellation
  - Reduced Current Ripple for Higher System Reliability and Smaller Bulk Capacitor
  - Reduced EMI Filter Size
- Phase Management Capability
- Fail-Safe OVP with Dual Paths Prevents Output Overvoltage Conditions by Voltage-Sensing Failures
- Sensorless Current-Shaping Simplifies Board Layout and Improves Efficiency
- Advanced Audible Noise Performance
- Non-linear Error-Amplifier Gain
- Soft Recovery on Overvoltage
- Integrated Brownout and Dropout Handling
- Reduced Bias Currents
- Improved Efficiency and Design Flexibility Over Traditional Single-Phase Continuous Conduction Mode (CCM)
- Inrush-Safe Current Limiting:
  - Prevents MOSFET Conduction During Inrush
  - Eliminates reverse Recovery Events in Output rectifiers
- Enables Use of Low-Cost Diodes Without Extensive Snubber Circuitry
- Improved Light-Load Efficiency
- Fast, Smooth Transient Response
- Expanded System-Level Protections
- 1-A Source/1.8-A Sink Gate Drivers
- –40°C to 125°C Operating Temperature Range in a 16-Lead SOIC Package

2 Applications

- 100-W to 800-W Power Supplies
- Gaming
- D-to-A Set-Top Boxes
- Adapters
- LCD, Plasma and DLP™ TVs
- Home Audio Systems

3 Description

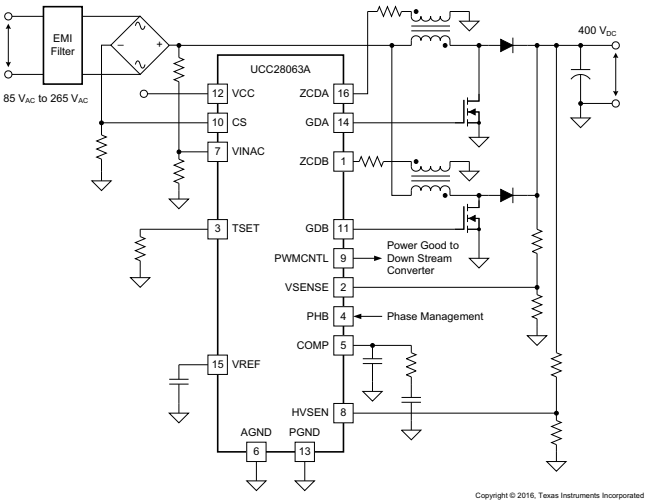
This part is identical to UCC28063 with the exception that the TSET pin Open/ Short Fault Detect and the CS pin Open Fault Detect features are removed. Removal of these Fault Detect features provides a higher degree of noise immunity to provide increased "ride-through" for applications where significant voltage noise could be coupled onto the TSET or CS pins during conditions of fast transient, surge or impulse noise on the AC Supply.

Device Information(1)

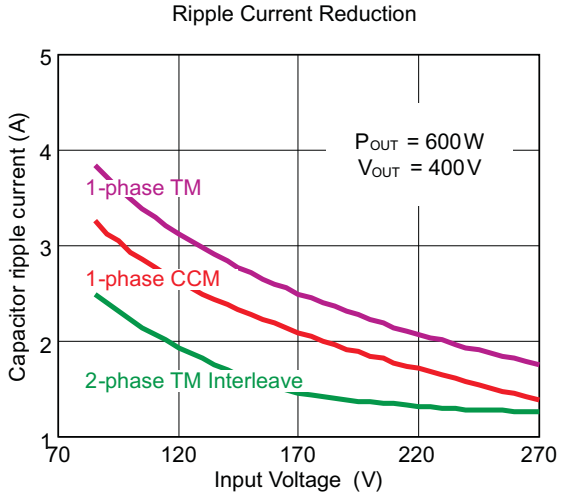
PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC28063A	SOIC (16)	9.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Diagram



Input Ripple Current Reduction with Interleaving



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision B (March 2015) to Revision C **Page**

- Added GDA, GDB Absolute Maximum ratings. ... 4

Changes from Revision A (February 2015) to Revision B **Page**

- Changed from Product Preview to Production Data ... 1

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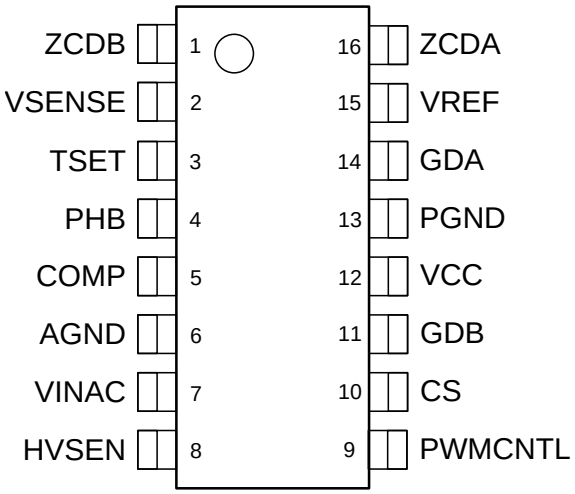
5 Description (Continued)

Optimized for consumer applications concerned with audible noise elimination, this solution extends the advantages of transition mode – high efficiency with low-cost components – to higher power ratings than previously possible. By utilizing a Natural Interleaving™ technique, both channels operate as masters (that is, there is no slave channel) synchronized to the same frequency. This approach delivers inherently strong matching, faster responses, and ensures that each channel operates in transition mode.

Expanded system level protections feature input brownout and dropout recovery, output over-voltage, open-loop, overload, soft-start, phase-fail detection, and thermal shutdown. The additional FailSafe over-voltage protection (OVP) feature protects against shorts to an intermediate voltage that, if undetected, could lead to catastrophic device failure. Advanced non-linear gain results in rapid, yet smoother response to line and load transient events. Reduced bias currents improve stand-by power efficiency. Special line-dropout handling avoids significant current disruption and minimizes audible-noise generation.

6 Pin Configuration and Functions

D Package
16-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	6	-	Analog Ground
COMP	5	O	Error Amplifier Output
CS	10	I	Current Sense Input
GDA	14	O	Channel A and Channel B Gate Drive Output
GDB	11	O	
HVSEN	8	I	High Voltage Output Sense
PHB	4	I	Phase-B Enable/Disable
PWMCNTL	9	O	PWM-Control Output
TSET	3	I	Timing Set
VCC	12	-	Bias Supply Input
VINAC	7	I	Input AC Voltage Sense
VREF	15	O	Voltage Reference Output
VSENSE	2	I	Output DC Voltage Sense
ZCDA	16	I	Zero Current Detection Inputs
ZCDB	1	I	

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7 Specifications

7.1 Absolute Maximum Ratings(1)

All voltages are with respect to GND, −40 °C < T_J = T_A < 125 °C, currents are positive into and negative out of the specified terminal, unless otherwise noted.

			MIN	MAX	UNIT
	Continuous input voltage range	VCC(2)	−0.5	21	V
		PWMCNTL	−0.5	20	
		COMP(3), PHB, HVSEN(4), VINAC(4), VSENSE(4)	–0.5	7	
		ZCDA, ZCDB	–0.5	4	
		CS(5)	–0.5	3	
		GDA, GDB(6)	–0.5	VCC+0.3	
	Continuous input current	VCC		20	mA
		PWMCNTL		10	
		ZCDA, ZCDB		±5	
	Peak input current	CS		–30	
	Output current	VREF		–10	
	Continuous gate current	GDA, GDB(6)		±25	
T_J	Junction Temperature	Operating	–40	125	°C
		Storage	–65	150	
T_{SOL}	Lead Temperature	Soldering, 10s		260	
T_{stg}	Storage temperature		–40	125	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those included under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods of time may affect device reliability.
(2) Voltage on VCC is internally clamped. VCC may exceed the continuous absolute maximum input voltage rating if the source is current limited below the absolute maximum continuous VCC input current level.
(3) In normal use, COMP is connected to capacitors and resistors and is internally limited in voltage swing.
(4) In normal use, VINAC, VSENSE, and HVSEN are connected to high-value resistors and are internally limited in negative-voltage swing. Although not recommended for extended use, VINAC, VSENSE, and HVSEN can survive input currents as high as -10mA from negative voltage sources, and input currents as high as +0.5mA from positive voltage sources.
(5) In normal use, CS is connected to a series resistor to limit peak input current during brief system line-inrush conditions. In these situations, negative voltage on CS may exceed the continuous absolute maximum rating.
(6) No GDA or GDB current limiting is required when driving a power MOSFET gate. However, a small series resistor may be required to damp resonant ringing due to stray inductance.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

All voltages are with respect to GND, −40 °C < T_J = T_A < 125 °C, currents are positive into and negative out of the specified terminal, unless otherwise noted.

	MIN	MAX	UNIT
VCC input voltage from a low-impedance source	14	21	V
VCC input current from a high-impedance source	8	18	mA
VREF load current	0	–2	
VINAC input voltage	0	6	V
ZCDA, ZCDB series resistor	20	80	kΩ
TSET resistor to program PWM on-time	66.5	400	
HVSEN input voltage	0.8	4.5	V

7.4 Thermal Information

THERMAL METRIC(1)		UCC28063A SOIC (D) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	91.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance(3)	52.1	
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	48.6	
ψ_{JT}	Junction-to-top characterization parameter(5)	14.9	
ψ_{JB}	Junction-to-board characterization parameter(6)	48.3	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).

7.5 Electrical Characteristics

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 5 V, R_{TSET} = 133 kΩ, all voltages are with respect to GND, all outputs unloaded, −40 °C < T_J = T_A < 125 °C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC BIAS SUPPLY						
VCC_{SHUNT}	VCC shunt voltage(1)	I_{VCC} = 10 mA	22	24	26	V
$I_{VCC(ULVO)}$	VCC current, UVLO	VCC = 11.4 V prior to turn-on		95	200	µA
$I_{VCC(stby)}$	VCC current, disabled	VSENSE = 0 V		100	200	
$I_{VCC(on)}$	VCC current, enabled	VSENSE = 2 V		5	8	mA
UNDERVOLTAGE LOCKOUT (UVLO)						
VCC_{ON}	VCC turn-on threshold	VCC rising	11.5	12.6	13.5	V
VCC_{OFF}	VCC turn-off threshold	VCC falling	9.5	10.35	11.5	
	UVLO Hysteresis		1.85	2.15	2.45	
REFERENCE						
V_{REF}	VREF output voltage, no load	I_{VREF} = 0 mA	5.82	6.00	6.18	V

(1) Excessive VCC input voltage and current will damage the device. This clamp will not protect the device from an unregulated bias supply. If an unregulated bias supply is used, a series-connected Fixed Positive-Voltage Regulator such as the UA78L15A is recommended. See the Absolute Maximum Ratings table for the limits on VCC voltage, current, and junction temperature.

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Electrical Characteristics (continued)

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 5 V, R_{TSET} = 133 kΩ, all voltages are with respect to GND, all outputs unloaded, −40 °C < T_J = T_A < 125 °C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	VREF change with load	0 mA ≤ I_{VREF} ≤ −2 mA		−1	−6	mV
	VREF change with VCC	12 V ≤ VCC ≤ 20 V		2	10	
ERROR AMPLIFIER						
VSENSEreg25	VSENSE input regulation voltage	T_A = 25 °C	5.85	6	6.15	V
VSENSEreg	VSENSE input regulation voltage		5.82	6	6.18	
I_{VSENSE}	VSENSE input bias current	In regulation	50	100	150	nA
V_{ENAB}	VSENSE enable threshold, rising		1.15	1.25	1.35	V
	VSENSE enable hysteresis		0.02	0.07	0.15	
$V_{COMPCLMP}$	COMP high voltage, clamped	VSENSE = VSENSEreg – 0.3 V	4.70	4.95	5.10	
	COMP low voltage, saturated	VSENSE = VSENSEreg + 0.3 V		0.03	0.125	
g_M	VSENSE to COMP transconductance, small signal	0.99(VSENSEreg) < VSENSE < 1.01(VSENSEreg), COMP = 3 V	40	55	70	µS
	VSENSE high-going threshold to enable COMP large signal gain, percent	Relative to VSENSEreg, COMP = 3 V	3.25%	5%	6.75%	
	VSENSE low-going threshold to enable COMP large signal gain, percent	Relative to VSENSEreg, COMP = 3 V	−3.25%	−5%	−6.75%	
	VSENSE to COMP transconductance, large signal	VSENSE = VSENSEreg – 0.4 V , COMP = 3 V	210	290	370	µS
	VSENSE to COMP transconductance, large signal	VSENSE = VSENSEreg + 0.4 V, COMP = 3 V	210	290	370	
	COMP maximum source current	VSENSE = 5 V, COMP = 3 V	−80	−125	−170	µA
$R_{COMPDCHG}$	COMP discharge resistance	HVSEN = 5.2 V, COMP = 3 V	1.6	2	2.4	kΩ
I_{DODCHG}	COMP discharge current during Dropout	VSENSE = 5 V, VINAC = 0.3 V	3.2	4	4.8	µA
V_{LOW_OV}	VSENSE over-voltage threshold, rising	Relative to VSENSEreg	7%	8%	10%	
	VSENSE over-voltage hysteresis	Relative to V_{LOW_OV}	−1.5%	−2%	−3%	
V_{HIGH_OV}	VSENSE 2nd over-voltage threshold, rising	Relative to VSENSEreg	10.5%	11.3%	14%	
SOFT START						
V_{SSTHR}	COMP Soft-Start threshold, falling	VSENSE = 1.5 V	15	23	30	mV
$I_{SS,FAST}$	COMP Soft-Start current, fast	SS-state, V_{ENAB} < VSENSE < VREF/2	−80	−125	−170	µA
$I_{SS,SLOW}$	COMP Soft-Start current, slow	SS-state, VREF/2 < VSENSE < 0.88VREF	−11.5	−16	−20	
K_{EOSS}	VSENSE End-of-Soft-Start threshold factor	Percent of VSENSEreg	96.5%	98.3%	99.8%	
OUTPUT MONITORING						
$V_{PWMCNTL}$	HVSEN threshold to PWMCNTL	HVSEN rising	2.35	2.50	2.65	V
I_{HVSEN}	HVSEN input bias current, high	HVSEN = 3 V		±0.03	±0.5	µA
I_{HV_HYS}	HVSEN hysteresis bias current, low	HVSEN = 2 V	9.2	11.4	14	

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Electrical Characteristics (continued)

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 5 V, R_{TSET} = 133 kΩ, all voltages are with respect to GND, all outputs unloaded, −40 °C < T_J = T_A < 125 °C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{HV_OV_FLT}$	HVSEN threshold to over-voltage fault	HVSEN rising	4.64	4.87	5.1	V
$V_{HV_OV_CLR}$	HVSEN threshold to over-voltage clear	HVSEN falling	4.45	4.67	4.8	
V_{COMP_PHFOFF}	Phase Fail monitoring-disable threshold	COMP falling	0.21	0.225	0.25	
V_{COMP_PHFHYS}	Phase Fail monitoring hysteresis	COMP rising		0.051		
	PWMCNTL output voltage low	HVSEN = 3 V, $I_{PWMCNTL}$ = 5 mA, COMP = 0 V		0.2	0.5	
t_{PHFDLY}	Phase Fail filter time to PWMCNTL high	PHB = 5 V, ZCDA switching, ZCDB = 0.5 V, COMP = 3 V	7.9	12	17	ms
$I_{PWMCNTL_LEAK}$	PWMCNTL leakage current, high	HVSEN = 2 V, PWMCNTL = 15 V		±0.03	±0.5	µA
GATE DRIVE(2)						
	GDA, GDB output voltage, high	I_{GDA}, I_{GDB} = −100 mA	11.5	12.4	15	V
	GDA, GDB on-resistance, high	I_{GDA}, I_{GDB} = −100 mA		8.8	14	Ω
	GDA, GDB output voltage, low	I_{GDA}, I_{GDB} = 100 mA		0.18	0.32	V
	GDA, GDB on-resistance, low	I_{GDA}, I_{GDB} = 100 mA		2	3.2	Ω
	GDA, GDB output voltage high, clamped	VCC = 20 V, I_{GDA}, I_{GDB} = −5 mA	12	13.5	15	V
	GDA, GDB output voltage high, low VCC	VCC = 12 V, I_{GDA}, I_{GDB} = −5 mA	10	10.5	11.5	
	Rise time	1 V to 9 V, C_{LOAD} = 1 nF		18	30	ns
	Fall time	9 V to 1 V, C_{LOAD} = 1 nF		12	25	
	GDA, GDB output voltage, UVLO	VCC = 3.0 V, I_{GDA}, I_{GDB} = 2.5 mA		100	200	mV
ZERO CURRENT DETECTOR						
	ZCDA, ZCDB voltage threshold, falling		0.8	1	1.2	V
	ZCDA, ZCDB voltage threshold, rising		1.5	1.7	1.9	
	ZCDA, ZCDB clamp, high	I_{ZCDA} = +2 mA, I_{ZCDB} = +2 mA	2.6	3	3.4	
	ZCDA, ZCDB clamp, low	I_{ZCDA} = −2 mA, I_{ZCDB} = −2 mA	0	−0.2	−0.4	
	ZCDA, ZCDB input bias current	ZCDA = 1.4 V, ZCDB = 1.4 V		±0.03	±0.5	µA
	ZCDA, ZCDB delay to GDA, GDB outputs(2)	From ZCDx input falling to 1 V to respective gate drive output rising 10%		50	100	ns
	ZCDA blanking time(3)	From GDA rising and GDA falling		100		
	ZCDB blanking time(3)	From GDB rising and GDB falling		100		
CURRENT SENSE						
	CS input bias current, dual-phase	At rising threshold	−120	−166	−200	µA
	CS current-limit rising threshold, dual-phase	PHB = 5 V	−0.18	−0.2	−0.22	V
	CS current-limit rising threshold, single-phase	PHB = 0 V	−0.149	−0.166	−0.183	
	CS current-limit reset falling threshold		−0.003	–0.015	−0.025	

(2) Refer to Figure 13, Figure 14, Figure 15, and Figure 16 of the Typical Characteristics for typical gate drive waveforms.
(3) ZCD blanking times are ensured by design.

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Electrical Characteristics (continued)

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 5 V, R_{TSET} = 133 kΩ, all voltages are with respect to GND, all outputs unloaded, −40 °C < T_J = T_A < 125 °C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	CS current-limit response time(2)	From CS exceeding threshold−0.05 V to GDx dropping 10%		60	100	ns
	CS blanking time	From GDx rising and falling edges		100		
VINAC INPUT						
I_{VINAC}	VINAC input bias current, above brownout	VINAC = 2 V		±0.03	±0.5	µA
V_{BODET}	VINAC brownout detection threshold	VINAC falling	1.33	1.39	1.44	V
t_{BODLY}	VINAC brownout filter time	VINAC below the brownout detection threshold for the brownout filter time	340	440	540	ms
V_{BOHYS}	VINAC brownout threshold hysteresis	VINAC rising	30	62	75	mV
I_{BOHYS}	VINAC brownout hysteresis current	VINAC = 1 V for > t_{BODLY}	1.6	2	2.5	µA
V_{DODET}	VINAC dropout detection threshold	VINAC falling	0.315	0.35	0.38	V
t_{DODLY}	VINAC dropout filter time	VINAC below the dropout detection threshold for the dropout filter time	3.5	5	7	ms
V_{DOCLR}	VINAC dropout clear threshold	VINAC rising	0.67	0.71	0.75	V
PULSE-WIDTH MODULATOR						
K_T	On-time factor, phases A and B	VSENSE = 5.8 V(4)	3.6	4.0	4.4	µs/V
K_{TS}	On-time factor, single-phase, A	VSENSE = 5.8 V, PHB = 0 V(4)	7.2	8.0	8.9	
	Phase B to phase A on-time matching error	VSENSE = 5.8 V		±2%	±6%	
	Zero-crossing distortion correction additional on time	COMP = 0.25 V, VINAC = 1 V	1.2	2	2.8	µs
		COMP = 0.25 V, VINAC = 0.1 V	12.6	20	29	
V_{PHBF}	PHB threshold falling, to single-phase operation	To GDB output shutdown, VINAC = 1.5 V	0.7	0.8	0.9	V
V_{PHBR}	PHB threshold rising, to two-phase operation	To GDB output running, VINAC = 1.5 V	0.9	1	1.1	
T_{MIN}	Minimum switching period	R_{TSET} = 133 kΩ(4)	1.7	2.2	3	µs
T_{START}	PWM restart time	ZCDA = ZCDB = 2 V(5)	165	210	265	
THERMAL SHUTDOWN						
T_J	Thermal shutdown temperature	Temperature rising(6)		160		°C
T_J	Thermal restart temperature	Temperature falling(6)		140		

(4) Gate drive on-time is proportional to (V_{COMP} – 0.125 V). The on-time proportionality factor, K_T, scales linearly with the value of R_{TSET} and is different in two-phase and single-phase modes. The minimum switching period is proportional to R_{TSET}.
(5) An output on-time is generated at both GDA and GDB if both ZCDA and ZCDB negative-going edges are not detected for the restart time. In single-phase mode, the restart time applies for the ZCDA input and the GDA output.
(6) Thermal shutdown occurs at temperatures higher than the normal operating range. Device performance above the normal operating temperature is not specified or assured.

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7.6 Typical Characteristics

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 5 V, R_{TSET} = 133 kΩ; all voltages are with respect to GND, all outputs unloaded, $T_J = T_A$ = +25 °C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

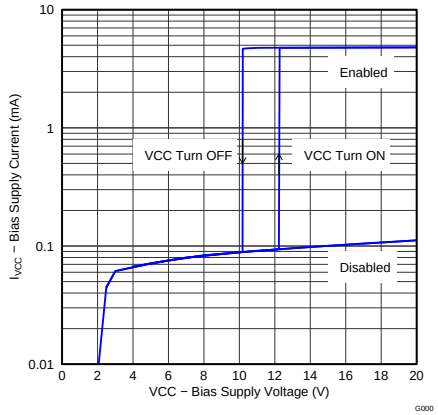


Figure 1. Bias Supply Current vs Bias Supply Voltage

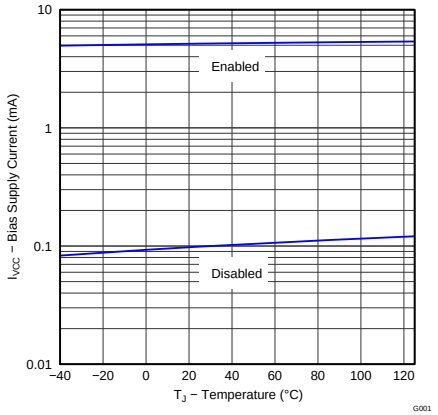
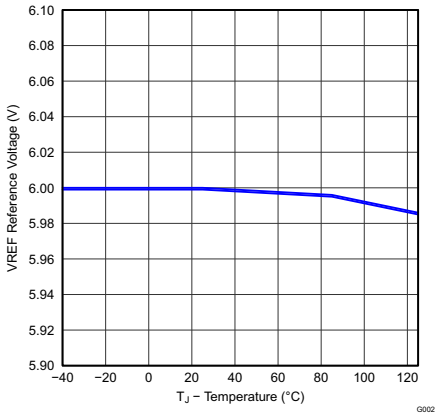


Figure 2. Bias Supply Current vs Temperature



I_{VREF} = 0 to –2 mA

Figure 3. Reference Voltage vs Temperature

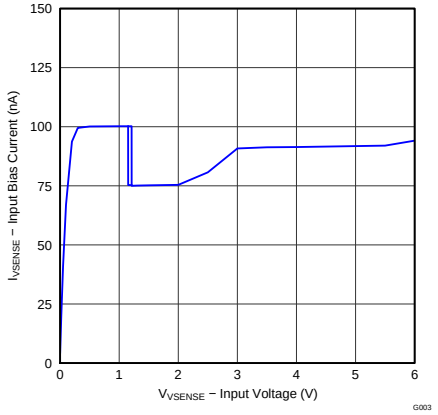
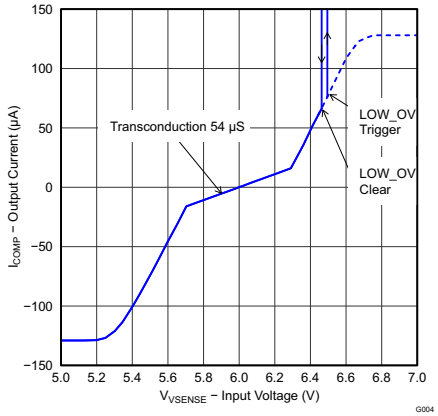


Figure 4. VSENSE Input Bias Current vs Input Voltage



Soft-Start Completed

Figure 5. Error Amplifier Output Current vs Input Voltage

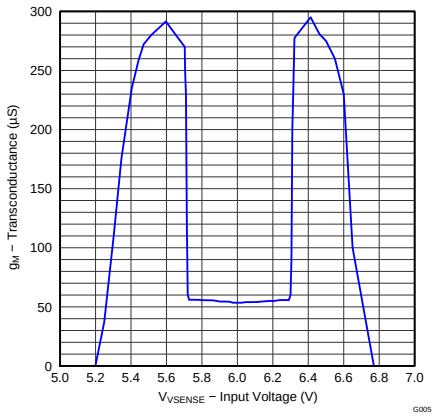
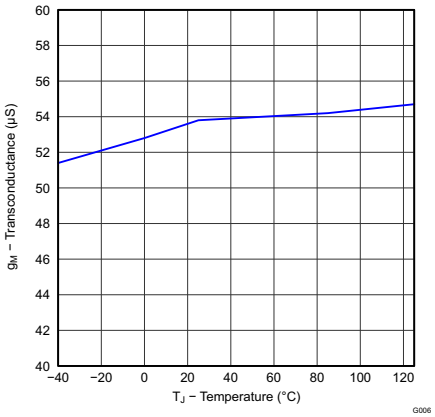


Figure 6. Error Amplifier Transconductance vs VSENSE

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Typical Characteristics (continued)



5.9 V < V_{VSENSE} < 6.1 V

Figure 7. Error Amplifier Transconductance vs Temperature

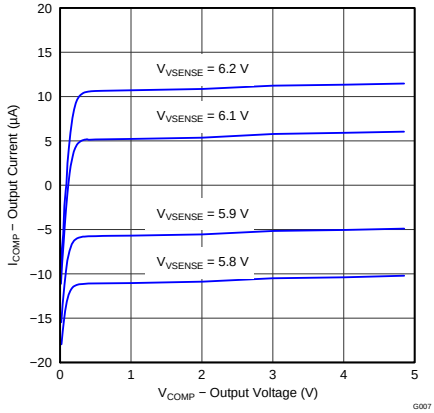


Figure 8. Error Amplifier Output Current vs Output Voltage

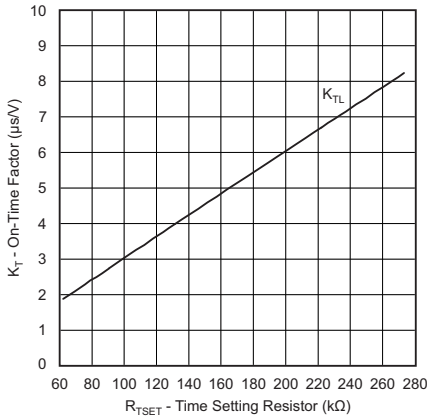


Figure 9. On-Time Factor vs Time Setting Resistor

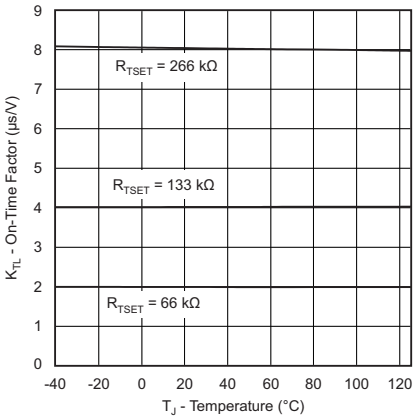
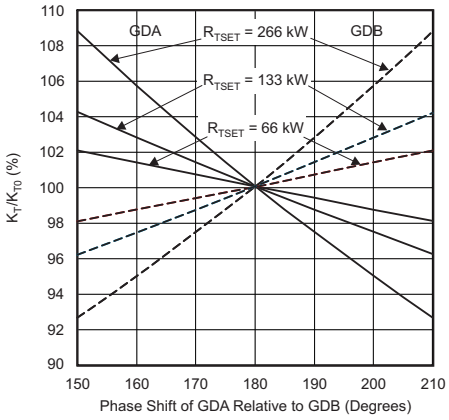


Figure 10. On-Time Factor Phase A and B vs Temperature



$K_{TO} = 2(K_{TA} \times K_{TB}) / K_{TA} + K_{TB}$

Figure 11. On-Time Factor vs Phase Error

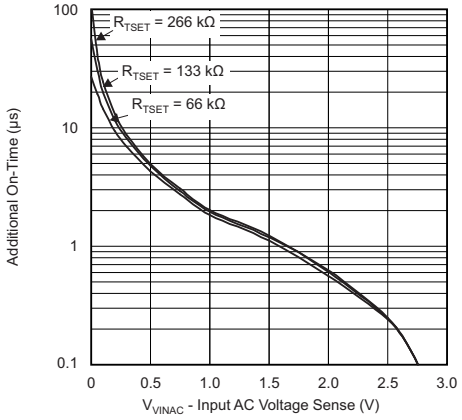
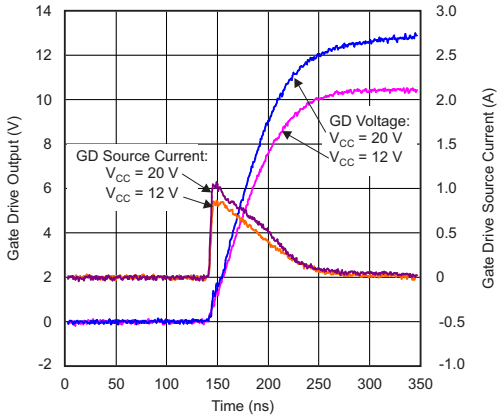


Figure 12. Additional On Time vs VINAC

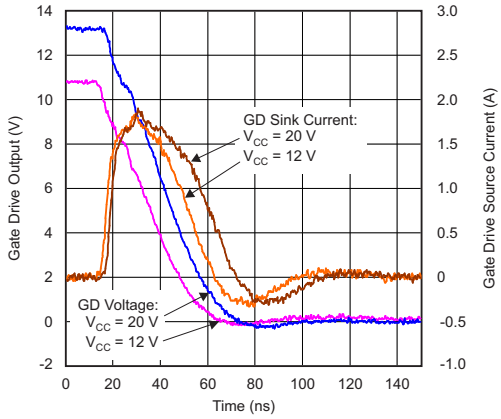
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Typical Characteristics (continued)



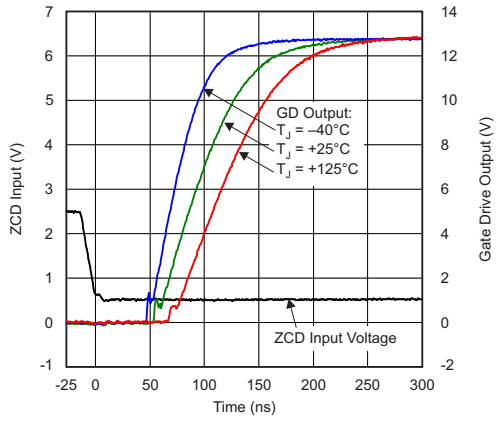
C_{LOAD} = 4.7 nF

Figure 13. Gate Drive Rising vs Time



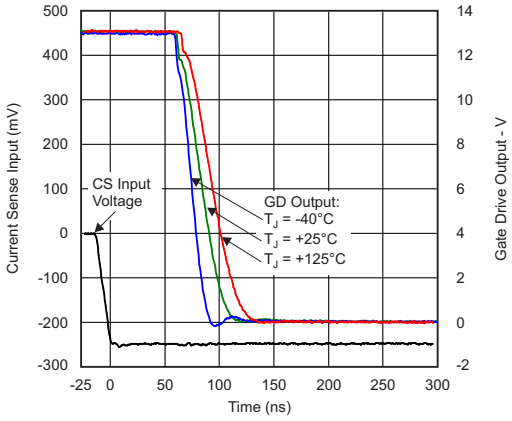
C_{LOAD} = 4.7 nF

Figure 14. Gate Drive Falling vs Time



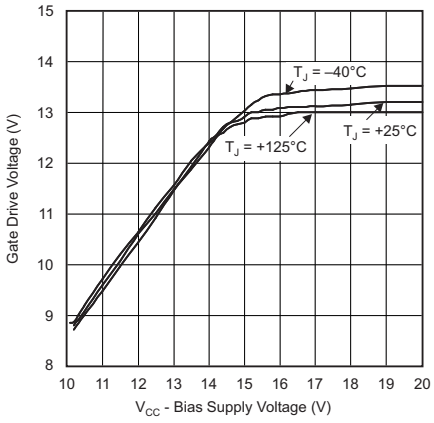
C_{LOAD} = 4.7 nF

Figure 15. Gate Drive Rising and Delay From ZCD Input vs Time



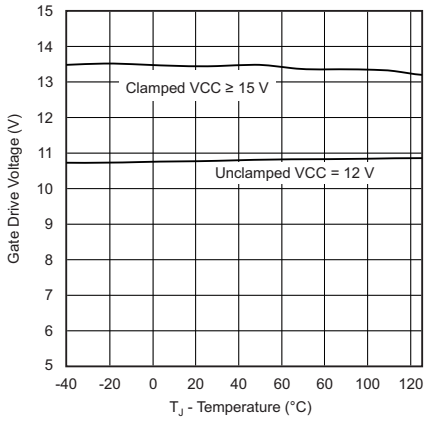
C_{LOAD} = 4.7 nF

Figure 16. Gate Drive Falling and Delay From CS Input vs Time



R_{LOAD} = 2.7 kΩ

Figure 17. Gate Drive Output High vs VCC

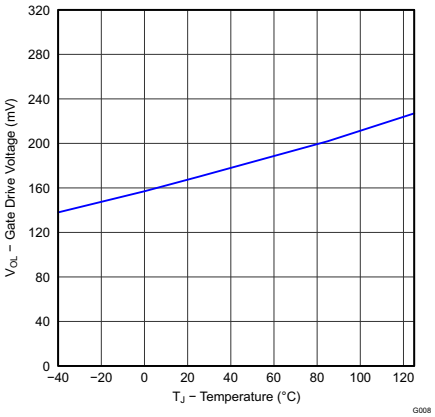


R_{LOAD} = 2.7 kΩ

Figure 18. Gate Drive High Voltage vs Temperature

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Typical Characteristics (continued)



Load = 100 mA

Figure 19. Gate Drive Low Voltage vs Temperature

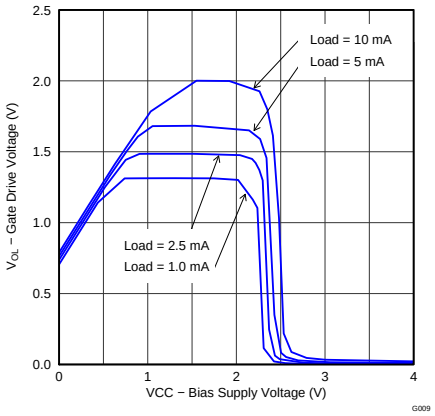


Figure 20. Gate Drive Low Voltage in UVLO vs Bias Supply Voltage

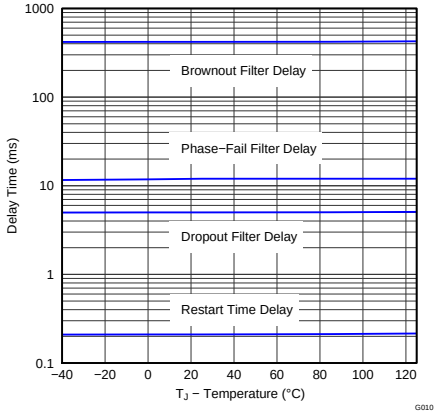


Figure 21. Various Delay Times vs Temperature

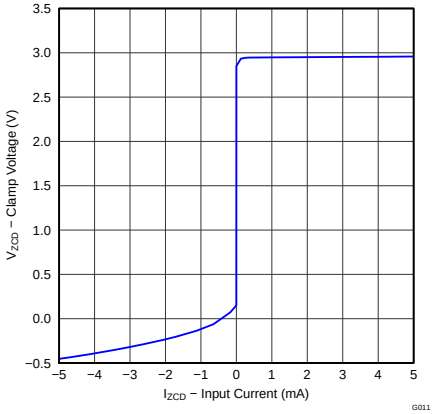
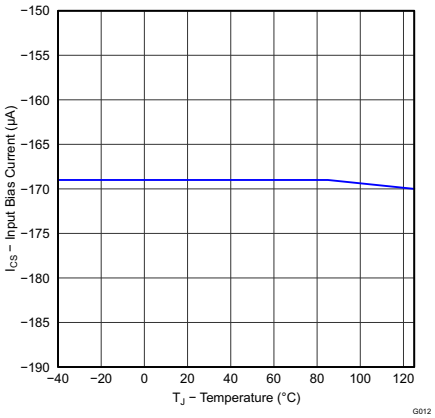


Figure 22. Zero Current Detect Clamp Voltage vs Input Current



V_{CS} = –195 mV

Figure 23. Current Sense Input Bias Current vs Temperature

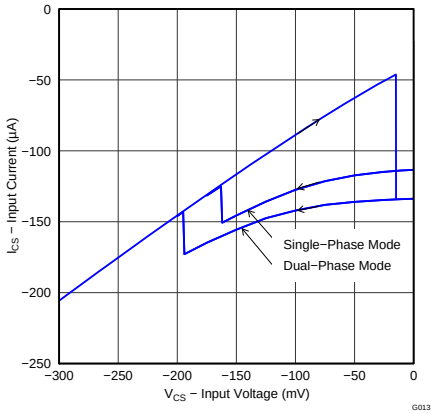


Figure 24. Current Sense Input Bias Current vs Input Voltage

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8 Detailed Description

8.1 Overview

This part is identical to UCC28063 with the exception that the TSET pin Open/ Short Fault Detect and the CS pin Open Fault Detect features are removed. Removal of these fault detect mechanisms provides a higher degree of noise immunity for applications where significant voltage noise could be coupled onto the TSET or CS pins during conditions of extreme fast transient, surge or impulse noise events. The Soft Re-Start fault protection which would be triggered on the UCC28063 will not occur with the UCC28063A. The system will continue to provide power delivery through such events, albeit with the possibility of some dynamic regulation irregularity.

Transition Mode Control is the most popular choice for the Boost Power Factor Correction topology at lower power levels because of its lower complexity in achieving high power factor while at the same time not placing demanding requirements on the power component specifications. A lower cost boost diode with higher reverse recovery current specification may be used, for instance, in the Transition Mode Boost. Interleaved Transition Mode Control retains this benefit and generally extends the applicability up to much higher power levels while simultaneously conferring the interleaving benefits of reduced input and output ripple, phase management for light load efficiency enhancement, redundancy, system thermal optimization and low profile or planar solutions.

The UCC28063A enables a very cost effective solution with a particular focus on ruggedness, fault management, fault recovery, efficiency and higher end performance in areas such as acoustic management and fast transient response. It may be regarded as an enhanced and new generation UCC28061.

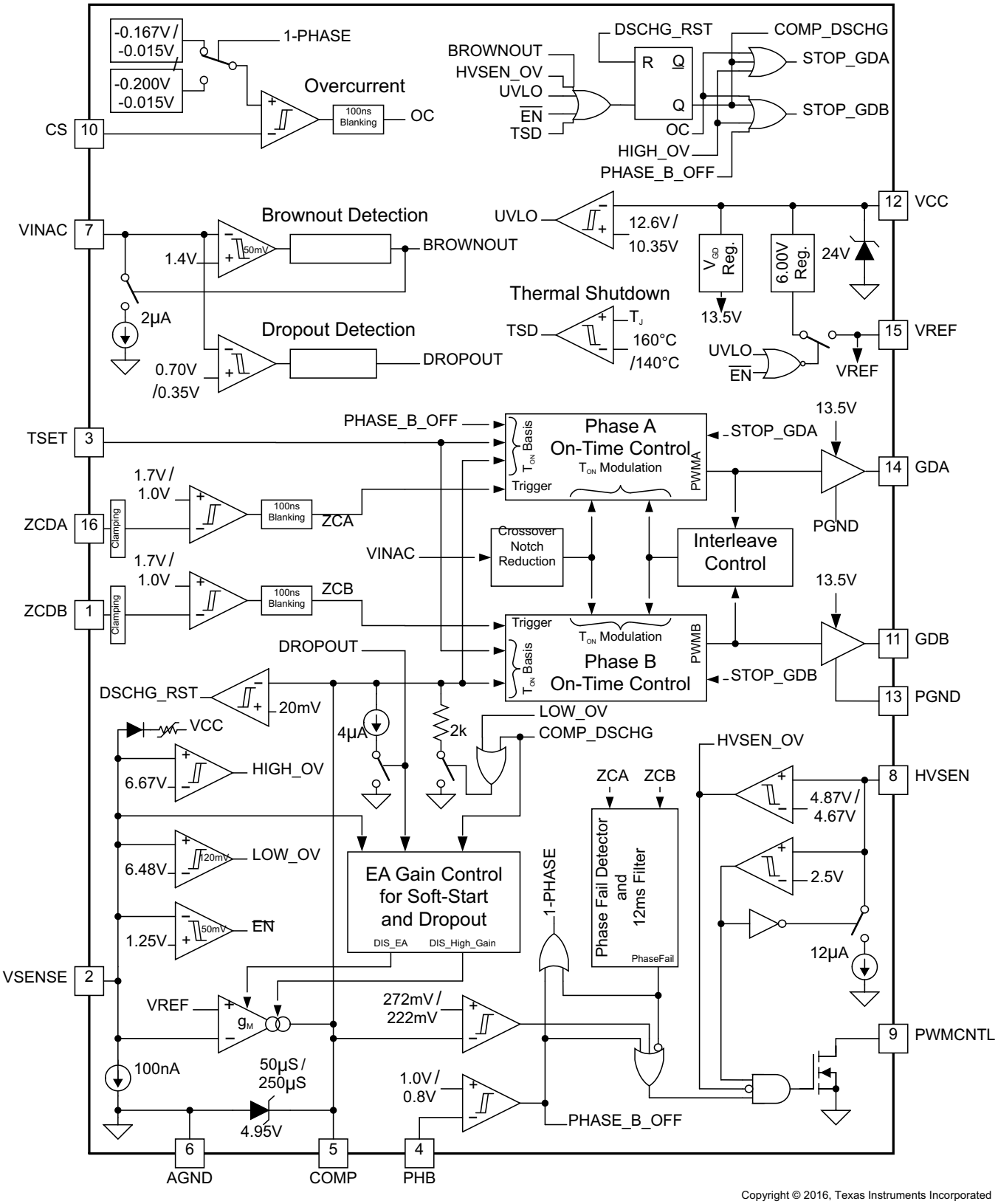
Interleaving control and phase management facilitates 80+ and Energy Star designs with reduced input and output ripple. The Natural Interleaving method allows TM operation and achieves 180 degrees between the phases by On-time management and does not rely on tight tolerance requirements on the inductors. The Crossover Notch Reduction block implements a non-linear current shaping characteristic on the instantaneous voltage sense (VINAC) in order to reduce distortion and increase Power Factor. Negative current sensing is implemented on the total input current instead of just the MOSFET current which prevents MOSFET switching during inrush surges or in any mode where the inductor current may become substantially continuous (CCM). This prevents reverse recovery conduction events between the MOSFET and output rectifier. Downstream power stage management is facilitated by the PWMCNTL signal. This open drain signal provides an enable with hysteresis for a downstream converter when the PFC stage voltage is above an operating threshold, FailSafe OV protection is not in operation and there is no PhaseFail fault.

Independent output voltage sense chains with their separate fault management behaviors provide a high degree of redundancy against PFC stage overvoltage. Brown-Out, HVSENSE OV, UVLO, and IC Overtemperature will all cause a complete Soft-Start cycle. Other faults such as short duration AC Drop-Out, minor overvoltage or cycle-by-cycle overcurrent cause a live recovery process to initiate by pulling down on the COMP pin or by terminating the pulses early.

In general IC operation is designed to ensure smooth and acoustic noise free start-up, good transient response behavior and well behaved recovery from faults. The Error amplifier transconductance is designed to allow smaller compensation components and optimum transient response for larger deviations. The Soft-Start process is carefully optimized. A complete Soft Start is implemented on recovery from every fault, for consistency. The Soft Start speed is dependent on the output voltage sense to speed up start-up from low AC line and to minimize the effect of excessive "COMP" during start-up into no-load. This complete discharge of COMP aids with preventing excessive currents on recovery from an AC Brown-Out event.

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8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Principles of Operation

The UCC28063A contains the control circuits for two parallel-connected boost pulse-width modulated (PWM) power converters. The boost PWM power converters ramp current in the boost inductors for a time period proportional to the voltage on the error amplifier output. Each power converter then turns off the power MOSFET until current in the boost inductor decays to zero, as sensed on the zero current detection inputs (ZCDA and ZCDB). Once the inductor is demagnetized, the power converter starts another cycle. This on/off cycling produces a triangle wave of current, with peak current set by the on-time and instantaneous power mains input voltage, $V_{IN}(t)$, as shown in Equation 1.

$$I_{PEAK}(t) = \frac{V_{IN}(t) \times T_{ON}}{L} \tag{1}$$

The average line current is exactly equal to half of the peak line current, as shown in Equation 2.

$$I_{AVG}(t) = \frac{V_{IN}(t) \times T_{ON}}{2 \times L} \tag{2}$$

With T_{ON} and L being essentially constant during an AC-line period, the resulting triangular current waveform during each switching cycle will have an average value proportional to the instantaneous value of the rectified AC-line voltage. This architecture results in a resistive input impedance characteristic at the line frequency and a near-unity power factor.

8.3.2 Natural Interleaving

Under normal operating conditions, the UCC28063A regulates the relative phasing of the channel A and channel B inductor currents to be very close to 180°. This greatly reduces the switching-frequency ripple currents seen at the line-filter and output capacitors, compared to the ripple current of each individual converter. This design allows a reduction in the size and cost of input and output filtering. The phase-control function differentially modulates the on-times of the A and B channels based on their phase and frequency relationship. The Natural Interleaving method allows the converter to achieve 180° phase-shift and transition-mode operation for both phases without tight requirements on boost inductor tolerance.

Ideally, the best current-sharing is achieved when both inductors are exactly the same value. Typically the inductances are not the same, so the current-sharing of the A and B channels is proportional to the inductor tolerance. Also, switching delays and resonances of each channel typically differ slightly, and the controller allows some necessary phase-error deviation from 180° to maintain equal switching frequencies. Optimal phase balance occurs if the individual power stages and the on-times are well matched. Mismatches in inductor values do not affect the phase relationship.

8.3.3 On-Time Control, Maximum Frequency Limiting, and Restart Timer

Gate-drive on-time varies proportionately with the error-amplifier output voltage by a factor called K_T (in units of μs/V), as shown in Equation 3.

$$T_{ON} = K_T \left(V_{COMP} - 125\,mV\right) \tag{3}$$

Where:

- V_{COMP} is the output voltage of the error amplifier and 125 mV is a modulator offset voltage.

The maximum output of the error amplifier is limited to 4.95 V. This value, minus the 125-mV modulator offset, limits maximum on-time as determined by Equation 4.

$$T_{ON(max)} = K_T \times 4.825\,V \tag{4}$$

This on-time limit sets the maximum power that can be delivered by the converter at a given input voltage.

At lower power, one boost channel (phase) may be turned off to achieve efficiency benefits (see Phase Management section, below). To provide a smooth transition between two-phase and single-phase operation, K_T increases by a factor of two in single-phase mode:

$$K_{TS} = 2 \times K_T; \text{ active during single-phase operation} \tag{5}$$

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Feature Description (continued)

The maximum switching frequency of each phase is limited by minimum-period timers. If inductor current decays to zero before the minimum-period timer elapses, the next turn-on will be delayed, resulting in discontinuous phase current.

A restart timer ensures starting under all circumstances by restarting both phases if the ZCD input of either phase has not transitioned from high-to-low within approximately 200 µs. To prevent the circuit from operating in continuous conduction mode (CCM), the restart timer does not trigger turn-on until both phase-currents return to zero.

The on-time factors (K_T, K_{TS}) and the minimum switching period, $T_{(MIN)}$, are proportional to the time-setting resistor R_{TSET} (the resistor from the TSET pin to ground), and these factors can be calculated by Equation 5, Equation 6 and Equation 7:

$$K_T = \frac{R_{TSET}}{133\,k\Omega} \times 4.0 \frac{\mu s}{volt} \quad (6)$$

$$T_{(MIN)} = \frac{R_{TSET}}{133\,k\Omega} \times 2.2\,\mu s \text{ ; Minimum Switching Period} \quad (7)$$

The proper value of R_{TSET} will result in the clamped maximum on-time, $T_{ON(max)}$, required by the converter operating at the minimum input line voltage and maximum load.

8.3.4 Distortion Reduction

Due to the parasitic resonance between the drain-source capacitance of the switching MOSFET and the boost inductor, conventional transition-mode PFC circuits may not be able to absorb power from the input line when the input voltage is near zero. This limitation increases total harmonic distortion as a result of ac-line current waveform distortion in the form of flat spots. To help reduce line-current distortion, the UCC28063A increases switching MOSFET on-time when the input voltage is near 0 V to improve the power absorption capability and compensate for this effect.

Figure 12 in the Typical Characteristics section shows the increase in on-time with respect to VINAC voltage. Excessive filtering of the VINAC signal will nullify this function.

8.3.5 Zero-Current Detection and Valley Switching

In transition-mode PFC circuits, the MOSFET turns on when the boost inductor current reaches zero. Because of the resonance between the boost inductor and the parasitic capacitance at the MOSFET drain node, part of the energy stored in the MOSFET junction capacitor can be recovered, reducing switching losses. Furthermore, when the rectified input voltage is less than half of the output voltage, all the energy stored in the MOSFET junction capacitor can be recovered and zero-voltage switching (ZVS) can be realized. By adding an appropriate delay, the MOSFET can be turned on at the valley of its resonating drain voltage (valley-switching). In this way, the energy recovery can be maximized and switching loss is minimized.

The optimal time delay is generally derived empirically, but a good starting point is a value equal to 25% of the resonant period of the drain circuit. The delay can be realized by a simple RC filter, as shown in Figure 25, but the delay time increases slightly as the input voltage nears the output voltage. Because the ZCD pin is internally clamped, a more accurate delay can also be realized by using the circuit shown in Figure 26.

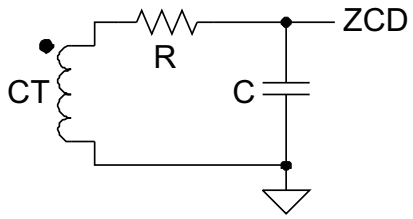


Figure 25. Simple RC Delay Circuit

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Feature Description (continued)

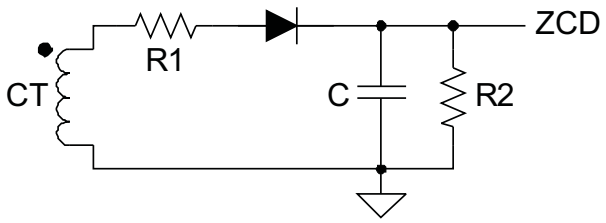


Figure 26. More Accurate Time Delay Circuit

8.3.6 Phase Management and Light-Load Operation

Under light-load conditions, switching losses may dominate over conduction losses and efficiency may be improved if one phase (channel) is turned off. At a certain power level, the reduction of switching losses is greater than the increase in conduction losses. Turning off one phase at light load is especially valuable for meeting light-load efficiency standards. This is one of the major benefits of interleaved PFC and it is especially valuable for meeting 80+ design requirements.

The PHB input can be used to force the UCC28063A to operate in single-phase mode. When PHB is driven below 0.8 V, channel B will stop switching and channel A on-time will automatically double to compensate. The device will resume dual-phase mode when PHB is raised above 1.0 V. For customized phase management, an external circuit can detect the conditions for switching to single-phase operation and drive PHB accordingly. To operate continuously in two-phase mode (normal mode) when phase management is not desired, simply connect PHB to VREF.

As load current decreases, the error amplifier commands less ac-line input current by lowering COMP voltage. In applications where the ac-line is limited to the low-voltage range only, it may be advantageous to connect PHB directly to COMP to allow automatic selection of single-phase operation without additional external circuitry.

8.3.7 External Disable

The UCC28063A can be externally disabled by purposefully grounding the VSENSE pin with an open-drain or open-collector driver. When disabled, the device supply current drops significantly and COMP is actively pulled low. This disable method forces the device into standby mode and minimizes its power consumption. This is particularly useful when standby power is a key design aspect. When VSENSE is released, the device enters soft-start mode.

8.3.8 Improved Error Amplifier

The voltage-error amplifier is a transconductance amplifier. Voltage-loop compensation is connected from the error amplifier output, COMP, to analog ground, AGND. The recommended Type-II compensation network is shown in Figure 27. For loop-stability purposes, the compensation network values are calculated based on small-signal perturbations of the output voltage using the nominal transconductance (gain) of 55 μS.

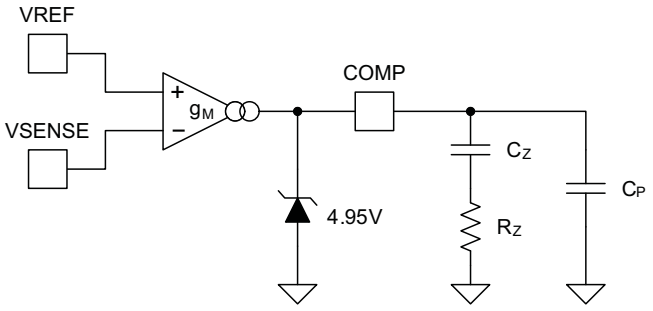
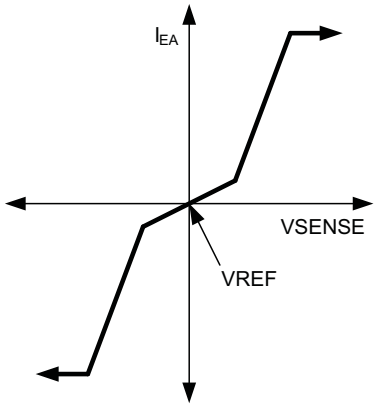


Figure 27. Transconductance Error Amplifier With Typical Compensation Network

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Feature Description (continued)

To improve the transient response to large perturbations, the error amplifier gain increases by a factor of ~5X when the error amp input deviates more than ±5% from the nominal regulation voltage, VSENSEreg. This increase allows faster charging and discharging of the compensation components following sudden load-current increases or decreases (also refer to Figure 5 in the *Typical Characteristics*).



Basic voltage-error amplifier transconductance curve showing small-signal and large-signal gain sections, with maximum current limitations.

Figure 28. Basic Voltage-Error Amplifier Transconductance Curve

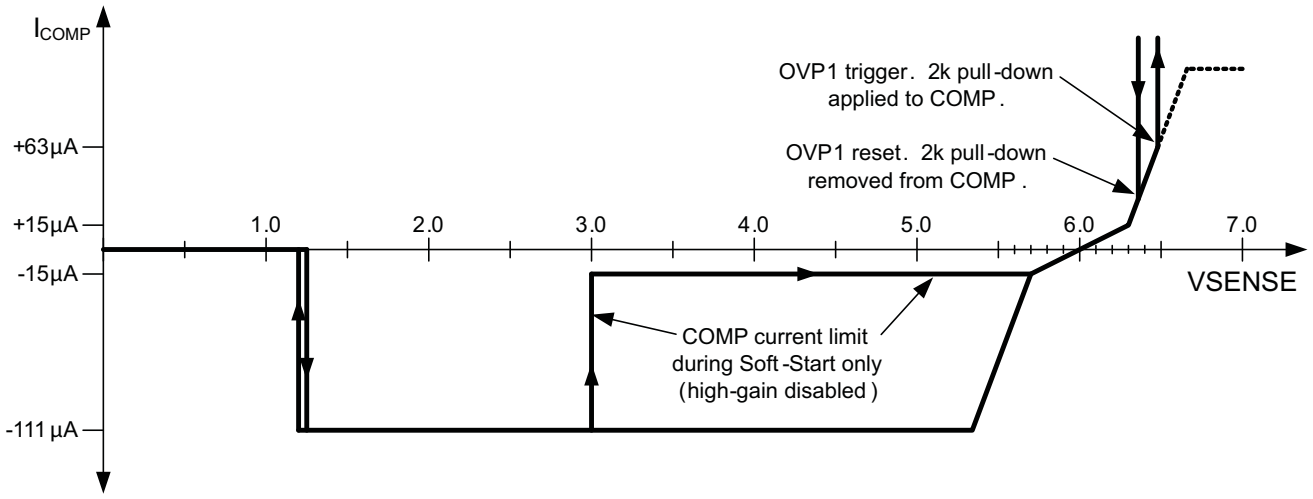
8.3.9 Soft Start

Soft-start is a process for boosting the output voltage of the PFC converter from the peak of the ac-line input voltage to the desired regulation voltage under controlled conditions. Instead of a dedicated soft-start pin, the UCC28063A uses the voltage error amplifier as a controlled current source to increase the PWM duty-cycle by way of increasing the COMP voltage. To avoid excessive start-up time-delay when the ac-line voltage is low, a higher current is applied until VSENSE exceeds 3 V at which point the current is reduced to minimize the tendency for excess COMP voltage at no-load start-up.

The PWM gradually ramps from zero on-time to normal on-time as the compensation capacitor from COMP to AGND charges from zero to near its final value. This process implements a soft-start, with timing set by the output current of the error amplifier and the value of the compensation capacitors. In the event of a HVSEN FailSafe OVP, brownout, external-disable, UVLO fault, or other protection faults, COMP is actively discharged and the UCC28063A will soft-start after the triggering event is cleared. Even if a fault event happens very briefly, the fault is latched into the soft-start state and soft-start is delayed until COMP is fully discharged to 20 mV and the fault is cleared. See Figure 29 for details on the COMP current. See Figure 30 which illustrates an example of typical system behavior during soft-start.

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Feature Description (continued)



Expanded COMP output current curve including voltage-error amplifier transconductance and modifications applicable to soft-start and overvoltage conditions.

Figure 29. Expanded Comp Output Current Curve

Feature Description (continued)

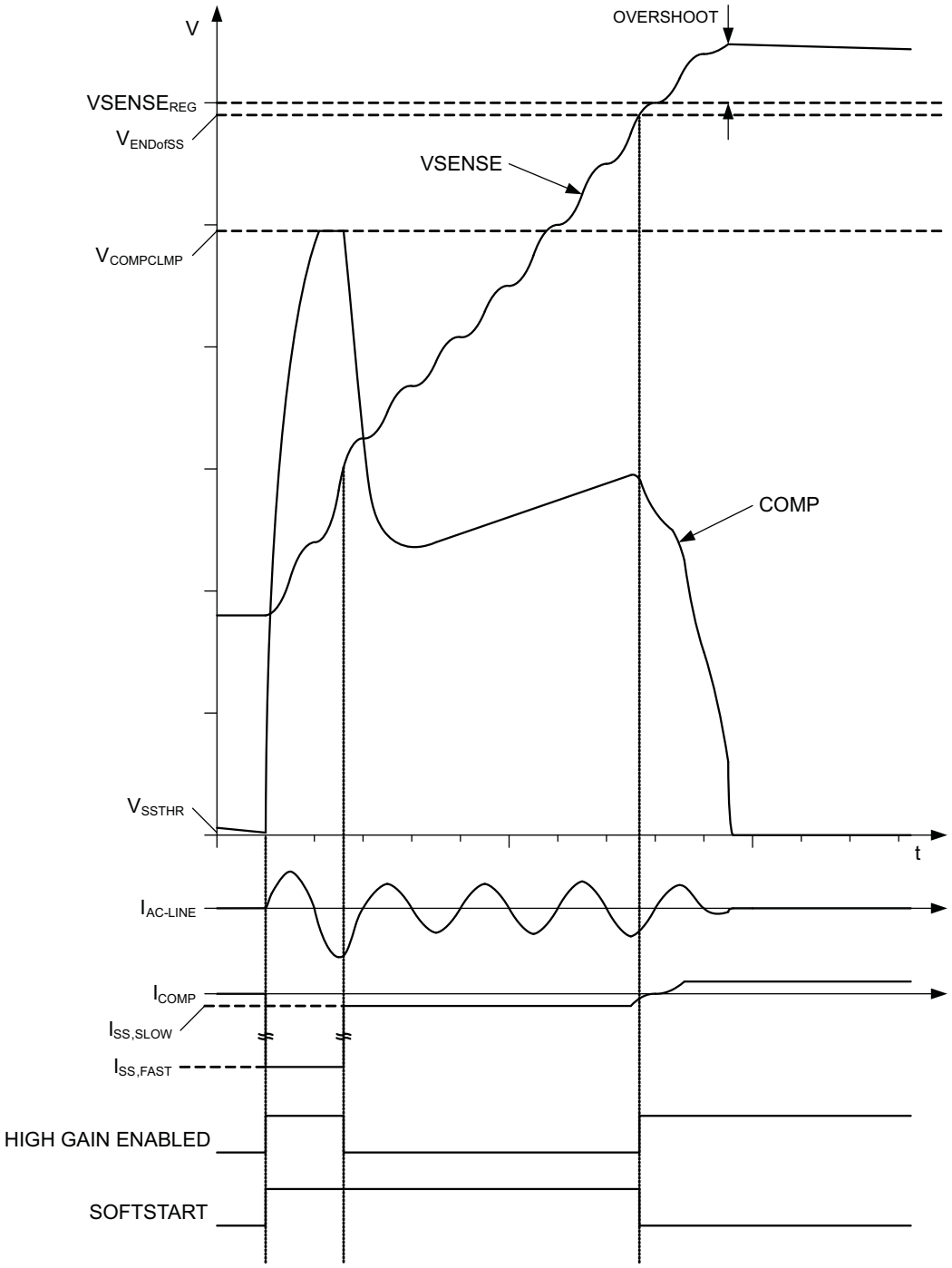


Figure 30. Soft-Start Timing With Illustrative System Behavior

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Feature Description (continued)

8.3.10 Brownout Protection

As the power line RMS voltage decreases, RMS input current must increase to maintain a constant output voltage for a specific load. Brownout protection helps prevent excess system thermal stress (due to the higher RMS input current) from exceeding a safe operating level. Power-line voltage is sensed at VINAC. When the VINAC fails to exceed the brownout threshold for the brownout filter time, a brownout condition is detected and both gate drive outputs are turned off. During brownout, COMP is actively pulled low and a soft-start condition is initiated. Hysteresis is built into the brownout detection circuit to avoid chatter around the threshold. When VINAC rises above the brownout threshold, the power stage soft-starts as COMP rises with controlled current.

The brownout detection threshold and its hysteresis are set by the voltage-divider ratio and resistor values. Brownout protection is based on VINAC peak voltage; the threshold and hysteresis are also based on the line peak voltage. Major hysteresis is provided by a 2-μA current-sink (I_{BOHYS}) enabled whenever VINAC falls below the brownout detection threshold. Minor hysteresis is also present in the form of a 50-mV offset (V_{BOHYS}) between the VINAC detection and clear thresholds. The peak VINAC voltage can be easily translated into an RMS value. Example resistor values for the voltage divider are 8.61 MΩ ±1% from the rectified input voltage to VINAC and 133 kΩ ±1% from VINAC to ground. These resistors set the typical thresholds for RMS line voltages, as shown in Table 1.

Table 1. Brownout Thresholds (For Conditions Stated in the Text)

THRESHOLD	AC-LINE VOLTAGE (RMS)
Falling	66 V
Rising	78 V

Equation 8 and Equation 9 can be used to calculate the VINAC divider-resistor values based on desired brownout detection and brownout clear voltage levels. V_{AC_OK} is the desired RMS turn-on voltage, V_{AC_BO} is the desired RMS turn-off brownout voltage, and V_{LOSS} is total series voltage drop due to wiring, EMI-filter, and bridge-rectifier impedances at V_{AC_BO}. V_{BODET}, V_{BOHYS} and I_{BOHYS} are found in the data-tables of this datasheet.

$$R_A = \left(\frac{\sqrt{2}(V_{AC_OK} - V_{AC_BO}) - V_{BOHYS}}{I_{BOHYS}} \right) \left(1 + \frac{V_{BOHYS}}{V_{BODET}} \right) \tag{8}$$

$$R_B = \frac{R_A}{\left(\frac{\sqrt{2} V_{AC_BO} - V_{LOSS}}{V_{BODET}} - 1 \right)} \tag{9}$$

Once standard values for the VINAC divider-resistors R_A and R_B are selected, the actual turn-on and brownout threshold RMS voltages for the ac-line can be back-calculated with Equation 10 and Equation 11:

$$V_{AC_BO} = \left(1 + \frac{R_A}{R_B} \right) \frac{V_{BODET}}{\sqrt{2}} + \frac{V_{LOSS}}{\sqrt{2}} \tag{10}$$

$$V_{AC_OK} = V_{AC_BO} + \frac{R_A I_{BOHYS}}{\sqrt{2}\left(1 + \frac{V_{BOHYS}}{V_{BODET}} \right)} + \frac{V_{BOHYS}}{\sqrt{2}} \tag{11}$$

An example of the timing for the brownout function is illustrated in Figure 31.

For a quick estimation of the turn-on and brownout voltages, simplify the foregoing equations by setting the V_{LOSS} and V_{BOHYS} terms to zero.

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8.3.11 Dropout Detection

It is often the case that the ac-line voltage momentarily drops to zero or nearly zero, due to transient abnormal events affecting the local ac power distribution network. Referred to as ac-line dropouts (or sometimes as line-dips) the duration of such events usually extends to only 1 or 2 line cycles. During a dropout, the down-stream power conversion stages depend on sufficient energy storage in the PFC output capacitance, which is sized to provide the ride-through energy for a specified hold-up time. Typically while the PFC output voltage is falling, the voltage-loop error amplifier output rises in an attempt to maintain regulation. As a consequence, excess duty-cycle is commanded when the ac-line voltage returns and high peak current surges may saturate the boost inductors with possible overstress and audible noise.

The UCC28063A incorporates a dropout detection feature which suspends the action of the error amplifier for the duration of the dropout. If the VINAC voltage falls below 0.35 V for longer than 5 ms, a dropout condition is detected and the error amplifier output is turned off. In addition, a 4-μA pull-down current is applied to COMP to gently discharge the compensation network capacitors. In this way, when the ac-line voltage returns, the COMP voltage (and corresponding duty-cycle setting) remains very near or even slightly below the level it was before the dropout occurred. Current surges due to excess duty-cycle, and their undesired attendant effects, are avoided. The dropout condition is cancelled and the error amplifier resumes normal operation when VINAC rises above 0.71 V.

Based on the VINAC divider-resistor values calculated for brownout in the previous section, the input RMS voltage thresholds for dropout detection V_{AC_DO} and dropout clearing V_{DO_CLR} can be determined using Equation 12 and Equation 13, below.

$$V_{AC_DO} = \frac{V_{DODET}\left(\frac{R_A}{R_B}+1\right)+V_{LOSS}}{\sqrt{2}} \quad (12)$$

$$V_{DO_CLR} = \frac{V_{DOCLR}\left(\frac{R_A}{R_B}+1\right)+V_{LOSS}}{\sqrt{2}} \quad (13)$$

Avoid excessive filtering of the VINAC signal, or dropout detection may be delayed or defeated. An RC time-constant of ≤ 100-μs should provide good performance. An example of the timing for the dropout function is illustrated in Figure 32.

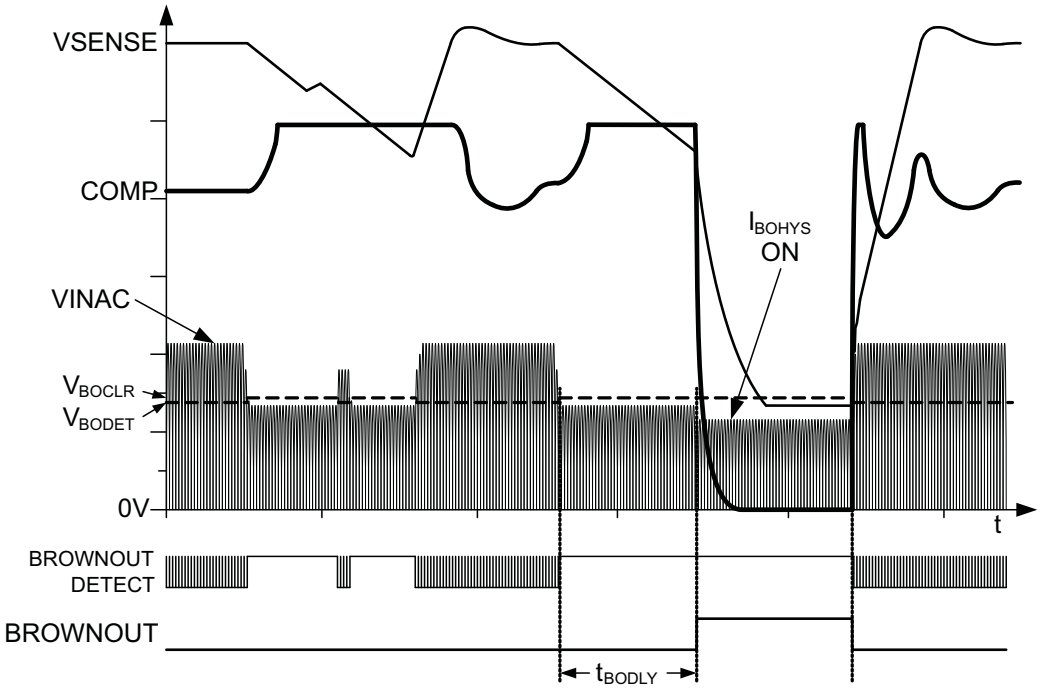


Figure 31. AC-Line Brownout Timing With Illustrative System Behavior

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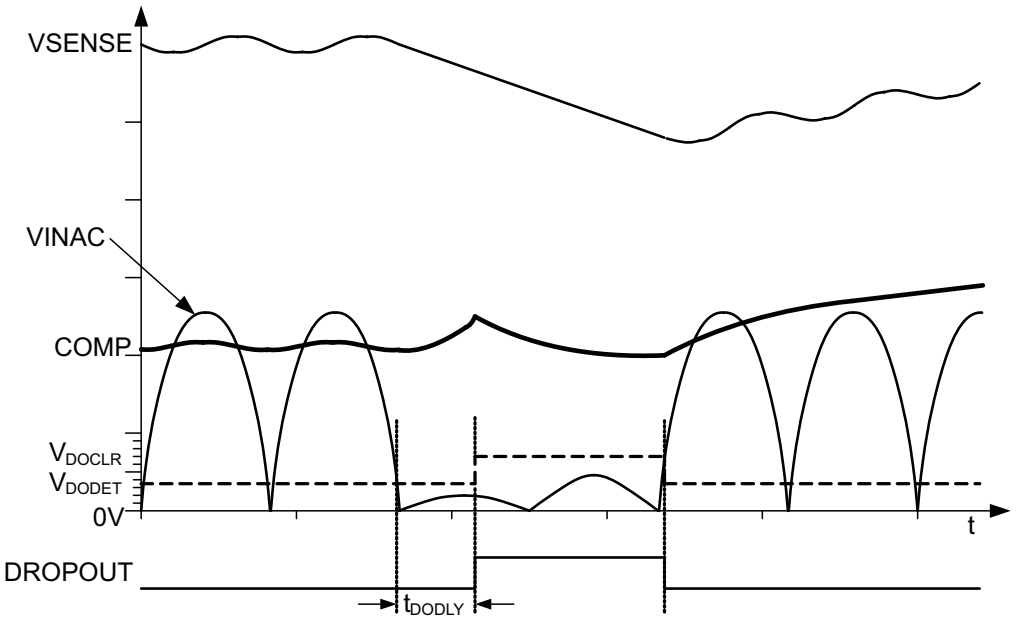


Figure 32. AC-Line Dropout Timing With Illustrative System Behavior

8.3.12 VREF

VREF is an output which supplies a well-regulated reference voltage to circuits within the device as well as serving as a limited source for external circuits. This output must be bypassed to GND with a low-impedance 0.1-μF or larger capacitor placed as close to the VREF and GND pins as possible. Current draw by external circuits should not exceed a few milli-amperes and should not be pulsing.

The VREF output is disabled under the following conditions: when VCC is in UVLO, or when VSENSE is below the Enable threshold. This output can only source current and is unable to accept current into the pin.

8.3.13 VCC

VCC is usually connected to a bias supply of between 13 V and 21 V. To minimize switching ripple voltage on VCC, it should be by-passed with a low-impedance capacitor as close to the VCC and GND pins as possible. The capacitance should be sized to adequately decouple the peak currents due to gate-drive switching at the highest operating frequency. When powered from a poorly-regulated low-impedance supply, an external zener diode is recommended to prevent excessive current into VCC.

The undervoltage-lockout (UVLO) condition is when VCC voltage has not yet reached the turn-on threshold or has fallen below the turn-off threshold, having already been turned on. While in UVLO, the VREF output and most circuits within the device are disabled and VCC current falls significantly below the normal operating level. The same situation applies when VSENSE is below its Enable threshold. This helps minimize power loss during pre-powerup and standby conditions.

8.3.14 Control of Downstream Converter

In the UCC28063A, the PWMCNTL pin can be used to coordinate the PFC stage with a downstream converter. Through the HVSEN pin, the PFC output voltage is monitored. A 12-μA current source (I_{HV_HYS}) is enabled as long as the output voltage remains below a programmed threshold. When the output voltage exceeds that threshold, PWMCNTL pin is pulled to ground internally and can be used to enable a downstream converter. At the same time the current source is disabled, providing hysteresis for a lower threshold at which the downstream converter should be turned off. The enable/disable hysteresis is adjusted through the HVSEN voltage-divider ratio and resistor values. The HVSEN pin is also used for the FailSafe over-voltage protection (OVP). When designing the voltage divider, make sure this FailSafe OVP level is set above normal VSENSE OVP levels.

Because there are two thresholds associated with the HVSEN input detected through a single resistor divider, the PWMCNTL turn-off voltage, $V_{PWM-OFF}$, is linked to the FailSafe OVP voltage, V_{FLSF_OV}, as shown by Equation 14:

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$$\frac{V_{PWM-OFF}}{2.5\,V} = \frac{V_{FLSF_OV}}{4.87\,V} \quad (14)$$

Choosing either one first arbitrarily determines the other, so a trade-off may be necessary. The PWMCNTL turn-on voltage, V_{PWM-ON}, is programmed by choosing the upper divider resistor value in consideration with the HVSEN hysteresis current, as shown in Equation 15 and Equation 16. The lower divider resistor is then calculated as shown in Equation 17.

$$V_{PWM-ON} = V_{PWM-OFF} + I_{HV_HYS} R_{HV_UPPER} \quad (15)$$

$$R_{HV_UPPER} = \frac{V_{PWM-ON} - V_{PWM-OFF}}{I_{HV_HYS}} \quad (16)$$

$$R_{HV_LOWER} = \frac{R_{HV_UPPER}}{\left(\frac{V_{PWM-OFF}}{2.5\,V} - 1\right)} \quad (17)$$

8.3.15 System Level Protections

8.3.15.1 Failsafe OVP - Output Overvoltage Protection

FailSafe OVP prevents any single failure from allowing the output to boost above safe levels. Redundant paths for output voltage sensing provide additional protection against output over-voltage. Over-voltage protection is implemented through two independent paths: VSENSE and HVSEN. The converter shuts down if either input senses a severe over-voltage condition. The output voltage can still remain below a safe limit if either sense path fails. The device is re-enabled when both sense inputs fall back into their normal ranges. At that time, the gate drive outputs will resume switching under PWM control. A low-level over-voltage on VSENSE does not trigger soft-start, but the COMP pin is discharged by an internal 2-kΩ resistance until the output voltage falls below the 2% hysteresis OV-clear threshold. A higher-level over-voltage on VSENSE additionally shuts off the gate-drive outputs until the OV clears, but still does not trigger a soft-start. However, an overvoltage detected on HVSEN does trigger a full soft-start and the COMP pin is fully discharged to 20 mV before the soft-start can begin.

8.3.15.2 Overcurrent Protection

Under certain conditions (such as inrush, brownout-recovery, and output over-load) the PFC power stage sees large currents. It is critical that the power devices be protected from switching during these conditions.

The conventional current-sensing method uses a shunt resistor in series with each MOSFET source leg to sense the converter currents, resulting in multiple ground points and high power dissipation. Furthermore, since no current information is available when the MOSFETs are off, the source-resistor current-sensing method results in repeated turn-on of the MOSFETs during overcurrent (OC) conditions. Consequently, the converter may temporarily operate in continuous conduction mode (CCM) and may experience failures induced by excessive reverse-recovery currents in the boost diodes or other abnormal stresses.

The UCC28063A uses a single resistor to continuously sense the combined total inductor (input) current. This way, turn-on of the MOSFETs is completely avoided when the inductor currents are excessive. The gate drive to the MOSFETs is inhibited until total inductor current drops to near zero, precluding reverse-recovery-induced failures (these failures are most likely to occur when the ac-line recovers from a brownout condition).

The nominal OC threshold voltage during two-phase operation is -200 mV, which helps minimize losses. This threshold is automatically reduced to -166 mV during single-phase operation, either by detection of a phase failure or because PHB is driven below 0.8 V. Note that the single-phase threshold is not simply 1/2 of the dual-phase threshold, because the ratio of the single-phase peak current to the interleaved peak current is higher than 1/2.

An OC condition immediately turns off both gate-drive outputs, but does not trigger a soft-start and does not modify the error amplifier operation. The over-current condition is cleared when the total inductor current-sense voltage falls below the OC-clear threshold (-15 mV).

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Following an over-current condition, both MOSFETs are turned on simultaneously once the input current drops to near zero. Because the two phase currents are temporarily operating in-phase, the current-sense resistance should be chosen so that OC protection is not triggered with twice the maximum current peak value of either phase in order to allow quick return to normal operation after an over-current event. Automatic phase-shift control will re-establish interleaving within a few switching cycles.

8.3.15.3 Open-Loop Protection

If the feedback loop is disconnected from the device, a 100-nA current source internal to the UCC28063A pulls the VSENSE pin voltage towards ground. When VSENSE falls below 1.20 V, the device becomes disabled. When disabled, the bias supply current decreases, both gate-drive outputs and COMP are actively pulled low, and a soft-start condition is initiated. The device is re-enabled when VSENSE rises above 1.25 V. At that time, the gate drive outputs will begin switching under soft-start PWM control.

If the feedback loop is disconnected from ground, the VSENSE voltage will be pulled high. When VSENSE rises above the 2nd-level over-voltage protection threshold, both gate drive outputs are shut off and COMP is actively pulled low. The device is re-enabled when VSENSE falls below the OV-clear threshold. The VSENSE input can tolerate a limited amount of current into the device under abnormally high input voltage conditions. Refer to the Absolute Maximum Ratings table near the beginning of this datasheet for details.

8.3.15.4 VCC Undervoltage Lock-Out (UVLO) Protection

VCC must rise above the turn-on threshold for the PWM to begin functioning. If VCC drops below the UVLO threshold during operation, both gate-drive outputs are actively pulled low, COMP is actively pulled low, and a soft-start condition is triggered. VCC must again rise above the turn-on threshold for the PWM function to restart in soft-start mode.

8.3.15.5 Phase-Fail Protection

The UCC28063A detects failure of either of the phases by monitoring the sequence of ZCD pulses. During normal two-phase operation, if one ZCD input remains idle for longer than approximately 12 ms while the other ZCD input switches normally, the over-current threshold is reduced and PWMCNTL goes to a high-impedance state, indicating that the PFC power stage is not operating correctly. During normal single-phase operation (PHB < 0.8 V), phase failure is not monitored. Also on the UCC28063A, phase failure is not monitored when COMP is below approximately 222 mV.

8.3.15.6 Thermal Shutdown Protection

Overloading of the gate-drive outputs, VREF, or both can dissipate excess power within the device which may raise the internal temperature of the circuits beyond a safe level. Even normal power dissipation can generate excess heat if the thermal impedance is too high or the ambient temperature is too high. When the UCC28063A detects an internal over-temperature condition it will shutdown the outputs and trigger a full soft-start condition. When the internal device junction temperature has cooled below the thermal hysteresis temperature, operation will resume under soft-start control.

8.3.15.7 AC-Line Brownout and Dropout Protections

See specific discussions for each topic in previous sections of this data sheet.

8.3.15.8 Fault Logic Diagram

Figure 33 depicts the fault-handling logic involving VSENSE, COMP, and several internal states.

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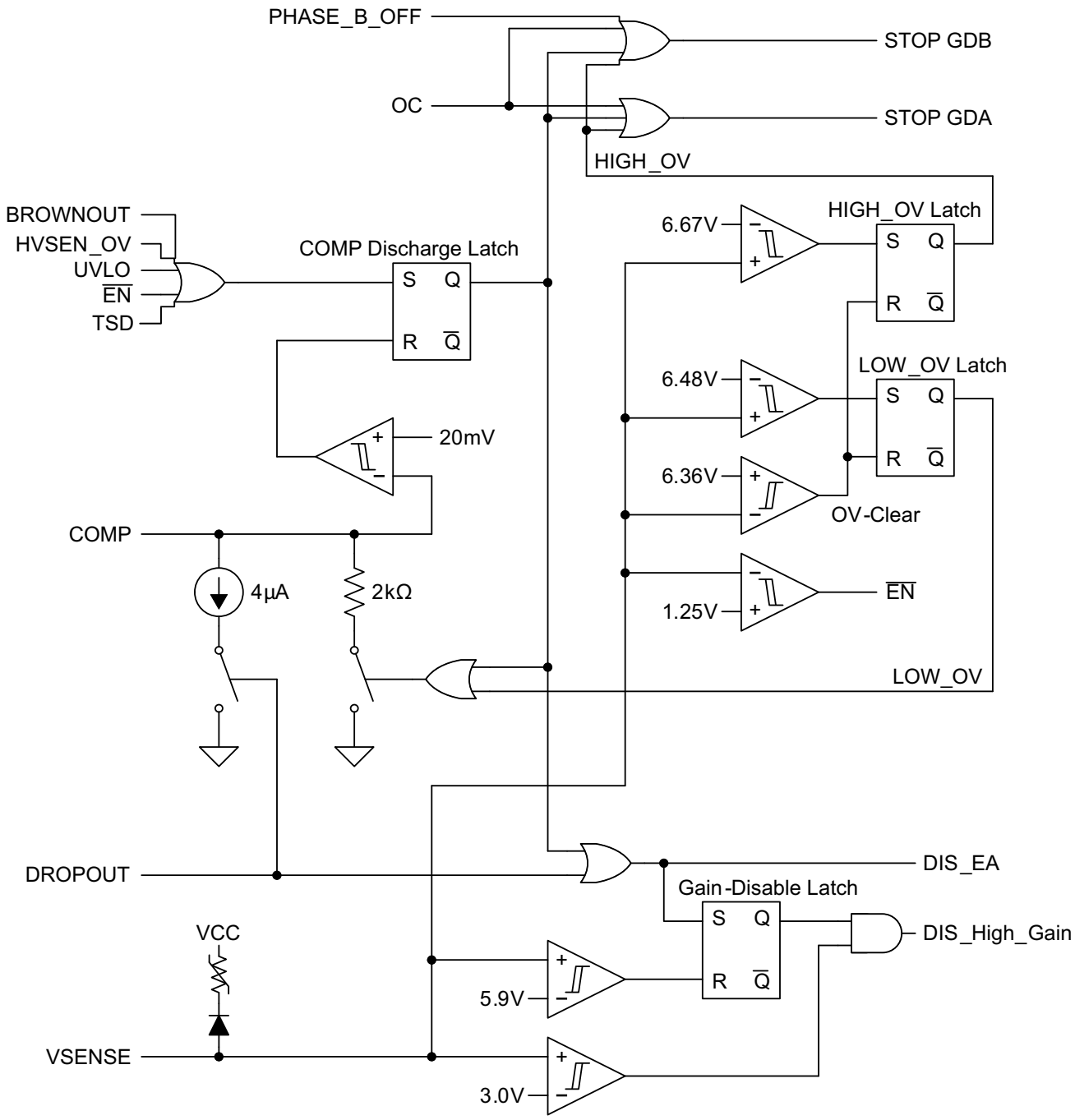


Figure 33. Fault Logic With VSENSE Detections and Error Amplifier Control

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8.4 Device Functional Modes

The controller is primarily intended for set up as a dual phase interleaved PFC which utilizes inductor demagnetization information based on inductor sense winding voltages which are routed to ZCDA and ZCDB to trigger the start of a switching cycle.

The functionality may be extended in a couple of ways:

- **Phase-B Enable and Disable:** Phase-B may be *shed* by explicit user control or it may be set up as an automatic light load efficiency management feature. When the voltage applied to the PHB pin is below VPHBF threshold, Phase B and the Phase Fail Detector will be disabled. The commanded On-time for Phase-A will be doubled to minimize the output voltage transient which would otherwise occur. When the voltage on the PHB pin is greater than the VPHBR threshold, two phase mode is continuously enabled. Tie PHB to VREF pin for this mode. Alternatively PHB may be tied to the COMP pin for *automatic* phase shedding at light load.
- **PFC Stage Enable and Disable Control:** Controller operation is enabled when VSENSE voltage exceeds the 1.25-V enable threshold. The primary disable method should be by pulling VSENSE low by an open drain or open collector logic output. This will disable the outputs and significantly reduce VCC current. Releasing VSENSE will initiate a Soft-Start. Avoid any PCB traces which would couple any noise into this node.

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9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

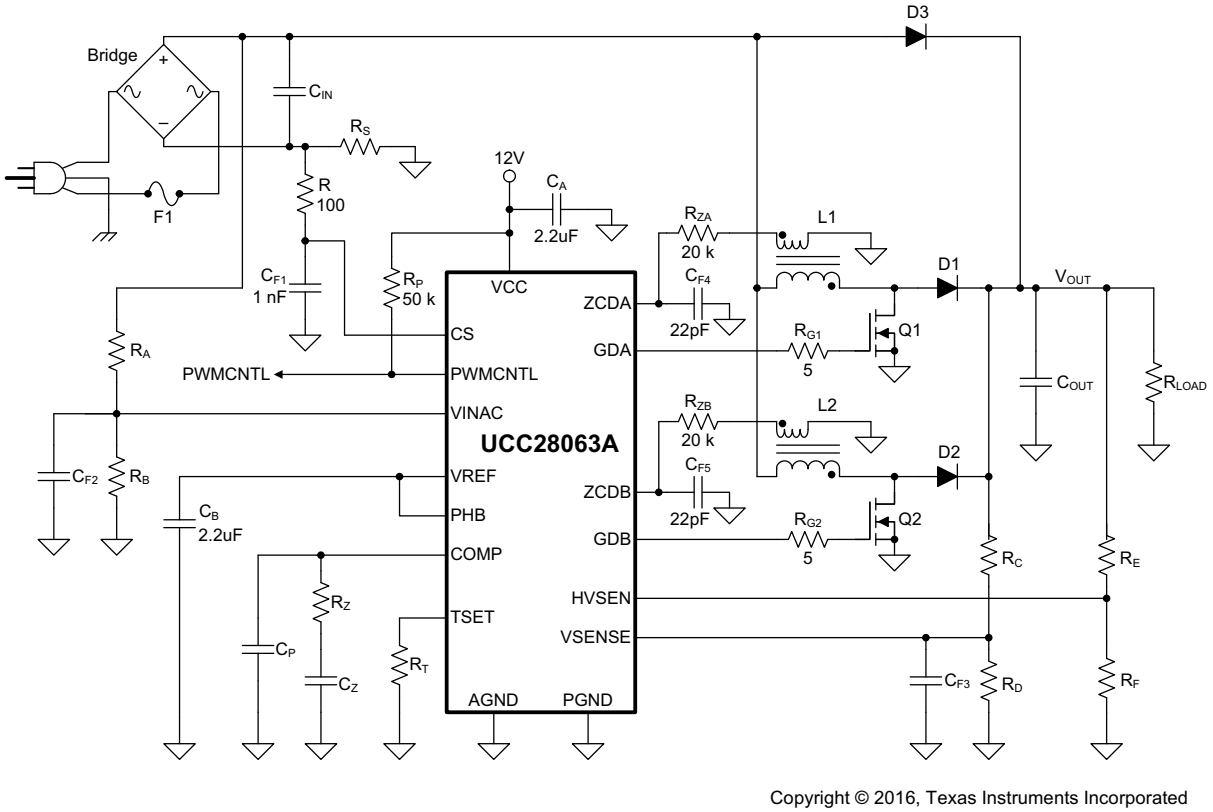
This control IC is generally applicable to the control of AC-DC power supplies which require Active Power Factor Correction off Universal AC line. Applications using this IC will generally meet the Class D equipment input current harmonics standards per EN61000-3-2. This standard applies to equipment with rated Powers higher than 75W. The IC brings two phase interleaved control capability to the Transition Mode Boost and hence will be generally a very good choice for cost optimized applications in the 150W to 800W space, or to even lower powers that wish to exploit the interleaving benefits of reduced filtering component size, lower profile solutions and distributed thermal management.

The *UCC28063EVM-723 300-W Interleaved PFC Pre-Regulator User's Guide* (SLUU512) describes an EVM design for a 300W Application.

This EVM has an associated Excel file to help automate calculations for its component choices available at SLUC292.

9.2 Typical Application

An example of the UCC28063A PFC controller in a two-phase interleaved, transition-mode PFC pre-regulator is shown in .



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Figure 34. Typical Interleaved Transition-Mode PFC Pre-Regulator

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Typical Application (continued)

9.2.1 Design Requirements

The specifications for this design were chosen based on the power requirements of a typical 300-W LCD TV. These specifications are shown in Table 2.

Table 2. Design Specifications

DESIGN PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	RMS input voltage	85 (VIN_MIN)		265 (VIN_MAX)	VRMS
V_{OUT}	Output voltage		390		V
f_{LINE}	AC-line frequency	47		63	Hz
PF	Power factor at maximum load	0.90			
P_{OUT}				300	W
η	Full-load efficiency	92%			
f_{MIN}	Minimum switching frequency	45			kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

The boost inductor is selected based on the inductor ripple current requirements at the peak of low line. Selecting the inductor requires calculating the boost converter duty cycle at the peak of low line ($D_{PEAK_LOW_LINE}$), as shown in Equation 18.

$$D_{PEAK_LOW_LINE} = \frac{V_{OUT} - V_{IN_MIN}\sqrt{2}}{V_{OUT}} = \frac{390\,V - 85\,V\sqrt{2}}{390\,V} \approx 0.69 \quad (18)$$

The minimum switching frequency of the converter (f_{MIN}) under low line conditions occurs at the peak of low line and is set between 25 kHz and 50 kHz to avoid audible noise. For this design example, f_{MIN} is set to 45 kHz. For a 2-phase interleaved design, L1 and L2 are determined as shown in Equation 19.

$$L1 = L2 = \frac{\eta \times V_{IN_MIN}^{2} \times D_{PEAK_LOW_LINE}}{P_{OUT} \times f_{MIN}} = \frac{0.92(85\,V)^{2}0.69}{300\,W \times 45\,kHz} \approx 340\,\mu H \quad (19)$$

The inductor for this design would have a peak current (I_{LPEAK}) of 5.4 A, as shown in Equation 20, and an RMS current (I_{LRMS}) of 2.2 A, as shown in Equation 21.

$$I_{LPEAK} = \frac{P_{OUT}\sqrt{2}}{V_{IN_MIN} \times \eta} = \frac{300\,W\sqrt{2}}{85\,V \times 0.92} \approx 5.4\,Apk \quad (20)$$

$$I_{LRMS} = \frac{I_{LPEAK}}{\sqrt{6}} = \frac{5.4\,A}{\sqrt{6}} \approx 2.2\,Arms \quad (21)$$

This converter uses constant on time (T_{ON}) and zero-current detection (ZCD) to set up the converter timing. Auxiliary windings on L1 and L2 detect when the inductor currents are zero. Selecting the turns ratio using Equation 22 ensures that there will be at least 2 V at the peak of high line to reset the ZCD comparator after every switching cycle.

The turns-ratio of each auxiliary winding is:

$$\frac{N_P}{N_s} = \frac{V_{OUT} - V_{IN_MAX}\sqrt{2}}{2\,V} = \frac{390\,V - 265\,V\sqrt{2}}{2\,V} \approx 8 \quad (22)$$

9.2.2.2 ZCD Resistor Selection (R_{ZA}, R_{ZB})

The minimum value of the ZCD resistors is selected based on the internal clamps maximum current ratings of 3 mA, as shown in Equation 23.

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$$R_{ZA} = R_{ZB} \geq \frac{V_{OUT} N_S}{N_P \times 3\,mA} = \frac{390\,V}{8 \times 3\,mA} \approx 16.3\,k\Omega \quad (23)$$

In this design the ZCD resistors are set to 20 kΩ, as shown in Equation 24.

$$R_{ZA} = R_{ZB} = 20\,k\Omega \quad (24)$$

9.2.2.3 HVSEN

The HVSEN pin programs the PWMCNTL output of the UCC28063A. The PWMCNTL open-drain output can be used to disable a downstream converter while the PFC output capacitor is charging. PWMCNTL starts high impedance and pulls to ground when HVSEN increases above 2.5 V. Setting the point where PWMCNTL becomes active requires a voltage divider from the boost voltage to the HVSEN pin to ground. Equation 25 to Equation 30 show how to set the PWMCNTL pin to activate when the output voltage is within 90% of its nominal value.

$$V_{OUT_OK} = V_{OUT} \times 0.90 \approx 351\,V \quad (25)$$

Resistor R_E sets up the high side of the voltage divider and programs the hysteresis of the PWMCNTL signal. For this example, R_E was selected to provide 99 V of hysteresis, as shown in Equation 26. Three resistors in series were used to meet voltage requirements.

$$R_E = \frac{Hysteresis}{12\,\mu A} = \frac{99\,V}{12\,\mu A} = 8.25\,M\Omega \approx 3 \times 2.74\,M\Omega \quad (26)$$

Resistor R_F is used to program the PWMCNTL active threshold, as shown in Equation 27.

$$R_F = \frac{2.5\,V}{\frac{V_{OUT_OK} - 2.5\,V}{R_E} - 12\,\mu A} = \frac{2.5\,V}{\frac{351\,V - 2.5\,V}{8.22\,M\Omega} - 12\,\mu A} = 82.25\,k\Omega \quad (27)$$

Select a standard resistor value for R_F.

$$R_F = 82.5\,k\Omega \quad (28)$$

This PWMCNTL output will remain active until a minimum output voltage (V_{OUT_MIN}) is reached, as shown in Equation 29.

$$V_{OUT_MIN} = \frac{2.5\,V\,(R_E + R_F)}{R_F} = \frac{2.5\,V\,(8.22\,M\Omega + 82.5\,k\Omega)}{82.5\,k\Omega} \approx 252\,V \quad (29)$$

According to these resistor values, the FailSafe OVP threshold will be set according to Equation 30

$$V_{OV_FAILSAFE} = \frac{4.87\,V\,(R_E + R_F)}{R_F} = \frac{4.87\,V\,(8.22\,M\Omega + 82.5\,k\Omega)}{82.5\,k\Omega} \approx 490\,V \quad (30)$$

9.2.2.4 Output Capacitor Selection

The output capacitor (C_{OUT}) is selected based on holdup requirements, as shown in Equation 31.

$$C_{OUT} \geq \frac{2\frac{P_{OUT}}{\eta}\frac{1}{f_{LINE}}}{V_{OUT}^2 - (V_{OUT_MIN})^2} = \frac{2\frac{300\,W}{0.92}\frac{1}{47\,Hz}}{390\,V^2 - (252\,V)^2} \approx 156\,\mu F \quad (31)$$

Two 100-µF capacitors were used in parallel for the output capacitor.

$$C_{OUT} = 200\,\mu F \quad (32)$$

For this size capacitor, the low-frequency peak-to-peak output voltage ripple (V_{RIPPLE}) is approximately 14 V, as shown in Equation 33:

$$V_{RIPPLE} = \frac{2 \times P_{OUT}}{\eta} \frac{1}{V_{OUT} \times 4\pi \times f_{LINE} \times C_{OUT}} = \frac{2 \times 300\,W}{0.92 \times 390\,V \times 4\pi \times 47\,Hz \times 200\,\mu F} \approx 14\,Vppk \quad (33)$$

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In addition to holdup requirements, a capacitor must be selected so that it can withstand the low-frequency RMS current (I_{COUT_100Hz}) and the high-frequency RMS current (I_{COUT_HF}); see Equation 34 to Equation 36. High-voltage electrolytic capacitors generally have both a low- and a high-frequency RMS current ratings on the product data sheets.

$$I_{COUT_100Hz} = \frac{P_{OUT}}{V_{OUT} \times \eta \times \sqrt{2}} = \frac{300\,W}{390\,V \times 0.92 \times \sqrt{2}} = 0.591\ Arms \tag{34}$$

$$I_{COUT_HF} = \sqrt{\left(\frac{P_{OUT} 2\sqrt{2}}{2 \times \eta \times V_{IN_MIN}} \sqrt{\frac{4\sqrt{2} V_{IN_MIN}}{9\pi V_{OUT}}} \right)^2 - \left(I_{COUT_100Hz}\right)^2} \tag{35}$$

$$I_{COUT_HF} = \sqrt{\left(\frac{300\,W \times 2\sqrt{2}}{2 \times 0.92 \times 85\,V} \sqrt{\frac{4\sqrt{2} \times 85\,V}{9\pi \times 390\,V}} \right)^2 - (0.591A)^2} \approx 0.966\ Arms \tag{36}$$

9.2.2.5 Selecting (R_S) For Peak Current Limiting

The UCC28063A peak limit comparator senses the total input current and is used to protect the MOSFETs during inrush and over-load conditions. For reliability, the peak current limit (I_{PEAK}) threshold in this design is set for 120% of the nominal maximum current that will be observed during power up, as shown in Equation 37.

$$I_{PEAK} = \frac{2P_{OUT}\sqrt{2}(1.2)}{\eta \times V_{IN_MIN}} = \frac{2 \times 300\,W\sqrt{2} \times 1.2}{0.92 \times 85\,V} \approx 13\,A \tag{37}$$

A standard 15-mΩ metal-film current-sense resistor will be used for current sensing, as shown in Equation 38. The estimated power loss of the current-sense resistor (P_{RS}) is less than 0.25 W during normal operation, as shown in Equation 39.

$$R_S = \frac{200\,mV}{I_{PEAK}} = \frac{200\,mV}{13\,A} \approx 15\,m\Omega \tag{38}$$

$$P_{RS} = \left(\frac{P_{OUT}}{V_{IN_MIN} \times \eta} \right)^2 R_S = \left(\frac{300\,W}{85\,V \times 0.92} \right)^2 \times 15\,m\Omega \approx 0.22\ W \tag{39}$$

The most critical parameter in selecting a current-sense resistor is the surge rating. The resistor needs to withstand a short-circuit current larger than the current required to open the fuse (F1). I^2t (ampere-squared-seconds) is a measure of thermal energy resulting from current flow required to melt the fuse, where I^2t is equal to RMS current squared times the duration of the current flow in seconds. A 4-A fuse with an I^2t of 14 A^2s was chosen to protect the design from a short-circuit condition. To ensure the current-sense resistor has high-enough surge protection, a 15-mΩ, 500-mW, metal-strip resistor was chosen for the design. The resistor has a 2.5-W surge rating for 5 seconds. This result translates into 833 A^2s and has a high-enough I^2t rating to survive a short-circuit before the fuse opens, as described in Equation 40.

$$I^2t = \frac{2.5\,W}{0.015\,\Omega} \times 5s = 833\,A^2s \tag{40}$$

9.2.2.6 Power Semiconductor Selection (Q1, Q2, D1, D2)

The selection of Q1, Q2, D1, and D2 are based on the power requirements of the design. Application Note SLUU138, *UCC38050 100-W Critical Conduction Power Factor Corrected (PFC) Pre-regulator*, explains how to select power semiconductor components for transition-mode PFC pre-regulators.

The MOSFET (Q1, Q2) pulsed-drain maximum current is shown in Equation 41:

$$I_{DM} \geq I_{PEAK} = 13\,A \tag{41}$$

The MOSFET (Q1, Q2) RMS current calculation is shown in Equation 42:

$$I_{DS} = \frac{I_{PEAK}}{2}\sqrt{\frac{1}{6} - \frac{4\sqrt{2}\,V_{IN_MIN}}{9\pi \times V_{OUT}}} = \frac{13\,A}{2}\sqrt{\frac{1}{6} - \frac{4\sqrt{2} \times 85\,V}{9\pi \times 390\,V}} \approx 2.3\,A \quad (42)$$

To meet the power requirements of the design, IRFB11N50A 500-V MOSFETs were chosen for Q1 and Q2.

The boost diode (D1, D2) RMS current is shown in Equation 43:

$$I_D = \frac{I_{PEAK}}{2}\sqrt{\frac{4\sqrt{2} \times V_{IN_MIN}}{9\pi \times V_{OUT}}} = \frac{13\,A}{2}\sqrt{\frac{4\sqrt{2} \times 85\,V}{9\pi \times 390\,V}} \approx 1.4\,A \quad (43)$$

To meet the power requirements of the design, MURS360T3, 600-V diodes were chosen for D1 and D2.

9.2.2.7 Brownout Protection

Resistor R_A and R_B are selected to activate brownout protection at ~75% of the specified minimum-operating input voltage. Resistor R_A programs the brownout hysteresis comparator, which is selected to provide 17 V (~12 V_{RMS}) of hysteresis. Calculations for R_A and R_B are shown in Equation 44 through Equation 47.

$$R_A = \frac{\text{Hysteresis}}{2\,\mu A} = \frac{17\,V}{2\,\mu A} = 8.5\,M\Omega \quad (44)$$

To meet voltage requirements, three 2.87-MΩ resistors were used in series for R_A.

$$R_A = 3 \times 2.87\,M\Omega = 8.61\,M\Omega \quad (45)$$

$$R_B = \frac{1.4\,V \times R_A}{V_{IN_MIN} \times 0.75\sqrt{2} - 1.4\,V} = \frac{1.4\,V \times 8.61\,M\Omega}{85\,V \times 0.75\sqrt{2} - 1.4\,V} = 135.8\,k\Omega \quad (46)$$

Select a standard value for R_B.

$$R_B = 133\,k\Omega \quad (47)$$

In this design example, brownout becomes active (shuts down PFC) when the input drops below 66 V_{RMS} for longer than 440 ms and deactivates (restarts with a full soft start) when the input reaches 78 V_{RMS}.

9.2.2.8 Converter Timing

The maximum on-time T_{ON} depends on f_{MIN} as determined by Equation 48. To ensure proper operation, the timing must be set based on the highest boost inductance ($L1_{MAX}$) and output power (P_{OUT}). In this design example, the boost inductor could be as high as 390 µH. Calculate the timing resistor R_T as shown in Equation 49.

$$f_{MIN} = \frac{\eta \times \left(V_{IN_MIN}\right)^2 \left(1 - \frac{V_{IN_MIN} \times \sqrt{2}}{V_{OUT}}\right)}{P_{OUT} \times L1_{MAX}} = \frac{0.92 \times (85\,V)^2 \left(1 - \frac{85\,V \times \sqrt{2}}{390\,V}\right)}{300\,W \times 390\,\mu H} = 39.2\,kHz \quad (48)$$

$$R_T = \frac{133\,k\Omega\left(1 - \frac{V_{IN_MIN} \times \sqrt{2}}{Vout}\right)}{4.85\,V \times \frac{4\,\mu s}{V} \times f_{MIN}} = \frac{133\,k\Omega\left(1 - \frac{85\,V \times \sqrt{2}}{390\,V}\right)}{4.85\,V \times \frac{4\,\mu s}{V} \times 39.2\,kHz} \approx 121\,k\Omega \quad (49)$$

This result sets the maximum frequency clamp (f_{MAX}), as shown in Equation 50, which improves efficiency at light load.

$$f_{MAX} = \frac{133\,k\Omega}{2\,\mu s \times R_T} = \frac{133\,k\Omega}{2\,\mu s \times 121\,k\Omega} \approx 550\,kHz \quad (50)$$

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9.2.2.9 Programming V_{OUT}

Resistor R_C is selected to minimize loading on the power line when the PFC is disabled. Construct resistor R_C from two or more resistors in series to meet high-voltage requirements. Resistor R_D is then calculated based on R_C, the reference voltage, V_{REF}, and the required output voltage, V_{OUT}. Based on the values shown in Equation 51 to Equation 54, the primary output over-voltage protection threshold should be as shown in Equation 55:

$$R_C = 2.74\,M\Omega + 2.74\,M\Omega + 3.01\,M\Omega = 8.49\,M\Omega \quad (51)$$

$$V_{REF} = 6\ V \quad (52)$$

$$R_D = \frac{V_{REF} \times R_C}{V_{OUT} - V_{REF}} = \frac{6\,V \times 8.49\,M\Omega}{390\,V - 6\,V} = 132.7\,k\Omega \quad (53)$$

Select a standard value for R_D.

$$R_D = 133\,k\Omega \quad (54)$$

$$V_{OVP} = 6.48\,V\,\frac{R_C + R_D}{R_D} = 6.48\,V\,\frac{8.49\,M\Omega + 133\,k\Omega}{133\,k\Omega} = 420.1V \quad (55)$$

9.2.2.10 Voltage Loop Compensation

Resistor R_Z is sized to attenuate low-frequency ripple to less than 2% of the voltage amplifier output range. This value ensures good power factor and low harmonic distortion on the input current.

The transconductance amplifier small-signal gain is shown in Equation 56:

$$g_m = 50\,\mu S \quad (56)$$

The voltage-divider feedback gain is shown in Equation 57:

$$H = \frac{V_{REF}}{V_{OUT}} = \frac{6\,V}{390\,V} \approx 0.015 \quad (57)$$

The value of R_Z is calculated as shown in Equation 58:

$$R_Z = \frac{100\,mV}{V_{RIPPLE} \times H \times g_m} = \frac{100\,mV}{14\,V \times 0.015 \times 50\,\mu S} = 9.52\ k\Omega \quad (58)$$

C_Z is then set to add 45° phase margin at 1/5th of the line frequency, as shown in Equation 59:

$$C_Z = \frac{1}{2\pi \times \frac{f_{LINE}}{5} \times R_Z} = \frac{1}{2\pi \times \frac{47\,Hz}{5} \times 9.52\,k\Omega} = 1.78\,\mu F \quad (59)$$

C_P is sized to attenuate high-frequency switching noise, as shown in Equation 60:

$$C_p = \frac{1}{2\pi \times \frac{f_{MIN}}{2} \times R_Z} = \frac{1}{2\pi \times \frac{45\,kHz}{2} \times 9.52\,k\Omega} = 770\,pF \quad (60)$$

Standard values should be chosen for R_Z, C_Z and C_P, as shown in Equation 61 to Equation 63.

$$R_Z = 9.53\,k\Omega \quad (61)$$

$$C_Z = 2.2\,\mu F \quad (62)$$

$$C_P = 820\,pF \quad (63)$$

9.2.3 Application Curves

Refer to *UCC28063EVM-723 300-W Interleaved PFC Pre-Regulator EVM User's Guide*, SLUU512, for more implementation details and application curves.

9.2.3.1 Input Ripple Current Cancellation with Natural Interleaving

Figure 35 through Figure 37 show the input current (M1= IL1 + IL2), Inductor Ripple Currents (IL1, IL2) versus rectified line voltage. From these graphs, it can be observed that natural interleaving reduces the overall magnitude of input (and output) ripple current caused by the individual inductor current ripples.

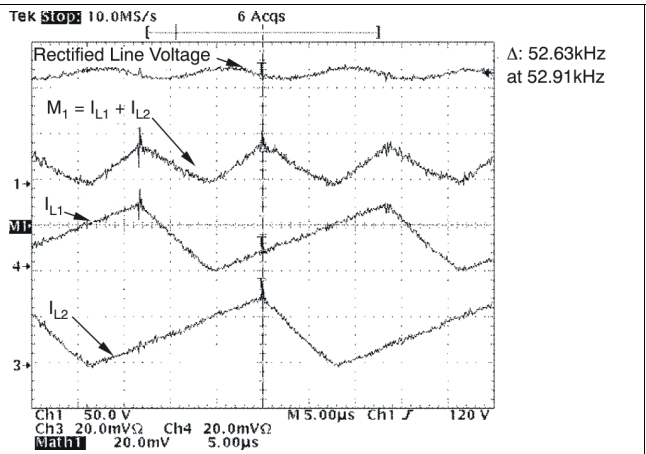


Figure 35. Inductor and Input Ripple Current at 85 V_{RMS} at Peak of Line Voltage

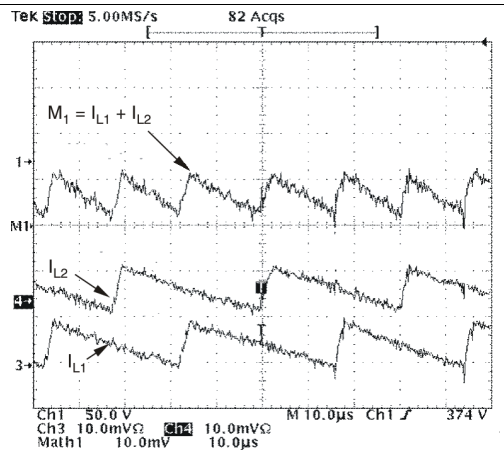


Figure 36. Inductor and Input Ripple Current at 265 V_{RMS} Input at Peak Line Voltage

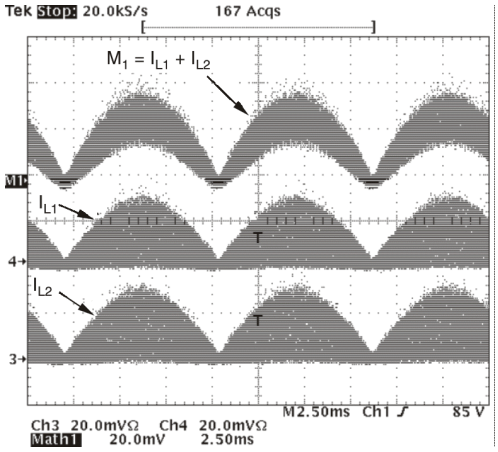


Figure 37. Inductor and Input Ripple Current at V_{IN} = 85 V_{RMS}, P_{OUT} = 300 W

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9.2.3.2 Brownout Protection

The UCC28063A has a brownout protection that shuts down both gate drives (GDA and GDB) when the VINAC pin detects that the RMS input voltage is too low. This EVM was designed to go into a brownout state when the line drops below 64 VRMS. Once the UCC28063A control device has determined that the input is in a brownout condition, a 400-ms timer starts to allow the line to recover before shutting down the gate drivers. After 400 ms of brownout, both gate drivers turn off, as shown in Figure 38.

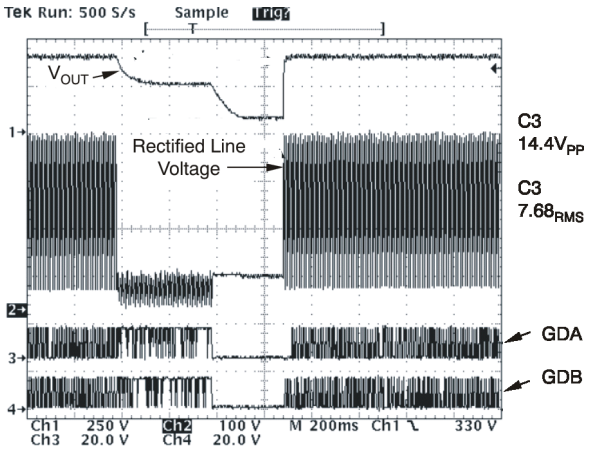


Figure 38. UCC28063A Response to a Line Brownout Event at 265 V_{RMS}

10 Power Supply Recommendations

The IC receives all of its power through the VCC pin. This voltage should be as well regulated as possible through all of the operating conditions of the PFC stage. Consider creating the steady state bias for this stage from a downstream DC:DC stage which will in general be able to provide a bias winding with very well regulated voltage. This strategy will enhance the overall efficiency of the bias generation. A lower efficiency alternative will be to consider a series connected Fixed Positive Voltage Regulator such as the UA78L15A.

For all normal and abnormal operating conditions it is critically important that VCC remains within its Recommended Operating Range for both Voltage and Input Current. VCC overvoltage may cause excessive power dissipation in the internal voltage clamp and undervoltage may cause inadequate drive levels for power MOSFETs, UVLO events (causing interrupted PFC operation) or inadequate headroom for the various on-chip linear regulators and references.

Note also that the high RMS and peak currents required for the MOSFET gate drives are provided through the IC 13.5-V linear regulator, which does not have provision for the addition of external decoupling capacitance. For higher Powers, very high Q_G power MOSFETs or high switching frequencies, consider using external driver transistors, local to the power MOSFETs. These will reduce the IC operating temperature and ensure that the VCC maximum input current rating is not exceeded.

Use decoupling capacitances between VREF and AGND and between VCC and PGND which are as local as possible to the IC. These should have some ceramic capacitance which will provide very low ESR. PGND and AGND should ideally be star connected at the control IC so that there is negligible DC or high frequency AC voltage difference between PGND and AGND. Use values for decoupling capacitors similar to or a little larger than those used in the EVM.

Pay close attention to start-up and shutdown VCC bias bootstrap arrangements so that these provide adequate regulated bias power as early as possible during power application and as late as possible during power removal. Ensure that these start-up bias bootstrap circuits do not cause unnecessary steady-state power drain.

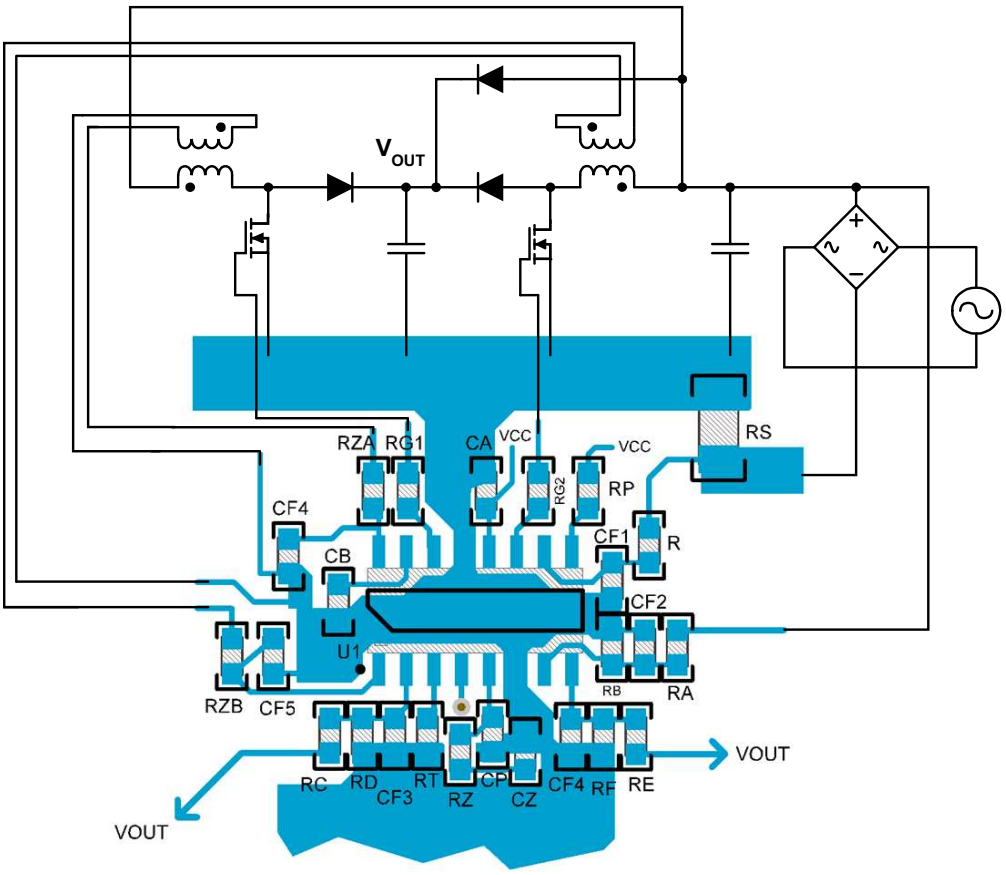
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11 Layout

11.1 Layout Guidelines

Interleaved transition-mode PFC system architecture dramatically reduces input and output ripple current, allowing the circuit to use smaller and less expensive filters. To maximize the benefits of interleaving, the input and output filter capacitors should be located after the two phase currents are combined together. Similar to other power management devices, when laying out the printed circuit board (PCB) it is important to use star grounding techniques and keep filter capacitors as close to device ground as possible. To minimize the interference caused by capacitive coupling from the boost inductor, the device should be located at least 1 in (25.4 mm) away from the boost inductor. It is also recommended that the device not be placed underneath magnetic elements. Because of the precise timing requirement, timing-setting resistor R_T should be placed as close as possible to the TSET pin and returned to the analog ground pin with the shortest possible path. See Figure 39 for a recommended component placement and layout.

11.2 Layout Example



PHB and VREF pins are connected by a jumper on the back of the board.

Figure 39. Recommended PCB Layout

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Related Parts

Table 3 lists several TI parts that have characteristics similar to the UCC28063A.

Table 3. TI Related Parts

DEVICE	DESCRIPTION
UCC28050/51	Transition-mode PFC controller for low to medium power applications
UCC28019	8-pin continuous-conduction-mode (ccm) pfc controller (with slew-rate correction current)
UCC28019A	8-pin continuous-conduction-mode (ccm) pfc controller (with 2-level voltage-error gain)
UCC28060	Two-phase interleaved transition-mode pfc controller (with input voltage range gain change)
UCC28061	Two-phase interleaved transition-mode pfc controller (with no input voltage gain change)
UCC28070	Two-phase interleaved ccm (average current mode) pfc controller
UCC28063	Two-phase interleaved transition-mode pfc controller (with improved audible noise)

12.1.2 Device Nomenclature

12.1.2.1 Detailed Pin Description

Analog Ground: Connect analog signal bypass capacitors, compensation components, and analog signal returns to this pin. Connect the analog and power grounds at a single point to isolate high-current noise signals of the power components from interference with the low-current analog circuits.

Error Amplifier Output: The error amplifier is a transconductance amplifier, so this output is a high-impedance current source. Connect voltage-regulation loop-compensation components from this pin to AGND. The on-time seen at the gate-drive outputs is proportional to the voltage at this pin minus an offset of approximately 125 mV. During normal operation, the error amplifier maintains a transconductance of 55 μS for small-signal disturbances on VSENSE, and shifts to ~290 μS when VSENSE deviates more than ±5% from VSENSEreg. During an AC-line Dropout condition, the error amplifier output is disabled and an internal 4-μA source discharges COMP for the duration of the Dropout condition. During a VSENSE-based OV event, an internal 2-kΩ resistor is applied from COMP to GND until the OV condition clears. During soft-start triggering events (UVLO, Disable, Brownout, HVSEN over-voltage, or Thermal Shutdown), the error-amp output is disabled and COMP is pulled low by an internal 2-kΩ resistor. The soft-start condition begins only after the triggering event clears and COMP has been discharged below 20 mV, ensuring that the circuit restarts with a low COMP voltage and a short on-time. (Do not connect COMP to a low-impedance source that would interfere with COMP falling below 20 mV.) During Soft-Start, the error amplifier high transconductance is enabled and COMP current is -125 μA as long as VSENSE < VREF/2. Once VSENSE exceeds VREF/2, the high gain is disabled and only the small-signal gain capability is available with a maximum COMP current of approximately –16 μA. Normal operation resumes once VSENSE > 0.983VREF (~5.9 V).

Current Sense Input: Connect the current-sense resistor and the negative terminal of the diode bridge to this pin. Connect the return of the current sense resistor to the AGND pin with a separate trace. As input current increases, the voltage on CS will go more negative. This cycle-by-cycle over-current protection limits input current by turning off both gate driver outputs (GDx) when CS is more negative than the CS rising threshold (approximately -200 mV in two-phase operation and approximately -167 mV in single-phase and phase-fail condition). The gate drive outputs will remain low until CS falls to the CS falling threshold (approx. -15 mV). Current sense is blanked for approximately 100 ns following the rising and falling edge of either GDx output. This filters noise that may occur from gate-drive current or when inductor current switches from a power FET to a boost diode. In most cases, no additional current sense filtering is required. If external filtering is deemed necessary, or to prevent excessive negative voltage on the CS pin during AC-inrush conditions, a series resistor is recommended to connect the current sensing resistor to the CS pin. Due to the CS bias current, this external resistor should be less than 100 Ω to maintain accuracy.

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Channel A and Channel B Gate Drive Output: Connect these pins to the gate of the power FET for each phase through the shortest connection practicable. If it is necessary to use a trace longer than 0.5 inch (12.6 mm) for this connection, some ringing may occur due to trace series inductance. This ringing can be damped by adding a low-value resistor in series with GDA and GDB.

High Voltage Output Sense: The UCC28063A incorporates FailSafe OVP so that any single failure does not allow the output to boost above safe levels. Output over-voltage is monitored by both VSENSE and HVSEN but their actions are different if either pin exceeds their respective over-voltage thresholds. Using two pins to monitor for over-voltage provides redundant protection and fault tolerance. When HVSEN exceeds its over-voltage threshold, it triggers a full soft-start of the controller. HVSEN can also be used to enable a downstream power converter when the voltage on HVSEN is within the operating region. When HVSEN is greater than 2.5 V, the PWMCNTL output may be driven Low (provided no other fault exists). When HVSEN falls below 2.5 V, the PWMCNTL output becomes high-impedance. Select the HVSEN divider ratio for the desired over-voltage and power-good thresholds. Select the HVSEN divider impedance for the desired power-good hysteresis based on the hysteresis current. During operation, HVSEN must never fall below 0.8 V. Dropping HVSEN below 0.8 V puts the UCC28063A into a special test mode, used only for factory testing. A bypass capacitor from HVSEN to AGND is recommended to filter noise and avoid false over-voltage shutdown.

Phase-B Enable/Disable: When the voltage applied to this pin is below the Phase-B enable threshold, Phase B of the boost converter and the Phase Fail detector are disabled. The commanded on-time for Phase A is immediately doubled when Phase B is disabled, which helps keep COMP voltage constant during the phase-management transient. The PHB pin allows the user to add external phase-management control circuitry, if desired. To disable phase-management, connect the PHB pin to the VREF pin.

PWM-Control Output: This open-drain output goes low when HVSEN is within the HVSEN-good region (HVSEN > 2.5 V), there is no FailSafe OV, and there is no Phase-Fail condition when operating in two-phase mode (see PHB pin). Otherwise, PWMCNTL is high-impedance.

Timing Set: PWM on-time programming input. Connect a resistor from TSET to AGND to set the on-time versus COMP voltage and the minimum switching period at the gate-drive outputs.

Bias Supply Input: Connect this pin to a controlled bias supply of between 14 V and 21 V. Also connect a 0.1-μF or larger ceramic bypass capacitor from this pin to PGND with the shortest possible board trace. This bias supply powers all circuits within the device and must be capable of delivering the steady-state dc current plus the transient power-MOSFET gate-charging current. Input bias current is very low during undervoltage-lockout (UVLO) or stand-by conditions (VSENSE < 1.25 V).

Input AC Voltage Sense: For normal operation, connect this pin to a voltage divider across the rectified input power mains. When the voltage on VINAC remains below the brownout threshold for longer than the brownout filter time, the device enters a brownout mode, both output drivers are disabled and a full soft-start is triggered. Select the input voltage divider ratio for the desired brownout threshold. Select the divider impedance for the desired brownout hysteresis based on the hysteresis current. A dropout condition is triggered when VINAC remains below the dropout threshold for longer than the dropout filter time. The error amplifier is disabled and an internal 4-μA current source discharges COMP for the duration of the dropout condition. The dropout condition is immediately cleared and normal operation resumes when VINAC exceeds the dropout-clear threshold.

Voltage Reference Output: Connect a 0.1-μF or larger ceramic bypass capacitor from this pin to AGND. VREF turns off during UVLO and VSENSE-disable to save bias current and increase stand-by efficiency. This reference output can be used to bias other circuits requiring less than a few milliamperes of non-pulsing total supply current.

Output DC Voltage Sense: Connect this pin to a voltage divider across the output of the power converter. In a closed-loop system, the voltage at VSENSE is regulated to the error amplifier reference voltage. Select the output voltage divider ratio for the desired output voltage. Connect the ground side of this divider to analog ground (AGND) through a separate short trace for best output regulation accuracy and noise immunity. Controller operation may be enabled when VSENSE voltage exceeds the 1.25-V enable threshold. VSENSE can be pulled low by an open-drain logic output, or >6-V logic output in series with a low-leakage diode, to disable the outputs and reduce VCC current. Two levels of output overvoltage are detected at this input. If VSENSE exceeds the first-level overvoltage protection threshold V_{LOW_OV}, an internal 2-kΩ resistor is applied to COMP to quickly reduce gate-drive on-time. If VSENSE continues to rise past the second-level threshold V_{HIGH_OV}, GDA and GDB are immediately latched off. This latch is cleared when VSENSE falls below the OV-clear threshold. If VSENSE becomes disconnected, open-loop protection provides an internal current source to pull VSENSE low, which disables the controller and triggers a soft-start condition.

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Zero Current Detection Inputs: These inputs are used to detect a negative-going edge when the boost inductor current in each respective phase goes to zero. The inputs are clamped between 0 V and 3 V. Connect each pin through a current limiting resistor to the zero-crossing detection (ZCD) winding of the corresponding boost inductor. The resistor value should be chosen to limit the clamping currents to less than ±3 mA. The inductor winding polarity must be arranged so that this ZCD voltage falls when the inductor current decays to zero. When the inductor current falls to zero, the ZCD input must drop below the falling threshold (approximately 1 V) to cause the gate drive output to rise. Subsequently, when the power-MOSFET turns off, the ZCD input must rise above the rising threshold (approximately 1.7 V) to arm the logic for another falling ZCD edge.

12.2 Documentation Support

12.2.1 Related Documentation

These references, design tools, and links to additional references, including design software, may be found at www.power.ti.com.

- Evaluation Module, *UCC28063EVM 300W Interleaved PFC Pre-regulator* (SLUU512)
- Application Note, *UCC38050 100-W Critical Conduction Power Factor Corrected (PFC) Pre-regulator* (SLUU138)

12.3 Trademarks

DLP, Natural Interleaving are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28063AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28063A	Samples
UCC28063ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28063A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

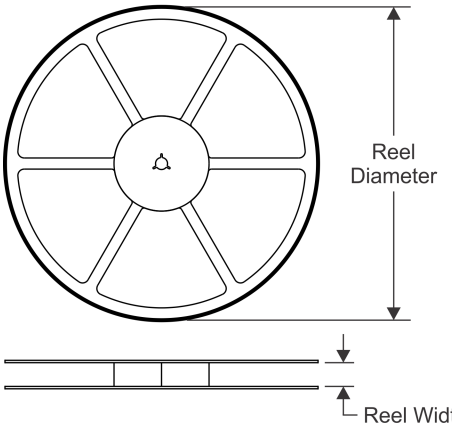
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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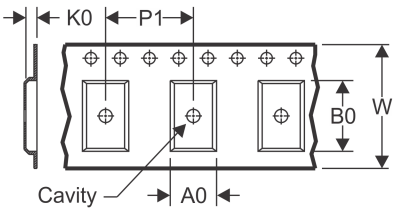
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

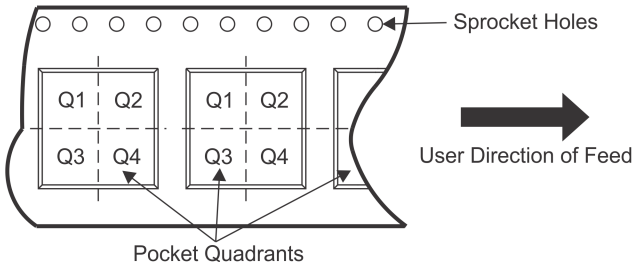


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

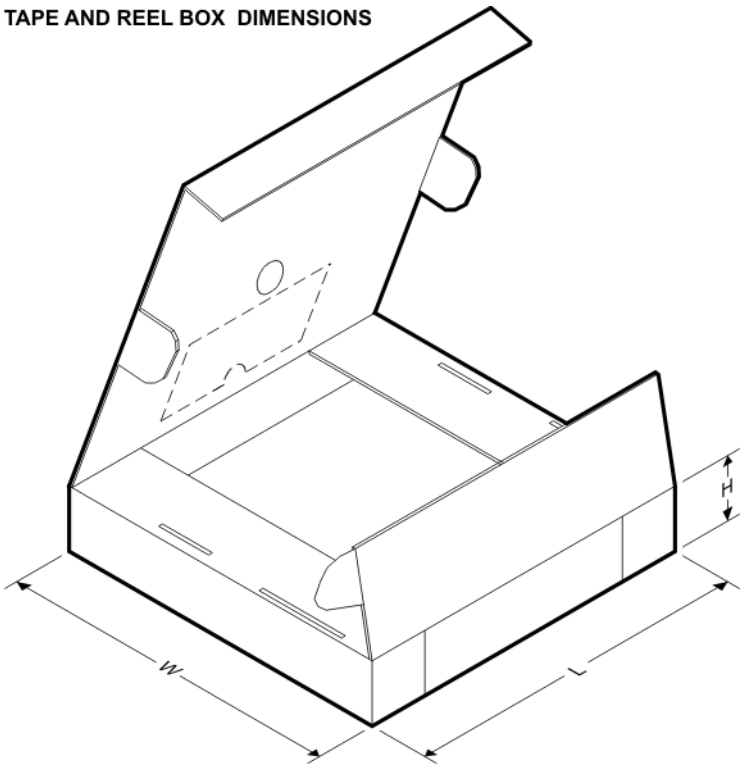
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28063ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

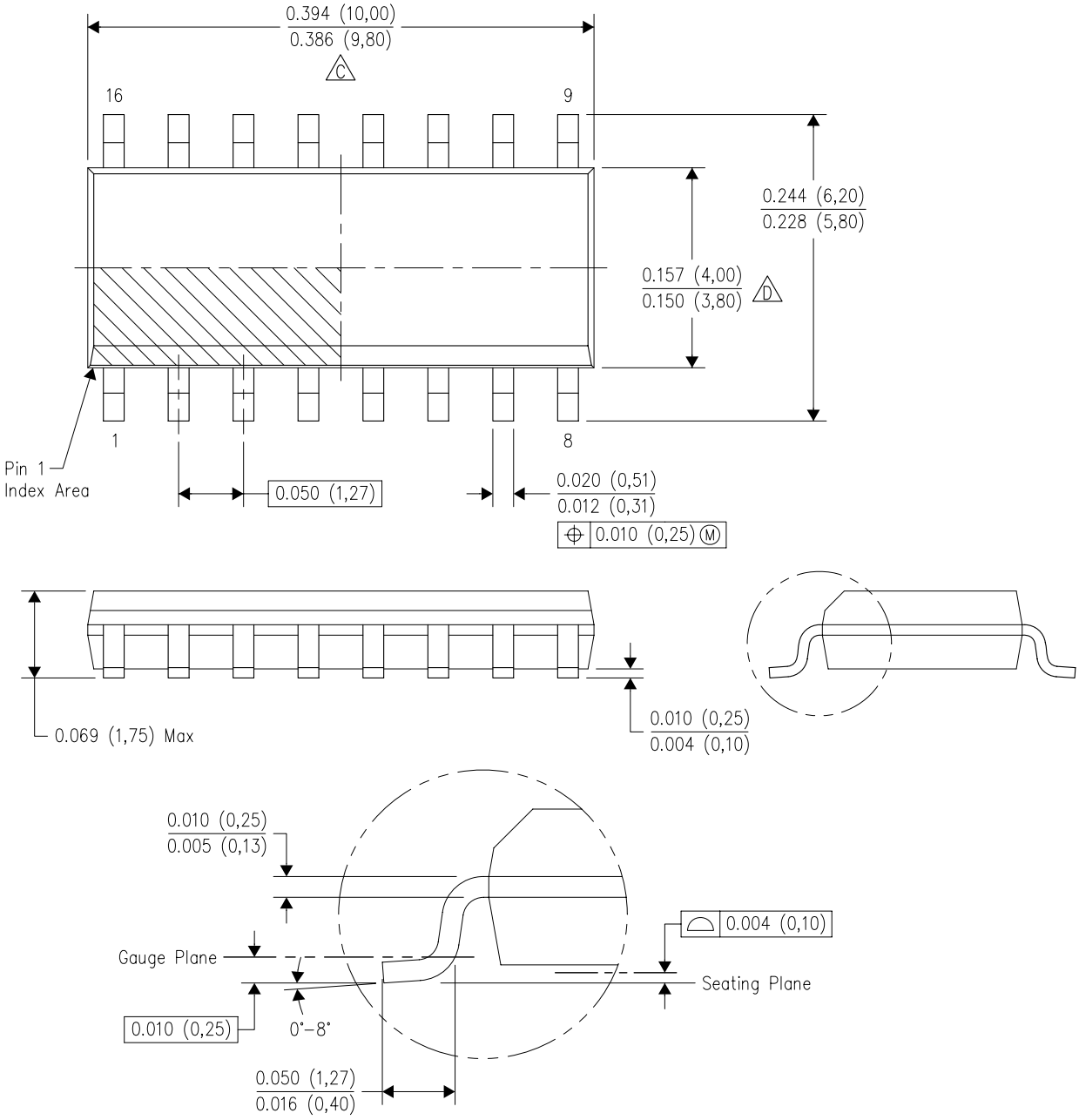
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

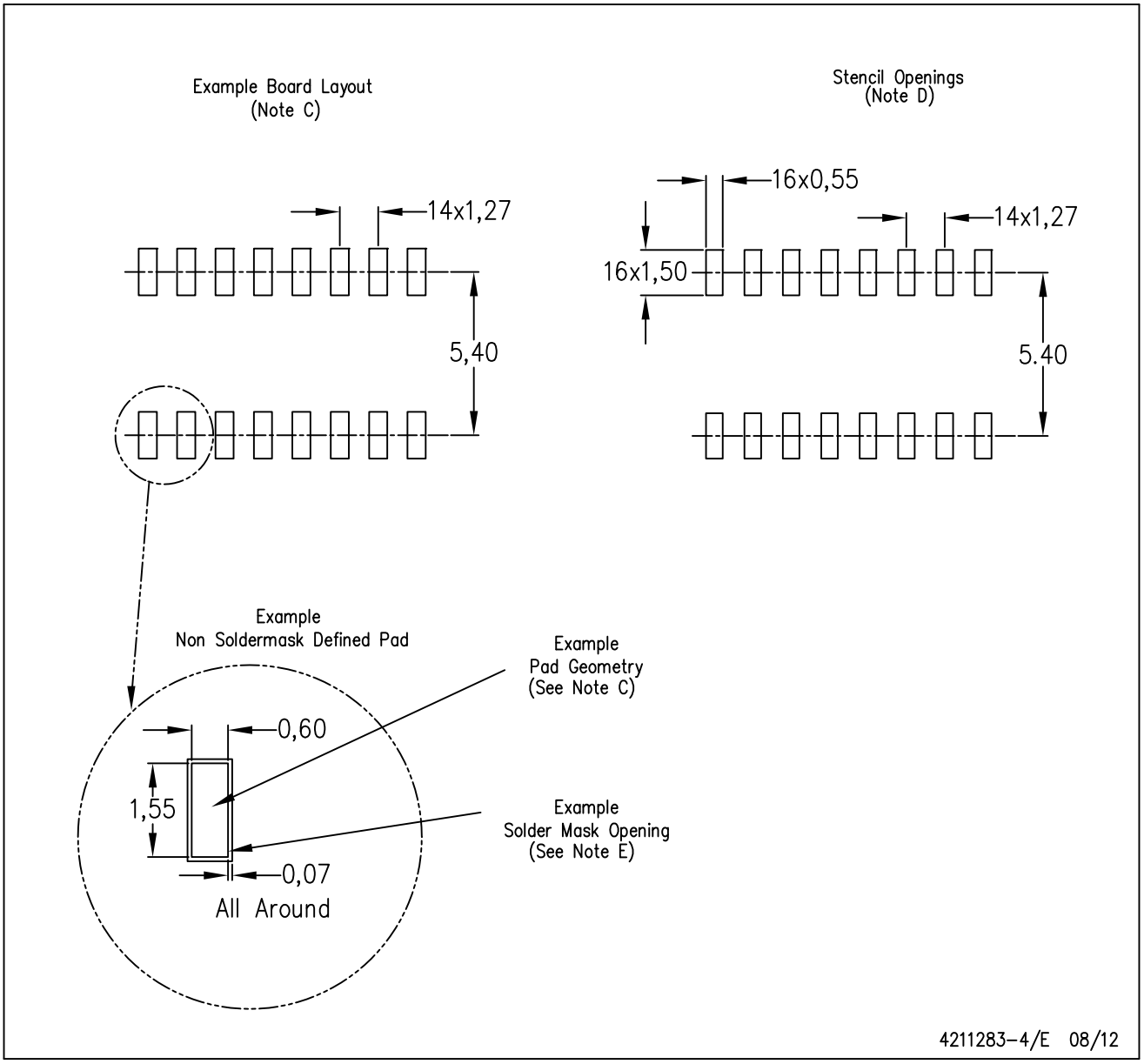
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28063ADR	SOIC	D	16	2500	333.2	345.9	28.6

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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