USB Charging Port Power Switch and Controller

Check for Samples: TPS2540, TPS2540A, TPS2541, TPS2541A

FEATURES

- **Meets Battery Charging Specification BC1.2 for DCP and CDP**
- **Meets Chinese Telecommunications Industry Standard YD/T 1591-2009**
- **Supports Sleep-Mode Charging for Most Available Apple® Devices and/or BC1.2 Compliant Devices**
- **Compatible With USB 2.0 and 3.0 Power Switch Requirements**
- **2.6-GHz Bandwidth USB 2.0 Data Switch**
- **73-mΩ (typ.) High-Side MOSFET**
- **Adjustable Current Limit up to 2.8 A (typical)**
- **OUT Discharge Through CTLx=000 (TPS2540/40A) or DSC (TPS2541/41A) Input**
- **Longer Detach Detection Time (TPS2540A/41A) Supporting Additional Legacy Devices**
- **Available in 16-Pin QFN Package**

APPLICATIONS

- **USB Ports/Hubs**
- **Notebook PCs**
- **Universal Wall Charging Adapter**

DESCRIPTION

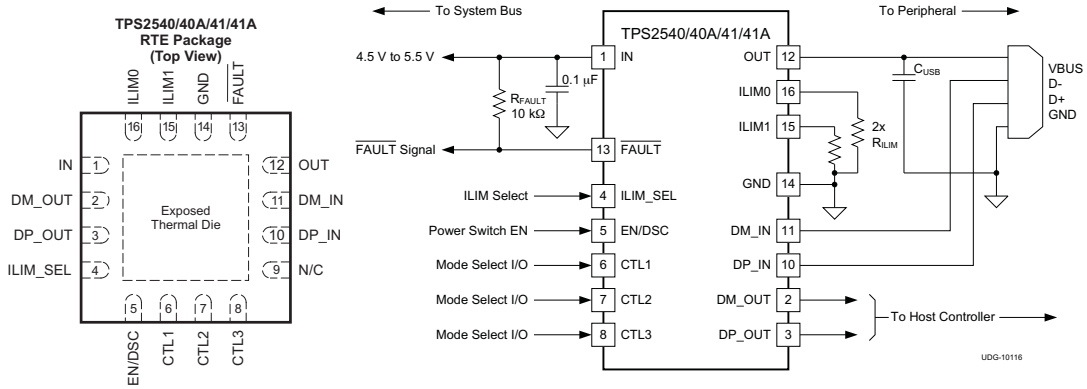
The TPS2540/40A and TPS2541/41A are a combination of current-limited USB port power switch with a USB 2.0 high-speed data line (D+/D-) switch and a USB charging port identification circuit. Applications include notebook PCs and other intelligent USB host devices. The wide bandwidth (2.6 GHz) data-line switch also features low capacitance and low on resistance, allowing signals to pass with minimum edge and phase distortion. The TPS2540/40A/41/41A monitors D+ and D-, providing the correct hand-shaking protocol with compliant client devices.

The TPS2540/40A/41/41A supports the following charging logic schemes:

- USB 2.0 BC1.2
- Chinese Telecom Standard YD/T 1591-2009
- Divider Mode, compliant with Apple devices such as iPod® and iPhone®

CTL1-CTL3 logic inputs are used to select one of the various charge modes provided by the TPS2540/40A and TPS2541/41A. These charge modes allow the host device to actively select between Dedicated Charging Port (DCP) (wall-adapter emulation), Charging Downstream Port (CDP) (active USB 2.0 data communications with 1.5-A support), or Standard Downstream Port (SDP) USB 2.0 Mode (active USB 2.0 data communications with 500-mA support). The TPS2540/40A/41/41A also integrates an *auto-detect* feature that supports both DCP schemes for Battery Charging Specification (BC1.2) and the Divider Mode without the need for outside user interaction.

TPS2540/40A/41/41A RTE Package and Typical Application Diagram



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONT.)

The TPS2540A/41A auto detect mode also has a longer detach detection time, so that it can support certain unique non-compliant devices. The TPS2540/40A/41/41A power-distribution switch is intended for applications where heavy capacitive loads and short-circuits are likely to be encountered, incorporating a 73-mΩ, N-channel MOSFET in a single package. Constant-current mode is used when the output load exceeds the current-limit threshold. ILIM_SEL logic input selects one of two current-limit thresholds, each one being individually adjustable via an external resistor. Additional USB switch features include a de-glitched output fault reporting ($\overline{FAULT}$), and a logic-level enable EN (TPS2540/40A) or OUT discharge control DSC (TPS2541/41A). With the TPS2540/40A, the mode “000” is used to force an output discharge.

PRODUCT INFORMATION(1)

T_A	FUNCTION	T_{DCPLOW} (2)	PACKAGE	MARKING
-40°C to 85°C	Enable	≤0.9 s	QFN16	2540
	Output Discharge			2541
	Enable	≤9 s		2540A
	Output Discharge			2541A

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Low DP_IN period in DCP mode, see Figure 31.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range, voltages are referenced to GND (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
Supply voltage range	IN	-0.3	7	V
Input voltage range	EN (TPS2540/40A), DSC (TPS2541/41A), ILIM0, ILIM1, ILIM_SEL, CTL1, CTL2, CTL3	-0.3	7	
Voltage range	OUT, $\overline{FAULT}$ (2)	-0.3	7	
Voltage range	IN to OUT	-7	7	
Voltage range	DP_IN, DM_IN, DP_OUT, DM_OUT	-0.3	(IN + 0.3) or 5.7	
Input clamp current	DP_IN, DM_IN, DP_OUT, DM_OUT		±20	mA
Continuous current in SDP or CDP mode	DP_IN to DP_OUT or DM_IN to DM_OUT		±100	
Continuous current in BC1.2 DCP mode	DP_IN to DM_IN		±35	
Continuous output current	I_{OUT}	Internally limited		
Continuous output sink current	$\overline{FAULT}$		25	mA
Continuous output source current	ILIM0, ILIM1		1	
Continuous total power dissipation		Internally limited		
ESD rating, Human Body Model (HBM)	IN, ILIM_SEL, EN, DSC, CTL1, CTL2, CTL3, N/C, OUT, $\overline{FAULT}$, GND, ILIM1, ILIM0		2	kV
	DP_IN, DM_IN, DP_OUT, DM_OUT		8	
ESD rating, Charged Device Model (CDM)			500	V
Operating Junction temperature	T_J	Internally limited		
Storage temperature range	T_{stg}	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Do not apply external voltage sources directly.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage, IN	4.5		5.5	V
	Input voltage, logic-level inputs, (CTL1, CTL2, CTL3, EN (TPS2540/40A), DSC (TPS2541/41A), ILIM_SEL)	0		5.5	
	Input voltage, data line inputs, (DP_IN, DM_IN, DP_OUT, DM_OUT)			5.5	
	Continuous current, data line inputs, (SDP or CDP mode, DP_IN to DP_OUT or DM_IN to DM_OUT)			±30	mA
	Continuous current, data line inputs, (BC1.2 DCP mode, DP_IN to DM_IN)			±10	
I_{OUT}	Continuous output current, OUT	0		2.5	A
R_{ILIMx}	Current-limit set resistors, (ILIM0 to GND, ILIM1 to GND)	16.9		750	kΩ
T_J	Operating virtual junction temperature	-40		125	°C

THERMAL INFORMATION

THERMAL METRIC(1)		TPS2540 TPS2540A TPS2541 TPS2541A	UNITS
		RTE	
		16 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(2)	53.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	51.4	
θ_{JB}	Junction-to-board thermal resistance(4)	17.2	
ψ_{JT}	Junction-to-top characterization parameter(5)	3.7	
ψ_{JB}	Junction-to-board characterization parameter(6)	20.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	3.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

Conditions are -40 ≤ T_J ≤ 125°C unless otherwise noted. V_{EN} (if TPS2540 or TPS2540A) = V_{DSC} (if TPS2541 or TPS2541A) = V_{IN} = 5 V, $R_{\overline{FAULT}}$ = 10 kΩ, R_{ILIM0} = 210 kΩ, R_{ILIM1} = 20 kΩ, I_{LIM_SEL} = 0 V, CTL1 = CTL2 = GND, CTL3 = V_{IN} (TPS2540/40A) or CTL3 = GND (TPS2541/41A), unless otherwise noted. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power Switch							
$R_{DS(on)}$	Static drain-source on-state resistance	I_{OUT} = 2 A, V_{ILIM_SEL} = Logic HI			73	120	mΩ
		I_{OUT} = 100 mA, V_{ILIM_SEL} = Logic LO			73	120	
		-40°C ≤ T_A = T_J ≤ 85°C, I_{OUT} = 2 A, V_{ILIM_SEL} = Logic HI			73	105	
		T_A = T_J = 25°C, I_{OUT} = 2 A, V_{ILIM_SEL} = Logic HI			73	84	
t_r	Rise time, output	C_L = 1 µF, RL = 100 Ω, (see Figure 27, Figure 28)			1	1.5	ms
t_f	Fall time, output	C_L = 1 µF, RL = 100 Ω, (see Figure 27, Figure 28)		0.2		0.5	
R_{DIS}	OUT discharge resistance			400	500	630	Ω
I_{REV}	Reverse leakage current	V_{OUT} = 5.5 V, V_{IN} = V_{EN} = 0 V , T_J = 25°C			0	1	µA
Enable Input EN (TPS2540/40A), Output Discharge Input DSC (TPS2541/41A)							
V_{EN}	Enable pin turn on/off threshold, falling			0.9	1.1	1.65	V
V_{EN_HYS}	EN Hysteresis				200		mV
I_{EN}	Input current	V_{EN} = 0 V or 5.5 V		-0.5		0.5	µA
V_{DSC}	DSC pin turn on/off threshold, falling			0.9	1.1	1.65	V
V_{DSC_HYS}	DSC Hysteresis				200		mV
I_{DSC}	Input current	V_{DSC} = 0 V or 5.5 V		-0.5		0.5	µA
t_{ON}	Turn-on time	C_L = 1 µF, R_L = 100 Ω(see Figure 27, Figure 29)			3.4	5	ms
t_{OFF}	Turn-off time	C_L = 1 µF, R_L = 100 Ω(see Figure 27, Figure 29)			1.7	3	
Current Limit							
V_{ILIM_SEL}	I_{LIM_SEL} turn on/off threshold, falling			0.9	1.1	1.65	V
V_{ILIM_HYS}	I_{LIM_SEL} Hysteresis				200		mV
	ILIM_SEL input current	V_{ILIM_SEL} = 0 V or 5.5 V		-0.5		0.5	µA
I_{SHORT}	Maximum DC output current from IN to OUT	V_{ILIM_SEL} = Logic LO	R_{ILIM0} = 210 kΩ	185	230	265	mA
			R_{ILIM0} = 100 kΩ	420	480	530	
		V_{ILIM_SEL} = Logic HI	R_{ILIM1} = 20 kΩ	2150	2430	2650	
			R_{ILIM1} = 16.9 kΩ	2550	2840	3100	
		V_{ILIM_SEL} = Logic LO	R_{ILIM0} = 698 kΩ	25	55	85	
			-40 ≤ T_J ≤ 85°C				
t_{IOS}	Response time to short-circuit	V_{IN} = 5.0 V (see Figure 30)			1.5		µs
Supply Current							
I_{CCL}	Supply current, switch disabled	V_{EN} = V_{DSC} = 0 V, OUT grounded, -40 ≤ T_J ≤ 85°C			0.1	2	µA
I_{CCH}	Supply current, operating	V_{EN} = V_{DSC} = V_{IN},	V_{ILIM_SEL} = Logic HI		150	185	
			V_{ILIM_SEL} = Logic LOW		130	170	

ELECTRICAL CHARACTERISTICS (continued)

Conditions are -40 ≤ T_J ≤ 125°C unless otherwise noted. V_{EN} (if TPS2540 or TPS2540A) = V_{DSC} (if TPS2541 or TPS2541A) = V_{IN} = 5 V, $R_{\overline{FAULT}}$ = 10 kΩ, R_{ILIM0} = 210 kΩ, R_{ILIM1} = 20 kΩ, I_{LIM_SEL} = 0 V, CTL1 = CTL2 = GND, CTL3 = V_{IN} (TPS2540/40A) or CTL3 = GND (TPS2541/41A), unless otherwise noted. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Undervoltage Lockout						
V_{UVLO}	Low-level input voltage, IN	V_{IN} rising	3.9	4.1	4.3	V
	Hysteresis, IN			100		mV
$\overline{FAULT}$						
	Output low voltage, $\overline{FAULT}$	$I_{\overline{FAULT}}$ = 1 mA			100	mV
	Off-state leakage	$V_{\overline{FAULT}}$ = 5.5 V			1	µA
	$\overline{FAULT}$ deglitch	$\overline{FAULT}$ assertion or de-assertion due to over-current condition	5	8.5	12	ms
CTLx Inputs						
V_{CTL}	CTLx pins turn on/off threshold, falling		0.9	1.1	1.65	V
V_{CTL_HYS}	CTLx hysteresis			200		mV
	Input current	V_{CTL} = 0 V or 5.5 V	-0.5		0.5	µA
Thermal Shutdown						
	Thermal shutdown threshold		155			°C
	Thermal shutdown threshold in current-limit		135			
	Hysteresis			10		
High-Bandwidth Analog Switch						
R_{HS_ON}	On resistance DP/DM high-speed switch	V_{DP/DM_OUT} = 0 V, I_{DP/DM_IN} = + 30 mA		2	4	Ω
		V_{DP/DM_OUT} = 2.4 V, I_{DP/DM_IN} = - 15 mA		3	6	
ΔR_{HS_ON}	On resistance match between channels DP/DM switch	V_{DP/DM_OUT} = 0 V, I_{DP/DM_IN} = + 30 mA		0.05	0.15	
		V_{DP/DM_OUT} = 2.4 V, I_{DP/DM_IN} = - 15 mA		0.05	0.15	
C_{IO_OFF}	DP/DM off state capacitance (1)	f = 1 MHz, switch off		3	3.6	pF
C_{IO_ON}	DP/DM on state capacitance (2)	f = 1 MHz, switch on		5.4	6.2	
O_{IRR}	Off state isolation	R_L = 50 Ω, f = 250 MHz, -40 ≤ T_J ≤ 125°C		33		dB
X_{TALK}	On-state cross channel isolation	R_L = 50 Ω, f = 250 MHz, -40 ≤ T_J ≤ 125°C		52		
I_{OFF}	Off state leakage	V_{DM_IN} = V_{DP_IN} = 3.6 V, V_{DM_OUT} = V_{DP_OUT} = 0 V		0.1	1.5	µA
BW	Bandwidth (-3 dB)	R_L = 50 Ω		2.6		GHz
t_{pd}	Propagation delay			0.25		ns
t_{SK}	Skew between opposite transitions of the same port (t_{PHL} – t_{PLH})			0.1	0.2	

(1) The resistance in series with this parasitic capacitance to GND is typically 250 Ω.
(2) The resistance in series with this parasitic capacitance to GND is typically 150 Ω.

ELECTRICAL CHARACTERISTICS (continued)

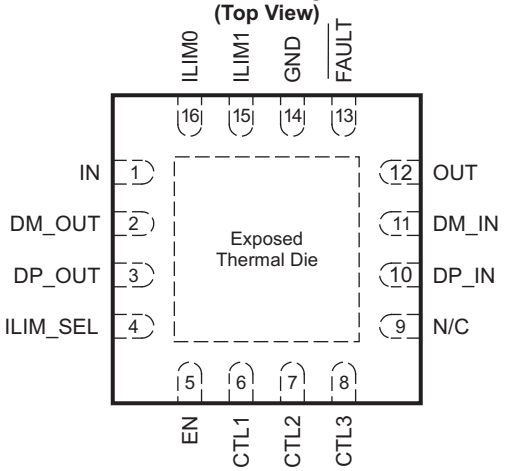
Conditions are -40 ≤ T_J ≤ 125°C unless otherwise noted. V_{EN} (if TPS2540 or TPS2540A) = V_{DSC} (if TPS2541 or TPS2541A) = V_{IN} = 5 V, $R_{\overline{FAULT}}$ = 10 kΩ, R_{ILIM0} = 210 kΩ, R_{ILIM1} = 20 kΩ, I_{LIM_SEL} = 0 V, CTL1 = CTL2 = GND, CTL3 = V_{IN} (TPS2540/40A) or CTL3 = GND (TPS2541/41A), unless otherwise noted. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to GND unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DCP Shorted Mode Charger Interface						
R_{DPM_short}	DP_IN/DM_IN shorting resistance	CTLx configured for DCP BC1.2		125	200	Ω
R_{DCHG_PW}	Discharge resistance DM_IN and DP_IN to GND	CTLx configured for DCP BC1.2	2	3.2	6	MΩ
Divider Mode Charger Interface						
V_{DP_AM}	DP_IN output voltage	CTLx configured for divider mode	1.9	2	2.1	V
V_{DM_AM}	DM_IN output voltage		2.57	2.7	2.84	
Z_{OUT_DP}	DP_IN output impedance		8	10	12.5	kΩ
Z_{OUT_DM}	DM_IN output impedance		8	10	12.5	
CDP Interface						
V_{DM_SRC}	Voltage source on DM_IN for CDP detect	V_{DP_IN} = 0.6 V, CTLx configured for CDP	0.5	0.6	0.7	V
V_{DAT_REF}	DP_IN rising voltage threshold to activate V_{DM_SRC}	I_{DM_IN} = - 250 µA, CTLx configured for CDP	0.25		0.4	
	V_{DAT_REF} hysteresis			50		mV
V_{LGC_SRC}	DP_IN rising voltage threshold to deactivate V_{DM_SRC}		0.8		1	V
	V_{LGC_SRC} hysteresis			100		mV
I_{DP_SINK}	DP_IN sink current	0.4 V ≤V_{DP_IN} ≤ 0.8 V, CTLx configured for CDP operation	50		150	µA
Timings						
t_{VDMSRC_EN}	DM_IN voltage source enable time, CDP mode	From V_{DP_IN} = 0 -> 0.6 V to V_{DM_IN} = V_{DM_SRC} , CTLx configured for CDP	1		10	ms
t_{VDMSRC_DIS}	DM_IN voltage source disable time, CDP mode	From V_{DP_IN} = 0.6 V -> 0 V to V_{DM_IN} = 0 V, CTLx configured for CDP			10	
t_{VBUS_REAPP}	Time for OUT to be reapplied after V_{OUT} falls below 0.7 V during discharge	Any transition to and from CDP, or to and from SDP. Also during Auto-detect to shorted mode.	200		500	
Timing Requirements						
$t_{SLVD\_CON\_P}$	Session valid (IN high) to VDP_SRC in DCP mode	TPS2540/TPS2541			1	s
t_{DCPLOW}	Low DP_IN period in DCP mode	When VBUS is high, (TPS2540, TPS2541)			0.9	
		When VBUS is high, (TPS2540A, TPS2541A)			9	

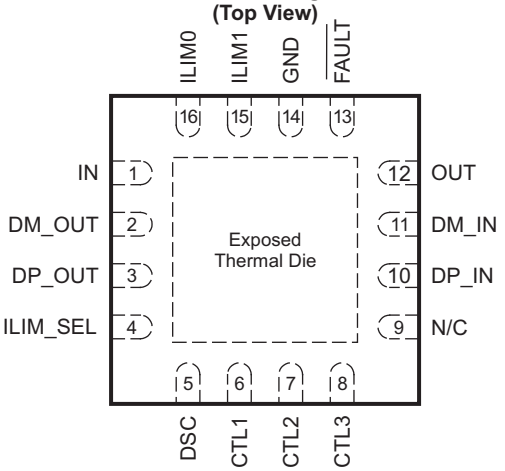
DEVICE INFORMATION

TPS2540, TPS2540A, TPS2541 and TPS2541A

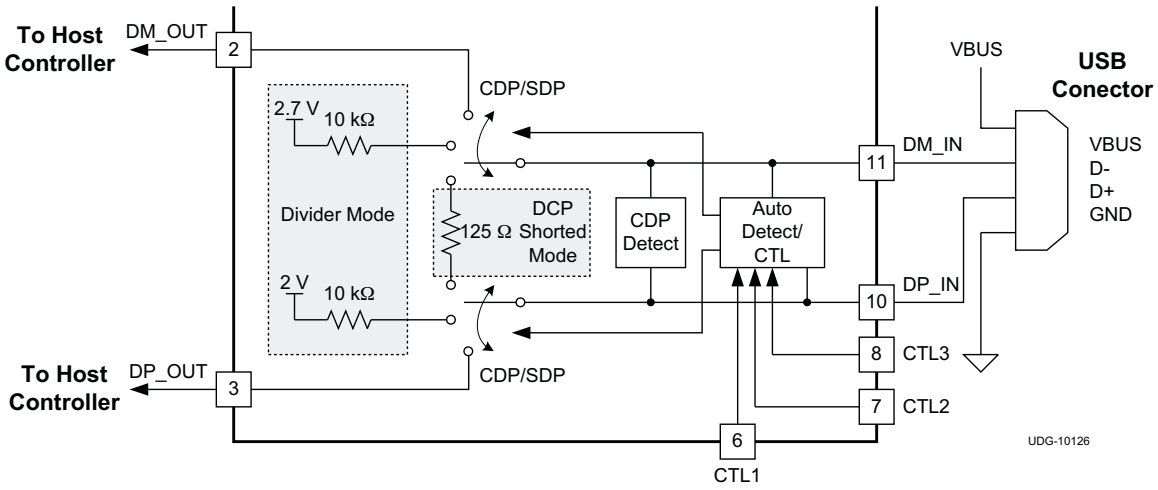
TPS2540/TPS2540A
RTE Package
(Top View)



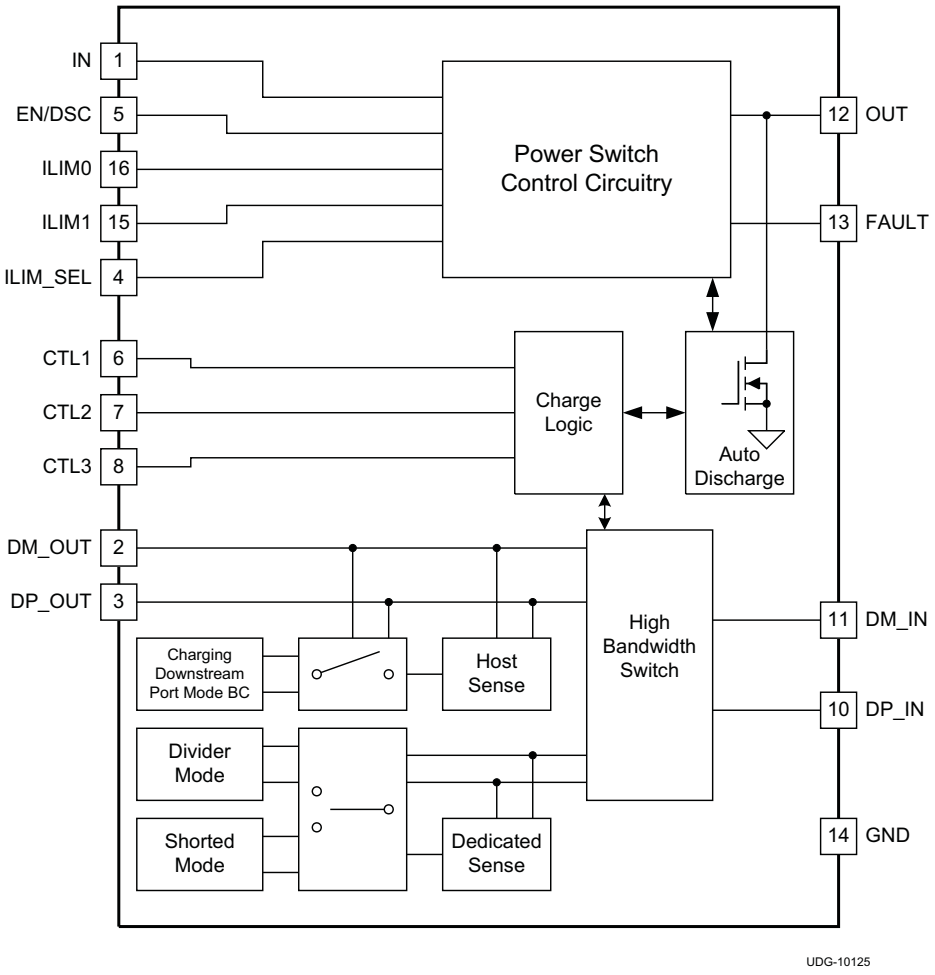
TPS2541/TPS2541A
RTE Package
(Top View)



Detection Block Diagram



TPS2540/40A/41/41A Top-Level Functional Block Diagram



PIN DESCRIPTIONS

Pin Descriptions

NAME	PIN	I/O	DESCRIPTION
Power Switch			
IN	1	PWR	Input voltage; connect a 0.1-µF or greater ceramic capacitor from IN to GND as close to the device as possible.
OUT	12	PWR	Power-switch output.
GND	14	PWR	Ground connection; should be connected externally to Power PAD.
POWERPAD	N/A		Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect to GND plane.
Current-Limit Threholds and Indication			
ILIM0	16	I	External resistor used to set current-limit threshold when ILIM_SEL is LO; recommended 16.9 kΩ ≤ R_{ILIM} ≤ 750 kΩ;
ILIM1	15	I	External resistor used to set current-limit threshold when ILIM_SEL is HI; recommended 16.9 kΩ ≤ R_{ILIM} ≤ 750 kΩ;
ILIM_SEL	4	I	Logic-level input signal used to dynamically change power switch current-limit threshold; logic LO selects ILIM0, logic HI selects ILIM1.
$\overline{\text{FAULT}}$	13	O	Active-low open-drain output, asserted during over-temperature or current limit conditions.
Input Logic Control Signals			
EN, DSC	5	I	Logic-level control input for turning the power switch and the signal switches on/off. **TPS2540/40A:** When EN is low, the device is disabled, the signal and power switches are OFF. **TPS2541/41A:** When DSC is low, the device is disabled, the signal and power switches are OFF and the output (OUT) capacitor is discharged.
CTL1	6	I	Logic-level control inputs for controlling the charging mode and the signal switches. The TPS2540/40A and TPS2541/41A use different control line truth tables. With the TPS2540/40A, the “000” configuration is used to force a discharge of the output (OUT) capacitor.
CTL2	7	I	
CTL3	8	I	
D+/D- Data Line Signals			
DM_IN	11	I/O	D- data line to connector, input/output used for hand-shaking with portable equipment.
DP_IN	10	I/O	D+ data line to connector, input/output used for hand-shaking with portable equipment.
DM_OUT	2	I/O	D- data line to USB host controller.
DP_OUT	3	I/O	D+ data line to USB host controller.
N/C	9		No connect pin. Can be grounded or left floating.

TYPICAL CHARACTERISTICS

IN UVLO RISING vs TEMPERATURE

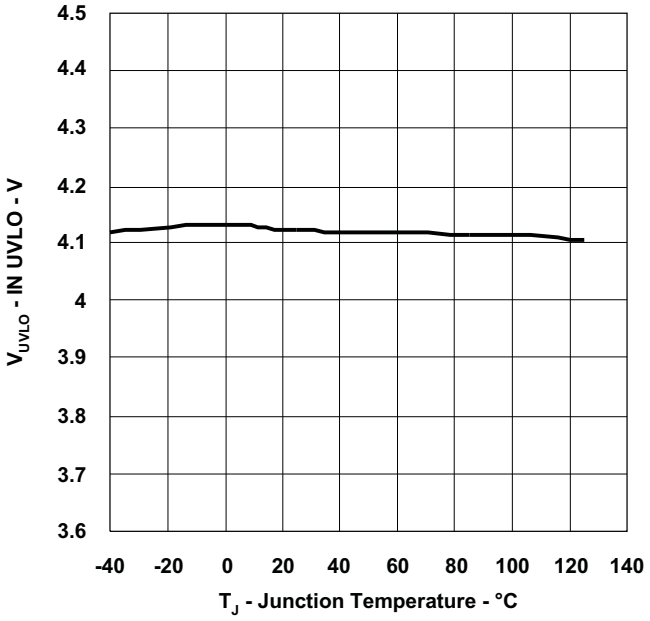


Figure 1.

SUPPLY CURRENT - DISABLED vs TEMPERATURE

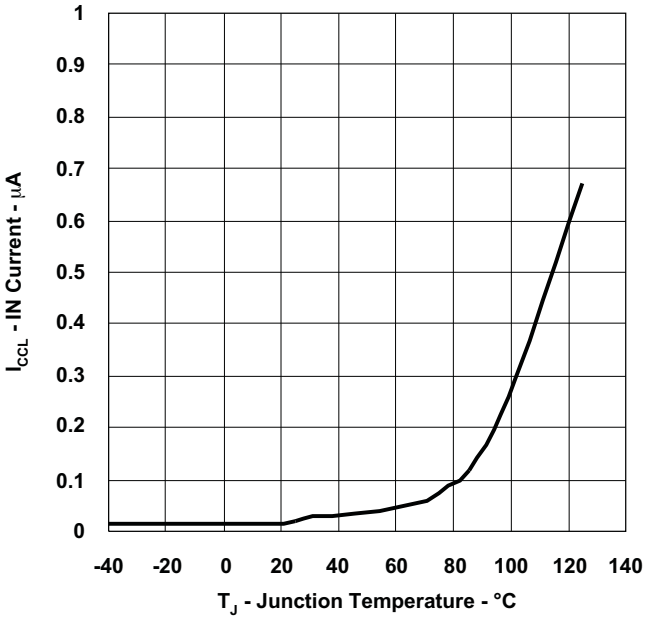


Figure 2.

SUPPLY CURRENT - SDP or DCP BC vs TEMPERATURE

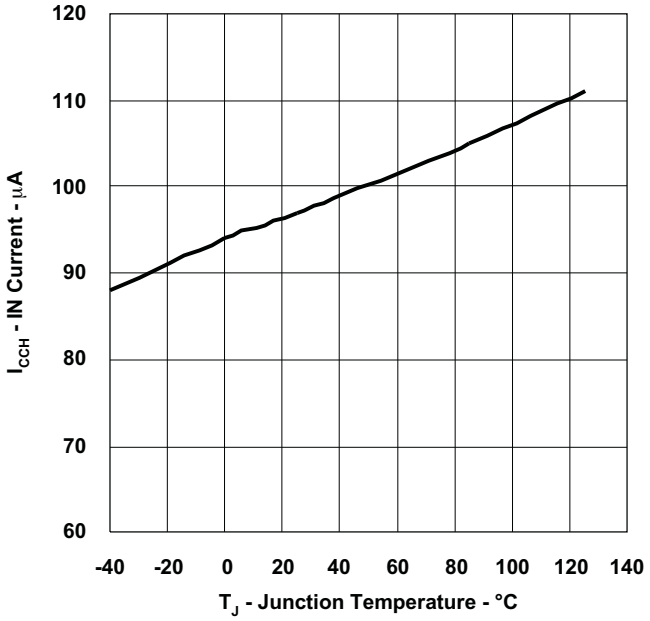


Figure 3.

SUPPLY CURRENT - AUTO-DETECT vs TEMPERATURE

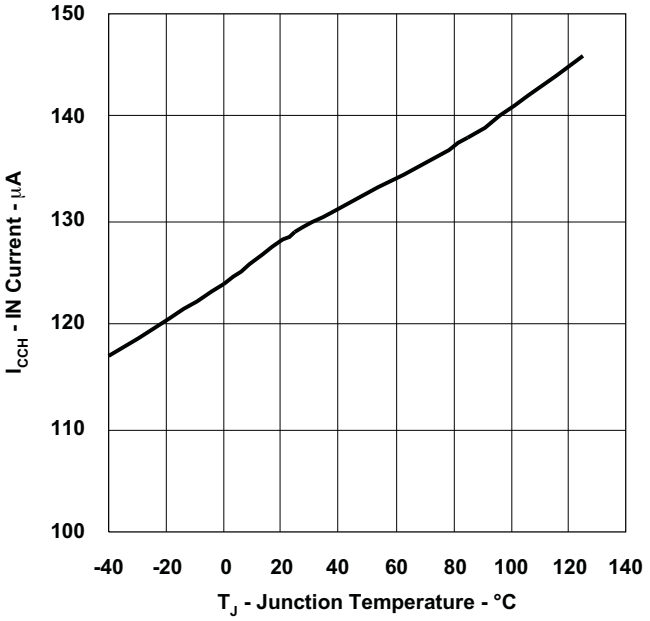


Figure 4.

TYPICAL CHARACTERISTICS (continued)

SUPPLY CURRENT - CDP or DIVIDER MODE vs TEMPERATURE

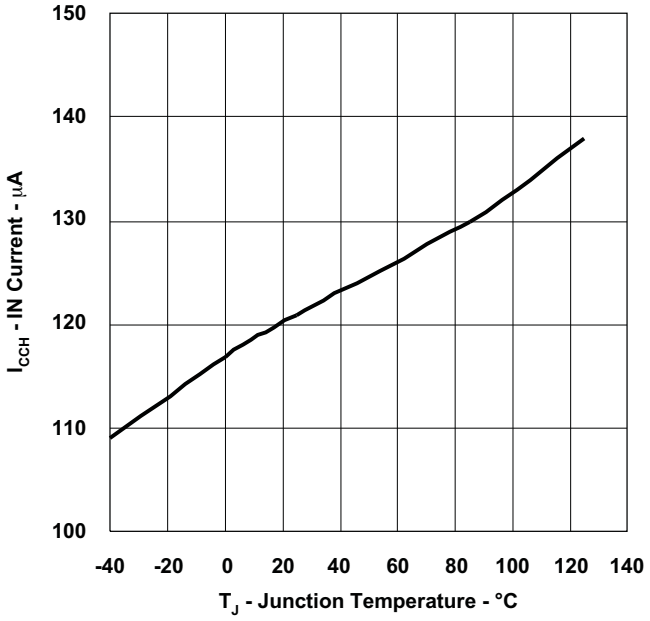


Figure 5.

CURRENT LIMIT vs CURRENT LIMIT RESISTANCE

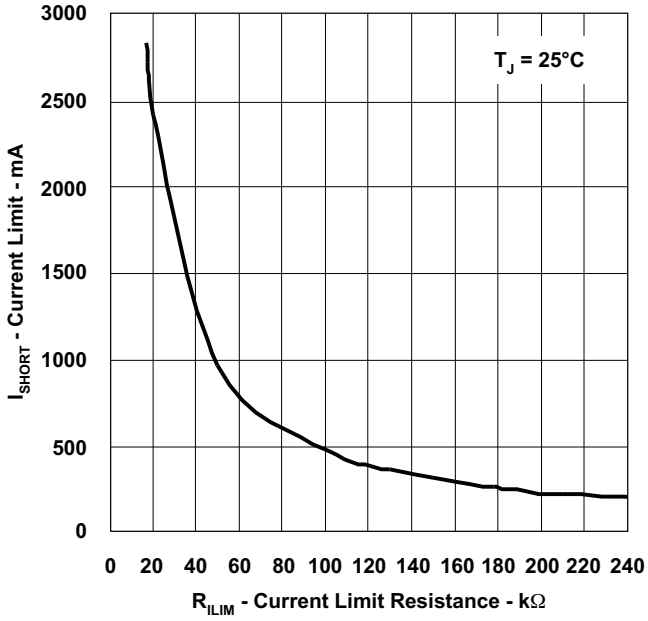


Figure 6.

CURRENT LIMIT vs TEMPERATURE

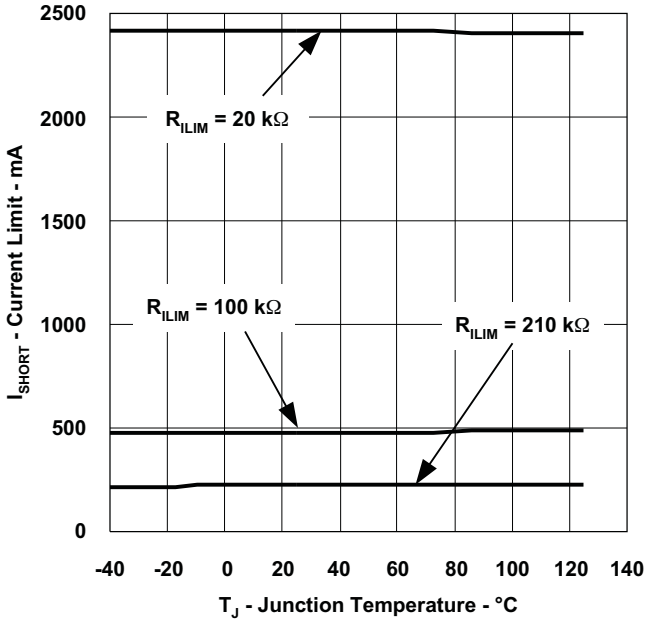


Figure 7.

POWER SWITCH ON-RESISTANCE vs TEMPERATURE

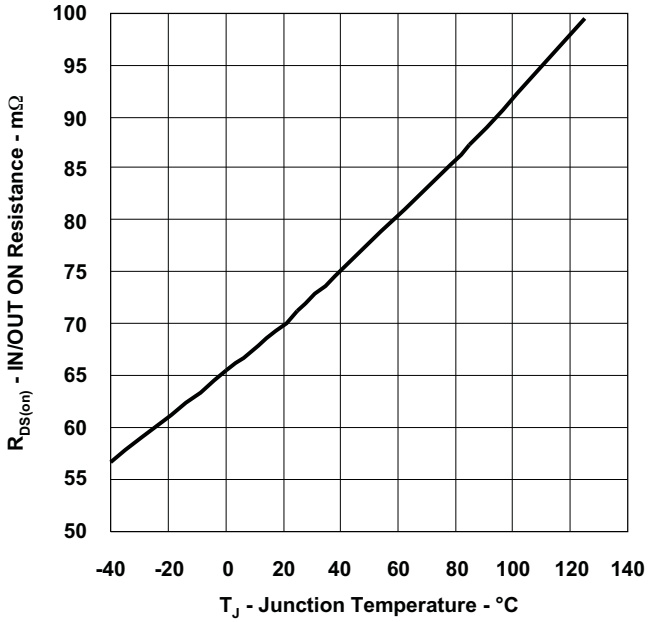


Figure 8.

TYPICAL CHARACTERISTICS (continued)

TURN-ON TIME, TURN-OFF TIME vs TEMPERATURE

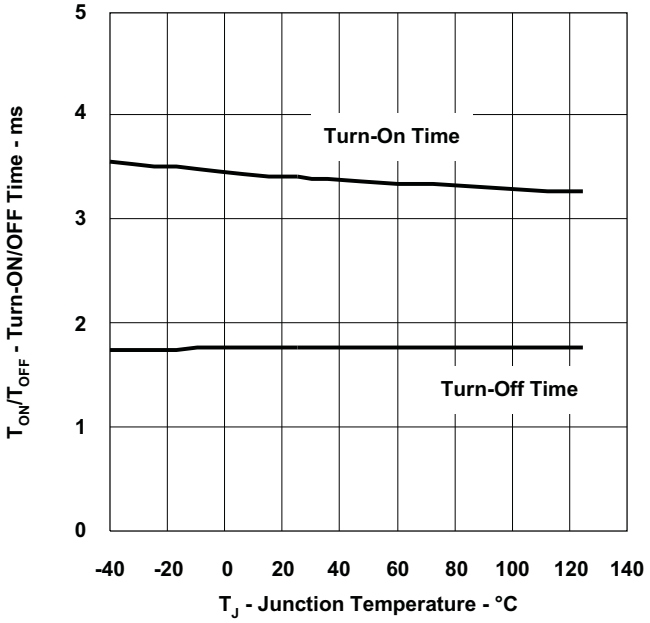


Figure 9.

DATA SWITCH ON-RESISTANCE vs TEMPERATURE

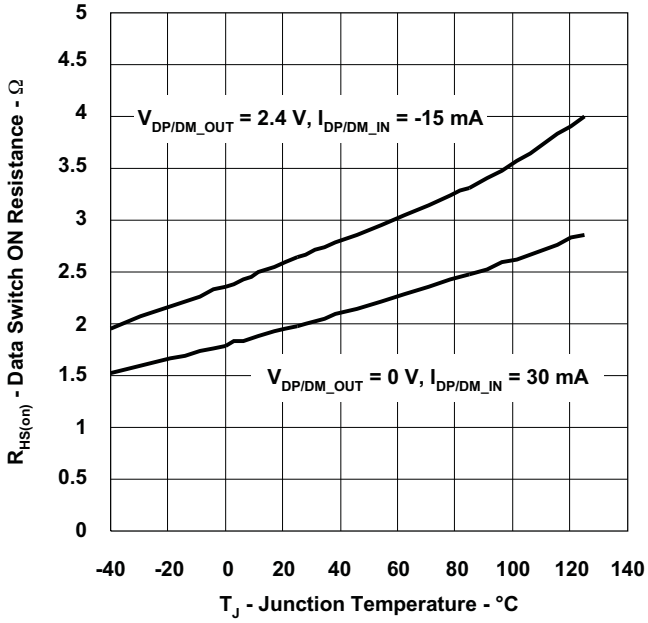


Figure 10.

FAULT OUTPUT VOLTAGE vs SINK CURRENT

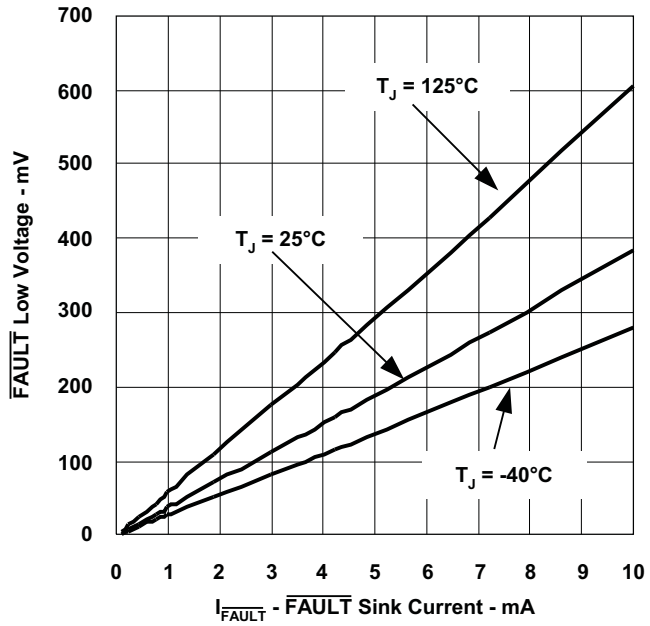


Figure 11.

EN THRESHOLD FALLING vs TEMPERATURE

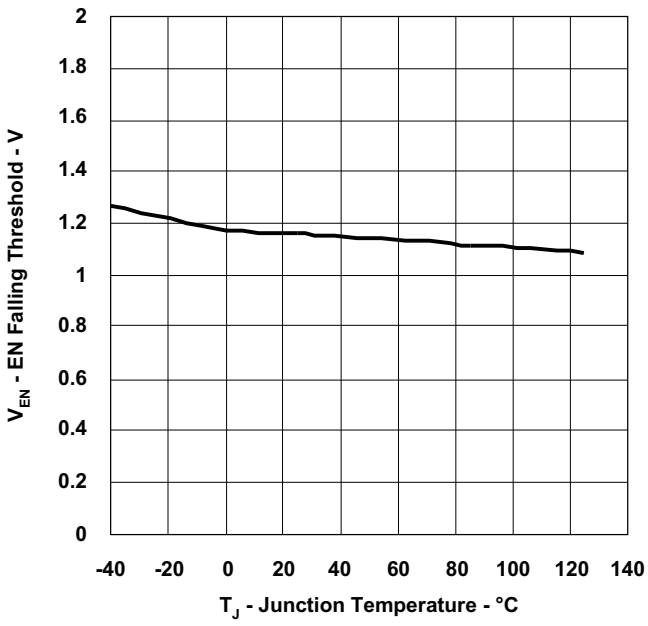


Figure 12.

TYPICAL CHARACTERISTICS (continued)

CTL1-3 THRESHOLD FALLING vs TEMPERATURE

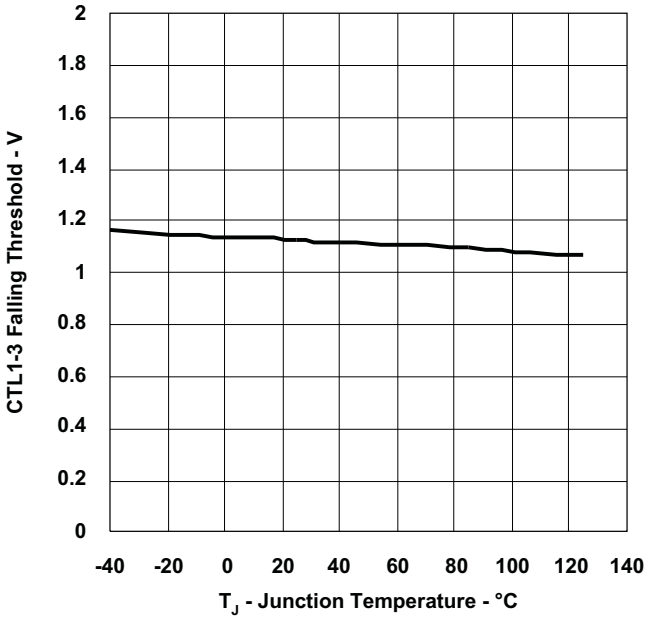


Figure 13.

DIVIDER MODE DP/DM VOLTAGE vs TEMPERATURE

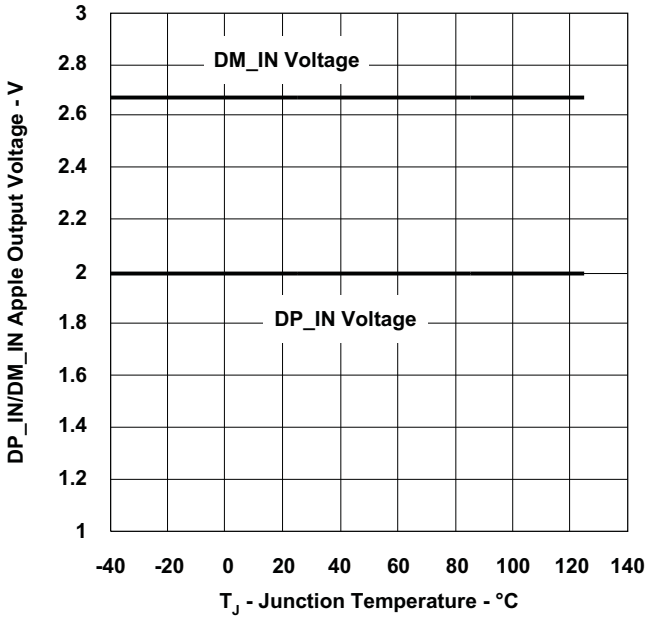


Figure 14.

DATA TRANSMISSION CHARACTERISTICS vs FREQUENCY

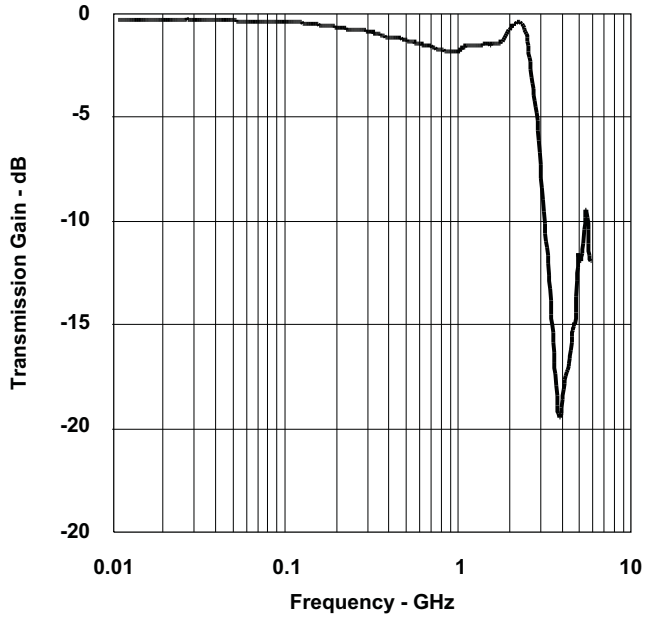


Figure 15.

OFF STATE DATA SWITCH ISOLATION vs FREQUENCY

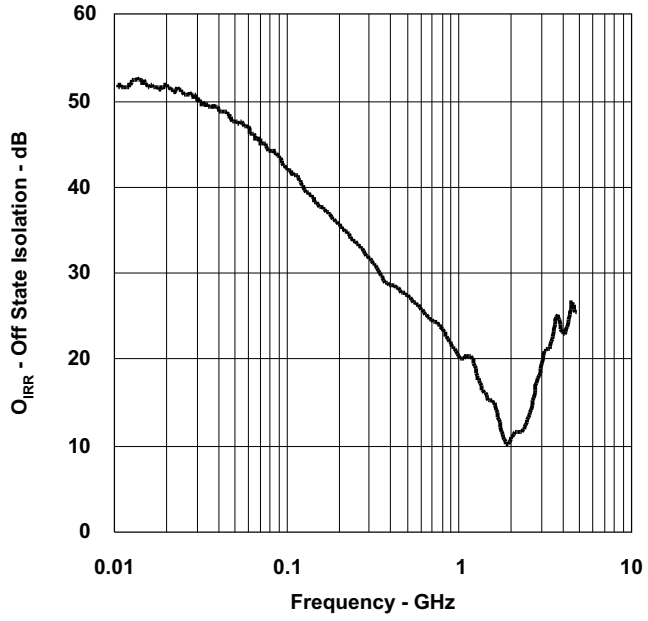


Figure 16.

TYPICAL CHARACTERISTICS (continued)

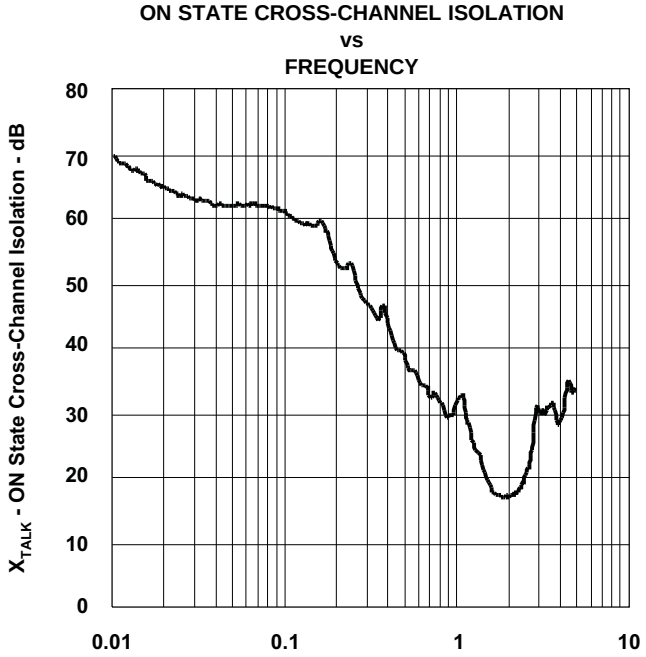


Figure 17.

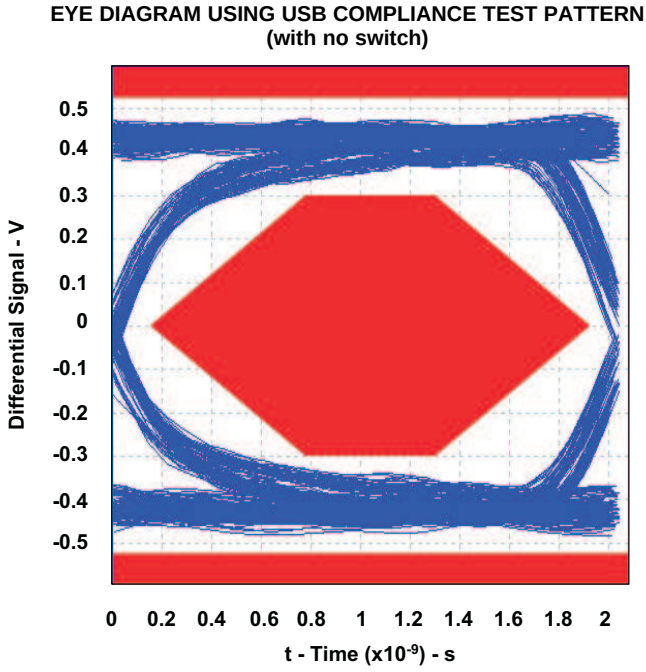


Figure 18.

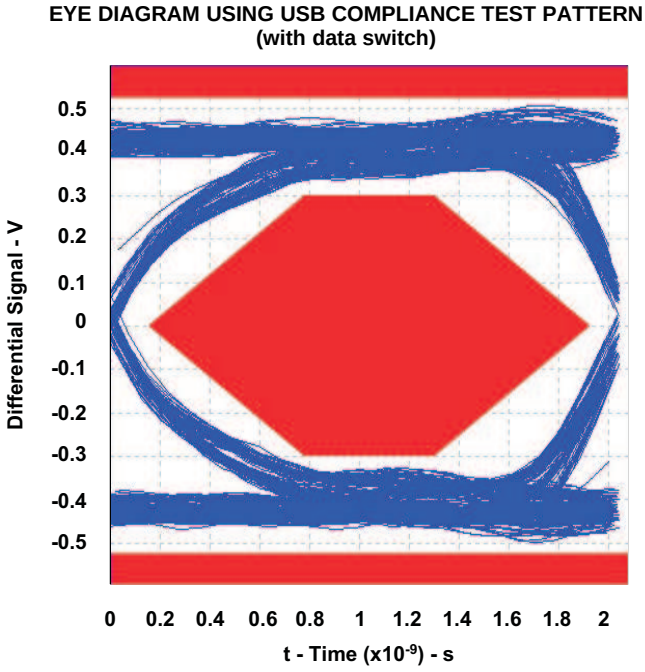
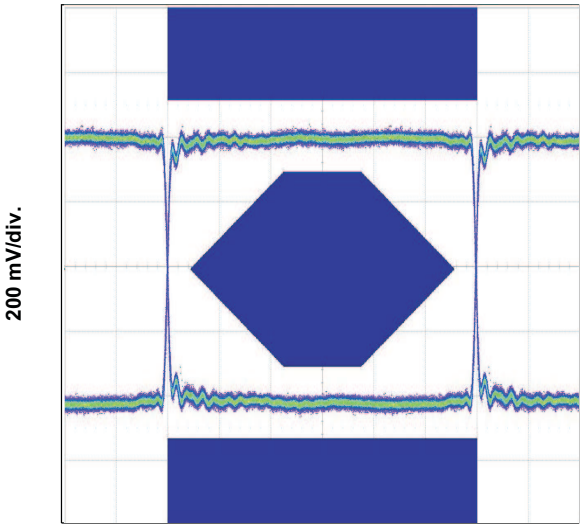


Figure 19.

TYPICAL CHARACTERISTICS (continued)

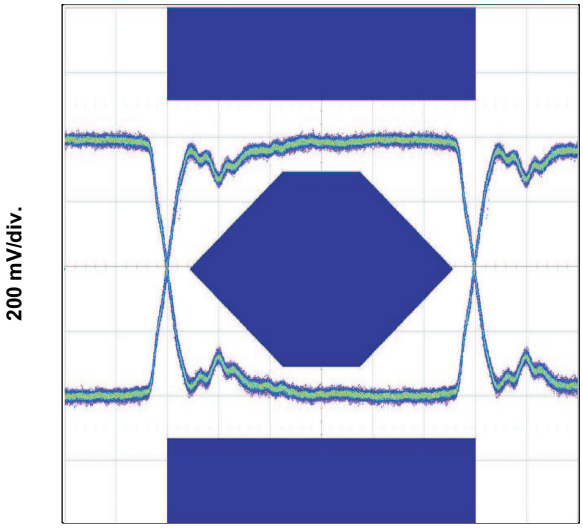
EYE DIAGRAM OF NEARLY IDEAL PULSE (with no switch)



348ps/div.

Figure 20.

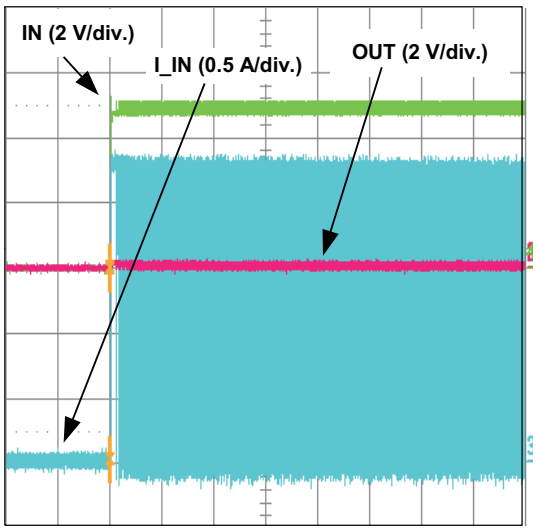
EYE DIAGRAM OF NEARLY IDEAL PULSE (with data switch)



348ps/div.

Figure 21.

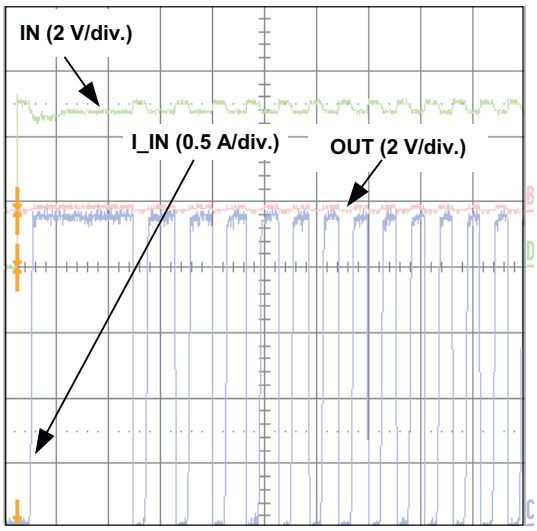
TURN ON INTO A SHORT CIRCUIT



0.2 s/div

Figure 22.

TURN ON INTO A SHORT CIRCUIT

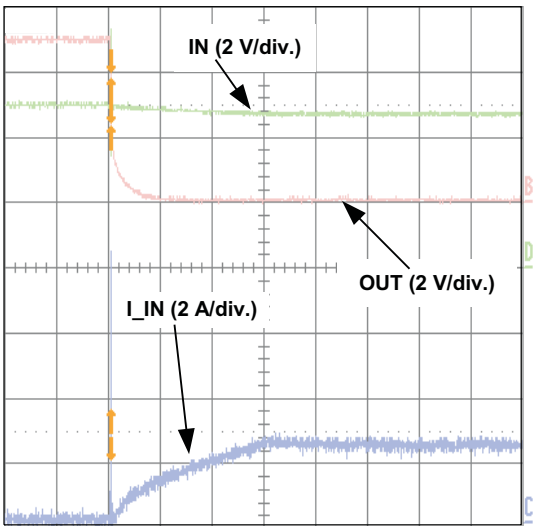


10 ms/div

Figure 23.

TYPICAL CHARACTERISTICS (continued)

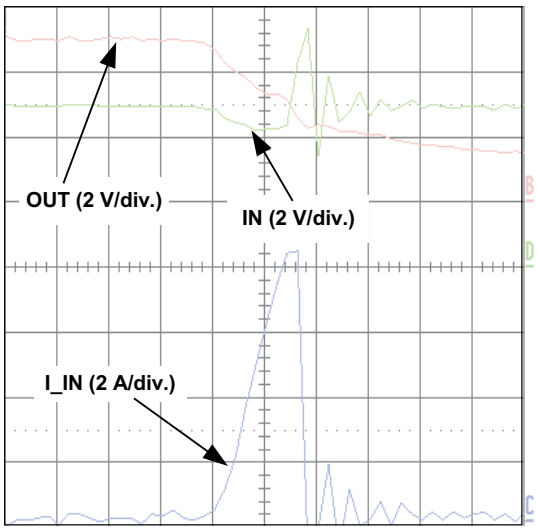
RESPONSE TO A SHORT-CIRCUIT (from no-load condition)



100 μs/div

Figure 24.

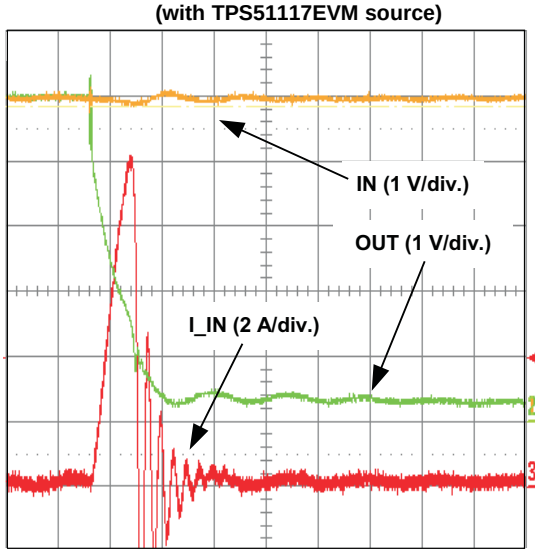
RESPONSE TO A SHORT-CIRCUIT (from no-load condition)



1 μs/div

Figure 25.

RESPONSE TO A SHORT-CIRCUIT FROM NO LOAD CONDITION (with TPS51117EVM source)



2 μs/div

Figure 26.

PARAMETER MEASUREMENT INFORMATION

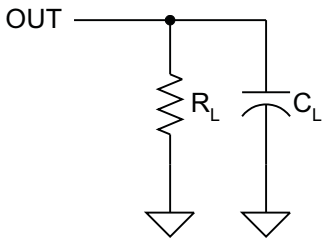


Figure 27. Test Circuit

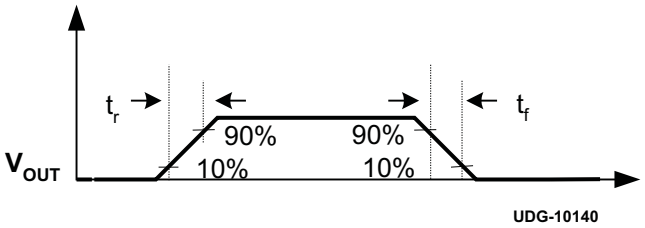


Figure 28. Voltage Waveform

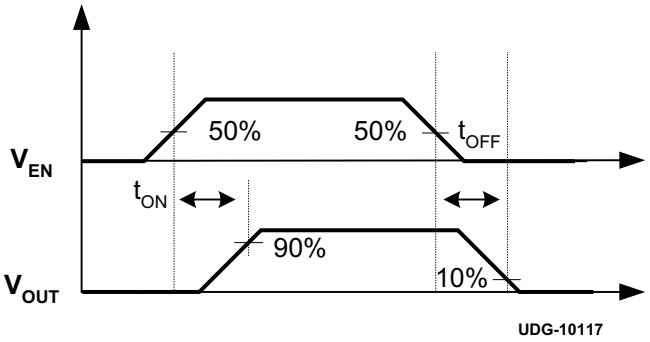


Figure 29. Voltage Waveforms

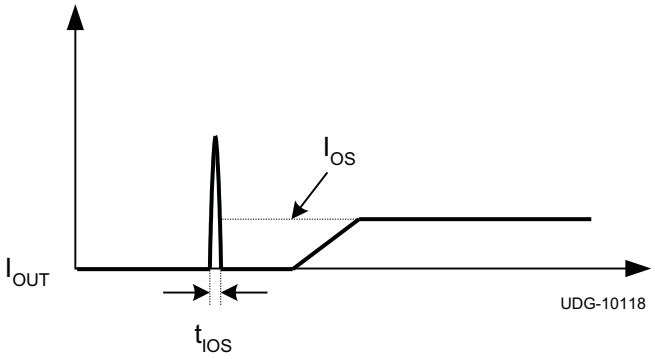


Figure 30. Response Time to Short-Circuit Waveform

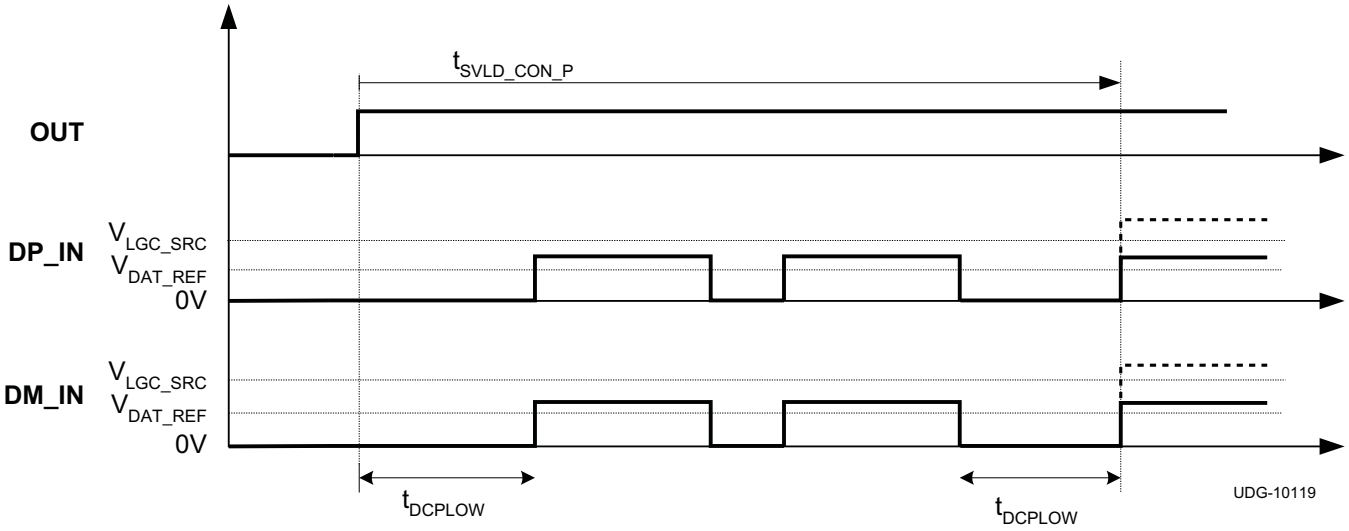


Figure 31. DCP BC1.2 Operation

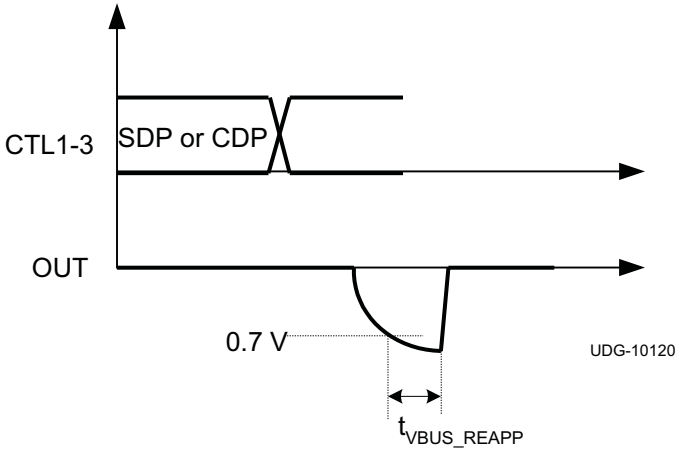


Figure 32. OUT Discharge During CTLx Lines Change

Divider Only Mode

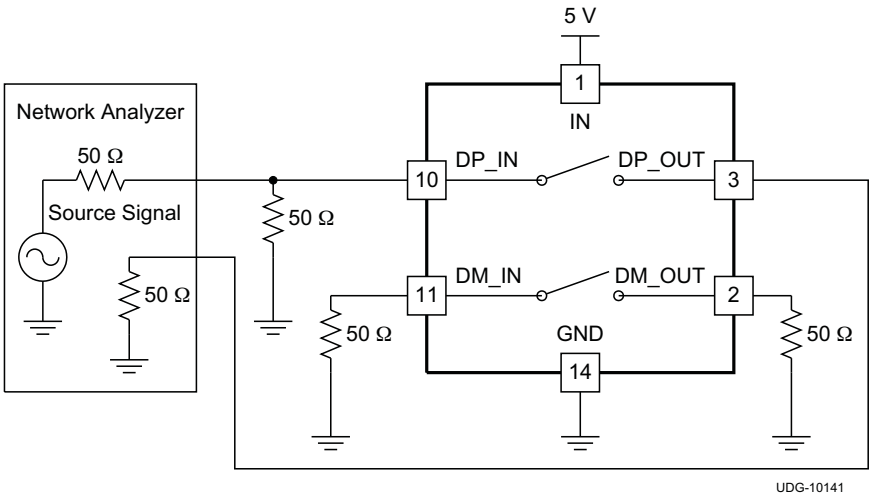


Figure 33. OFF State Isolation (O_{IRR})

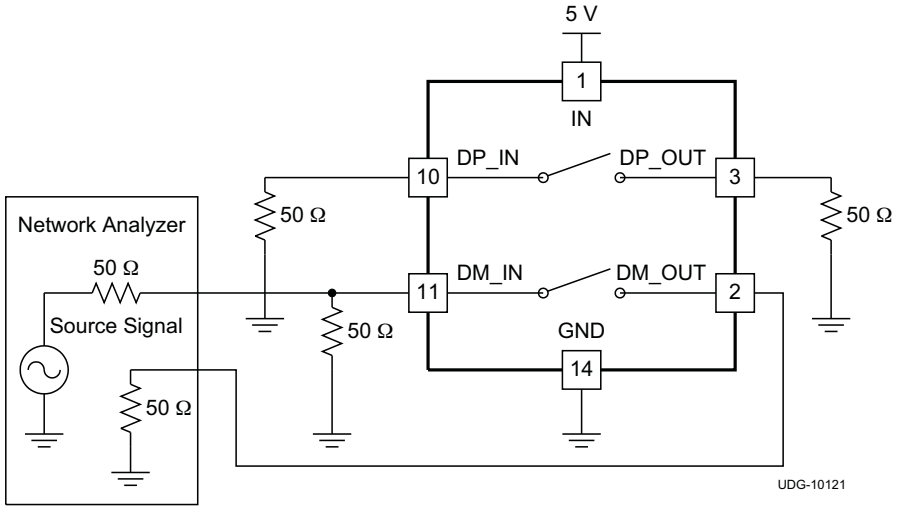


Figure 34. OFF State Isolation (O_{IRR})

Network Analyzer Setup

- Source signal = 600-mV peak-to-peak at 50-Ω load
- DC bias = 300 mV

SDP Mode

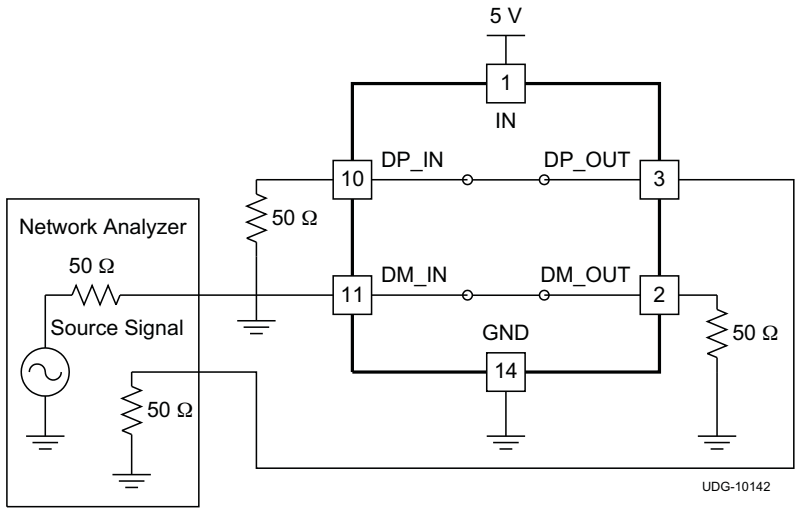


Figure 35. ON State Cross Channel Isolation (X_{TALK})

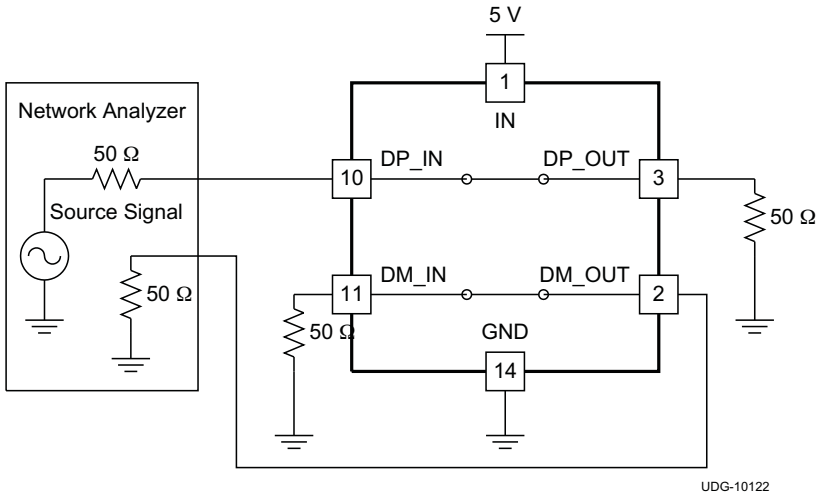


Figure 36. ON State Cross Channel Isolation (X_{TALK})

Network Analyzer Setup

- Source signal = 600-mV peak-to-peak at 50-Ω load
- DC bias = 300 mV

SDP Mode

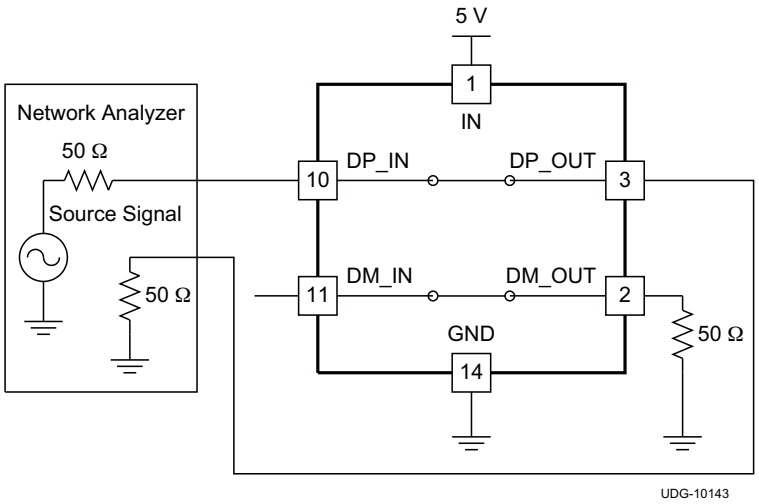


Figure 37. Bandwidth (BW)

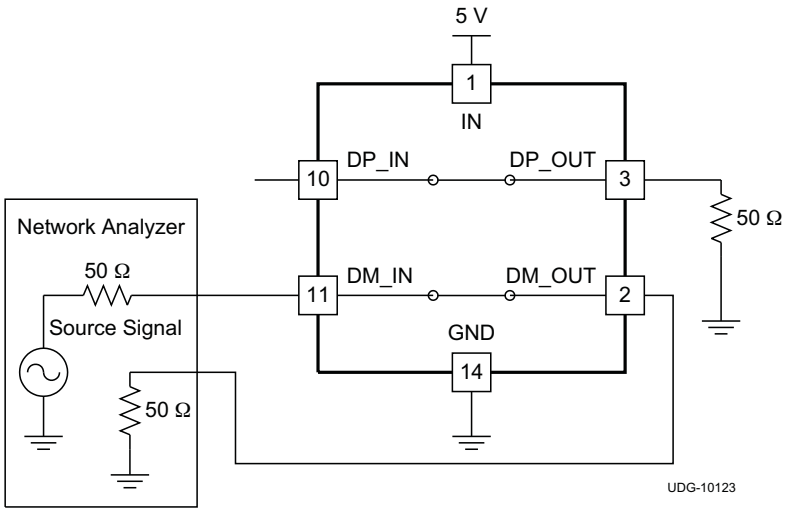


Figure 38. Bandwidth (BW)

Network Analyzer Setup

- Source signal = 600-mV peak-to-peak at 50-Ω load
- DC bias = 300 mV

SDP Mode

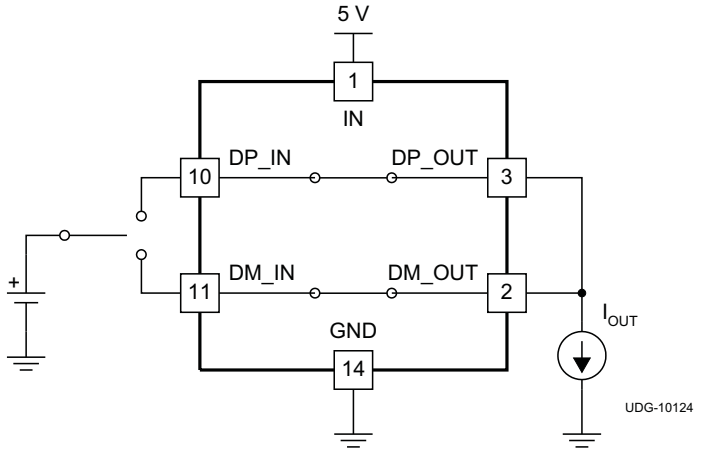


Figure 39. On Resistance DP/DM High-Speed Switch (R_{HS_ON})

$$R_{HS\_ON} = \frac{V_{DP\_IN} - V_{DP\_OUT}}{I_{OUT}} \quad (1)$$

$$R_{HS\_ON} = \frac{V_{DM\_IN} - V_{DM\_OUT}}{I_{OUT}} \quad (2)$$

GENERAL INFORMATION

Overview

The following overview references various industry standards. It is always recommended to consult the most up-to-date standard to ensure the most recent and accurate information.

Rechargeable portable equipment requires an external power source to charge its batteries. USB ports are a convenient location for charging because of an available 5-V power source. Universally accepted standards are required to make sure host and client-side devices operate together in a system to ensure power management requirements are met. Traditionally, USB host ports following the USB 2.0 specification must provide at least 500 mA to downstream client-side devices. Because multiple USB devices can be attached to a single USB port through a bus-powered hub, it is the responsibility of the client-side device to negotiate its power allotment from the host to ensure the total current draw does not exceed 500 mA. In general, each USB device is granted 100 mA and may request more current in 100 mA unit steps up to 500 mA. The host may grant or deny based on the available current.

Additionally, the success of USB has made the mini-USB connector a popular choice for wall adapter cables. This allows a portable device to charge from both a wall adapter and USB port with only one connector.

One common difficulty has resulted from this. As USB charging has gained popularity, the 500 mA minimum defined by USB 2.0 has become insufficient for many handset and personal media players which need a higher charging rate. On the other hand, wall adapters can provide much more current than 500 mA. Several new standards have been introduced defining protocol handshaking methods that allow host and client devices to acknowledge and draw additional current beyond the 500 mA minimum defined by USB 2.0 while still using a single micro-USB input connector.

The TPS2540, TPS2540A, TPS2541 and TPS2541A support three of the most common protocols:

- USB 2.0 Battery Charging Specification BC1.2
- Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider Mode

All three methods have similarities and differences, but the biggest commonality is that all three define three types of *charging ports* that provide charging current to client-side devices. These charging ports are defined as:

- Standard Downstream Port (USB 2.0) (SDP)
- Charging Downstream Port (CDP)
- Dedicated Charging Port (DCP)

BC1.2 defines a Charging Port as a downstream facing USB port that provides power for charging portable equipment.

The table below shows the differences between these ports according to BC1.2 .

Table 1. Operating Modes

PORT TYPE	SUPPORTS USB 2.0 COMMUNICATION	MAXIMUM ALLOWABLE CURRENT DRAW BY PORTABLE EQUIPMENT (A)
SDP (USB 2.0)	Yes	0.5
CDP	Yes	1.5
DCP	No	1.5

BC1.2 defines the protocol necessary to allow portable equipment to determine what type of port it is connected to so that it can allot its maximum allowable current draw. The hand-shaking process has two steps. During step one, the primary detection, the portable equipment outputs a nominal 0.6-V output on its D+ line and reads the voltage input on its D- line. The portable device concludes it is connected to an SDP if the voltage is less than the nominal data detect voltage of 0.3 V. The portable device concludes that it is connected to a Charging Port if the D- voltage is greater than the nominal data detect voltage of 0.3 V and less than 0.8 V. The second step, the secondary detection, is necessary for portable equipment to determine between a CDP and a DCP. The portable device outputs a nominal 0.6 V output on its D- line and reads the voltage input on its D+ line. The portable device concludes it is connected to a CDP if the data line being read remains less than the nominal data detect voltage of 0.3 V. The portable device concludes it is connected to a DCP if the data line being read is greater than the nominal data detect voltage of 0.3V and less than 0.8 V.

Standard Downstream Port (SDP) USB 2.0

An SDP is a traditional USB port that follows USB 2.0 and supplies a minimum of 500 mA per port. USB 2.0 communications is supported, and the host controller must be active to allow charging.

Charging Downstream Port (CDP)

A CDP is a USB port that follows USB 2.0 BC1.2 and supplies a minimum of 1.5 A per port. It provides power and meets USB 2.0 requirements for device enumeration. USB 2.0 communications is supported, and the host controller must be active to allow charging. What separates a CDP from an SDP is the host-charge handshaking logic that identifies this port as a CDP. A CDP is identifiable by a compliant BC1.2 client device and allows for additional current draw by the client device.

The CDP hand-shaking process is two steps. During step one the portable equipment outputs a nominal 0.6 V output on its D+ line and reads the voltage input on its D- line. The portable device concludes it is connected to an SDP if the voltage is less than the nominal data detect voltage of 0.3 V. The portable device concludes that it is connected to a Charging Port if the D- voltage is greater than the nominal data detect voltage of 0.3V and less than 0.8 V.

The second step is necessary for portable equipment to determine between a CDP and a DCP. The portable device outputs a nominal 0.6 V output on its D- line and reads the voltage input on its D+ line. The portable device concludes it is connected to a CDP if the data line being read remains less than the nominal data detect voltage of 0.3 V. The portable device concludes it is connected to a DCP if the data line being read is greater than the nominal data detect voltage of 0.3V and less than 0.8 V.

Dedicated Charging Port (DCP)

A DCP is a special type of wall-adapter used in charging applications that uses a micro-B connector to connect to portable devices. A DCP only provides power and cannot enumerate upstream facing portable equipment. It does not support USB 2.0 communications, but it does provide specific impedances on the data lines reserved for USB 2.0 so that it is identifiable as a dedicated charger.

The impedances presented on D+ and D- are different depending on the specific standard the dedicated charger is designed to. BC1.2 and the Chinese Telecommunications Industry Standard YD/T 1591-2009 define that the D+ and D- data lines should be shorted together with a maximum series impedance of 200 Ω.

On the other hand, with the divider mode, 2 V and 2.7 V are presented on D+ and on D-.

The TPS2540/40A/41/41A integrates an *auto-detect* feature that supports both DCP schemes. It starts in Divider Mode. If a BC1.2 -compliant device is attached, the TPS2540/40A/41/41A responds by discharging OUT, turning back ON the power switch and operating in BC1.2 DCP mode. It then stays in that mode until the device is unattached, in which case it goes back to Divider Mode.

High-Bandwidth Data Line Switch

The TPS2540/40A/41/41A passes the D+ and D- data lines through the device to enable monitoring and handshaking while supporting charging operation. A wide bandwidth signal switch is used, allowing data to pass through the device without corrupting signal integrity. The data line switches are turned on in any of CDP or SDP operating modes. The EN (or DSC if TPS2541/41A) input also needs to be at logic High for the data line switches to be enabled.

NOTE

1. While in CDP mode, the data switches are ON even while CDP handshaking is occurring.
2. The data line switches are OFF if EN (or DSC) is low, or if in DCP mode (BC1.2, Divider mode or Auto-detect). They are not automatically turned off if the power switch (IN to OUT) is doing current limiting. With TPS2540/40A, the data line switches are also off when in “000” mode.
3. The data switches are for USB 2.0 differential pair only. In the case of a USB 3.0 host, the super speed differential pairs must be routed directly to the USB connector without passing through the TPS2540/40A/41/41A.

Logic Control Modes

Both the TPS2540/40A and TPS2541/41A support the listed standards above for the SDP, CDP and DCP modes using the CTL1, CTL2, and CTL3 logic I/O control pins, although their truth tables are different as shown below. The different CTLx settings correspond to the different types of charge modes. Also, using the *Auto-Detect* Mode, the Divider Mode or BC1.2 / YD/T 1591-2009 can be automatically selected without external user interaction.

NOTE

With the TPS2540/40A, if the "000" mode is selected, the power switch will be turned off and an output discharge resistor will be connected, while the data line switches will be turned off.

Table 2. TPS2540/40A Control Truth Table

CTL1	CTL2	CTL3	MODE
0	0	0	OUT discharge, power switch OFF.
0	X	1	Dedicated charging port, auto-detect.
X	1	0	Standard downstream port, USB 2.0 Mode.
1	0	0	Dedicated charging port, BC1.2 only.
1	0	1	Dedicated charging port, Divider Mode only.
1	1	1	Charging downstream port, BC1.2.

Table 3. TPS2541/41A Control Truth Table

CTL1	CTL2	CTL3	MODE
0	0	X	Dedicated charging port, auto-detect.
0	1	X	Dedicated charging port, BC1.2.
1	0	X	Dedicated charging port, Divider Mode only.
1	1	0	Standard downstream port, USB 2.0 Mode.
1	1	1	Charging downstream port, BC1.2.

Output Discharge

To allow a charging port to renegotiate current with a portable device, TPS2540/40A/41/41A uses the VBUS discharge function. It proceeds by turning off the power switch while discharging OUT, then turning back ON the power switch to reassert the OUT voltage.

This discharge function is automatically applied when a change at the CTLx lines results in any of the following mode transitions.

- Any transition to and from CDP
- Any transition to and from SDP

In addition to this, a direct discharge control, DSC, is available with the TPS2541/41A, while with the TPS2540/40A, a discharge can be achieved using the mode "000".

Overcurrent Protection

When an over-current condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before V_{IN} has been applied.

The TPS2540/40A/41/41A senses the short and immediately switches into a constant-current output. In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for nominally one to two microseconds before the current-limit circuit can react. The device operates in constant-current mode after the current-limit circuit has responded. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting. The device will remain off until the junction temperature cools approximately 10°C and will then re-start. The device will continue to cycle on/off until the over-current condition is removed.

Current-Limit Thresholds

The TPS2540/40A/41/41A has two independent current-limit thresholds that are each programmed externally with a resistor. The following equation programs the typical current-limit threshold:

$$I_{SHORT} = \frac{48000}{R_{ILIMx}} \quad (3)$$

where I_{SHORT} is in mA and R_{ILIMx} is in kΩ. R_{ILIMx} corresponds to RILIM0 when ILIM_SEL is logic LO and to RILIM1 when ILIM_SEL is logic HI. The ILIM_SEL pin allows the system to digitally select between two current-limit thresholds, which is useful in end equipment that may require a lower setting when powered from batteries vs. wall adapters.

$\overline{\text{FAULT}}$ Response

The $\overline{\text{FAULT}}$ open-drain output is asserted (active low) during an over-temperature or current limit condition. The output remains asserted until the fault condition is removed. The TPS2540/40A/41/41A is designed to eliminate false $\overline{\text{FAULT}}$ reporting by using an internal deglitch circuit for current limit conditions without the need for external circuitry. This ensures that $\overline{\text{FAULT}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. Over-temperature conditions are not deglitched and assert the $\overline{\text{FAULT}}$ signal immediately.

Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted oscillations on the output due to input voltage drop from large current surges.

Thermal Sense

The TPS2540/40A/41/41A protects itself with two independent thermal sensing circuits that monitor the operating temperature of the power distribution switch and disables operation if the temperature exceeds recommended operating conditions. The device operates in constant-current mode during an over-current condition, which increases the voltage drop across power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, so the junction temperature rises during an over-current condition. The first thermal sensor turns off the power switch when the die temperature exceeds 135°C and the part is in current limit. The second thermal sensor turns off the power switch when the die temperature exceeds 155°C regardless of whether the power switch is in current limit. Hysteresis is built into both thermal sensors, and the switch turns on after the device has cooled by approximately 10°C. The switch continues to cycle off and on until the fault is removed. The open-drain false reporting output $\overline{\text{FAULT}}$ is asserted (active low) during an over-temperature shutdown condition.

APPLICATION INFORMATION

Programming the Current Limit Threshold

There are two overcurrent thresholds, which are user programmable via R_{ILIM0} and R_{ILIM1}. The TPS2540/40A/41/41A uses an internal regulation loop to provide a regulated voltage on the ILIM0 and ILIM1 pins. The current-limit thresholds are proportional to the current sourced out of ILIM0 and ILIM1. The recommended 1% resistor range for R_{ILIM0} and R_{ILIM1} are 16.9 kΩ ≤ R_{ILIM} ≤ 750 kΩ to ensure stability of the internal regulation loop, although not exceeding 210 kΩ results in a better accuracy. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for R_{ILIMx}. The following equations calculates the resulting overcurrent threshold for a given external resistor value (R_{ILIMx}). The traces routing the R_{ILIMx} resistors to the TPS2540/40A/41/41A should be as short as possible to reduce parasitic effects on the current-limit accuracy.

The equations and the graph below can be used to estimate the minimum and maximum variation of the current limit threshold for a predefined resistor value. This variation is an approximation only and does not take into account the resistor tolerance or the variation of ILIM. For exact variation of ILIM, refer to the current limit section of the electrical specification table.

$$I_{SHORT\_min} = \frac{48000}{R_{ILIMx}^{1.037}} \quad (4)$$

$$I_{SHORT\_max} = \frac{48000}{R_{ILIMx}^{0.962}} \quad (5)$$

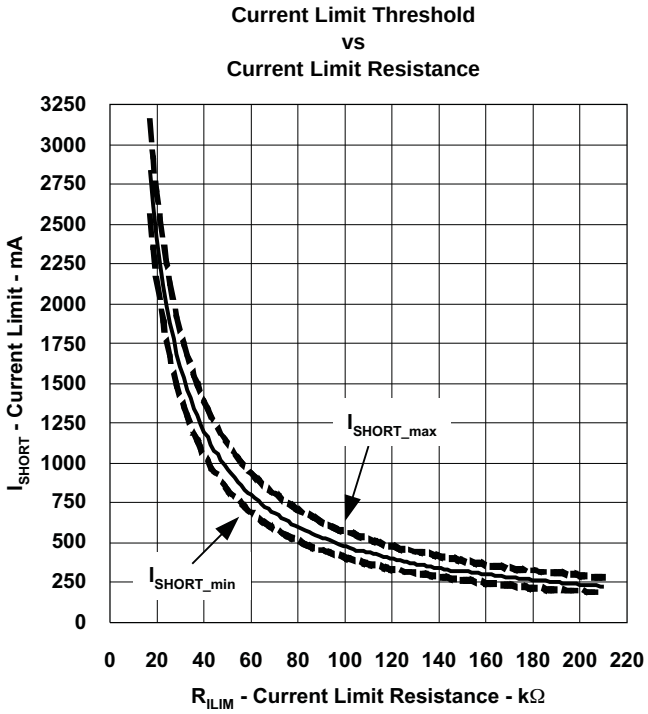


Figure 40.

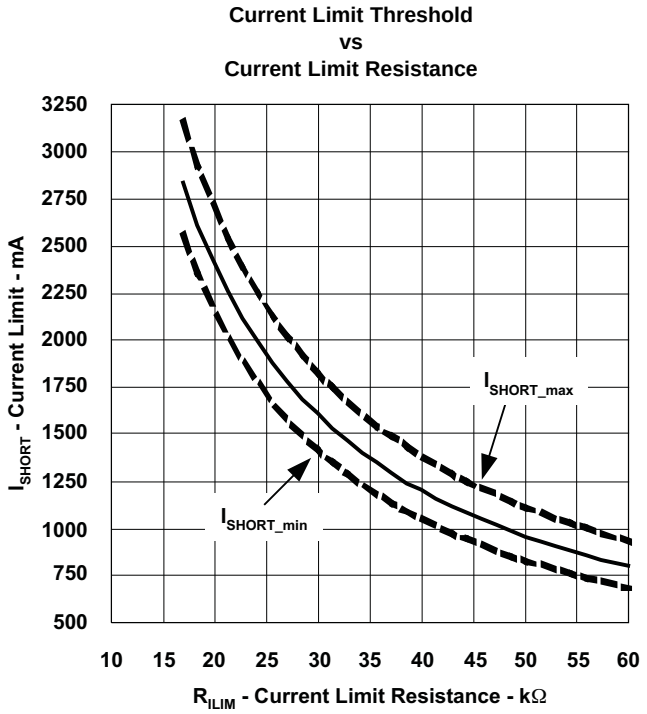


Figure 41.

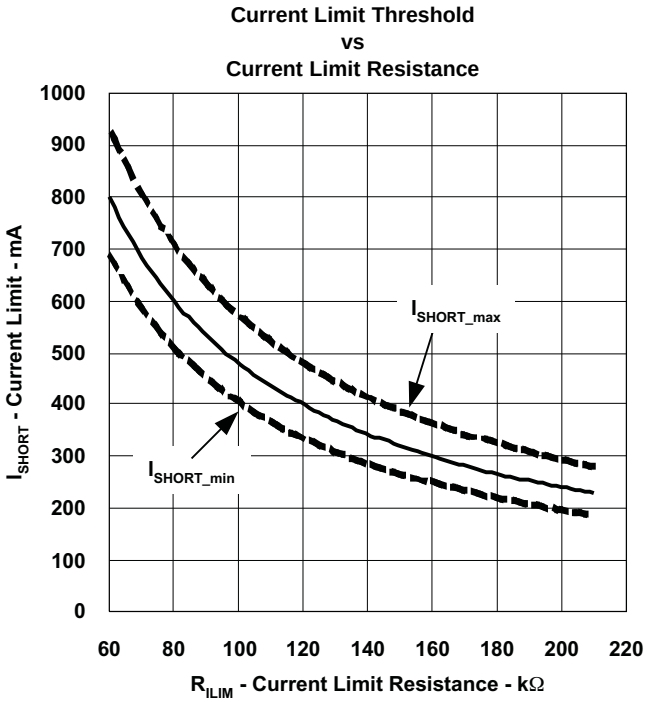


Figure 42.

Current Limit Setpoint Example

In the following example, choose the ILIM resistor to ensure that the TPS2540/40A/41/41A does not trip off under worst case conditions of ILIM and resistor tolerance (assume 1% resistor tolerance). For this example, IOS_{MIN} = 2500 mA.

$$IOS_{MIN} = \frac{48000}{R_{ILIMx}^{1.037}} = 2500\,mA \tag{6}$$

$$R_{ILIMx} = \left[\frac{48000}{IOS_{MIN}}\right]^{\frac{1}{1.037}} = \left[\frac{48000}{2500\,mA}\right]^{\frac{1}{1.037}} = 17.28\,k\Omega \tag{7}$$

Including resistor tolerance, target maximum:

$$R_{ILIMx} = \frac{17.28k\Omega}{1.01} = 17.11k\Omega \tag{8}$$

Choose:

$$R_{ILIMx} = 16.9k\Omega \tag{9}$$

CTL Pin Configuration for Notebook States

The CTL pins provide the user with mode flexibility. Specifically, within a notebook, states S0, S3, S4, and S5 are important for controlling power consumption. For S0 the host controller is active, so either SDP or CDP should be selected. The notebook is responsible for sourcing at least 500mA when SDP is selected and at least 1500 mA when CDP is selected. Figure 43 illustrates the circuit connection for TPS2541/41A using one control signal (STATE). When STATE = logic 0, auto detect is selected (S3/S4/S5, 1.5 A). When STATE = logic 1, CDP mode is selected (S0, 1.5 A).

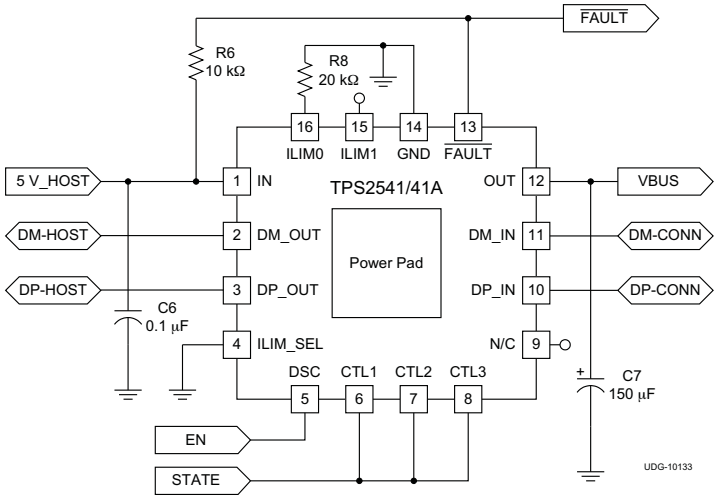


Figure 43. TPS2541/41A Application Using Single STATE Control Signal

Figure 44 illustrates the circuit connection for TPS2540/40A with STATE and ADAPTER control signals. If the adapter is present (ADAPTER = logic 1), the TPS2540/40A supports auto detect operation when STATE = logic 0 (S3/S4/S5, 1.5 A) and CDP operation when STATE = logic 1 (S0, 1.5 A). If the adapter is not present (ADAPTER = logic 0), the TPS2540/40A disables sleep charge when STATE = logic 0 (S3/S4/S5, power switch off) and SDP operation when STATE = logic 1 (S0, 0.5 A).

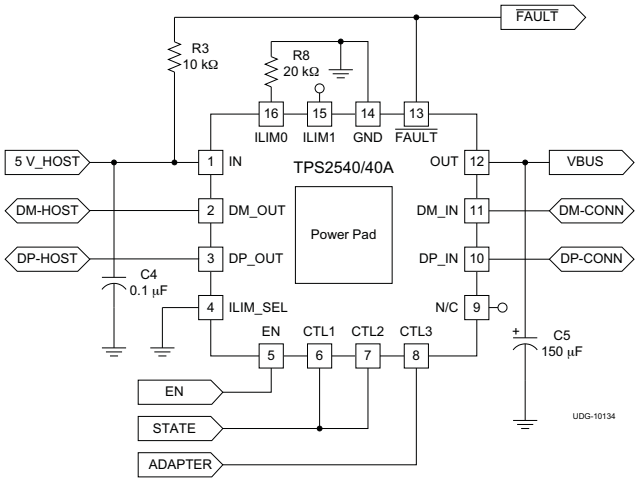


Figure 44. TPS2540/40A Application Using STATE and ADAPTER Control Signals

Layout Guidelines

TPS2540/40A/41/41A Placement: Place the TPS2540/40A/41/41A near the USB output connector and 150-µF OUT pin filter capacitor. Connect the exposed Power PAD to the GND pin and to the system ground plane using a via array.

IN Pin Bypass Capacitance: Place the 0.1-µF bypass capacitor near the IN pin and make the connection using a low inductance trace.

D+ and D- Traces: Route in and out traces as controlled impedance differential pairs per the USB specification and the Intel guideline for USB-2.0. Minimize the use of vias in the high speed data lines.

ESD

The use of a common mode choke in the upstream datapath can provide additional ESD protection from client side cable insertion transients. In addition, a low capacitance ESD protection array such as the TPD2E001 provides a robust solution. The TPS2540EVM-623 (SLVU401) provides a good example of routing and output datapath protection.

Using a system board, applying same design rules and protection devices as the TPS2540EVM-623 , the TPS2540 has been tested to EN61000-4-2. The levels used were 8-kV contact discharge and 15-kV air discharge. Voltage transients were applied between D+ terminal and the earth ground, and between D- terminal and the earth ground, V- being connected to earth ground. Tests were performed while both powered and unpowered. No TPS2540 failures were observed and operation was continuous.

ILIM0 and ILIM1 Pin Connections

Current limit set point accuracy can be compromised by stray leakage from a higher voltage source to the ILIM0 or ILIM1 pins. Ensure that there is adequate spacing between IN pin copper/trace and ILIM0 pin trace to prevent contaminant buildup during the PCB assembly process. If a low current limit set point is required (RILIMx > 200 kΩ), use ILIM1 for this case as it is further away from the IN pin.

REVISION HISTORY

Changes from Original (October 2010) to Revision A **Page**

- Added TPS2540A device to the datasheet. 1
- Deleted All (Draft) notations for BC1.2. 1
- Added Longer Detach Detection Time (TPS2540A) bullet. 1
- Changed Typical Application Diagram. 1
- Added TPS2540A description information. 2
- Added Low DP_IN period in DCP mode information for the TPS2541A device 7
- Changed pinout drawing. 8
- Changed TPS2540/40A Control Signal drawing. 30

Changes from Revision A (April 2011) to Revision B **Page**

- Added PRODUCT INFORMATION for device number TPS2540A. 2

Changes from Revision B (July 2011) to Revision C **Page**

- Added TPS2541A device to the datasheet. 1
- Added T_{DCPLOW} column for A and non-A versions 2
- Added PRODUCT INFORMATION for device number TPS2541A. 2
- Added Low DP_IN period in DCP mode, see Figure 32, note 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2540ARTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2540A	Samples
TPS2540ARTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2540A	Samples
TPS2540RTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2540	Samples
TPS2540RTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2540	Samples
TPS2541ARTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2541A	Samples
TPS2541ARTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2541A	Samples
TPS2541RTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2541	Samples
TPS2541RTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2541	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

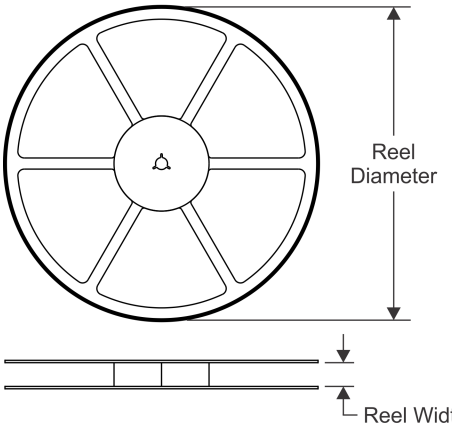
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

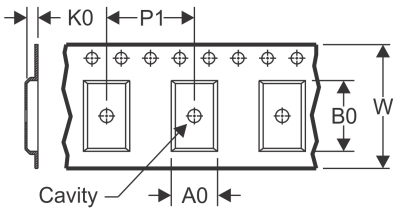
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

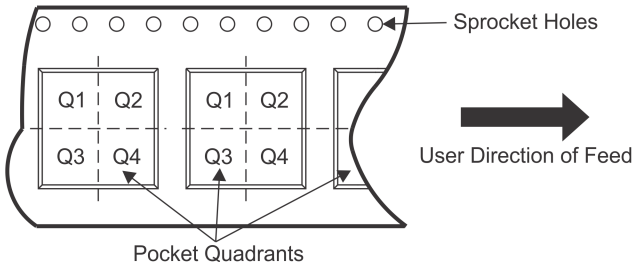


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

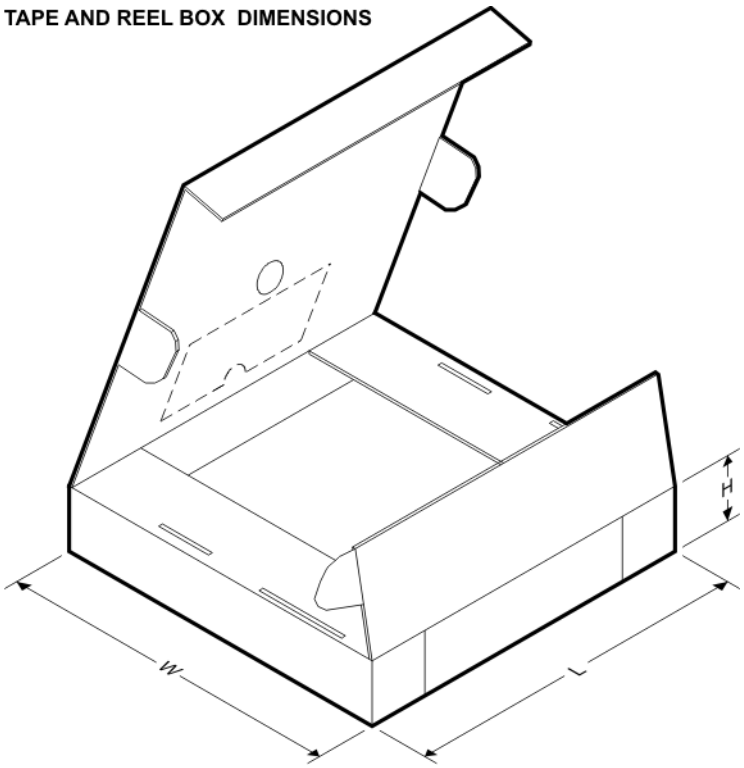
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2540ARTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2540ARTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2540ARTET	WQFN	RTE	16	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS2540ARTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2540RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2540RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2540RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2541ARTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2541ARTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2541ARTET	WQFN	RTE	16	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS2541ARTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2541RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2541RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2541RTET	WQFN	RTE	16	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS2541RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

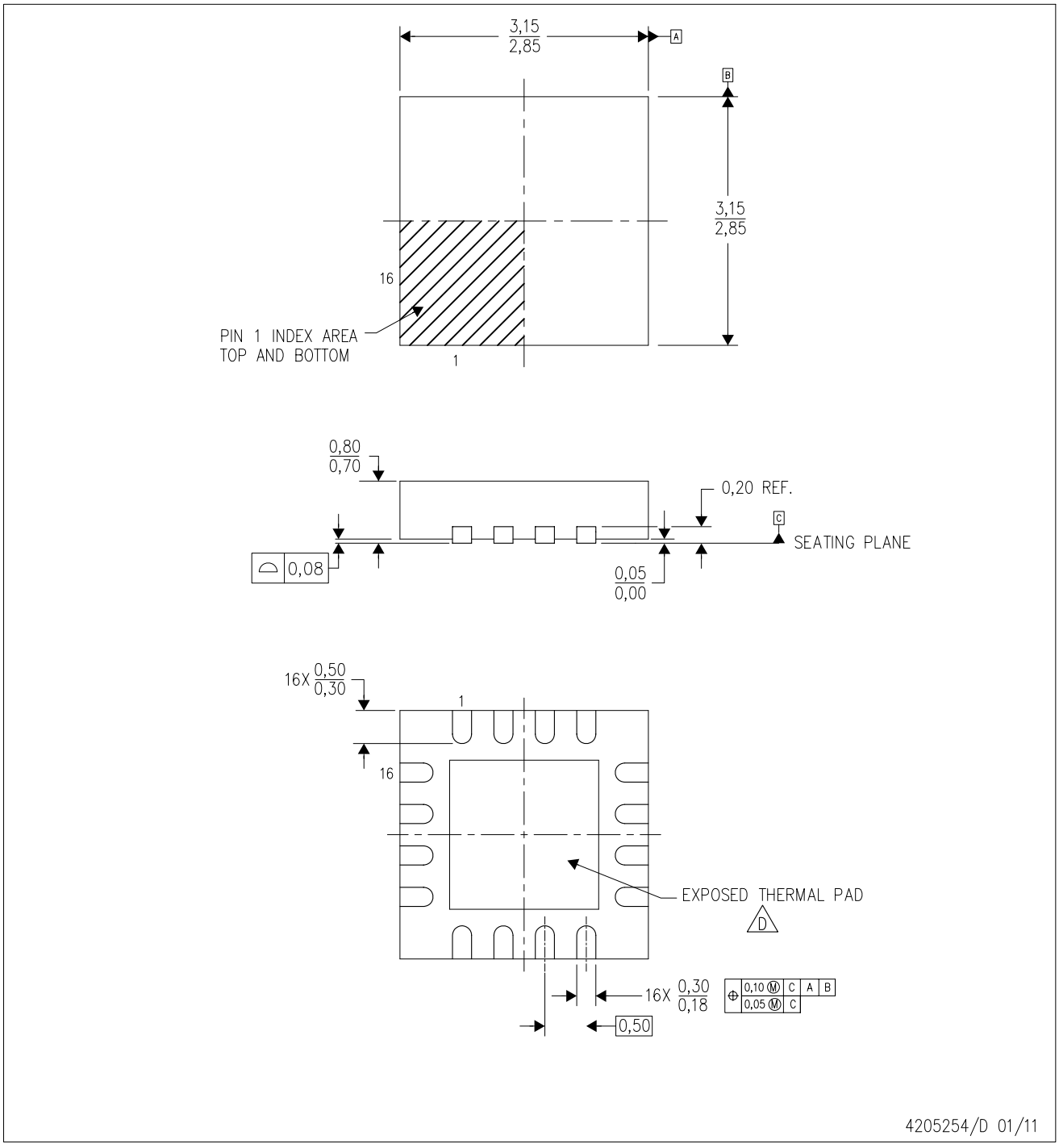
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2540ARTER	WQFN	RTE	16	3000	338.0	355.0	50.0
TPS2540ARTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS2540ARTET	WQFN	RTE	16	250	338.0	355.0	50.0
TPS2540ARTET	WQFN	RTE	16	250	210.0	185.0	35.0
TPS2540RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS2540RTET	WQFN	RTE	16	250	210.0	185.0	35.0
TPS2540RTET	WQFN	RTE	16	250	210.0	185.0	35.0
TPS2541ARTER	WQFN	RTE	16	3000	338.0	355.0	50.0
TPS2541ARTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS2541ARTET	WQFN	RTE	16	250	338.0	355.0	50.0
TPS2541ARTET	WQFN	RTE	16	250	210.0	185.0	35.0
TPS2541RTER	WQFN	RTE	16	3000	338.0	355.0	50.0
TPS2541RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS2541RTET	WQFN	RTE	16	250	338.0	355.0	50.0
TPS2541RTET	WQFN	RTE	16	250	210.0	185.0	35.0

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

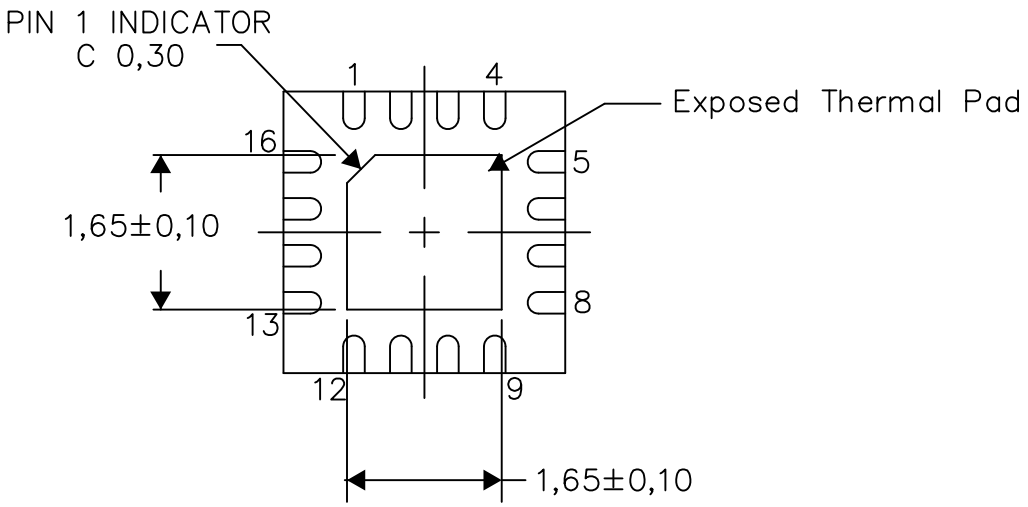
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



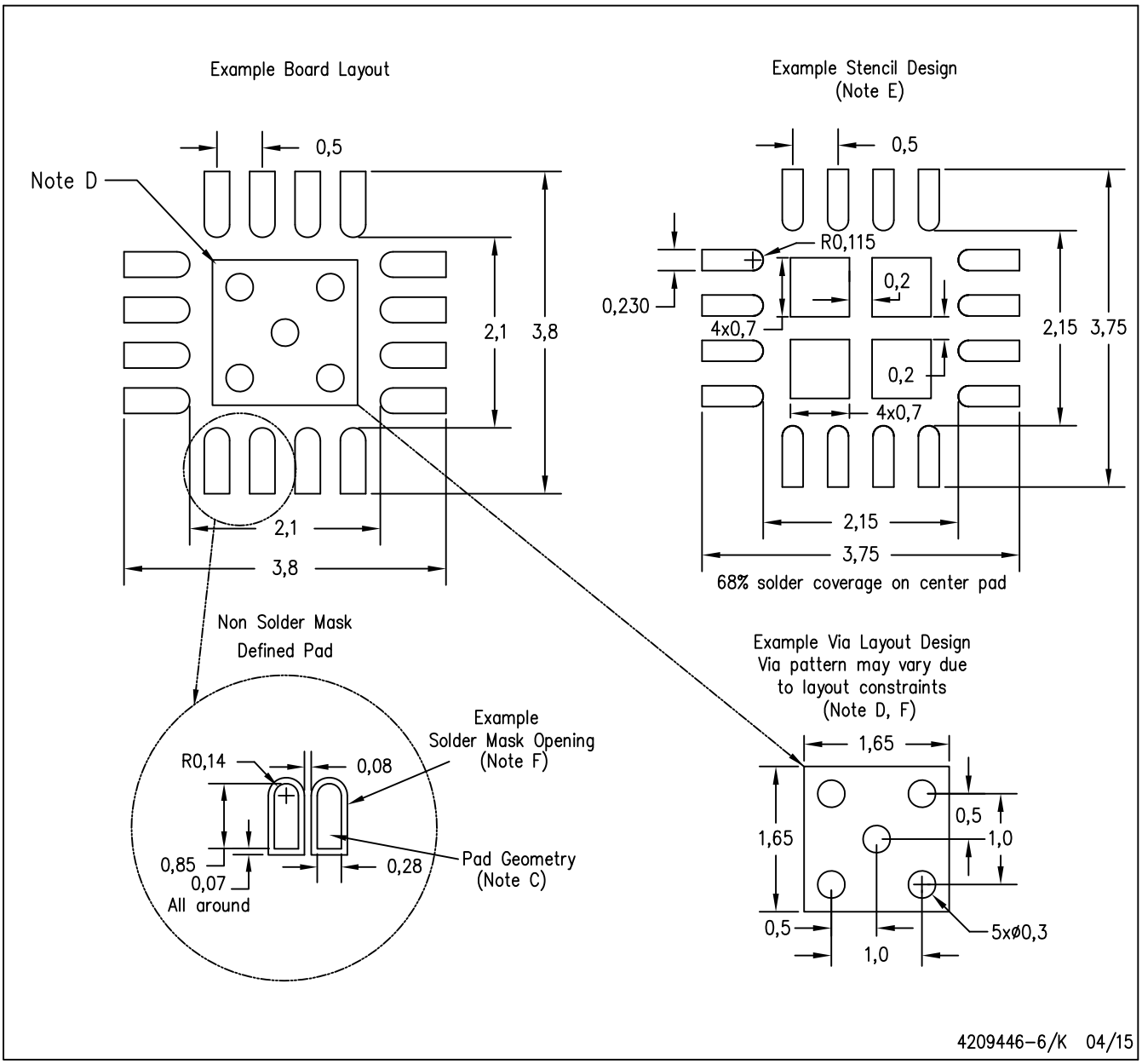
Bottom View

Exposed Thermal Pad Dimensions

4206446–4/U 08/15

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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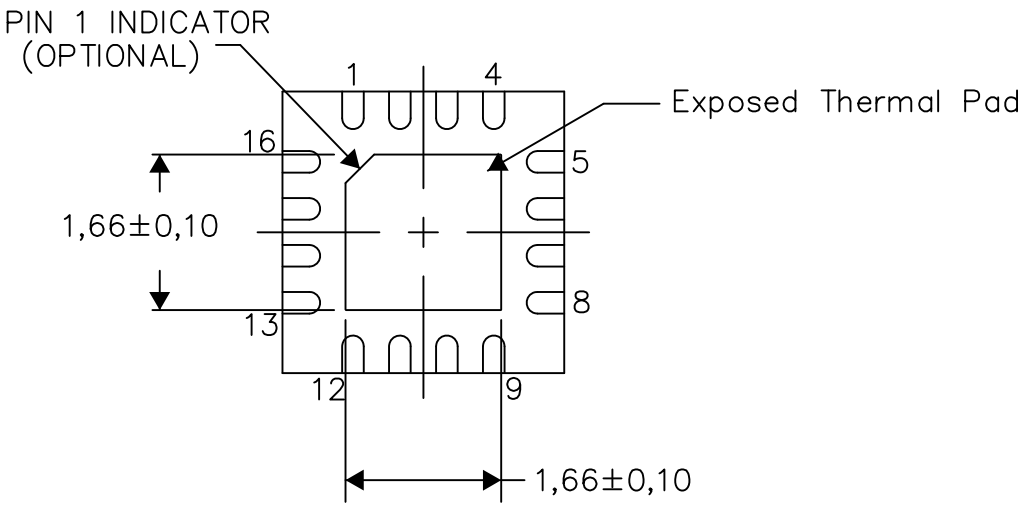
The exposed thermal pad dimensions for this package are shown in the following illustration.



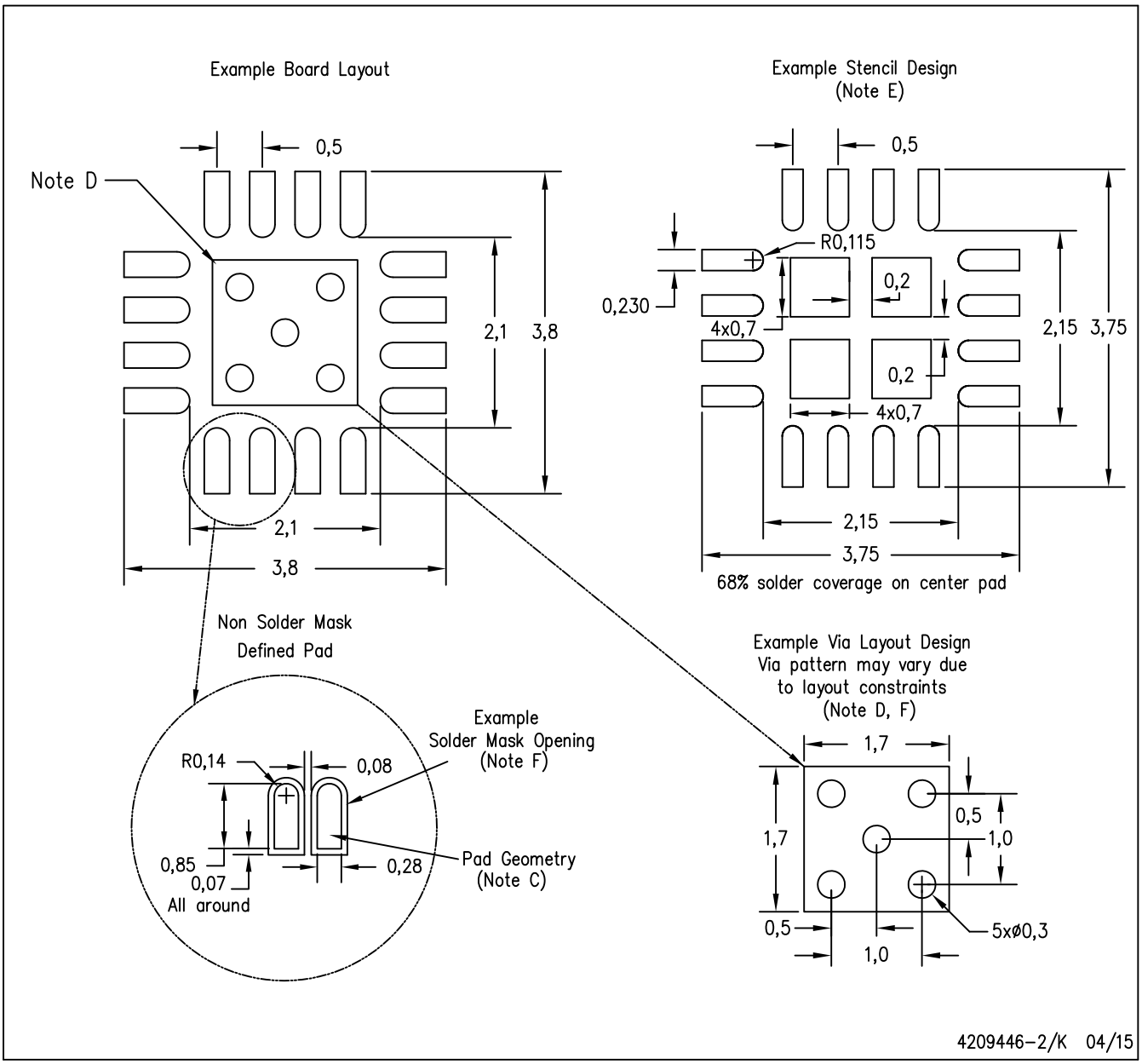
Bottom View

Exposed Thermal Pad Dimensions

4206446–8/U 08/15

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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