

MSP430F522x, MSP430F521x Mixed-Signal Microcontrollers

1 Device Overview

1.1 Features

- Dual-Supply Voltage Device
 - Primary Supply (AVCC, DVCC):
 - Powered From External Supply:
3.6 V Down to 1.8 V
 - Up to 22 General-Purpose I/Os With up to Four External Interrupts
 - Low-Voltage Interface Supply (DVIO):
 - Powered From Separate External Supply:
1.62 V to 1.98 V
 - Up to 31 General-Purpose I/Os With up to 12 External Interrupts
 - Serial Communications
- Ultra-Low Power Consumption
 - Active Mode (AM):
All System Clocks Active
290 μ A/MHz at 8 MHz, 3.0 V, Flash Program Execution (Typical)
150 μ A/MHz at 8 MHz, 3.0 V, RAM Program Execution (Typical)
 - Standby Mode (LPM3):
Real-Time Clock (RTC) With Crystal, Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wakeup:
1.9 μ A at 2.2 V, 2.1 μ A at 3.0 V (Typical)
Low-Power Oscillator (VLO), General-Purpose Counter, Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wakeup:
1.4 μ A at 3.0 V (Typical)
 - Off Mode (LPM4):
Full RAM Retention, Supply Supervisor Operational, Fast Wakeup:
1.1 μ A at 3.0 V (Typical)
 - Shutdown Mode (LPM4.5):
0.18 μ A at 3.0 V (Typical)
- Wake up From Standby Mode in 3.5 μ s (Typical)
- 16-Bit RISC Architecture, Extended Memory, up to 25-MHz System Clock
- Flexible Power-Management System
 - Fully Integrated LDO With Programmable Regulated Core Supply Voltage
 - Supply Voltage Supervision, Monitoring, and Brownout
- Unified Clock System
 - FLL Control Loop for Frequency Stabilization
 - Low-Power Low-Frequency Internal Clock Source (VLO)
 - Low-Frequency Trimmed Internal Reference Source (REFO)
 - 32-kHz Watch Crystals (XT1)
 - High-Frequency Crystals up to 32 MHz (XT2)
- 16-Bit Timer TA0, Timer_A With Five Capture/Compare Registers
- 16-Bit Timer TA1, Timer_A With Three Capture/Compare Registers
- 16-Bit Timer TA2, Timer_A With Three Capture/Compare Registers
- 16-Bit Timer TB0, Timer_B With Seven Capture/Compare Shadow Registers
- Two Universal Serial Communication Interfaces
 - USCI_A0 and USCI_A1 Each Support:
 - Enhanced UART With Automatic Baud Rate Detection
 - IrDA Encoder and Decoder
 - Synchronous SPI
 - USCI_B0 and USCI_B1 Each Support:
 - I²C
 - Synchronous SPI
- 10-Bit Analog-to-Digital Converter (ADC) With Internal Reference, Sample-and-Hold
- Comparator
- Hardware Multiplier Supports 32-Bit Operations
- Serial Onboard Programming, No External Programming Voltage Needed
- Three-Channel Internal DMA
- Basic Timer With RTC Feature
- [Device Comparison](#) Summarizes Available Family Members



1.2 Applications

- Analog and Digital Sensor Systems
- Data Loggers
- General-Purpose Applications

1.3 Description

The TI MSP430™ family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode in 3.5 μs (typical).

The MSP430F522x series are microcontrollers with four 16-bit timers, a high-performance 10-bit ADC, two universal serial communication interfaces (USCIs), a hardware multiplier, DMA, a comparator, and an RTC module with alarm capabilities.

The MSP430F521x series include all of the peripherals of the MSP430F522x series with the exception of the ADC.

All devices have a split I/O supply system that allows for a seamless interface to other devices that have a nominal 1.8-V I/O interface without the need for external level translation.

For complete module descriptions, see the [MSP430F5xx and MSP430F6xx Family User's Guide](#). For design guidelines, see [Designing With MSP430F522x and MSP430F521x Devices](#).

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE ⁽²⁾ |
|-----------------|------------|-------------------------------|
| MSP430F5229IRGC | VQFN (64) | 9 mm × 9 mm |
| MSP430F5229IZQE | BGA (80) | 5 mm × 5 mm |
| MSP430F5224IRGZ | VQFN (48) | 7 mm × 7 mm |
| MSP430F5219IYFF | DSBGA (64) | See Section 8 |

- (1) For the most current part, package, and ordering information, see the *Package Option Addendum* in [Section 8](#), or see the TI website at www.ti.com.
- (2) The dimensions shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in [Section 8](#).

1.4 Functional Block Diagrams

Figure 1-1 shows the functional block diagram for the MSP430F5229 and MSP430F5227 devices in the RGC, ZQE, YFF packages.

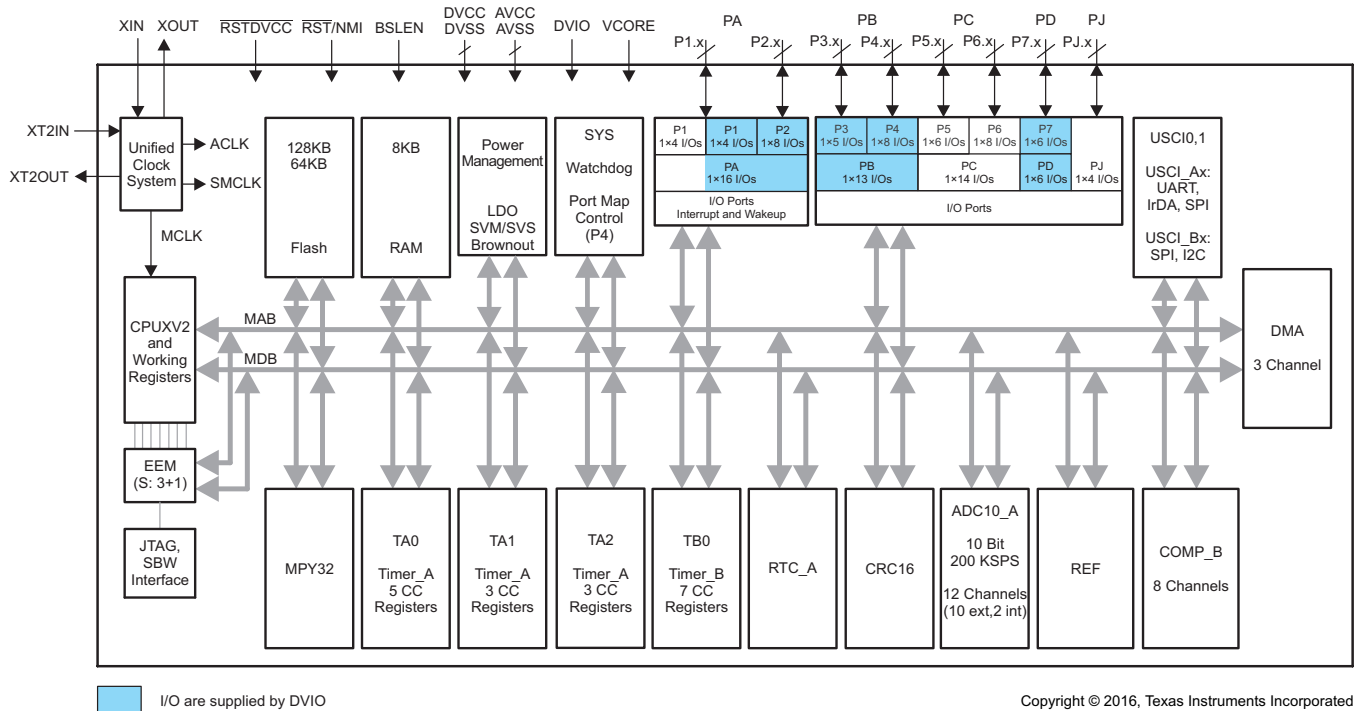


Figure 1-1. Functional Block Diagram – F5229, F5227 – RGC, ZQE, YFF Packages

Figure 1-2 shows the functional block diagram for the MSP430F5224 and MSP430F5222 devices in the RGZ package.

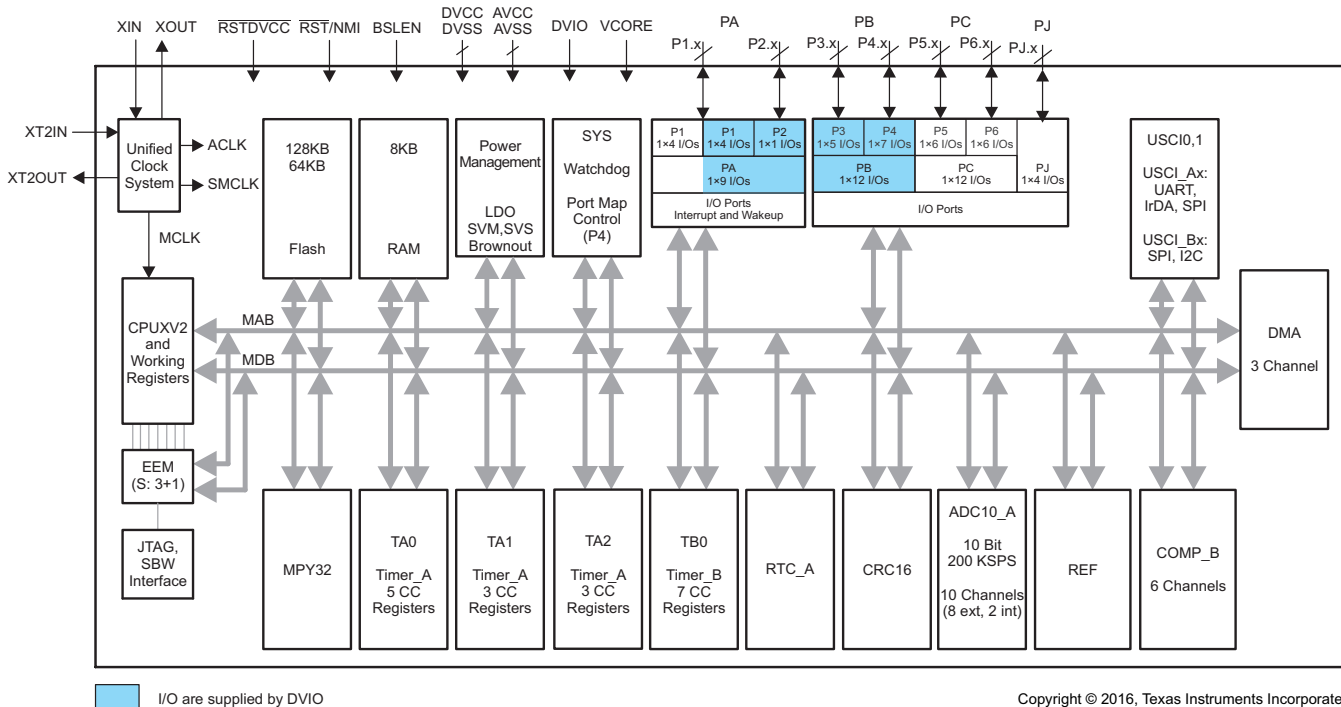


Figure 1-2. Functional Block Diagram – F5224, F5222 – RGZ Package

Figure 1-3 shows the functional block diagram for the MSP430F5219 and MSP430F5217 devices in the RGC, ZQE, and YFF packages.

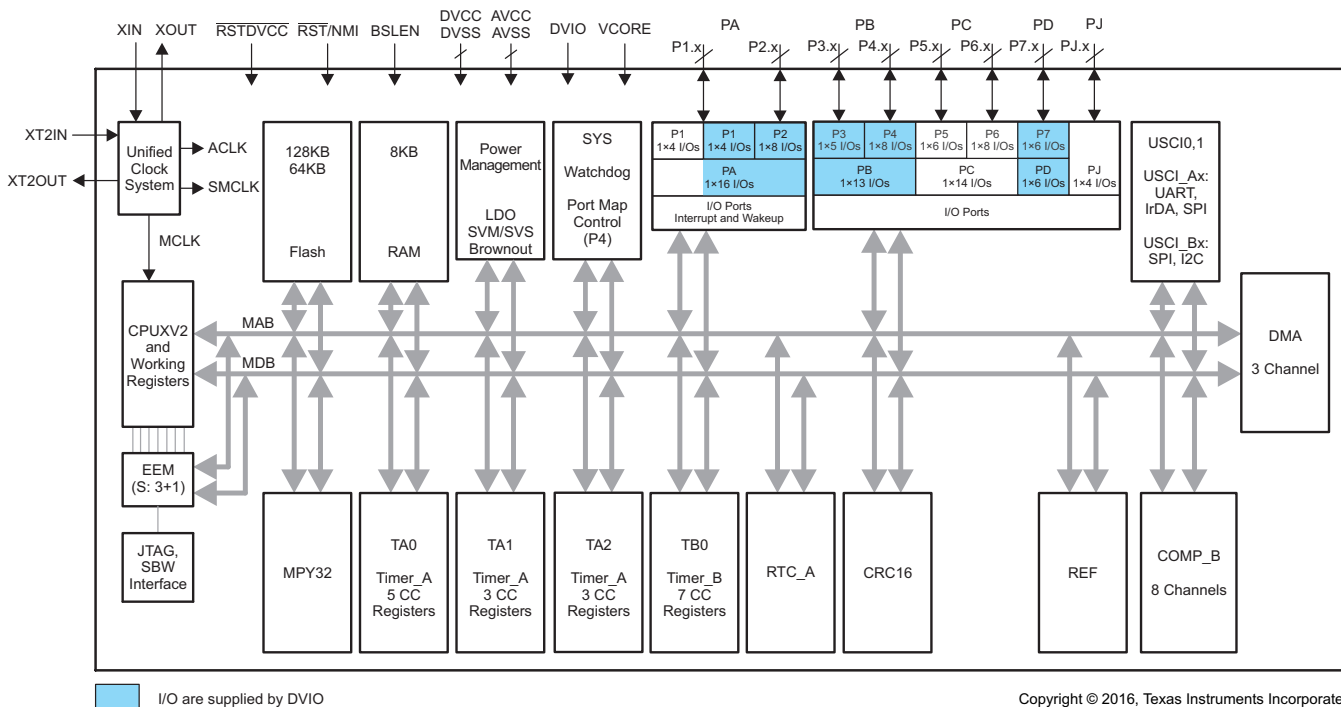


Figure 1-3. Functional Block Diagram – F5219, F5217 – RGC, ZQE, YFF Packages

Figure 1-4 shows the functional block diagram for the MSP430F5214 and MSP430F5212 devices in the RGZ package.

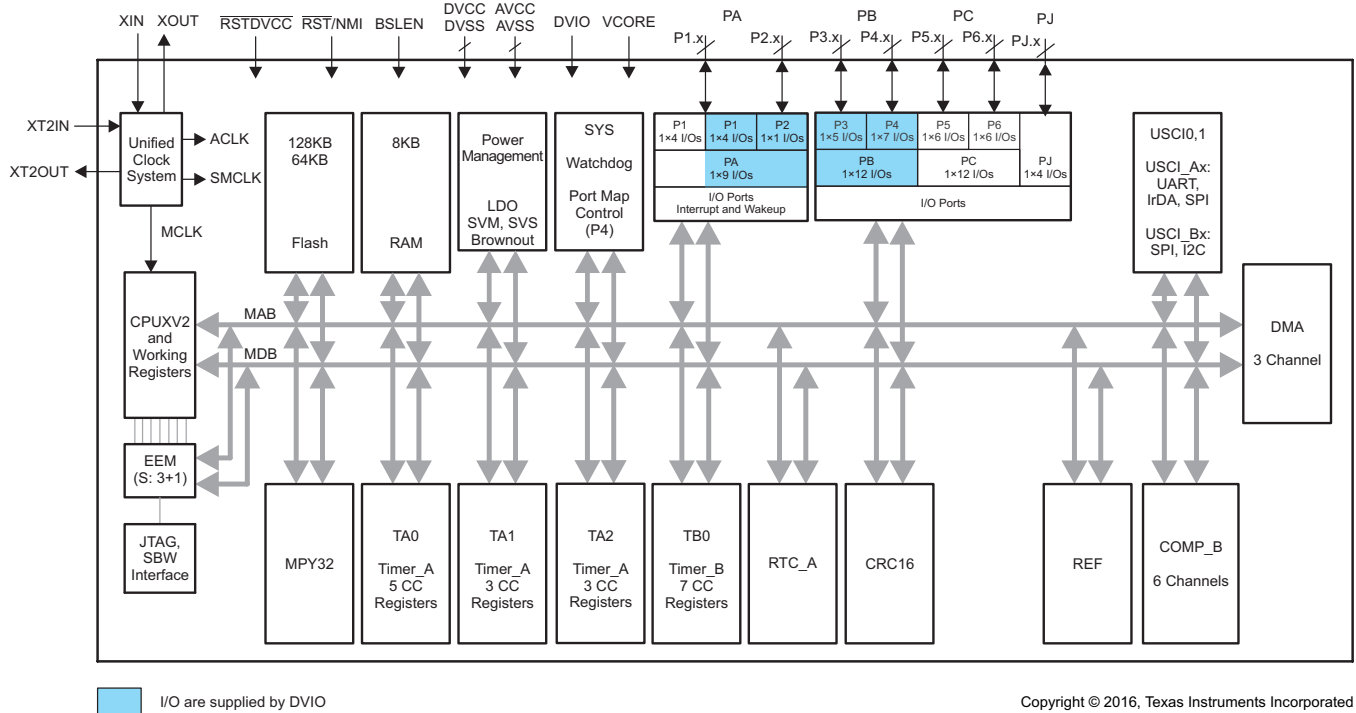


Figure 1-4. Functional Block Diagram – F5214, F5212 – RGZ Package

Table of Contents

| | | | | | |
|----------|--|-----------|----------|---|-----------|
| 1 | Device Overview | 1 | 5.18 | Output Frequency – General-Purpose I/O DVIO Domain (P1.4 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P7.0 to P7.5) | 30 |
| 1.1 | Features | 1 | 5.19 | Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0) | 31 |
| 1.2 | Applications | 2 | 5.20 | Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1) | 32 |
| 1.3 | Description | 2 | 5.21 | Crystal Oscillator, XT1, Low-Frequency Mode | 33 |
| 1.4 | Functional Block Diagrams | 3 | 5.22 | Crystal Oscillator, XT2 | 34 |
| 2 | Revision History | 8 | 5.23 | Internal Very-Low-Power Low-Frequency Oscillator (VLO) | 35 |
| 3 | Device Comparison | 9 | 5.24 | Internal Reference, Low-Frequency Oscillator (REFO) | 35 |
| 3.1 | Related Products | 9 | 5.25 | DCO Frequency | 36 |
| 4 | Terminal Configuration and Functions | 10 | 5.26 | PMM, Brownout Reset (BOR) | 37 |
| 4.1 | Pin Diagrams | 10 | 5.27 | PMM, Core Voltage | 37 |
| 4.2 | Signal Descriptions | 16 | 5.28 | PMM, SVS High Side | 38 |
| 5 | Specifications | 21 | 5.29 | PMM, SVM High Side | 39 |
| 5.1 | Absolute Maximum Ratings | 21 | 5.30 | PMM, SVS Low Side | 39 |
| 5.2 | ESD Ratings | 21 | 5.31 | PMM, SVM Low Side | 40 |
| 5.3 | Recommended Operating Conditions | 21 | 5.32 | Wake-up Times From Low-Power Modes and Reset | 40 |
| 5.4 | Active Mode Supply Current Into V _{CC} Excluding External Current | 24 | 5.33 | Timer_A | 41 |
| 5.5 | Low-Power Mode Supply Currents (Into V _{CC}) Excluding External Current | 25 | 5.34 | Timer_B | 41 |
| 5.6 | Thermal Resistance Characteristics | 26 | 5.35 | USCI (UART Mode), Recommended Operating Conditions | 42 |
| 5.7 | Schmitt-Trigger Inputs – General-Purpose I/O DVCC Domain (P1.0 to P1.3, P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3, RSTDVCC) | 27 | 5.36 | USCI (UART Mode) | 42 |
| 5.8 | Schmitt-Trigger Inputs – General-Purpose I/O DVIO Domain (P1.4 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P7.0 to P7.5, RST/NMI, BSLN) | 27 | 5.37 | USCI (SPI Master Mode), Recommended Operating Conditions | 42 |
| 5.9 | Inputs – Interrupts DVCC Domain Port P1 (P1.0 to P1.3) | 27 | 5.38 | USCI (SPI Master Mode) | 42 |
| 5.10 | Inputs – Interrupts DVIO Domain Ports P1 and P2 (P1.4 to P1.7, P2.0 to P2.7) | 27 | 5.39 | USCI (SPI Slave Mode) | 44 |
| 5.11 | Leakage Current – General-Purpose I/O DVCC Domain (P1.0 to P1.3, P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3) | 28 | 5.40 | USCI (I ² C Mode) | 46 |
| 5.12 | Leakage Current – General-Purpose I/O DVIO Domain (P1.4 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P7.0 to P7.5) | 28 | 5.41 | 10-Bit ADC, Power Supply and Input Range Conditions | 47 |
| 5.13 | Outputs – General-Purpose I/O DVCC Domain (Full Drive Strength) (P1.0 to P1.3, P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3) | 28 | 5.42 | 10-Bit ADC, Timing Parameters | 47 |
| 5.14 | Outputs – General-Purpose I/O DVCC Domain (Reduced Drive Strength) (P1.0 to P1.3, P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3) | 28 | 5.43 | 10-Bit ADC, Linearity Parameters | 48 |
| 5.15 | Outputs – General-Purpose I/O DVIO Domain (Full Drive Strength) (P1.4 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P7.0 to P7.5) | 29 | 5.44 | REF, External Reference | 48 |
| 5.16 | Outputs – General-Purpose I/O DVIO Domain (Reduced Drive Strength) (P1.4 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P7.0 to P7.5) | 29 | 5.45 | REF, Built-In Reference | 49 |
| 5.17 | Output Frequency – General-Purpose I/O DVCC Domain (P1.0 to P1.3, P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3) | 30 | 5.46 | Comparator_B | 50 |
| | | | 5.47 | Flash Memory | 51 |
| | | | 5.48 | JTAG and Spy-Bi-Wire Interface | 51 |
| | | | 5.49 | DVIO BSL Entry | 52 |
| | | | 6 | Detailed Description | 53 |
| | | | 6.1 | CPU (Link to user's guide) | 53 |
| | | | 6.2 | Operating Modes | 54 |
| | | | 6.3 | Interrupt Vector Addresses | 55 |
| | | | 6.4 | Memory Organization | 56 |
| | | | 6.5 | Bootloader (BSL) | 58 |
| | | | 6.6 | JTAG Operation | 59 |
| | | | 6.7 | Flash Memory (Link to user's guide) | 60 |
| | | | 6.8 | RAM (Link to user's guide) | 60 |
| | | | 6.9 | Peripherals | 61 |
| | | | 6.10 | Input/Output Diagrams | 82 |

| | | | | | |
|----------|---|----------------------------|----------|---|----------------------------|
| 6.11 | Device Descriptors | 99 | 7.5 | Related Links | 110 |
| 7 | Device and Documentation Support | 105 | 7.6 | Community Resources..... | 110 |
| 7.1 | Getting Started..... | 105 | 7.7 | Trademarks | 110 |
| 7.2 | Device Nomenclature | 105 | 7.8 | Electrostatic Discharge Caution | 110 |
| 7.3 | Tools and Software | 107 | 7.9 | Glossary..... | 110 |
| 7.4 | Documentation Support..... | 108 | 8 | Mechanical, Packaging, and Orderable Information | 110 |

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from June 29, 2016 to September 26, 2018 | Page |
|---|---------------------|
| • Added Section 3.1, Related Products | 9 |
| • Removed D and E dimension lines on the YFF pinout (for the package dimensions with tolerances, see the <i>Mechanical Data</i> in Section 8) | 15 |
| • Added typical conditions statements at the beginning of Section 5, Specifications | 21 |
| • Changed the MIN value of the V(DVCC_BOR_hys) parameter from 60 mV to 50 mV in Section 5.26, PMM, Brownout Reset (BOR) | 37 |
| • Updated notes (1) and (2) and added note (3) in Section 5.32, Wake-up Times From Low-Power Modes and Reset | 40 |
| • Removed ADC10DIV from the formula for the TYP value in the second row of the t _{CONVERT} parameter in Section 5.42, 10-Bit ADC, Timing Parameters (removed because ADC10CLK is after division) | 47 |
| • Added second row for t _{EN_CMP} with Test Conditions of "CBPWRMD = 10" and MAX value of 100 μs in Section 5.46, Comparator_B | 50 |
| • Renamed FCTL4.MGR0 and MGR1 in Section 5.47, Flash Memory , to be consistent with header files | 51 |
| • Throughout document, changed all instances of "bootstrap loader" to "bootloader" | 58 |
| • Replaced former section <i>Development Tools Support</i> with Section 7.3, Tools and Software | 107 |
| • Added content to Section 7.4, Documentation Support | 108 |

3 Device Comparison

Table 3-1 summarizes the available family members.

Table 3-1. Family Members⁽¹⁾⁽²⁾

| DEVICE | FLASH (KB) | SRAM (KB) | Timer_A ⁽³⁾ | Timer_B ⁽⁴⁾ | USCI | | ADC10_A (Ch) | Comp_B (Ch) | I/O DVCC ⁽⁵⁾ | I/O DVIO ⁽⁶⁾ | PACKAGE |
|-------------|------------|-----------|------------------------|------------------------|----------------------------|----------------------------------|---------------|-------------|-------------------------|-------------------------|----------------------------|
| | | | | | CHANNEL A: UART, IrDA, SPI | CHANNEL B: SPI, I ² C | | | | | |
| MSP430F5229 | 128 | 8 | 5, 3, 3 | 7 | 2 | 2 | 10 ext, 2 int | 8 | 22 | 31 | 64 RGC 64 YFF 80 ZQE |
| MSP430F5227 | 64 | 8 | 5, 3, 3 | 7 | 2 | 2 | 10 ext, 2 int | 8 | 22 | 31 | 64 RGC 64 YFF 80 ZQE |
| MSP430F5224 | 128 | 8 | 5, 3, 3 | 7 | 2 | 2 | 8 ext, 2 int | 6 | 20 | 17 | 48 RGZ |
| MSP430F5222 | 64 | 8 | 5, 3, 3 | 7 | 2 | 2 | 8 ext, 2 int | 6 | 20 | 17 | 48 RGZ |
| MSP430F5219 | 128 | 8 | 5, 3, 3 | 7 | 2 | 2 | - | 8 | 22 | 31 | 64 RGC 64 YFF 80 ZQE |
| MSP430F5217 | 64 | 8 | 5, 3, 3 | 7 | 2 | 2 | - | 8 | 22 | 31 | 64 RGC 64 YFF 80 ZQE |
| MSP430F5214 | 128 | 8 | 5, 3, 3 | 7 | 2 | 2 | - | 6 | 20 | 17 | 48 RGZ |
| MSP430F5212 | 64 | 8 | 5, 3, 3 | 7 | 2 | 2 | - | 6 | 20 | 17 | 48 RGZ |

- (1) For the most current device, package, and ordering information, see the *Package Option Addendum* in Section 8, or see the TI website at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.
- (3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (4) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (5) All of these I/Os reside on a single voltage rail supplied by DVCC.
- (6) All of these I/Os reside on a single voltage rail supplied by DVIO.

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

Products for TI Microcontrollers TI's low-power and high-performance MCUs, with wired and wireless connectivity options, are optimized for a broad range of applications.

Products for MSP430 Ultra-Low-Power Microcontrollers One platform. One ecosystem. Endless possibilities. Enabling the connected world with innovations in ultra-low-power microcontrollers with advanced peripherals for precise sensing and measurement.

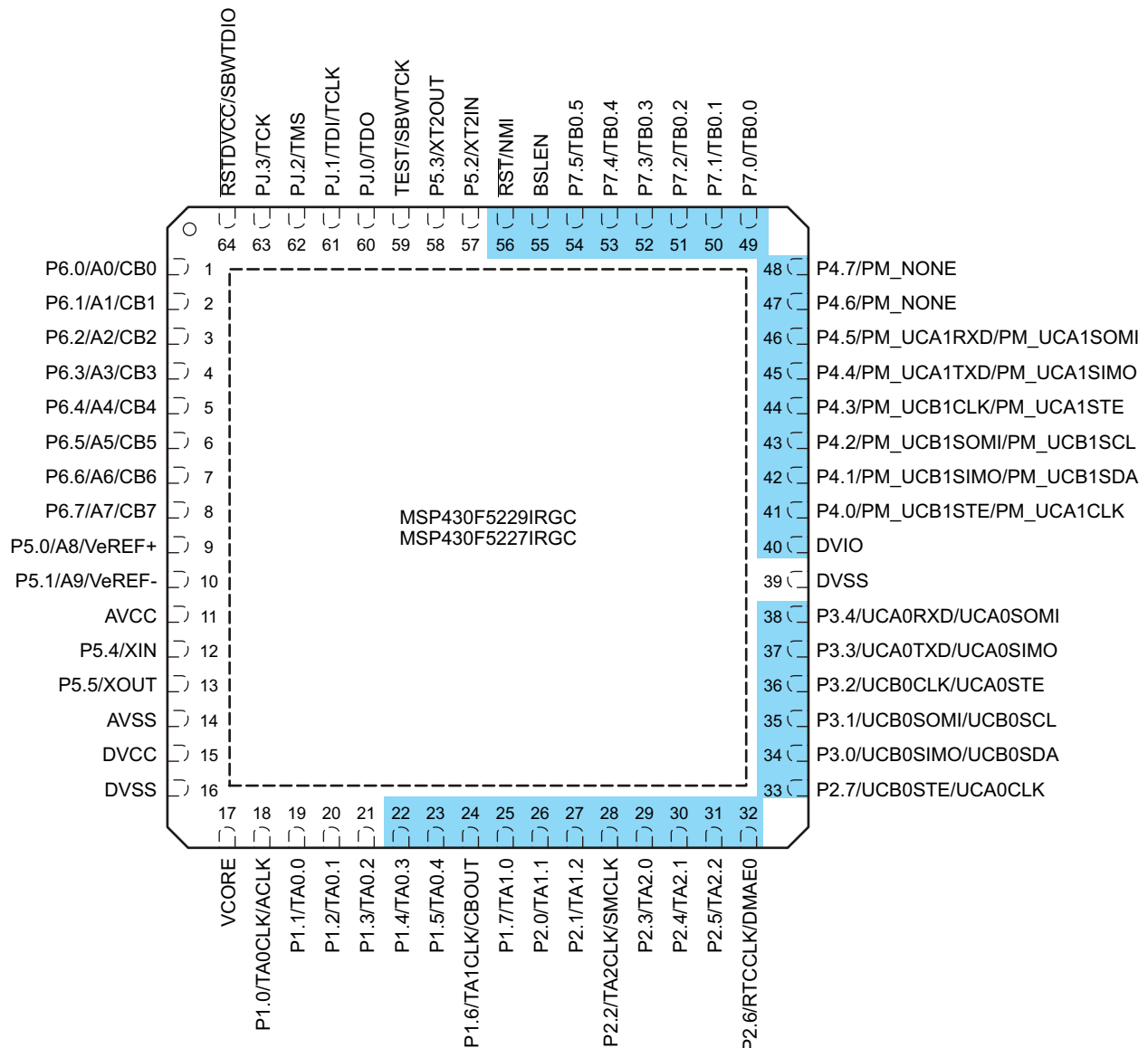
Companion Products for MSP430F5229 Review products that are frequently purchased or used with this product.

Reference Designs for MSP430F5229 Find reference designs that leverage the best in TI technology to solve your system-level challenges.

4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the pinout for the MSP430F5229 and MSP430F5227 devices in the 64-pin RGC package.

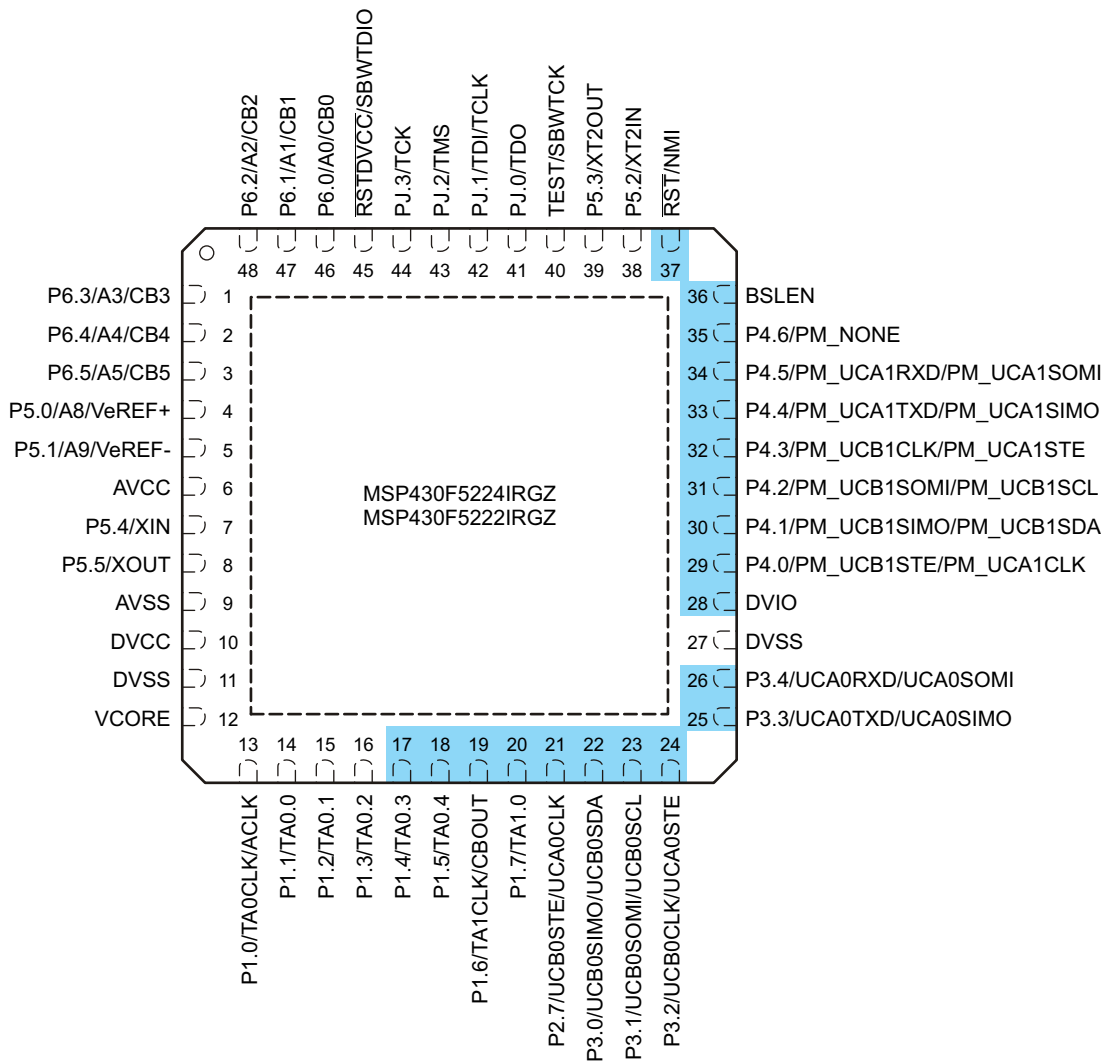


Supplied by DVIO

NOTE: TI recommends connection of exposed thermal pad to V_{SS}.

Figure 4-1. 64-Pin RGC Package – F5229, F5227

Figure 4-2 shows the pinout for the MSP430F5224 and MSP430F5222 devices in the 48-pin RGZ package.

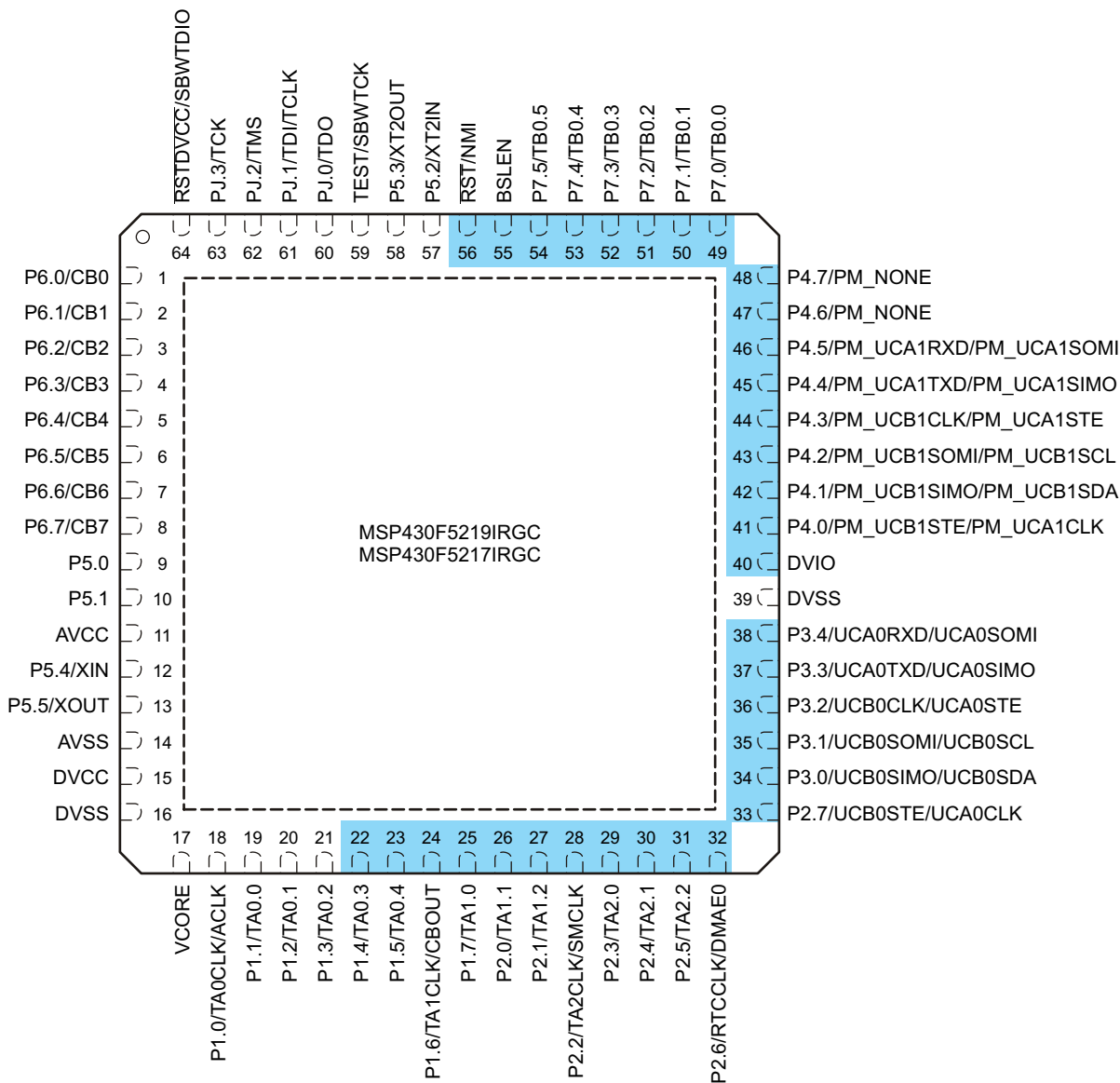


Supplied by DVIO

NOTE: TI recommends connection of exposed thermal pad to V_{SS}.

Figure 4-2. 48-Pin RGZ Package – F5224, F5222

Figure 4-3 shows the pinout for the MSP430F5219 and MSP430F5217 devices in the 64-pin RGC package.

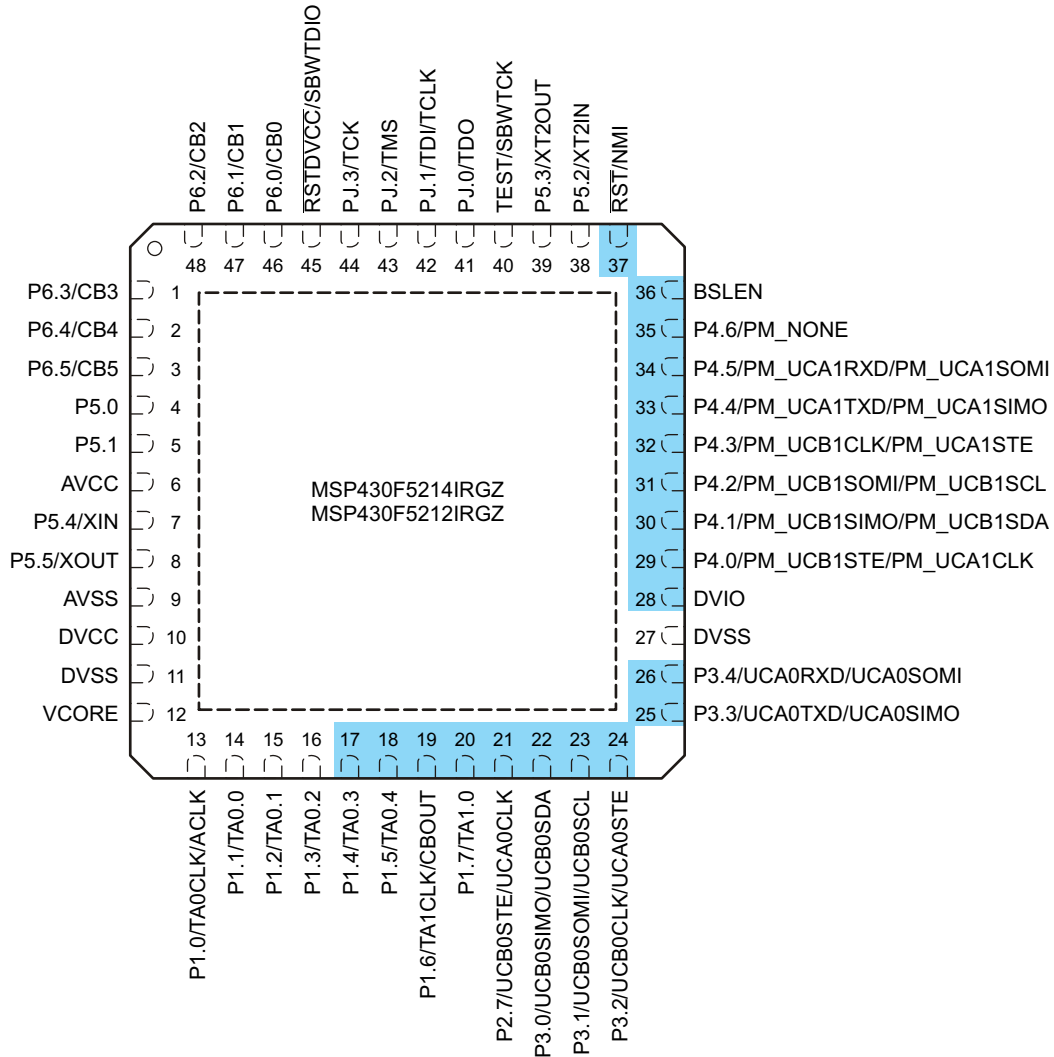


 Supplied by DVIO

NOTE: TI recommends connection of exposed thermal pad to V_{SS}.

Figure 4-3. 64-Pin RGC Package – F5219, F5217

Figure 4-4 shows the pinout for the MSP430F5214 and MSP430F5212 devices in the 48-pin RGZ package.

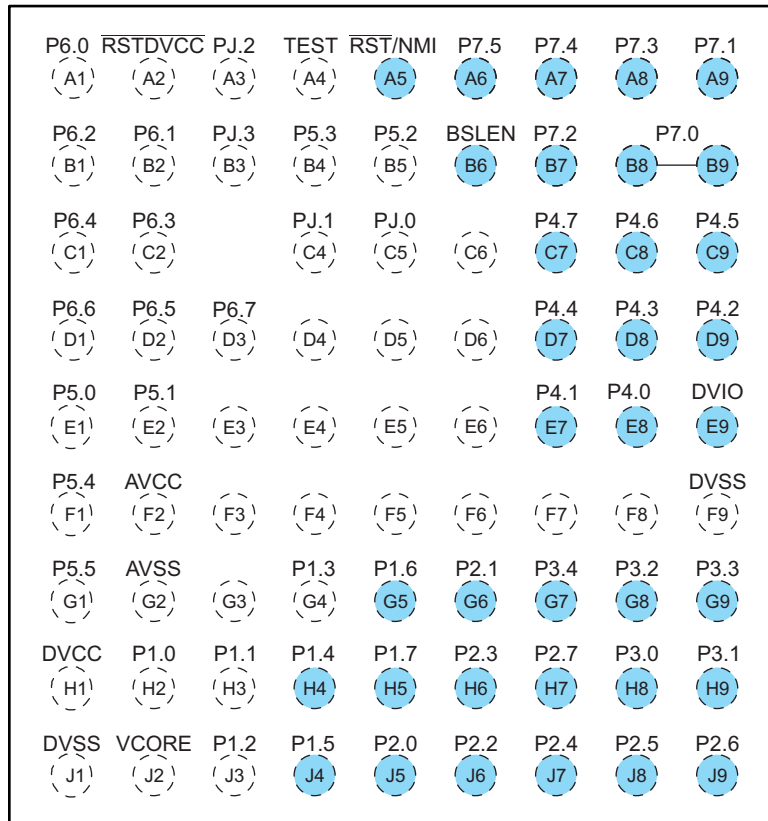


Supplied by DVIO

NOTE: TI recommends connection of exposed thermal pad to V_{SS}.

Figure 4-4. 48-Pin RGZ Package – F5214, F5212

Figure 4-5 shows the pinout for the MSP430F5229, MSP430F5227, MSP430F5219, and MSP430F5217 devices in the 80-pin ZQE package.



 Supplied by DVIO

Figure 4-5. 80-Pin ZQE Package – F5229, F5227, F5219, F5217

Figure 4-6 shows the pinout for the MSP430F5229, MSP430F5227, MSP430F5219, and MSP430F5217 devices in the 64-pin YFF package.

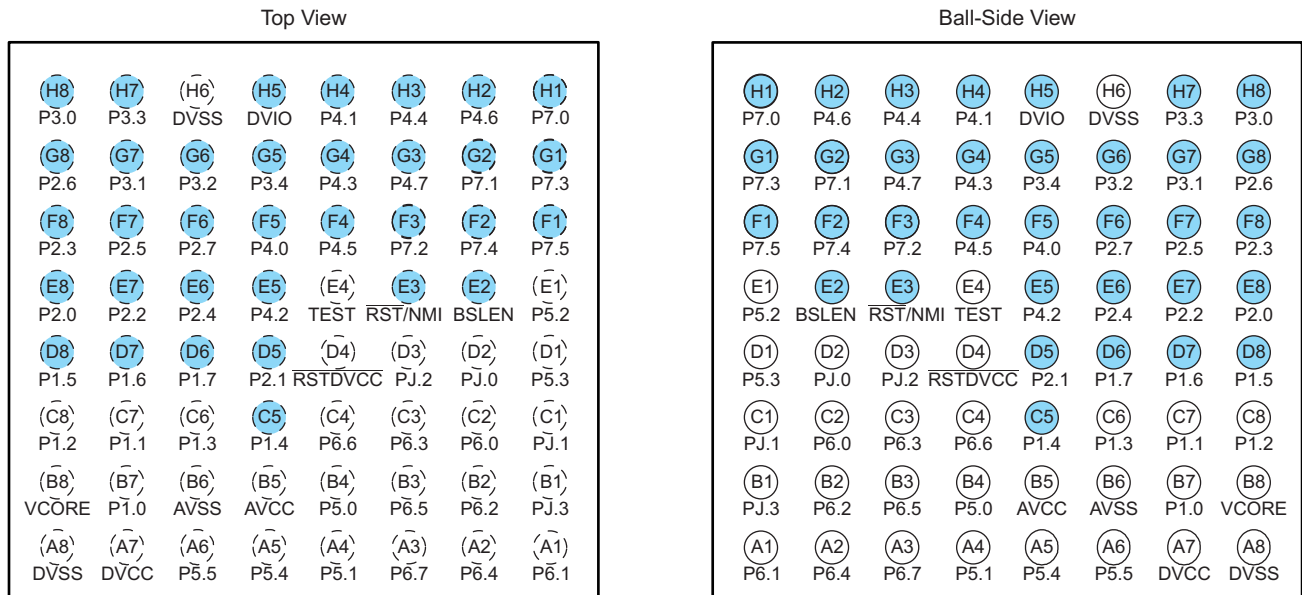


Figure 4-6. 64-Pin YFF Package – F5229, F5227, F5219, F5217

4.2 Signal Descriptions

Table 4-1 describes the signals for all device variants and package options.

Table 4-1. Terminal Functions

| NAME | TERMINAL NO. | | | | I/O ⁽¹⁾ | SUPPLY | DESCRIPTION |
|----------------|--------------|-----|-----|-----|--------------------|--------|---|
| | RGC | ZQE | YFF | RGZ | | | |
| P6.0/CB0/A0 | 1 | A1 | C2 | 46 | I/O | DVCC | General-purpose digital I/O Comparator_B input CB0 Analog input A0 for ADC (not available on all device types) |
| P6.1/CB1/A1 | 2 | B2 | A1 | 47 | I/O | DVCC | General-purpose digital I/O Comparator_B input CB1 Analog input A1 for ADC (not available on all device types) |
| P6.2/CB2/A2 | 3 | B1 | B2 | 48 | I/O | DVCC | General-purpose digital I/O Comparator_B input CB2 Analog input A2 for ADC (not available on all device types) |
| P6.3/CB3/A3 | 4 | C2 | C3 | 1 | I/O | DVCC | General-purpose digital I/O Comparator_B input CB3 Analog input A3 for ADC (not available on all device types) |
| P6.4/CB4/A4 | 5 | C1 | A2 | 2 | I/O | DVCC | General-purpose digital I/O Comparator_B input CB4 Analog input A4 for ADC (not available on all device types) |
| P6.5/CB5/A5 | 6 | D2 | B3 | 3 | I/O | DVCC | General-purpose digital I/O Comparator_B input CB5 Analog input A5 for ADC (not available on all device types) |
| P6.6/CB6/A6 | 7 | D1 | C4 | N/A | I/O | DVCC | General-purpose digital I/O (not available on all device types) Comparator_B input CB6 (not available on all device types) Analog input A6 for ADC (not available on all device types) |
| P6.7/CB7/A7 | 8 | D3 | A3 | N/A | I/O | DVCC | General-purpose digital I/O (not available on all device types) Comparator_B input CB7 (not available on all device types) Analog input A7 for ADC (not available on all device types) |
| P5.0/A8/VeREF+ | 9 | E1 | B4 | 4 | I/O | DVCC | General-purpose digital I/O Analog input A8 for ADC (not available on all device types) Input for an external reference voltage to the ADC (not available on all device types) |
| P5.1/A9/VeREF- | 10 | E2 | A4 | 5 | I/O | DVCC | General-purpose digital I/O Analog input A9 for ADC (not available on all device types) Negative terminal for the ADC reference voltage for an external applied reference voltage (not available on all device types) |
| AVCC | 11 | F2 | B5 | 6 | | | Analog power supply |
| P5.4/XIN | 12 | F1 | A5 | 7 | I/O | DVCC | General-purpose digital I/O Input terminal for crystal oscillator XT1 ⁽²⁾ |
| P5.5/XOUT | 13 | G1 | A6 | 8 | I/O | DVCC | General-purpose digital I/O Output terminal of crystal oscillator XT1 |
| AVSS | 14 | G2 | B6 | 9 | | | Analog ground supply |

(1) I = input, O = output, N/A = not available

(2) When in crystal bypass mode, XIN can be configured so that it can support an input digital waveform with swing levels from DVSS to DVCC or DVSS to DVIO. In this case, it is required that the pin be configured properly for the intended input swing.

Table 4-1. Terminal Functions (continued)

| TERMINAL | | | | | I/O ⁽¹⁾ | SUPPLY | DESCRIPTION |
|----------------------|-----|-----|-----|-----|--------------------|---------------------|--|
| NAME | NO. | | | | | | |
| | RGC | ZQE | YFF | RGZ | | | |
| DVCC | 15 | H1 | A7 | 10 | | | Digital power supply |
| DVSS | 16 | J1 | A8 | 11 | | | Digital ground supply |
| VCORE ⁽³⁾ | 17 | J2 | B8 | 12 | | DVCC | Regulated core power supply output (internal use only, no external current loading) |
| P1.0/TA0CLK/ACLK | 18 | H2 | B7 | 13 | I/O | DVCC | General-purpose digital I/O with port interrupt TA0 clock signal TA0CLK input ACLK output (divided by 1, 2, 4, 8, 16, or 32) |
| P1.1/TA0.0 | 19 | H3 | C7 | 14 | I/O | DVCC | General-purpose digital I/O with port interrupt TA0 CCR0 capture: CCI0A input, compare: Out0 output BSL transmit output |
| P1.2/TA0.1 | 20 | J3 | C8 | 15 | I/O | DVCC | General-purpose digital I/O with port interrupt TA0 CCR1 capture: CCI1A input, compare: Out1 output BSL receive input |
| P1.3/TA0.2 | 21 | G4 | C6 | 16 | I/O | DVCC | General-purpose digital I/O with port interrupt TA0 CCR2 capture: CCI2A input, compare: Out2 output |
| P1.4/TA0.3 | 22 | H4 | C5 | 17 | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O with port interrupt TA0 CCR3 capture: CCI3A input compare: Out3 output |
| P1.5/TA0.4 | 23 | J4 | D8 | 18 | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O with port interrupt TA0 CCR4 capture: CCI4A input, compare: Out4 output |
| P1.6/TA1CLK/CBOUT | 24 | G5 | D7 | 19 | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O with port interrupt TA1 clock signal TA1CLK input Comparator_B output |
| P1.7/TA1.0 | 25 | H5 | D6 | 20 | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O with port interrupt TA1 CCR0 capture: CCI0A input, compare: Out0 output |
| P2.0/TA1.1 | 26 | J5 | E8 | N/A | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O with port interrupt (not available on all device types) TA1 CCR1 capture: CCI1A input, compare: Out1 output (not available on all device types) |
| P2.1/TA1.2 | 27 | G6 | D5 | N/A | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O with port interrupt (not available on all device types) TA1 CCR2 capture: CCI2A input, compare: Out2 output (not available on all device types) |
| P2.2/TA2CLK/SMCLK | 28 | J6 | E7 | N/A | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O with port interrupt (not available on all device types) TA2 clock signal TA2CLK input SMCLK output (not available on all device types) |
| P2.3/TA2.0 | 29 | H6 | F8 | N/A | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O with port interrupt (not available on all device types) TA2 CCR0 capture: CCI0A input, compare: Out0 output (not available on all device types) |
| P2.4/TA2.1 | 30 | J7 | E6 | N/A | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O with port interrupt (not available on all device types) TA2 CCR1 capture: CCI1A input, compare: Out1 output (not available on all device types) |

(3) V_{CORE} is for internal use only. No external current loading is possible. V_{CORE} should only be connected to the recommended capacitor value, C_{V_{CORE}}.

(4) This pin function is supplied by DVIO. See Section 5.8 for input and output requirements.

Table 4-1. Terminal Functions (continued)

| TERMINAL | | | | | I/O ⁽¹⁾ | SUPPLY | DESCRIPTION |
|---------------------------------|-----|-----|-----|-----|--------------------|---------------------|--|
| NAME | NO. | | | | | | |
| | RGC | ZQE | YFF | RGZ | | | |
| P2.5/TA2.2 | 31 | J8 | F7 | N/A | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O with port interrupt (not available on all device types) TA2 CCR2 capture: CCI2A input, compare: Out2 output (not available on all device types) |
| P2.6/RTCCLK/DMAE0 | 32 | J9 | G8 | N/A | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O with port interrupt (not available on all device types) RTC clock output for calibration (not available on all device types) DMA external trigger input (not available on all device types) |
| P2.7/UCB0STE/ UCA0CLK | 33 | H7 | F6 | 21 | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O Slave transmit enable – USCI_B0 SPI mode Clock signal input – USCI_A0 SPI slave mode Clock signal output – USCI_A0 SPI master mode |
| P3.0/UCB0SIMO/ UCB0SDA | 34 | H8 | H8 | 22 | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O Slave in, master out – USCI_B0 SPI mode I ² C data – USCI_B0 I ² C mode |
| P3.1/UCB0SOMI/ UCB0SCL | 35 | H9 | G7 | 23 | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O Slave out, master in – USCI_B0 SPI mode I ² C clock – USCI_B0 I ² C mode |
| P3.2/UCB0CLK/ UCA0STE | 36 | G8 | G6 | 24 | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O Clock signal input – USCI_B0 SPI slave mode Clock signal output – USCI_B0 SPI master mode Slave transmit enable – USCI_A0 SPI mode |
| P3.3/UCA0TXD/ UCA0SIMO | 37 | G9 | H7 | 25 | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O Transmit data – USCI_A0 UART mode Slave in, master out – USCI_A0 SPI mode |
| P3.4/UCA0RXD/ UCA0SOMI | 38 | G7 | G5 | 26 | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O Receive data – USCI_A0 UART mode Slave out, master in – USCI_A0 SPI mode |
| DVSS | 39 | F9 | H6 | 27 | | | Digital ground supply |
| DVIO ⁽⁵⁾ | 40 | E9 | H5 | 28 | | | Digital I/O power supply |
| P4.0/PM_UCB1STE/ PM_UCA1CLK | 41 | E8 | F5 | 29 | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave transmit enable – USCI_B1 SPI mode Default mapping: Clock signal input – USCI_A1 SPI slave mode Default mapping: Clock signal output – USCI_A1 SPI master mode |
| P4.1/PM_UCB1SIMO/ PM_UCB1SDA | 42 | E7 | H4 | 30 | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave in, master out – USCI_B1 SPI mode Default mapping: I ² C data – USCI_B1 I ² C mode |
| P4.2/PM_UCB1SOMI/ PM_UCB1SCL | 43 | D9 | E5 | 31 | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave out, master in – USCI_B1 SPI mode Default mapping: I ² C clock – USCI_B1 I ² C mode |

(5) The voltage on DVIO is not supervised or monitored.

Table 4-1. Terminal Functions (continued)

| TERMINAL | | | | | I/O ⁽¹⁾ | SUPPLY | DESCRIPTION |
|---------------------------------|-----|-----------|-----|-----|--------------------|---------------------|--|
| NAME | NO. | | | | | | |
| | RGC | ZQE | YFF | RGZ | | | |
| P4.3/PM_UCB1CLK/ PM_UCA1STE | 44 | D8 | G4 | 32 | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Clock signal input – USCI_B1 SPI slave mode Default mapping: Clock signal output – USCI_B1 SPI master mode Default mapping: Slave transmit enable – USCI_A1 SPI mode |
| P4.4/PM_UCA1TXD/ PM_UCA1SIMO | 45 | D7 | H3 | 33 | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Transmit data – USCI_A1 UART mode Default mapping: Slave in, master out – USCI_A1 SPI mode |
| P4.5/PM_UCA1RXD/ PM_UCA1SOMI | 46 | C9 | F4 | 34 | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Receive data – USCI_A1 UART mode Default mapping: Slave out, master in – USCI_A1 SPI mode |
| P4.6/PM_NONE | 47 | C8 | H2 | 35 | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: no secondary function |
| P4.7/PM_NONE | 48 | C7 | G3 | N/A | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O with reconfigurable port mapping secondary function (not available on all device types) Default mapping: no secondary function (not available on all device types) |
| P7.0/TB0.0 | 49 | B8, B9 | H1 | N/A | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O (not available on all device types) TB0 CCR0 capture: CCI0A input, compare: Out0 output (not available on all device types) |
| P7.1/TB0.1 | 50 | A9 | G2 | N/A | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O (not available on all device types) TB0 CCR1 capture: CCI1A input, compare: Out1 output (not available on all device types) |
| P7.2/TB0.2 | 51 | B7 | F3 | N/A | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O (not available on all device types) TB0 CCR2 capture: CCI2A input, compare: Out2 output (not available on all device types) |
| P7.3/TB0.3 | 52 | A8 | G1 | N/A | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O (not available on all device types) TB0 CCR3 capture: CCI3A input, compare: Out3 output (not available on all device types) |
| P7.4/TB0.4 | 53 | A7 | F2 | N/A | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O (not available on all device types) TB0 CCR4 capture: CCI4A input, compare: Out4 output (not available on all device types) |
| P7.5/TB0.5 | 54 | A6 | F1 | N/A | I/O | DVIO ⁽⁴⁾ | General-purpose digital I/O (not available on all device types) TB0 CCR5 capture: CCI5A input, compare: Out5 output (not available on all device types) |
| BSLEN | 55 | B6 | E2 | 36 | I | DVIO ⁽⁴⁾ | BSL enable with internal pulldown |
| $\overline{\text{RST}}$ /NMI | 56 | A5 | E3 | 37 | I | DVIO ⁽⁴⁾ | Reset input active low ⁽⁶⁾⁽⁷⁾ Nonmaskable interrupt input ⁽⁶⁾ |
| P5.2/XT2IN | 57 | B5 | E1 | 38 | I/O | DVCC | General-purpose digital I/O Input terminal for crystal oscillator XT2 ⁽⁸⁾ |

(6) This pin is configurable as reset or NMI and resides on the DVIO supply domain. When driven from external, input swing levels from DVSS to DVIO are required.

(7) When this pin is configured as reset, the internal pullup resistor is enabled by default.

(8) When in crystal bypass mode, XT2IN can be configured so that it can support an input digital waveform with swing levels from DVSS to DVCC or DVSS to DVIO. In this case, it is required that the pin be configured properly for the intended input swing.

Table 4-1. Terminal Functions (continued)

| TERMINAL | | | | | I/O ⁽¹⁾ | SUPPLY | DESCRIPTION |
|--|-----|-----------------|-----|-----|--------------------|--------|--|
| NAME | NO. | | | | | | |
| | RGC | ZQE | YFF | RGZ | | | |
| P5.3/XT2OUT | 58 | B4 | D1 | 39 | I/O | DVCC | General-purpose digital I/O Output terminal of crystal oscillator XT2 |
| TEST/SBWTK ⁽⁹⁾ | 59 | A4 | E4 | 40 | I | DVCC | Test mode pin – Selects four wire JTAG operation Spy-Bi-Wire input clock when Spy-Bi-Wire operation activated |
| PJ.0/TDO ⁽¹⁰⁾ | 60 | C5 | D2 | 41 | I/O | DVCC | General-purpose digital I/O JTAG test data output port |
| PJ.1/TDI/TCLK ⁽¹⁰⁾ | 61 | C4 | C1 | 42 | I/O | DVCC | General-purpose digital I/O JTAG test data input or test clock input |
| PJ.2/TMS ⁽¹⁰⁾ | 62 | A3 | D3 | 43 | I/O | DVCC | General-purpose digital I/O JTAG test mode select |
| PJ.3/TCK ⁽¹⁰⁾ | 63 | B3 | B1 | 44 | I/O | DVCC | General-purpose digital I/O JTAG test clock |
| $\overline{\text{RST}}\text{DVCC}/$ SBWTDIO ⁽¹⁰⁾ | 64 | A2 | D4 | 45 | I/O | DVCC | Reset input, active-low ⁽¹¹⁾ Spy-Bi-Wire data input/output when Spy-Bi-Wire operation activated |
| Reserved | N/A | ⁽¹²⁾ | N/A | N/A | | | Reserved |
| QFN Pad | Pad | N/A | N/A | Pad | | | QFN thermal pad. TI recommends connecting to V _{SS} . |

(9) See [Section 6.5](#) and [Section 6.6](#) for use with BSL and JTAG functions.

(10) See [Section 6.6](#) for use with JTAG function.

(11) This nonconfigurable reset resides on the DVCC supply domain and has an internal pullup to DVCC. When driven from external, input swing levels from DVSS to DVCC are required. This reset must be used for Spy-Bi-Wire communication and is not the same $\overline{\text{RST}}/\text{NMI}$ reset as found on other devices in the MSP430 family. See [Section 6.5](#) and [Section 6.6](#) for details regarding the use of this pin.

(12) C6, D4, D5, D6, E3, E4, E5, E6, F3, F4, F5, F6, F7, F8, G3 are reserved and should be connected to ground.

5 Specifications

All graphs in this section are for typical conditions, unless otherwise noted.

Typical (TYP) values are specified at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$, unless otherwise noted.

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | MIN | MAX | UNIT |
|---|------|----------------|------|
| Voltage applied at V_{CC} to V_{SS} | -0.3 | 4.1 | V |
| Voltage applied at V_{IO} to V_{SS} | -0.3 | 2.2 | V |
| Voltage applied to any pin (excluding V _{CORE} and V_{IO} pins) ⁽²⁾ | -0.3 | $V_{CC} + 0.3$ | V |
| Voltage applied to V_{IO} pins | -0.3 | $V_{IO} + 0.2$ | V |
| Diode current at any device pin | | ±2 | mA |
| Storage temperature, T_{stg} ⁽³⁾ | -55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages referenced to V_{SS} . V_{CORE} is for internal device use only. No external DC loading or voltage should be applied.

(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

| | | VALUE | UNIT |
|-------------------------------------|--|-------|------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±1000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|----------------------|--|------------------------------------|-----|------|------|
| V_{CC} | Supply voltage during program execution and flash programming ($AVCC = DVCC$) ⁽¹⁾⁽²⁾⁽³⁾ | PMMCOREV _x = 0 | 1.8 | 3.6 | V |
| | | PMMCOREV _x = 0, 1 | 2.0 | 3.6 | |
| | | PMMCOREV _x = 0, 1, 2 | 2.2 | 3.6 | |
| | | PMMCOREV _x = 0, 1, 2, 3 | 2.4 | 3.6 | |
| V_{IO} | Supply voltage applied to DVIO referenced to V_{SS} ⁽²⁾ | 1.62 | | 1.98 | V |
| V_{SS} | Supply voltage ($AVSS = DVSS$) | | 0 | | V |
| T_A | Operating free-air temperature | -40 | | 85 | °C |
| T_J | Operating junction temperature | -40 | | 85 | °C |
| C_{VCORE} | Recommended capacitor at V _{CORE} ⁽⁴⁾ | | 470 | | nF |
| C_{DVCC}/C_{VCORE} | Capacitor ratio of DVCC to V _{CORE} | 10 | | | |

(1) TI recommends powering AVCC and DVCC from the same source. A maximum difference of 0.3 V between AVCC and DVCC can be tolerated during power up and operation.

(2) During V_{CC} and V_{IO} power up, it is required that $V_{IO} \geq V_{CC}$ during the ramp up phase of V_{IO} . During V_{CC} and V_{IO} power down, it is required that $V_{IO} \geq V_{CC}$ during the ramp down phase of V_{IO} (see [Figure 5-1](#)).

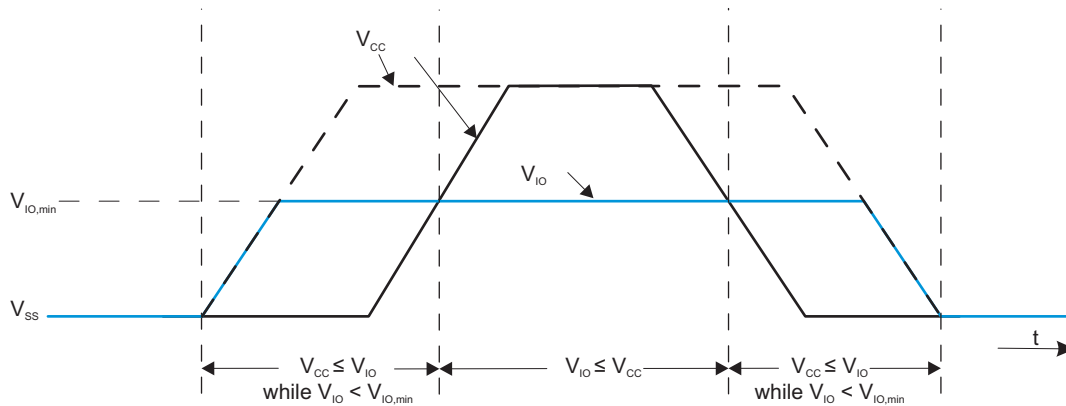
(3) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the [Section 5.28](#) threshold parameters for the exact values and further details.

(4) A capacitor tolerance of ±20% or better is required.

Recommended Operating Conditions (continued)

| | | MIN | NOM | MAX | UNIT |
|---------------------|---|--|-----|-----|------|
| f _{SYSTEM} | Processor frequency (maximum MCLK frequency) ⁽⁵⁾ (see Figure 5-3) | PMMCOREVx = 0 (default condition), 1.8 V ≤ V _{CC} ≤ 3.6 V | 0 | 8 | MHz |
| | | PMMCOREVx = 1, 2.0 V ≤ V _{CC} ≤ 3.6 V | 0 | 12 | |
| | | PMMCOREVx = 2, 2.2 V ≤ V _{CC} ≤ 3.6 V | 0 | 20 | |
| | | PMMCOREVx = 3, 2.4 V ≤ V _{CC} ≤ 3.6 V | 0 | 25 | |

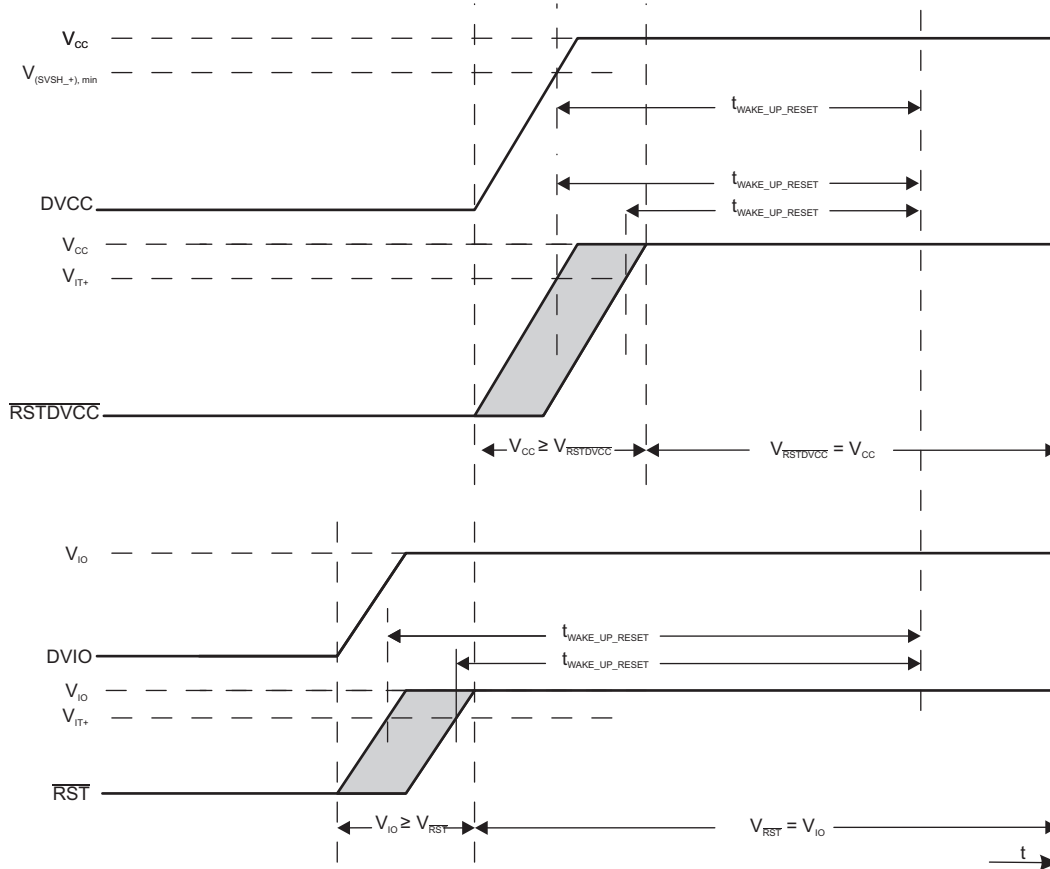
(5) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



NOTE: The device supports continuous operation with V_{CC} = V_{SS} while V_{IO} is fully within its specification. During this time, the general-purpose I/Os that reside on the V_{IO} supply domain are configured as inputs and pulled down to V_{SS} through their internal pulldown resistors. $\overline{\text{RST}}/\text{NMI}$ is high impedance. BSLEN is configured as an input and is pulled down to V_{SS} through its internal pulldown resistor. When V_{CC} reaches above the BOR threshold, the general-purpose I/Os become high-impedance inputs (no resistor enabled), $\overline{\text{RST}}/\text{NMI}$ becomes an input pulled up to V_{IO} through its internal pullup resistor, and BSLEN remains pulled down to V_{SS} through its internal pulldown resistor.

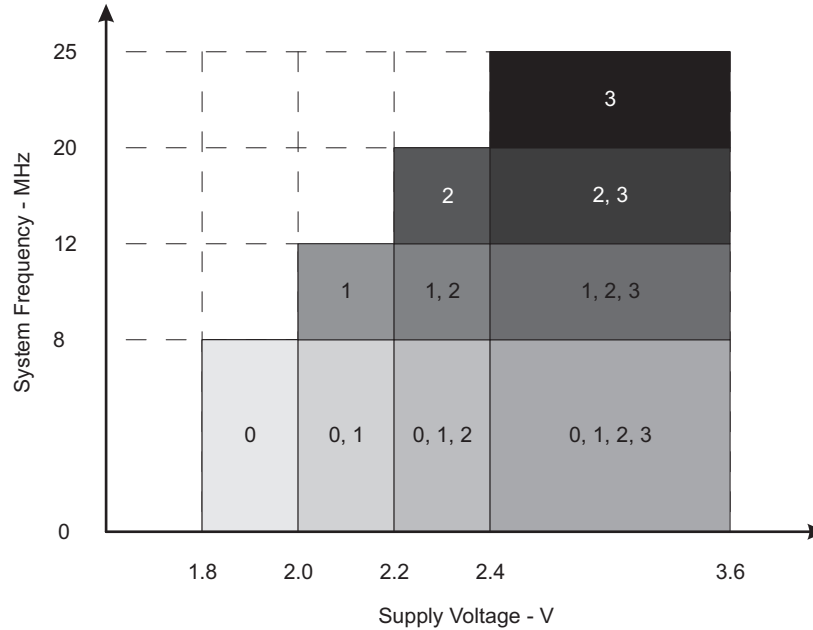
NOTE: Under certain conditions during the rising transition of V_{CC}, the general-purpose I/Os residing on the V_{IO} supply domain may actively transition high momentarily before settling to high-impedance inputs. These voltage transitions are temporary (typically resolving to high-impedance inputs when V_{CC} exceeds approximately 0.9 V) and are bounded by the V_{IO} supply.

Figure 5-1. V_{CC} and V_{IO} Power Sequencing



NOTE: The device remains in reset based on the conditions of the $\overline{\text{RSTDVCC}}$ and $\overline{\text{RST}}$ pins and the voltage present on DVCC voltage supply. If $\overline{\text{RSTDVCC}}$ or $\overline{\text{RST}}$ is held at a logic low or if DVCC is below the SVSH₊ minimum threshold, the device remains in its reset condition; that is, these conditions form a logical OR with respect to device reset.

Figure 5-2. Reset Timing



NOTE: The numbers within the fields denote the supported PMMCOREVx settings.

Figure 5-3. Maximum System Frequency

5.4 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)⁽¹⁾ ⁽²⁾ ⁽³⁾

| PARAMETER | EXECUTION MEMORY | V_{CC} | PMMCOREVx | FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$) | | | | | | | | | | UNIT |
|-----------------|------------------|----------|-----------|--|------|-------|------|--------|-----|--------|-----|--------|------|------|
| | | | | 1 MHz | | 8 MHz | | 12 MHz | | 20 MHz | | 25 MHz | | |
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{AM, Flash}$ | Flash | 3.0 V | 0 | 0.36 | 0.47 | 2.32 | 2.60 | | | | | | | mA |
| | | | 1 | 0.40 | | 2.65 | | 4.0 | 4.4 | | | | | |
| | | | 2 | 0.44 | | 2.90 | | 4.3 | | 7.1 | 7.7 | | | |
| | | | 3 | 0.46 | | 3.10 | | 4.6 | | 7.6 | | 10.1 | 11.0 | |
| $I_{AM, RAM}$ | RAM | 3.0 V | 0 | 0.20 | 0.29 | 1.20 | 1.30 | | | | | | | mA |
| | | | 1 | 0.22 | | 1.35 | | 2.0 | 2.2 | | | | | |
| | | | 2 | 0.24 | | 1.50 | | 2.2 | | 3.7 | 4.2 | | | |
| | | | 3 | 0.26 | | 1.60 | | 2.4 | | 3.9 | | 5.3 | 6.2 | |

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.

(3) Characterized with program executing typical data processing.

$f_{ACLK} = 32786$ Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.

XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0.

5.5 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

 over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾⁽²⁾

| PARAMETER | V_{CC} | PMMCOREVx | -40°C | | 25°C | | 60°C | | 85°C | | UNIT |
|---|----------|-----------|-------|-----|------|-----|------|-----|------|------|---------|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM0,1MHz}$ Low-power mode 0 ⁽³⁾⁽⁴⁾ | 2.2 V | 0 | 73 | | 77 | 91 | 80 | | 85 | 97 | μA |
| | 3.0 V | 3 | 79 | | 83 | 99 | 88 | | 95 | 107 | |
| I_{LPM2} Low-power mode 2 ⁽⁵⁾⁽⁴⁾ | 2.2 V | 0 | 6.5 | | 6.5 | 12 | 10 | | 11 | 17 | μA |
| | 3.0 V | 3 | 7.0 | | 7.0 | 13 | 11 | | 12 | 18 | |
| $I_{LPM3,XT1LF}$ Low-power mode 3, crystal mode ⁽⁶⁾⁽⁴⁾ | 2.2 V | 0 | 1.60 | | 1.90 | | 2.8 | | 6.0 | | μA |
| | | 1 | 1.65 | | 2.00 | | 3.0 | | 6.3 | | |
| | | 2 | 1.75 | | 2.15 | | 3.2 | | 6.6 | | |
| | 3.0 V | 0 | 1.8 | | 2.1 | 2.9 | 3.0 | | 6.2 | 9.4 | |
| | | 1 | 1.9 | | 2.3 | | 3.2 | | 6.5 | | |
| | | 2 | 2.0 | | 2.4 | | 3.3 | | 6.8 | | |
| $I_{LPM3,VLO}$ Low-power mode 3, VLO mode ⁽⁷⁾⁽⁴⁾ | 3.0 V | 3 | 2.0 | | 2.5 | 3.9 | 3.4 | | 6.8 | 10.9 | |
| | | 0 | 1.1 | | 1.4 | 2.7 | 2.0 | | 6.1 | 9.7 | |
| | | 1 | 1.1 | | 1.4 | | 2.2 | | 6.4 | | |
| | | 2 | 1.2 | | 1.5 | | 2.3 | | 6.8 | | |
| I_{LPM4} Low-power mode 4 ⁽⁸⁾⁽⁴⁾ | 3.0 V | 3 | 1.3 | | 1.6 | 3.0 | 2.3 | | 6.8 | 10.9 | |
| | | 0 | 0.9 | | 1.1 | 1.5 | 2.0 | | 5.1 | 8.8 | |
| | | 1 | 1.1 | | 1.2 | | 2.1 | | 5.3 | | |
| $I_{LPM4.5}$ Low-power mode 4.5 ⁽⁹⁾ | 3.0 V | 2 | 1.2 | | 1.2 | | 2.2 | | 5.5 | | |
| | | 3 | 1.3 | | 1.3 | 1.6 | 2.2 | | 5.5 | 9.8 | |
| I_{DVIO_START} Current supplied from DVIO while DVCC = AVCC = 0 V, DVIO = 1.62 V to 1.98 V, All DVIO I/O floating including BSLN and RST/NMI | 0 V | | 1.8 | | 1.8 | | 1.8 | | 1.8 | | μA |

- (1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
- (3) Current for the watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), $f_{ACLK} = 32768$ Hz, $f_{MCLK} = 0$ MHz, $f_{SMCLK} = f_{DCO} = 1$ MHz
- (4) Current for brownout and high-side supervisor (SVSH) normal mode included. Low-side supervisor (SVSL) and low-side monitor (SVM_L) disabled. High-side monitor (SVM_H) disabled. RAM retention enabled.
- (5) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2), $f_{ACLK} = 32768$ Hz, $f_{MCLK} = 0$ MHz, $f_{SMCLK} = f_{DCO} = 0$ MHz; DCO setting = 1 MHz operation, DCO bias generator enabled.)
- (6) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK} = 32768$ Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO} = 0$ MHz
- (7) Current for watchdog timer and RTC clocked by ACLK included. ACLK = VLO. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK} = f_{VLO}$, $f_{MCLK} = f_{SMCLK} = f_{DCO} = 0$ MHz
- (8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4), $f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$ MHz
- (9) Internal regulator disabled. No data retention. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5), $f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$ MHz

5.6 Thermal Resistance Characteristics

| THERMAL METRIC ⁽¹⁾ | | VALUE ⁽²⁾ | UNIT | |
|-------------------------------|--|----------------------|--------------------|------|
| R _{θJA} | Junction-to-ambient thermal resistance, still air | VQFN 48 (RGZ) | 27.8 | °C/W |
| | | VQFN 64 (RGC) | 29.6 | |
| | | DSBGA 64 (YFF) | 44.3 | |
| | | BGA 80 (ZQE) | 35.2 | |
| R _{θJC(TOP)} | Junction-to-case (top) thermal resistance | VQFN 48 (RGZ) | 13.6 | °C/W |
| | | VQFN 64 (RGC) | 14.8 | |
| | | DSBGA 64 (YFF) | 0.2 | |
| | | BGA 80 (ZQE) | 17.6 | |
| R _{θJC(BOTTOM)} | Junction-to-case (bottom) thermal resistance | VQFN 48 (RGZ) | 0.9 | °C/W |
| | | VQFN 64 (RGC) | 1.4 | |
| | | DSBGA 64 (YFF) | N/A ⁽³⁾ | |
| | | BGA 80 (ZQE) | N/A | |
| R _{θJB} | Junction-to-board thermal resistance | VQFN 48 (RGZ) | 4.7 | °C/W |
| | | VQFN 64 (RGC) | 8.5 | |
| | | DSBGA 64 (YFF) | 6.0 | |
| | | BGA 80 (ZQE) | 16.7 | |
| Ψ _{JT} | Junction-to-package-top thermal characterization parameter | VQFN 48 (RGZ) | 0.2 | °C/W |
| | | VQFN 64 (RGC) | 0.2 | |
| | | DSBGA 64 (YFF) | 0.6 | |
| | | BGA 80 (ZQE) | 0.3 | |
| Ψ _{JB} | Junction-to-board thermal characterization parameter | VQFN 48 (RGZ) | 4.7 | °C/W |
| | | VQFN 64 (RGC) | 8.4 | |
| | | DSBGA 64 (YFF) | 6.0 | |
| | | BGA 80 (ZQE) | 9.6 | |

- (1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).
- (2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [R_{θJC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
 - JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
 - JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
 - JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*
- (3) N/A = not applicable

5.7 Schmitt-Trigger Inputs – General-Purpose I/O DVCC Domain⁽¹⁾ (P1.0 to P1.3, P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3, RSTDVCC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------|---|--|-----------------|------|-----|------|------|
| V _{IT+} | Positive-going input threshold voltage | | 1.8 V | 0.80 | | 1.40 | V |
| | | | 3 V | 1.50 | | 2.10 | |
| V _{IT-} | Negative-going input threshold voltage | | 1.8 V | 0.45 | | 1.00 | V |
| | | | 3 V | 0.75 | | 1.65 | |
| V _{hys} | Input voltage hysteresis (V _{IT+} – V _{IT-}) | | 1.8 V | 0.3 | | 0.8 | V |
| | | | 3 V | 0.4 | | 1.0 | |
| R _{Pull} | Pullup or pulldown resistor ⁽²⁾ | For pullup: V _{IN} = V _{SS} , For pulldown: V _{IN} = V _{CC} | | 20 | 35 | 50 | kΩ |
| C _I | Input capacitance | V _{IN} = V _{SS} or V _{CC} | | | 5 | | pF |

(1) Same parametrics apply to clock input pin when crystal bypass mode is used on XT1 (XIN) or XT2 (XT2IN).

(2) RSTDVCC has a fixed pullup resistor that cannot be disabled.

5.8 Schmitt-Trigger Inputs – General-Purpose I/O DVIO Domain (P1.4 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P7.0 to P7.5, $\overline{\text{RST}}$ /NMI, BLEN)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{IO} | MIN | TYP | MAX | UNIT |
|-------------------|---|--|------------------|-----|-----|------|------|
| V _{IT+} | Positive-going input threshold voltage | V _{CC} = 3.0 V | 1.62 V | 0.8 | | 1.25 | V |
| | | | 1.98 V | 1.1 | | 1.40 | |
| V _{IT-} | Negative-going input threshold voltage | V _{CC} = 3.0 V | 1.62 V | 0.3 | | 0.7 | V |
| | | | 1.98 V | 0.5 | | 1.0 | |
| V _{hys} | Input voltage hysteresis (V _{IT+} – V _{IT-}) | V _{CC} = 3.0 V | 1.62 V to 1.98 V | 0.3 | | 0.8 | V |
| R _{Pull} | Pullup or pulldown resistor ⁽¹⁾ | For pullup: V _{IN} = V _{SS} , For pulldown: V _{IN} = V _{IO} | | 20 | 35 | 50 | kΩ |
| C _I | Input capacitance | V _{IN} = V _{SS} or V _{IO} | | | 5 | | pF |

(1) Also applies to $\overline{\text{RST}}$ pin when pullup or pulldown resistor is enabled.

5.9 Inputs – Interrupts DVCC Domain Port P1 (P1.0 to P1.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|--------------------|--|---|------------|-----|------|
| t _(int) | External interrupt timing ⁽¹⁾ | External trigger pulse duration to set interrupt flag | 1.8 V, 3 V | 20 | ns |

(1) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_(int) is met. It may be set by trigger signals shorter than t_(int).

5.10 Inputs – Interrupts DVIO Domain Ports P1 and P2 (P1.4 to P1.7, P2.0 to P2.7)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{IO} ⁽¹⁾ | MIN | MAX | UNIT |
|--------------------|--|--|------------------|-----|------|
| t _(int) | External interrupt timing ⁽²⁾ | External trigger pulse duration to set interrupt flag, V _{CC} = 1.8 V or 3.0 V | 1.62 V to 1.98 V | 20 | ns |

(1) In all test conditions, V_{IO} ≤ V_{CC}.

(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_(int) is met. It may be set by trigger signals shorter than t_(int).

5.11 Leakage Current – General-Purpose I/O DVCC Domain (P1.0 to P1.3, P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|--|-----------------|-----------------|-----|-----|------|
| I _{lkg} (Px.y) High-impedance leakage current | (1) (2) | 1.8 V, 3 V | -50 | 50 | nA |

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

5.12 Leakage Current – General-Purpose I/O DVIO Domain (P1.4 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P7.0 to P7.5)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{IO} (1) | MIN | MAX | UNIT |
|--|-----------------|---------------------|-----|-----|------|
| I _{lkg} (Px.y) High-impedance leakage current | (2) (3) | 1.62 V to 1.98 V | -50 | 50 | nA |

(1) In all test conditions, V_{IO} ≤ V_{CC}.

(2) The leakage current is measured with V_{SS} or V_{IO} applied to the corresponding pins, unless otherwise noted.

(3) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

5.13 Outputs – General-Purpose I/O DVCC Domain (Full Drive Strength) (P1.0 to P1.3, P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|---|-----------------------------------|-----------------|------------------------|------------------------|------|
| V _{OH} High-level output voltage | I _(OHmax) = -3 mA (1) | 1.8 V | V _{CC} - 0.25 | V _{CC} | V |
| | I _(OHmax) = -10 mA (2) | | V _{CC} - 0.60 | V _{CC} | |
| | I _(OHmax) = -5 mA (1) | 3 V | V _{CC} - 0.25 | V _{CC} | |
| | I _(OHmax) = -15 mA (2) | | V _{CC} - 0.60 | V _{CC} | |
| V _{OL} Low-level output voltage | I _(OLmax) = 3 mA (1) | 1.8 V | V _{SS} | V _{SS} + 0.25 | V |
| | I _(OLmax) = 10 mA (2) | | V _{SS} | V _{SS} + 0.60 | |
| | I _(OLmax) = 5 mA (1) | 3 V | V _{SS} | V _{SS} + 0.25 | |
| | I _(OLmax) = 15 mA (2) | | V _{SS} | V _{SS} + 0.60 | |

(1) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

(2) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

5.14 Outputs – General-Purpose I/O DVCC Domain (Reduced Drive Strength) (P1.0 to P1.3, P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|---|----------------------------------|-----------------|------------------------|------------------------|------|
| V _{OH} High-level output voltage | I _(OHmax) = -1 mA (2) | 1.8 V | V _{CC} - 0.25 | V _{CC} | V |
| | I _(OHmax) = -3 mA (3) | | V _{CC} - 0.60 | V _{CC} | |
| | I _(OHmax) = -2 mA (2) | 3.0 V | V _{CC} - 0.25 | V _{CC} | |
| | I _(OHmax) = -6 mA (3) | | V _{CC} - 0.60 | V _{CC} | |
| V _{OL} Low-level output voltage | I _(OLmax) = 1 mA (2) | 1.8 V | V _{SS} | V _{SS} + 0.25 | V |
| | I _(OLmax) = 3 mA (3) | | V _{SS} | V _{SS} + 0.60 | |
| | I _(OLmax) = 2 mA (2) | 3.0 V | V _{SS} | V _{SS} + 0.25 | |
| | I _(OLmax) = 6 mA (3) | | V _{SS} | V _{SS} + 0.60 | |

(1) Selecting reduced drive strength may reduce EMI.

(2) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

(3) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

5.15 Outputs – General-Purpose I/O DVIO Domain (Full Drive Strength) (P1.4 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P7.0 to P7.5)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{IO}^{(1)}$ | MIN | MAX | UNIT |
|-----------|---------------------------|-------------------------------------|------------------|-----------------|-----------------|------|
| V_{OH} | High-level output voltage | $I_{(OHmax)} = -3 \text{ mA}^{(2)}$ | 1.62 V to 1.98 V | $V_{IO} - 0.25$ | V_{IO} | V |
| | | $I_{(OHmax)} = -6 \text{ mA}^{(2)}$ | | $V_{IO} - 0.50$ | V_{IO} | |
| V_{OL} | Low-level output voltage | $I_{(OLmax)} = 3 \text{ mA}^{(2)}$ | 1.62 V to 1.98 V | V_{SS} | $V_{SS} + 0.25$ | V |
| | | $I_{(OLmax)} = 6 \text{ mA}^{(2)}$ | | V_{SS} | $V_{SS} + 0.50$ | |

(1) In all test conditions, $V_{IO} \leq V_{CC}$.

(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed $\pm 48 \text{ mA}$ to hold the maximum voltage drop specified.

5.16 Outputs – General-Purpose I/O DVIO Domain (Reduced Drive Strength) (P1.4 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P7.0 to P7.5)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | $V_{IO}^{(2)}$ | MIN | MAX | UNIT |
|-----------|---------------------------|-------------------------------------|------------------|-----------------|-----------------|------|
| V_{OH} | High-level output voltage | $I_{(OHmax)} = -1 \text{ mA}^{(3)}$ | 1.62 V to 1.98 V | $V_{IO} - 0.25$ | V_{IO} | V |
| | | $I_{(OHmax)} = -2 \text{ mA}^{(3)}$ | | $V_{IO} - 0.50$ | V_{IO} | |
| V_{OL} | Low-level output voltage | $I_{(OLmax)} = 1 \text{ mA}^{(3)}$ | 1.62 V to 1.98 V | V_{SS} | $V_{SS} + 0.25$ | V |
| | | $I_{(OLmax)} = 2 \text{ mA}^{(3)}$ | | V_{SS} | $V_{SS} + 0.50$ | |

(1) Selecting reduced drive strength may reduce EMI.

(2) In all test conditions, $V_{IO} \leq V_{CC}$.

(3) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed $\pm 48 \text{ mA}$ to hold the maximum voltage drop specified.

5.17 Output Frequency – General-Purpose I/O DVCC Domain (P1.0 to P1.3, P5.0 to P5.5, P6.0 to P6.7, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|-----------------------|--------------------------------------|--|---|-----|-----|------|
| f _{Px,y} | Port output frequency (with load) | (1)(2) | V _{CC} = 1.8 V, PMMCOREVx = 0 | | 16 | MHz |
| | | | V _{CC} = 3 V, PMMCOREVx = 3 | | 25 | |
| f _{Port_CLK} | Clock output frequency | ACLK, SMCLK, or MCLK, C _L = 20 pF ⁽²⁾ | V _{CC} = 1.8 V, PMMCOREVx = 0 | | 16 | MHz |
| | | | V _{CC} = 3 V, PMMCOREVx = 3 | | 25 | |

- (1) A resistive divider with 2 × R1 between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. For full drive strength, R1 = 550 Ω. For reduced drive strength, R1 = 1.6 kΩ. C_L = 20 pF is connected to the output to V_{SS}.
- (2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

5.18 Output Frequency – General-Purpose I/O DVIO Domain (P1.4 to P1.7, P2.0 to P2.7, P3.0 to P3.4, P4.0 to P4.7, P7.0 to P7.5)

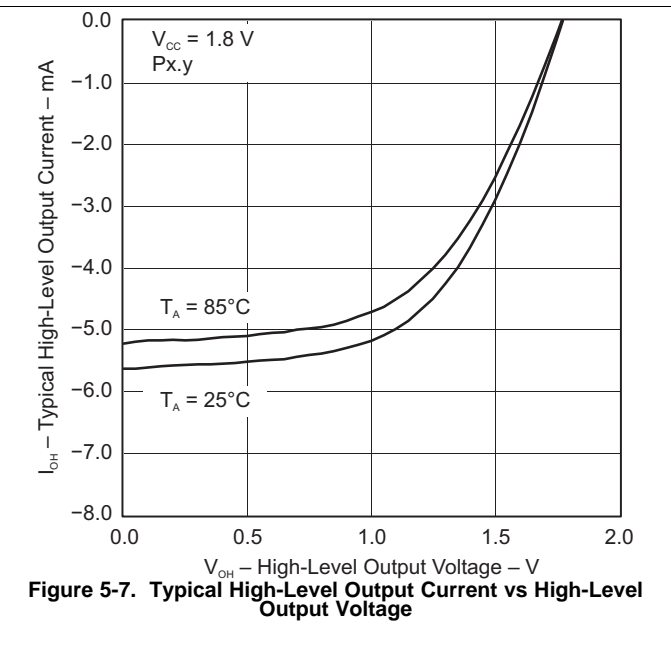
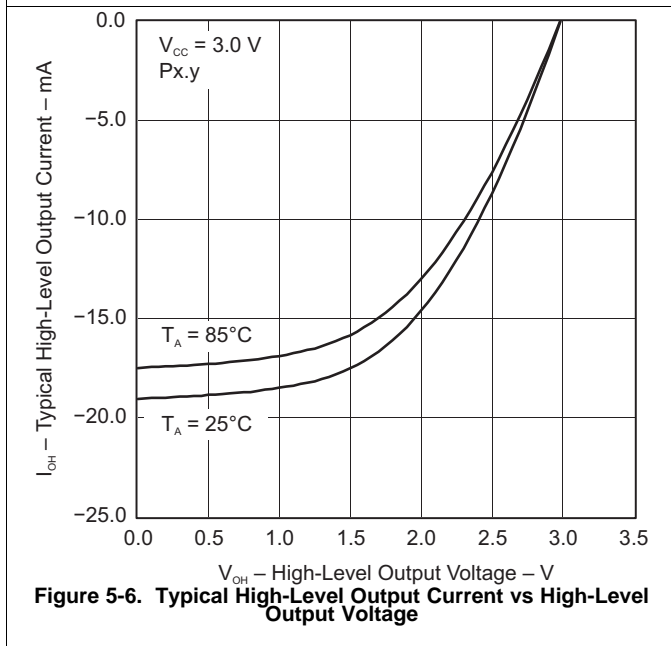
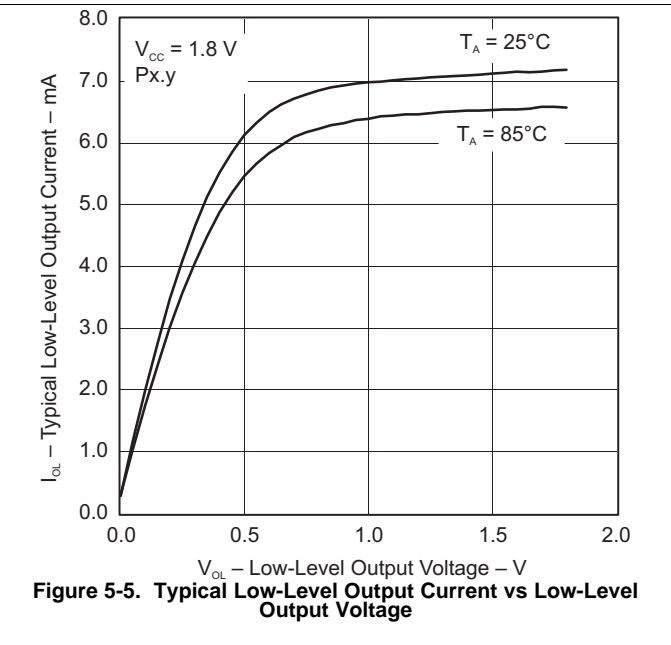
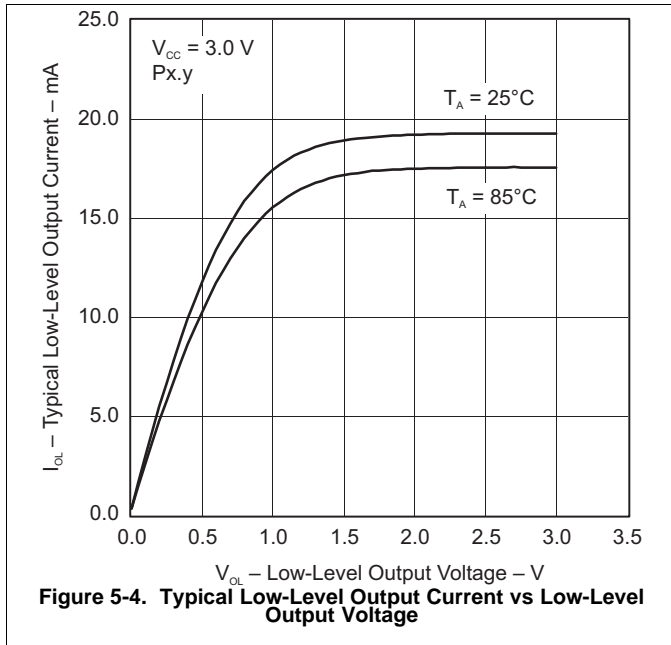
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|-----------------------|--------------------------------------|--|--|-----|-----|------|
| f _{Px,y} | Port output frequency (with load) | (1)(2) | V _{IO} = 1.62 V to 1.98 V ⁽³⁾ , PMMCOREVx = 0 | | 16 | MHz |
| | | | V _{IO} = 1.62 V to 1.98 V ⁽³⁾ , PMMCOREVx = 3 | | 25 | |
| f _{Port_CLK} | Clock output frequency | ACLK, SMCLK, or MCLK, C _L = 20 pF ⁽²⁾ | V _{IO} = 1.62 V to 1.98 V ⁽³⁾ , PMMCOREVx = 0 | | 16 | MHz |
| | | | V _{IO} = 1.62 V to 1.98 V ⁽³⁾ , PMMCOREVx = 3 | | 25 | |

- (1) A resistive divider with 2 × R1 between V_{IO} and V_{SS} is used as load. The output is connected to the center tap of the divider. For full drive strength, R1 = 550 Ω. For reduced drive strength, R1 = 1.6 kΩ. C_L = 20 pF is connected to the output to V_{SS}.
- (2) The output voltage reaches at least 10% and 90% V_{IO} at the specified toggle frequency.
- (3) In all test conditions, V_{IO} ≤ V_{CC}.

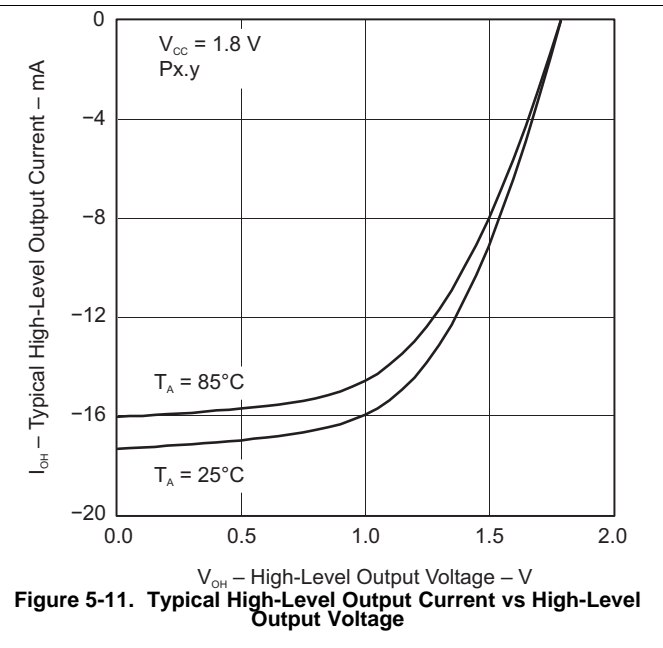
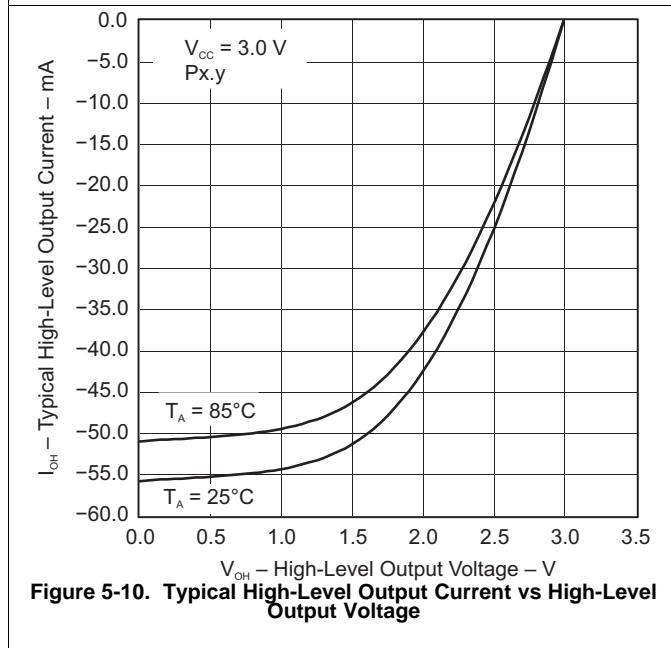
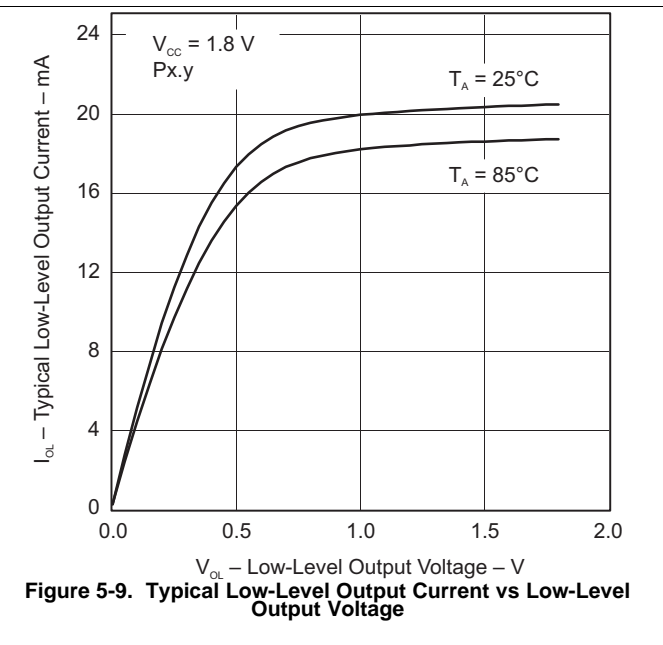
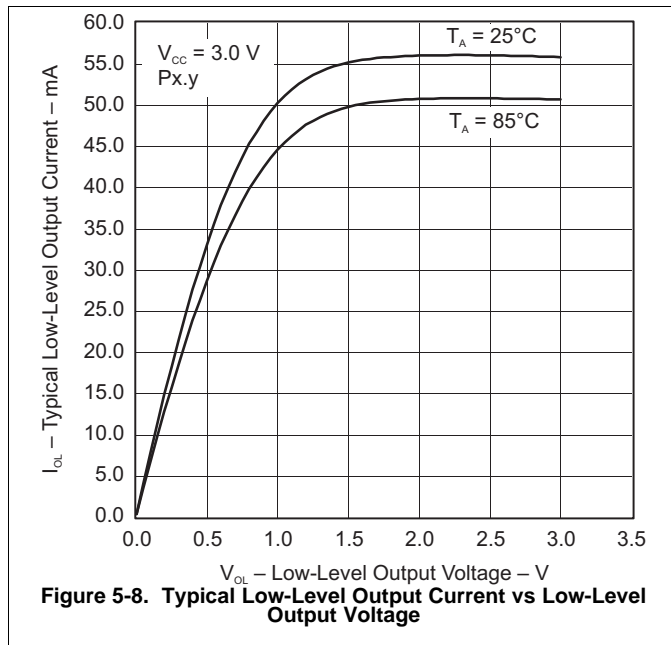
5.19 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)



5.20 Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)



5.21 Crystal Oscillator, XT1, Low-Frequency Mode

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|----------------------|--|-----------------|-----|--------|-------|------------|---|
| $\Delta I_{DVCC,LF}$ | Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode | 3.0 V | | 0.075 | | μA | |
| | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 1, T _A = 25°C | | | | | | |
| | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 2, T _A = 25°C | | | | | | |
| | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 3, T _A = 25°C | | | 0.290 | | | |
| $f_{XT1,LF0}$ | XT1 oscillator crystal frequency, LF mode | | | 32768 | | Hz | |
| $f_{XT1,LF,SW}$ | XT1 oscillator logic-level square-wave input frequency, LF mode | | 10 | 32.768 | 50 | kHz | |
| OA_{LF} | Oscillation allowance for LF crystals ⁽⁴⁾ | | | 210 | | k Ω | |
| | | | | | | | XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, $f_{XT1,LF} = 32768$ Hz, C _{L,eff} = 6 pF |
| | XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 1, $f_{XT1,LF} = 32768$ Hz, C _{L,eff} = 12 pF | | | 300 | | | |
| $C_{L,eff}$ | Integrated effective load capacitance, LF mode ⁽⁵⁾ | | | | | pF | |
| | | | | | | | XTS = 0, XCAP _x = 0 ⁽⁶⁾ |
| | | | | | | | XTS = 0, XCAP _x = 1 |
| | | | | | | | XTS = 0, XCAP _x = 2 |
| | XTS = 0, XCAP _x = 3 | | | 12.0 | | | |
| | Duty cycle, LF mode | | 30% | | 70% | | |
| $f_{Fault,LF}$ | Oscillator fault frequency, LF mode ⁽⁷⁾ | | 10 | | 10000 | Hz | |
| $t_{START,LF}$ | Start-up time, LF mode | 3.0 V | | 1000 | | ms | |
| | | | | | | | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, T _A = 25°C, C _{L,eff} = 6 pF |
| | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 3, T _A = 25°C, C _{L,eff} = 12 pF | | | 500 | | | |

- (1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
 - Keep the trace between the device and the crystal as short as possible.
 - Design a good ground plane around the oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
 - If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the [Schmitt-Trigger Inputs](#) section of this data sheet. When in crystal bypass mode, XIN can be configured so that it can support an input digital waveform with swing levels from DVSS to DVCC (XT1BYPASSLV = 0) or DVSS to DVIO (XT1BYPASSLV = 1). In this case, the pin must be configured properly for the intended input swing.
- (3) Maximum frequency of operation of the entire device cannot be exceeded.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVE_x settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but each application should be evaluated based on the actual crystal selected:
 - For XT1DRIVE_x = 0, C_{L,eff} ≤ 6 pF
 - For XT1DRIVE_x = 1, 6 pF ≤ C_{L,eff} ≤ 9 pF
 - For XT1DRIVE_x = 2, 6 pF ≤ C_{L,eff} ≤ 10 pF
 - For XT1DRIVE_x = 3, C_{L,eff} ≥ 6 pF
- (5) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
- (7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.
- (8) Measured with logic-level input frequency but also applies to operation with crystals.

5.22 Crystal Oscillator, XT2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾⁽²⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|---|--|---|-----|-----|-----|------|
| I _{DVCC,XT2} | XT2 oscillator crystal current consumption | f _{OSC} = 4 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 0, T _A = 25°C | 3.0 V | 200 | | μA | |
| | | f _{OSC} = 12 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 1, T _A = 25°C | | 260 | | | |
| | | f _{OSC} = 20 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 2, T _A = 25°C | | 325 | | | |
| | | f _{OSC} = 32 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVE _x = 3, T _A = 25°C | | 450 | | | |
| f _{XT2,HF0} | XT2 oscillator crystal frequency, mode 0 | XT2DRIVE _x = 0, XT2BYPASS = 0 ⁽³⁾ | | 4 | | 8 | MHz |
| f _{XT2,HF1} | XT2 oscillator crystal frequency, mode 1 | XT2DRIVE _x = 1, XT2BYPASS = 0 ⁽³⁾ | | 8 | | 16 | MHz |
| f _{XT2,HF2} | XT2 oscillator crystal frequency, mode 2 | XT2DRIVE _x = 2, XT2BYPASS = 0 ⁽³⁾ | | 16 | | 24 | MHz |
| f _{XT2,HF3} | XT2 oscillator crystal frequency, mode 3 | XT2DRIVE _x = 3, XT2BYPASS = 0 ⁽³⁾ | | 24 | | 32 | MHz |
| f _{XT2,HF,SW} | XT2 oscillator logic-level square-wave input frequency, bypass mode | XT2BYPASS = 1 ⁽⁴⁾⁽³⁾ XT2BYPASSLV = 0 or 1 | | 0.7 | | 32 | MHz |
| O _{AHF} | Oscillation allowance for HF crystals ⁽⁵⁾ | XT2DRIVE _x = 0, XT2BYPASS = 0, f _{XT2,HF0} = 6 MHz, C _{L,eff} = 15 pF | | 450 | | Ω | |
| | | XT2DRIVE _x = 1, XT2BYPASS = 0, f _{XT2,HF1} = 12 MHz, C _{L,eff} = 15 pF | | 320 | | | |
| | | XT2DRIVE _x = 2, XT2BYPASS = 0, f _{XT2,HF2} = 20 MHz, C _{L,eff} = 15 pF | | 200 | | | |
| | | XT2DRIVE _x = 3, XT2BYPASS = 0, f _{XT2,HF3} = 32 MHz, C _{L,eff} = 15 pF | | 200 | | | |
| t _{START,HF} | Start-up time | f _{OSC} = 6 MHz, XT2BYPASS = 0, XT2DRIVE _x = 0, T _A = 25°C, C _{L,eff} = 15 pF | 3.0 V | 0.5 | | ms | |
| | | f _{OSC} = 20 MHz, XT2BYPASS = 0, XT2DRIVE _x = 2, T _A = 25°C, C _{L,eff} = 15 pF | | 0.3 | | | |
| C _{L,eff} | Integrated effective load capacitance, HF mode ^{(6) (1)} | | | 1 | | pF | |
| | | Duty cycle | Measured at ACLK, f _{XT2,HF2} = 20 MHz | 40% | 50% | | 60% |

(1) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(2) To improve EMI on the XT2 oscillator the following guidelines should be observed.

- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
- Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(3) This represents the maximum frequency that can be input to the device externally. Maximum frequency achievable on the device operation is based on the frequencies present on ACLK, MCLK, and SMCLK cannot be exceed for a given range of operation.

(4) When XT2BYPASS is set, the XT2 circuit is automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet. When in crystal bypass mode, XT2IN can be configured so that it can support an input digital waveform with swing levels from DVSS to DVCC (XT2BYPASSLV = 0) or DVSS to DVIO (XT2BYPASSLV = 1). In this case, it is required that the pin be configured properly for the intended input swing.

(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.

(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).

Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

Crystal Oscillator, XT2 (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾⁽²⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|---|--|-----------------|-----|-----|-----|------|
| f _{Fault,HF} | Oscillator fault frequency ⁽⁷⁾ | XT2BYPASS = 1 ⁽⁸⁾ , XT2BYPASSLV = 0 or 1 | | 30 | | 300 | kHz |

(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.

(8) Measured with logic-level input frequency but also applies to operation with crystals. In general, an effective load capacitance of up to 18 pF can be supported.

5.23 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------------------|------------------------------------|---------------------------------|-----------------|-----|-----|-----|------|
| f _{VLO} | VLO frequency | Measured at ACLK | 1.8 V to 3.6 V | 6 | 9.4 | 14 | kHz |
| df _{VLO} /dT | VLO frequency temperature drift | Measured at ACLK ⁽¹⁾ | 1.8 V to 3.6 V | | 0.5 | | %/°C |
| df _{VLO} /dV _{CC} | VLO frequency supply voltage drift | Measured at ACLK ⁽²⁾ | 1.8 V to 3.6 V | | 4 | | %/V |
| | Duty cycle | Measured at ACLK | 1.8 V to 3.6 V | 40% | 50% | 60% | |

(1) Calculated using the box method: (MAX(−40°C to 85°C) – MIN(−40°C to 85°C)) / MIN(−40°C to 85°C) / (85°C – (−40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

5.24 Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--------------------------------------|-------------------------------------|---------------------------------|-----------------|-------|-------|------|------|
| I _{REFO} | REFO oscillator current consumption | T _A = 25°C | 1.8 V to 3.6 V | | 3 | | μA |
| f _{REFO} | REFO frequency | Measured at ACLK | 1.8 V to 3.6 V | | 32768 | | Hz |
| | REFO absolute tolerance | Full temperature range | 1.8 V to 3.6 V | −3.5% | | 3.5% | |
| | | T _A = 25°C | 3 V | −1.5% | | 1.5% | |
| df _{REFO} /dT | REFO frequency temperature drift | Measured at ACLK ⁽¹⁾ | 1.8 V to 3.6 V | | 0.01 | | %/°C |
| df _{REFO} /dV _{CC} | REFO frequency supply voltage drift | Measured at ACLK ⁽²⁾ | 1.8 V to 3.6 V | | 1.0 | | %/V |
| | Duty cycle | Measured at ACLK | 1.8 V to 3.6 V | 40% | 50% | 60% | |
| t _{START} | REFO start-up time | 40%/60% duty cycle | 1.8 V to 3.6 V | | 25 | | μs |

(1) Calculated using the box method: (MAX(−40°C to 85°C) – MIN(−40°C to 85°C)) / MIN(−40°C to 85°C) / (85°C – (−40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

5.25 DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|--|--|------|------|-------|
| $f_{DCO(0,0)}$ | DCO frequency (0, 0) ⁽¹⁾ | DCORSELx = 0, DCOx = 0, MODx = 0 | 0.07 | 0.20 | MHz |
| $f_{DCO(0,31)}$ | DCO frequency (0, 31) ⁽¹⁾ | DCORSELx = 0, DCOx = 31, MODx = 0 | 0.70 | 1.70 | MHz |
| $f_{DCO(1,0)}$ | DCO frequency (1, 0) ⁽¹⁾ | DCORSELx = 1, DCOx = 0, MODx = 0 | 0.15 | 0.36 | MHz |
| $f_{DCO(1,31)}$ | DCO frequency (1, 31) ⁽¹⁾ | DCORSELx = 1, DCOx = 31, MODx = 0 | 1.47 | 3.45 | MHz |
| $f_{DCO(2,0)}$ | DCO frequency (2, 0) ⁽¹⁾ | DCORSELx = 2, DCOx = 0, MODx = 0 | 0.32 | 0.75 | MHz |
| $f_{DCO(2,31)}$ | DCO frequency (2, 31) ⁽¹⁾ | DCORSELx = 2, DCOx = 31, MODx = 0 | 3.17 | 7.38 | MHz |
| $f_{DCO(3,0)}$ | DCO frequency (3, 0) ⁽¹⁾ | DCORSELx = 3, DCOx = 0, MODx = 0 | 0.64 | 1.51 | MHz |
| $f_{DCO(3,31)}$ | DCO frequency (3, 31) ⁽¹⁾ | DCORSELx = 3, DCOx = 31, MODx = 0 | 6.07 | 14.0 | MHz |
| $f_{DCO(4,0)}$ | DCO frequency (4, 0) ⁽¹⁾ | DCORSELx = 4, DCOx = 0, MODx = 0 | 1.3 | 3.2 | MHz |
| $f_{DCO(4,31)}$ | DCO frequency (4, 31) ⁽¹⁾ | DCORSELx = 4, DCOx = 31, MODx = 0 | 12.3 | 28.2 | MHz |
| $f_{DCO(5,0)}$ | DCO frequency (5, 0) ⁽¹⁾ | DCORSELx = 5, DCOx = 0, MODx = 0 | 2.5 | 6.0 | MHz |
| $f_{DCO(5,31)}$ | DCO frequency (5, 31) ⁽¹⁾ | DCORSELx = 5, DCOx = 31, MODx = 0 | 23.7 | 54.1 | MHz |
| $f_{DCO(6,0)}$ | DCO frequency (6, 0) ⁽¹⁾ | DCORSELx = 6, DCOx = 0, MODx = 0 | 4.6 | 10.7 | MHz |
| $f_{DCO(6,31)}$ | DCO frequency (6, 31) ⁽¹⁾ | DCORSELx = 6, DCOx = 31, MODx = 0 | 39.0 | 88.0 | MHz |
| $f_{DCO(7,0)}$ | DCO frequency (7, 0) ⁽¹⁾ | DCORSELx = 7, DCOx = 0, MODx = 0 | 8.5 | 19.6 | MHz |
| $f_{DCO(7,31)}$ | DCO frequency (7, 31) ⁽¹⁾ | DCORSELx = 7, DCOx = 31, MODx = 0 | 60 | 135 | MHz |
| $S_{DCORSEL}$ | Frequency step between range DCORSEL and DCORSEL + 1 | $S_{RSEL} = f_{DCO(DCORSEL+1,DCO)} / f_{DCO(DCORSEL,DCO)}$ | 1.2 | 2.3 | ratio |
| S_{DCO} | Frequency step between tap DCO and DCO + 1 | $S_{DCO} = f_{DCO(DCORSEL,DCO+1)} / f_{DCO(DCORSEL,DCO)}$ | 1.02 | 1.12 | ratio |
| | Duty cycle | Measured at SMCLK | 40% | 50% | 60% |
| df_{DCO}/dT | DCO frequency temperature drift ⁽²⁾ | $f_{DCO} = 1$ MHz | | 0.1 | %/°C |
| df_{DCO}/dV_{CC} | DCO frequency voltage drift ⁽³⁾ | $f_{DCO} = 1$ MHz | | 1.9 | %/V |

- (1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, f_{DCO} , should be set to reside within the range of $f_{DCO(n,0),MAX} \leq f_{DCO} \leq f_{DCO(n,31),MIN}$, where $f_{DCO(n,0),MAX}$ represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and $f_{DCO(n,31),MIN}$ represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual f_{DCO} frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.
- (2) Calculated using the box method: $(MAX(-40^{\circ}C \text{ to } 85^{\circ}C) - MIN(-40^{\circ}C \text{ to } 85^{\circ}C)) / MIN(-40^{\circ}C \text{ to } 85^{\circ}C) / (85^{\circ}C - (-40^{\circ}C))$
- (3) Calculated using the box method: $(MAX(1.8 \text{ V to } 3.6 \text{ V}) - MIN(1.8 \text{ V to } 3.6 \text{ V})) / MIN(1.8 \text{ V to } 3.6 \text{ V}) / (3.6 \text{ V} - 1.8 \text{ V})$

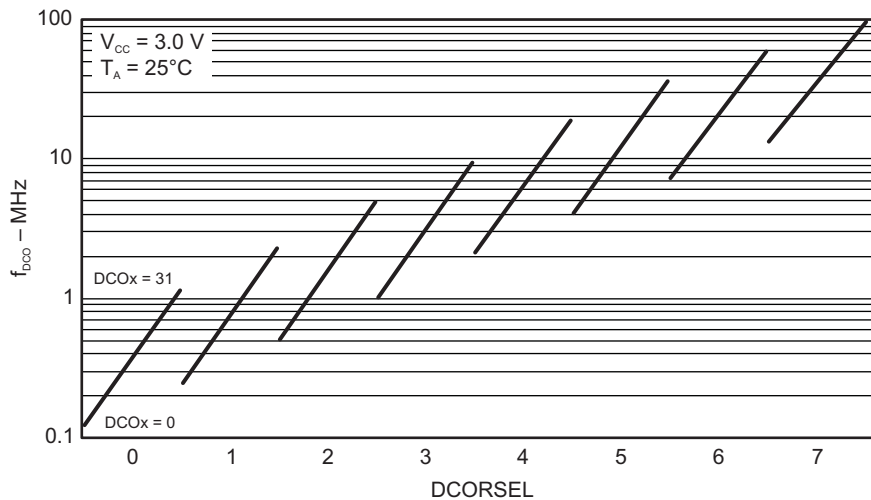


Figure 5-12. Typical DCO Frequency

5.26 PMM, Brownout Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|---|--------------------------------|------|------|------|------|
| V _{DVCC_BOR_IT-} | BOR _H on voltage, DV _{CC} falling level | dDV _{CC} /dt < 3 V/s | | | 1.45 | V |
| V _{DVCC_BOR_IT+} | BOR _H off voltage, DV _{CC} rising level | dDV _{CC} /dt < 3 V/s | 0.80 | 1.30 | 1.50 | V |
| V _{DVCC_BOR_hys} | BOR _H hysteresis | | 50 | | 250 | mV |
| t _{RESET} | Pulse duration required at RST/NMI pin to accept a reset | | 2 | | | μs |

5.27 PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|--|----------------------------------|-----|------|-----|------|
| V _{CORE3(AM)} | Core voltage, active mode, PMMCOREV = 3 | 2.4 V ≤ DV _{CC} ≤ 3.6 V | | 1.90 | | V |
| V _{CORE2(AM)} | Core voltage, active mode, PMMCOREV = 2 | 2.2 V ≤ DV _{CC} ≤ 3.6 V | | 1.80 | | V |
| V _{CORE1(AM)} | Core voltage, active mode, PMMCOREV = 1 | 2.0 V ≤ DV _{CC} ≤ 3.6 V | | 1.60 | | V |
| V _{CORE0(AM)} | Core voltage, active mode, PMMCOREV = 0 | 1.8 V ≤ DV _{CC} ≤ 3.6 V | | 1.40 | | V |
| V _{CORE3(LPM)} | Core voltage, low-current mode, PMMCOREV = 3 | 2.4 V ≤ DV _{CC} ≤ 3.6 V | | 1.94 | | V |
| V _{CORE2(LPM)} | Core voltage, low-current mode, PMMCOREV = 2 | 2.2 V ≤ DV _{CC} ≤ 3.6 V | | 1.84 | | V |
| V _{CORE1(LPM)} | Core voltage, low-current mode, PMMCOREV = 1 | 2.0 V ≤ DV _{CC} ≤ 3.6 V | | 1.64 | | V |
| V _{CORE0(LPM)} | Core voltage, low-current mode, PMMCOREV = 0 | 1.8 V ≤ DV _{CC} ≤ 3.6 V | | 1.44 | | V |

5.28 PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|---|--|------|------|------|------|
| $I_{(SVSH)}$ | SVS current consumption | SVSHE = 0, DV _{CC} = 3.6 V | | 0 | | nA |
| | | SVSHE = 1, DV _{CC} = 3.6 V, SVSHFP = 0 | | 200 | | |
| | | SVSHE = 1, DV _{CC} = 3.6 V, SVSHFP = 1 | | 1.5 | | μA |
| $V_{(SVSH_IT-)}$ | SVS _H on voltage level ⁽¹⁾ | SVSHE = 1, SVSHRVL = 0 | 1.57 | 1.68 | 1.78 | V |
| | | SVSHE = 1, SVSHRVL = 1 | 1.79 | 1.88 | 1.98 | |
| | | SVSHE = 1, SVSHRVL = 2 | 1.98 | 2.08 | 2.21 | |
| | | SVSHE = 1, SVSHRVL = 3 | 2.10 | 2.18 | 2.31 | |
| $V_{(SVSH_IT+)}$ | SVS _H off voltage level ⁽¹⁾ | SVSHE = 1, SVSMHRRRL = 0 | 1.62 | 1.74 | 1.85 | V |
| | | SVSHE = 1, SVSMHRRRL = 1 | 1.88 | 1.94 | 2.07 | |
| | | SVSHE = 1, SVSMHRRRL = 2 | 2.07 | 2.14 | 2.28 | |
| | | SVSHE = 1, SVSMHRRRL = 3 | 2.20 | 2.30 | 2.42 | |
| | | SVSHE = 1, SVSMHRRRL = 4 | 2.32 | 2.40 | 2.55 | |
| | | SVSHE = 1, SVSMHRRRL = 5 | 2.52 | 2.70 | 2.88 | |
| | | SVSHE = 1, SVSMHRRRL = 6 | 2.90 | 3.10 | 3.23 | |
| | | SVSHE = 1, SVSMHRRRL = 7 | 2.90 | 3.10 | 3.23 | |
| $t_{pd(SVSH)}$ | SVS _H propagation delay | SVSHE = 1, dV _{DVCC} /dt = 10 mV/μs, SVSHFP = 1 | | 2.5 | | μs |
| | | SVSHE = 1, dV _{DVCC} /dt = 1 mV/μs, SVSHFP = 0 | | 20 | | |
| $t_{(SVSH)}$ | SVS _H on or off delay time | SVSHE = 0 → 1, dV _{DVCC} /dt = 10 mV/μs, SVSHFP = 1 | | 12.5 | | μs |
| | | SVSHE = 0 → 1, dV _{DVCC} /dt = 1 mV/μs, SVSHFP = 0 | | 100 | | |
| dV _{DVCC} /dt | DV _{CC} rise time | | 0 | | 1000 | V/s |

(1) The SVS_H settings available depend on the V_{CORE} (PMMCOREV_x) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the [MSP430F5xx and MSP430F6xx Family User's Guide](#) on recommended settings and use.

5.29 PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|------|------|------|------|
| $I_{(SVMH)}$ SVM _H current consumption | SVMHE = 0, DV _{CC} = 3.6 V | | 0 | | nA |
| | SVMHE = 1, DV _{CC} = 3.6 V, SVMHFP = 0 | | 200 | | |
| | SVMHE = 1, DV _{CC} = 3.6 V, SVMHFP = 1 | | 1.5 | | μA |
| $V_{(SVMH)}$ SVM _H on or off voltage level ⁽¹⁾ | SVMHE = 1, SVSMHRRRL = 0 | 1.62 | 1.74 | 1.85 | V |
| | SVMHE = 1, SVSMHRRRL = 1 | 1.88 | 1.94 | 2.07 | |
| | SVMHE = 1, SVSMHRRRL = 2 | 2.07 | 2.14 | 2.28 | |
| | SVMHE = 1, SVSMHRRRL = 3 | 2.20 | 2.30 | 2.42 | |
| | SVMHE = 1, SVSMHRRRL = 4 | 2.32 | 2.40 | 2.55 | |
| | SVMHE = 1, SVSMHRRRL = 5 | 2.52 | 2.70 | 2.88 | |
| | SVMHE = 1, SVSMHRRRL = 6 | 2.90 | 3.10 | 3.23 | |
| | SVMHE = 1, SVSMHRRRL = 7 | 2.90 | 3.10 | 3.23 | |
| $t_{pd(SVMH)}$ SVM _H propagation delay | SVMHE = 1, dV _{DVCC} /dt = 10 mV/μs, SVMHFP = 1 | | 2.5 | | μs |
| | SVMHE = 1, dV _{DVCC} /dt = 1 mV/μs, SVMHFP = 0 | | 20 | | |
| $t_{(SVMH)}$ SVM _H on or off delay time | SVMHE = 0 → 1, dV _{DVCC} /dt = 10 mV/μs, SVMHFP = 1 | | 12.5 | | μs |
| | SVMHE = 0 → 1, dV _{DVCC} /dt = 1 mV/μs, SVMHFP = 0 | | 100 | | |

(1) The SVM_H settings available depend on the V_{CORE} (PMM_{COREVx}) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the [MSP430F5xx and MSP430F6xx Family User's Guide](#) on recommended settings and use.

5.30 PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----|------|-----|------|
| $I_{(SVSL)}$ SVS _L current consumption | SVSLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | SVSLE = 1, PMMCOREV = 2, SVSLFP = 0 | | 200 | | |
| | SVSLE = 1, PMMCOREV = 2, SVSLFP = 1 | | 1.5 | | μA |
| $t_{pd(SVSL)}$ SVS _L propagation delay | SVSLE = 1, dV _{CORE} /dt = 10 mV/μs, SVSLFP = 1 | | 2.5 | | μs |
| | SVSLE = 1, dV _{CORE} /dt = 1 mV/μs, SVSLFP = 0 | | 20 | | |
| $t_{(SVSL)}$ SVS _L on or off delay time | SVSLE = 0 → 1, dV _{CORE} /dt = 10 mV/μs, SVSLFP = 1 | | 12.5 | | μs |
| | SVSLE = 0 → 1, dV _{CORE} /dt = 1 mV/μs, SVSLFP = 0 | | 100 | | |

5.31 PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|---------------------------------------|--|-----|------|-----|------|
| $I_{(SVML)}$ | SVM _L current consumption | SVMLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | | SVMLE = 1, PMMCOREV = 2, SVMLFP = 0 | | 200 | | |
| | | SVMLE = 1, PMMCOREV = 2, SVMLFP = 1 | | 1.5 | | μA |
| $t_{pd(SVML)}$ | SVM _L propagation delay | SVMLE = 1, $dV_{CORE}/dt = 10 \text{ mV}/\mu\text{s}$, SVMLFP = 1 | | 2.5 | | μs |
| | | SVMLE = 1, $dV_{CORE}/dt = 1 \text{ mV}/\mu\text{s}$, SVMLFP = 0 | | 20 | | |
| $t_{(SVML)}$ | SVM _L on or off delay time | SVMLE = 0 → 1, $dV_{CORE}/dt = 10 \text{ mV}/\mu\text{s}$, SVMLFP = 1 | | 12.5 | | μs |
| | | SVMLE = 0 → 1, $dV_{CORE}/dt = 1 \text{ mV}/\mu\text{s}$, SVMLFP = 0 | | 100 | | |

5.32 Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|--|---|---|-----|-----|------|
| $t_{\text{WAKE-UP-FAST}}$ | Wake-up time from LPM2, LPM3, or LPM4 to active mode ⁽¹⁾ | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1 | $f_{\text{MCLK}} \geq 4.0 \text{ MHz}$ $1.0 \text{ MHz} < f_{\text{MCLK}} < 4.0 \text{ MHz}$ | 3.5 | 7.5 | μs |
| | | | | 4.5 | 9 | |
| $t_{\text{WAKE-UP-SLOW}}$ | Wake-up time from LPM2, LPM3, or LPM4 to active mode ⁽²⁾⁽³⁾ | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0 | | 150 | 175 | μs |
| $t_{\text{WAKE-UP-LPM5}}$ | Wake-up time from LPM4.5 to active mode ⁽⁴⁾ | | | 2 | 3 | ms |
| $t_{\text{WAKE-UP-RESET}}$ | Wake-up time from $\overline{\text{RST}}$ or BOR event to active mode ⁽⁴⁾ | | | 2 | 3 | ms |

- (1) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low-side monitor (SVM_L). $t_{\text{WAKE-UP-FAST}}$ is possible with SVS_L and SVM_L in full performance mode or disabled. For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the [MSP430F5xx and MSP430F6xx Family User's Guide](#).
- (2) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low-side monitor (SVM_L). $t_{\text{WAKE-UP-SLOW}}$ is set with SVS_L and SVM_L in normal mode (low current mode). For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the [MSP430F5xx and MSP430F6xx Family User's Guide](#).
- (3) The wake-up times from LPM0 and LPM1 to AM are not specified. They are proportional to MCLK cycle time but are not affected by the performance mode settings as for LPM2, LPM3, and LPM4.
- (4) This value represents the time from the wake-up event to the reset vector execution.

5.33 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | V _{IO} | MIN | TYP | MAX | UNIT |
|---------------------|---------------------------------------|---|-----------------|------------------|-----|-----|-----|------|
| f _{TA} | Timer_A input clock frequency | Internal: SMCLK or ACLK, External: TACLK, Duty cycle = 50% ±10% | 1.8 V | 1.62 V to 1.8 V | | | 25 | MHz |
| | | | 3.0 V | 1.62 V to 1.98 V | | | 25 | |
| t _{TA,cap} | Timer_A capture timing ⁽¹⁾ | All capture inputs, Minimum pulse duration required for capture | 1.8 V | 1.62 V to 1.8 V | 20 | | | ns |
| | | | 3.0 V | 1.62 V to 1.98 V | 20 | | | |

(1) The external signal sets the interrupt flag every time the minimum parameters are met. It may be set even with trigger signals shorter than t_{TA,cap}.

5.34 Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | V _{IO} | MIN | TYP | MAX | UNIT |
|---------------------|---------------------------------------|---|-----------------|------------------|-----|-----|-----|------|
| f _{TB} | Timer_B input clock frequency | Internal: SMCLK or ACLK, External: TBCLK, Duty cycle = 50% ±10% | 1.8 V | 1.62 V to 1.8 V | | | 25 | MHz |
| | | | 3.0 V | 1.62 V to 1.98 V | | | 25 | |
| t _{TB,cap} | Timer_B capture timing ⁽¹⁾ | All capture inputs, Minimum pulse duration required for capture | 1.8 V | 1.62 V to 1.8 V | 20 | | | ns |
| | | | 3.0 V | 1.62 V to 1.98 V | 20 | | | |

(1) The external signal sets the interrupt flag every time the minimum parameters are met. It may be set even with trigger signals shorter than t_{TB,cap}.

5.35 USCI (UART Mode), Recommended Operating Conditions

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---------------------|---|--|-----|---------------------|------|
| f _{USCI} | USCI input clock frequency | Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10% | | f _{SYSTEM} | MHz |
| f _{BITCLK} | BITCLK clock frequency (equals baud rate in MBaud) | | | 1 | MHz |

5.36 USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | V _{CC} | V _{IO} | MIN | MAX | UNIT |
|----------------|---|-----------------|------------------|-----|-----|------|
| t _r | UART receive deglitch time ⁽¹⁾ | 1.8 V | 1.62 V to 1.80 V | 50 | 600 | ns |
| | | 3.0 V | 1.62 V to 1.98 V | 50 | 600 | |

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

5.37 USCI (SPI Master Mode), Recommended Operating Conditions

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|-------------------|----------------------------|---|-----|---------------------|------|
| f _{USCI} | USCI input clock frequency | Internal: SMCLK or ACLK, Duty cycle = 50% ±10% | | f _{SYSTEM} | MHz |

5.38 USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾
(see [Figure 5-13](#) and [Figure 5-14](#))

| PARAMETER | | TEST CONDITIONS | V _{CC} | V _{IO} | MIN | MAX | UNIT |
|-----------------------|--|---|-----------------|------------------|-----|---------------------|------|
| f _{USCI} | USCI input clock frequency | SMCLK or ACLK, Duty cycle = 50% ±10% | | | | f _{SYSTEM} | MHz |
| t _{SU,MI} | SOMI input data setup time | PMMCOREV = 0 | 1.8 V | 1.62 V to 1.80 V | 55 | | ns |
| | | | 3.0 V | 1.62 V to 1.98 V | 55 | | |
| | | PMMCOREV = 3 | 2.4 V | 1.62 V to 1.98 V | 35 | | |
| | | | 3.0 V | 1.62 V to 1.98 V | 35 | | |
| t _{HD,MI} | SOMI input data hold time | PMMCOREV = 0 | 1.8 V | 1.62 V to 1.80 V | 0 | | ns |
| | | | 3.0 V | 1.62 V to 1.98 V | 0 | | |
| | | PMMCOREV = 3 | 2.4 V | 1.62 V to 1.98 V | 0 | | |
| | | | 3.0 V | 1.62 V to 1.98 V | 0 | | |
| t _{VALID,MO} | SIMO output data valid time ⁽²⁾ | UCLK edge to SIMO valid, C _L = 20 pF, PMMCOREV = 0 | 1.8 V | 1.62 V to 1.80 V | | 20 | ns |
| | | | 3.0 V | 1.62 V to 1.98 V | | 20 | |
| | | UCLK edge to SIMO valid, C _L = 20 pF, PMMCOREV = 3 | 2.4 V | 1.62 V to 1.98 V | | 16 | |
| | | | 3.0 V | 1.62 V to 1.98 V | | 16 | |
| t _{HD,MO} | SIMO output data hold time ⁽³⁾ | C _L = 20 pF, PMMCOREV = 0 | 1.8 V | 1.62 V to 1.80 V | -10 | | ns |
| | | | 3.0 V | 1.62 V to 1.98 V | -10 | | |
| | | C _L = 20 pF, PMMCOREV = 3 | 2.4 V | 1.62 V to 1.98 V | -10 | | |
| | | | 3.0 V | 1.62 V to 1.98 V | -10 | | |

- (1) $f_{UCxCLK} = 1/2t_{LO/Hi}$ with $t_{LO/Hi} \geq \max(t_{VALID,MO}(USCI) + t_{SU,SI}(Slave), t_{SU,MI}(USCI) + t_{VALID,SO}(Slave))$
For the slave parameters $t_{SU,SI}(Slave)$ and $t_{VALID,SO}(Slave)$, see the SPI parameters of the attached slave.
- (2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-13](#) and [Figure 5-14](#).
- (3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in [Figure 5-13](#) and [Figure 5-14](#).

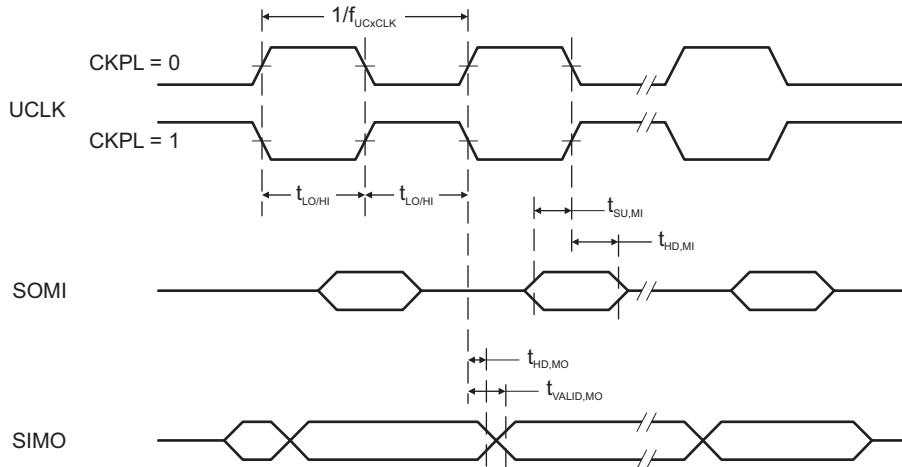


Figure 5-13. SPI Master Mode, CKPH = 0

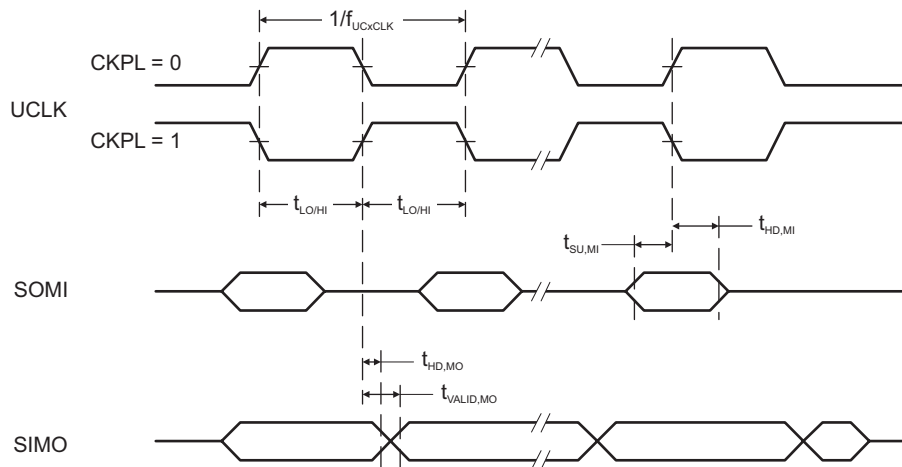


Figure 5-14. SPI Master Mode, CKPH = 1

5.39 USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾
(see [Figure 5-15](#) and [Figure 5-16](#))

| PARAMETER | TEST CONDITIONS | V _{CC} | V _{IO} | MIN | MAX | UNIT |
|--|---|-----------------|------------------|-----|-----|------|
| t _{STE,LEAD} STE lead time, STE low to clock | PMMCOREV = 0 | 1.8 V | 1.62 V to 1.80 V | 12 | | ns |
| | | 3.0 V | 1.62 V to 1.98 V | 12 | | |
| | PMMCOREV = 3 | 2.4 V | 1.62 V to 1.98 V | 10 | | |
| | | 3.0 V | 1.62 V to 1.98 V | 10 | | |
| t _{STE,LAG} STE lag time, Last clock to STE high | PMMCOREV = 0 | 1.8 V | 1.62 V to 1.80 V | 6 | | ns |
| | | 3.0 V | 1.62 V to 1.98 V | 6 | | |
| | PMMCOREV = 3 | 2.4 V | 1.62 V to 1.98 V | 6 | | |
| | | 3.0 V | 1.62 V to 1.98 V | 6 | | |
| t _{STE,ACC} STE access time, STE low to SOMI data out | PMMCOREV = 0 | 1.8 V | 1.62 V to 1.80 V | | 65 | ns |
| | | 3.0 V | 1.62 V to 1.98 V | | 65 | |
| | PMMCOREV = 3 | 2.4 V | 1.62 V to 1.98 V | | 45 | |
| | | 3.0 V | 1.62 V to 1.98 V | | 45 | |
| t _{STE,DIS} STE disable time, STE high to SOMI high impedance | PMMCOREV = 0 | 1.8 V | 1.62 V to 1.80 V | | 35 | ns |
| | | 3.0 V | 1.62 V to 1.98 V | | 35 | |
| | PMMCOREV = 3 | 2.4 V | 1.62 V to 1.98 V | | 25 | |
| | | 3.0 V | 1.62 V to 1.98 V | | 25 | |
| t _{SU,SI} SIMO input data setup time | PMMCOREV = 0 | 1.8 V | 1.62 V to 1.80 V | 5 | | ns |
| | | 3.0 V | 1.62 V to 1.98 V | 5 | | |
| | PMMCOREV = 3 | 2.4 V | 1.62 V to 1.98 V | 5 | | |
| | | 3.0 V | 1.62 V to 1.98 V | 5 | | |
| t _{HD,SI} SIMO input data hold time | PMMCOREV = 0 | 1.8 V | 1.62 V to 1.80 V | 5 | | ns |
| | | 3.0 V | 1.62 V to 1.98 V | 5 | | |
| | PMMCOREV = 3 | 2.4 V | 1.62 V to 1.98 V | 5 | | |
| | | 3.0 V | 1.62 V to 1.98 V | 5 | | |
| t _{VALID,SO} SOMI output data valid time ⁽²⁾ | UCLK edge to SOMI valid, C _L = 20 pF, PMMCOREV = 0 | 1.8 V | 1.62 V to 1.80 V | | 75 | ns |
| | | 3.0 V | 1.62 V to 1.98 V | | 75 | |
| | UCLK edge to SOMI valid, C _L = 20 pF, PMMCOREV = 3 | 2.4 V | 1.62 V to 1.98 V | | 50 | |
| | | 3.0 V | 1.62 V to 1.98 V | | 50 | |
| t _{HD,SO} SOMI output data hold time ⁽³⁾ | C _L = 20 pF, PMMCOREV = 0 | 1.8 V | 1.62 V to 1.80 V | 18 | | ns |
| | | 3.0 V | 1.62 V to 1.98 V | 18 | | |
| | C _L = 20 pF, PMMCOREV = 3 | 2.4 V | 1.62 V to 1.98 V | 10 | | |
| | | 3.0 V | 1.62 V to 1.98 V | 10 | | |

- (1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
- (2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-15](#) and [Figure 5-16](#).
- (3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-15](#) and [Figure 5-16](#).

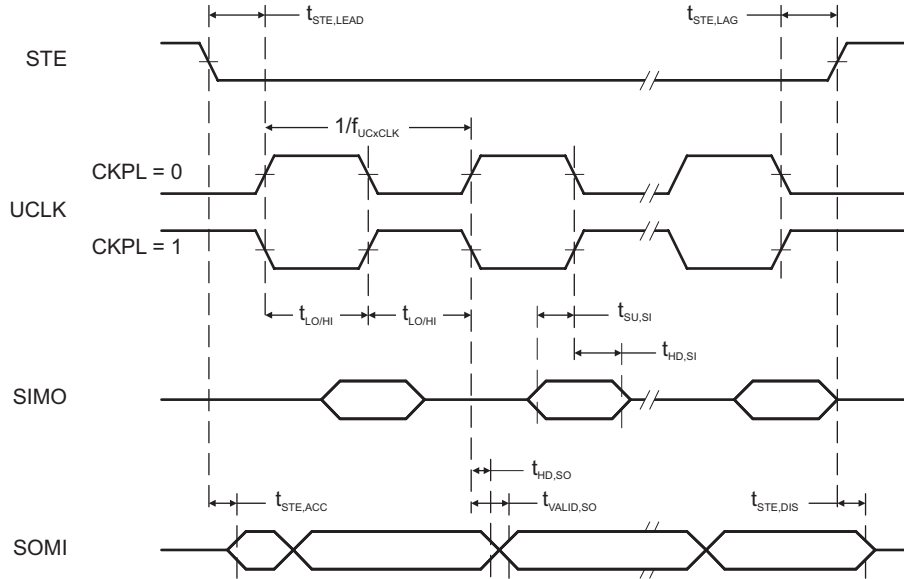


Figure 5-15. SPI Slave Mode, CKPH = 0

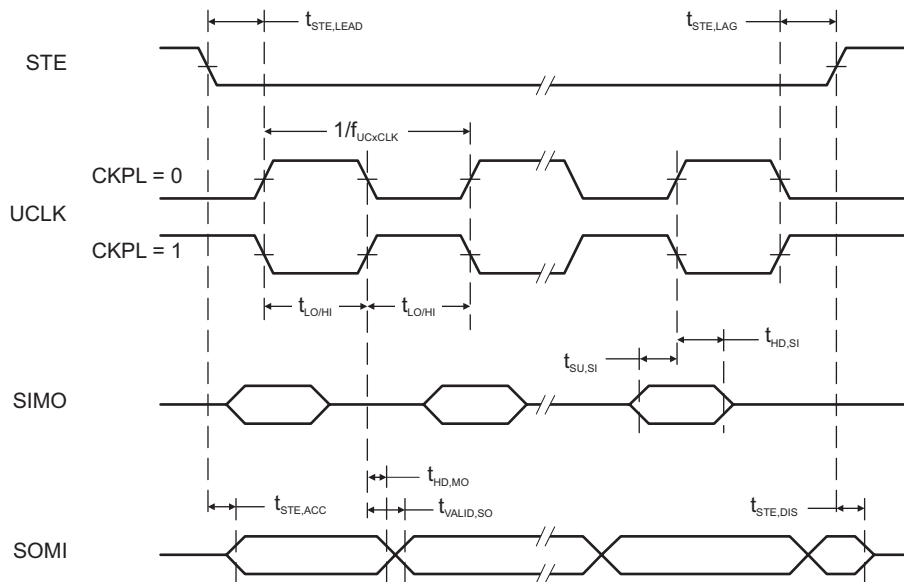


Figure 5-16. SPI Slave Mode, CKPH = 1

5.40 USCI (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5-17](#))

| PARAMETER | TEST CONDITIONS | V _{CC} | V _{IO} ⁽¹⁾ | MIN | MAX | UNIT | |
|---------------------|---|--|--------------------------------|---------------------|-----|------|----|
| f _{USCI} | USCI input clock frequency | | | f _{SYSTEM} | | MHz | |
| f _{SCL} | SCL clock frequency | 2.2 V, 3 V | 1.62 V to 1.98 V | 0 | 400 | kHz | |
| t _{HD,STA} | Hold time (repeated) START | f _{SCL} ≤ 100 kHz f _{SCL} > 100 kHz | 2.2 V, 3 V | 1.62 V to 1.98 V | 4.0 | μs | |
| | 0.6 | | | | | | |
| t _{SU,STA} | Setup time for a repeated START | f _{SCL} ≤ 100 kHz f _{SCL} > 100 kHz | 2.2 V, 3 V | 1.62 V to 1.98 V | 4.7 | μs | |
| | 0.6 | | | | | | |
| t _{HD,DAT} | Data hold time | | 2.2 V, 3 V | 1.62 V to 1.98 V | 0 | ns | |
| t _{SU,DAT} | Data setup time | | 2.2 V, 3 V | 1.62 V to 1.98 V | 250 | ns | |
| t _{SU,STO} | Setup time for STOP | f _{SCL} ≤ 100 kHz f _{SCL} > 100 kHz | 2.2 V, 3 V | 1.62 V to 1.98 V | 4.0 | μs | |
| | 0.6 | | | | | | |
| t _{SP} | Pulse duration of spikes suppressed by input filter | | 2.2 V, 3 V | 1.62 V to 1.98 V | 50 | 600 | ns |

(1) In all test conditions, V_{IO} ≤ V_{CC}

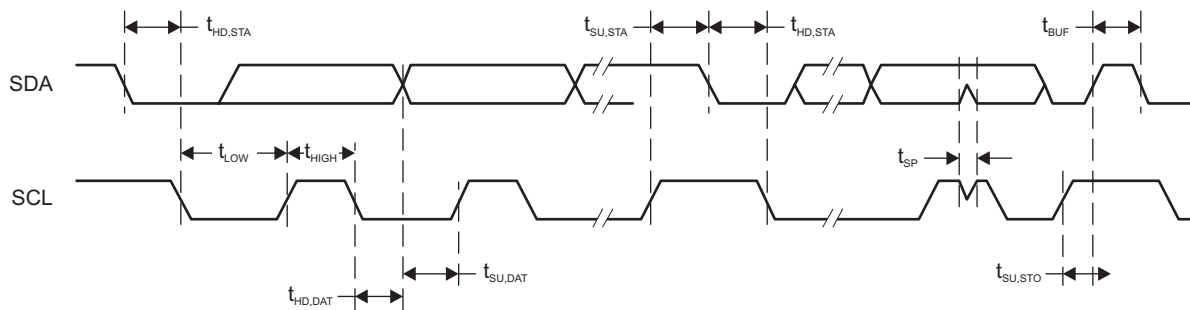


Figure 5-17. I²C Mode Timing

5.41 10-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------------|---|---|-----------------|-----|-----|------------------|------|
| AV _{CC} | Analog supply voltage | AV _{CC} and DV _{CC} are connected together, AV _{SS} and DV _{SS} are connected together, V _(AVSS) = V _(DVSS) = 0 V | | 1.8 | | 3.6 | V |
| V _(Ax) | Analog input voltage range ⁽²⁾ | All ADC10_A pins: P1.0 to P1.5 and P3.6 and P3.7 terminals | | 0 | | AV _{CC} | V |
| I _{ADC10_A} | Operating supply current into AV _{CC} terminal, REF module and reference buffer off | f _{ADC10CLK} = 5.0 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 00 | 2.2 V | | 60 | 100 | μA |
| | | | 3 V | | 75 | 110 | |
| | Operating supply current into AV _{CC} terminal, REF module on, reference buffer on | f _{ADC10CLK} = 5.0 MHz, ADC10ON = 1, REFON = 1, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 01 | 3 V | | 113 | 150 | |
| | Operating supply current into AV _{CC} terminal, REF module off, reference buffer on | f _{ADC10CLK} = 5.0 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 10, VREF = 2.5 V | 3 V | | 105 | 140 | |
| | Operating supply current into AV _{CC} terminal, REF module off, reference buffer off | f _{ADC10CLK} = 5.0 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 11, VREF = 2.5 V | 3 V | | 70 | 110 | |
| C _I | Input capacitance | Only one terminal Ax can be selected at one time from the pad to the ADC10_A capacitor array including wiring and pad. | 2.2 V | | 3.5 | | pF |
| R _I | Input MUX ON resistance | AV _{CC} > 2 V, 0 V ≤ V _{Ax} ≤ AV _{CC} | | | | 36 | kΩ |
| | | 1.8 V < AV _{CC} < 2 V, 0 V ≤ V _{Ax} ≤ AV _{CC} | | | | 96 | |

(1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.

(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. The external reference voltage requires decoupling capacitors. See 0.

5.42 10-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|--|---|-----------------|------|-----------------------------------|-----|------|
| f _{ADC10CLK} | Input clock frequency | For specified performance of ADC10_A linearity parameters | 2.2 V, 3 V | 0.45 | 5 | 5.5 | MHz |
| f _{ADC10OSC} | Internal ADC10_A oscillator ⁽¹⁾ | ADC10DIV = 0, f _{ADC10CLK} = f _{ADC10OSC} | 2.2 V, 3 V | 4.2 | 4.8 | 5.4 | MHz |
| t _{CONVERT} | Conversion time | REFON = 0, Internal oscillator, 12 ADC10CLK cycles, 10-bit mode, f _{ADC10OSC} = 4 MHz to 5 MHz | 2.2 V, 3 V | 2.4 | | 3.0 | μs |
| | | External f _{ADC10CLK} from ACLK, MCLK or SMCLK, ADC10SSEL ≠ 0 | | | 12 × 1 / f _{ADC10CLK} | | |
| t _{ADC10ON} | Turn on settling time of the ADC | See (2) | | | | 100 | ns |
| t _{Sample} | Sampling time | R _S = 1000 Ω, R _I = 96 k Ω, C _I = 3.5 pF ⁽³⁾ | 1.8 V | 3 | | | μs |
| | | | 3.0 V | 1 | | | μs |

(1) The ADC10OSC is sourced directly from MODOSC inside the UCS.

(2) The condition is that the error in a conversion started after t_{ADC10ON} is less than ±0.5 LSB. The reference and input signal are already settled.

(3) Approximately 8 Tau (τ) are needed to get an error of less than ±0.5 LSB

5.43 10-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------|------------------------------|--|-----------------|-----|------|------|------|
| E _I | Integral linearity error | 1.4 V ≤ (V _{eREF+} – V _{eREF-}) ≤ 1.6 V, C _{VeREF+} = 20 pF | 2.2 V, 3 V | | | ±1.0 | LSB |
| | | 1.6 V < (V _{eREF+} – V _{eREF-}) ≤ V _{AVCC} , C _{VeREF+} = 20 pF | | | | ±1.0 | |
| E _D | Differential linearity error | 1.4 V ≤ (V _{eREF+} – V _{eREF-}), C _{VeREF+} = 20 pF | 2.2 V, 3 V | | | ±1.0 | LSB |
| E _O | Offset error | 1.4 V ≤ (V _{eREF+} – V _{eREF-}), C _{VeREF+} = 20 pF Internal impedance of source R _S < 100 Ω | 2.2 V, 3 V | | | ±1.0 | LSB |
| E _G | Gain error | 1.4 V ≤ (V _{eREF+} – V _{eREF-}), C _{VeREF+} = 20 pF, ADC10SREFX = 11b | 2.2 V, 3 V | | | ±1.0 | LSB |
| E _T | Total unadjusted error | 1.4 V ≤ (V _{eREF+} – V _{eREF-}), C _{VeREF+} = 20 pF, ADC10SREFX = 11b | 2.2 V, 3 V | | ±1.0 | ±2.0 | LSB |

5.44 REF, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|--|---|---|-----------------|-----|------------------|------|
| V _{eREF+} | Positive external reference voltage input | V _{eREF+} > V _{eREF-} ⁽²⁾ | | 1.4 | AV _{CC} | V |
| V _{eREF-} | Negative external reference voltage input | V _{eREF+} > V _{eREF-} ⁽³⁾ | | 0 | 1.2 | V |
| (V _{eREF+} – V _{eREF-}) | Differential external reference voltage input | V _{eREF+} > V _{eREF-} ⁽⁴⁾ | | 1.4 | AV _{CC} | V |
| I _{VeREF+} , I _{VeREF-} | Static input current | 1.4 V ≤ V _{eREF+} ≤ V _{AVCC} , V _{eREF-} = 0 V, f _{ADC10CLK} = 5 MHz, ADC10SHTX = 0x0001, Conversion rate = 200 ksp/s | 2.2 V, 3 V | -26 | 26 | μA |
| | | 1.4 V ≤ V _{eREF+} ≤ V _{AVCC} , V _{eREF-} = 0 V, f _{ADC10CLK} = 5 MHz, ADC10SHTX = 0x1000, Conversion rate = 20 ksp/s | 2.2 V, 3 V | -1 | 1 | |
| C _{VeREF+} , C _{VeREF-} | Capacitance at VeREF+ or VeREF- terminal | ⁽⁵⁾ | | 10 | | μF |

- (1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance (C_I) is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
- (2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
- (3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
- (4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
- (5) Two decoupling capacitors, 10 μF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. See also the [MSP430F5xx and MSP430F6xx Family User's Guide](#).

5.45 REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------------|--|-----------------|-------|-------|-------|------------|
| V _{REF+} | REFVSEL = {2} for 2.5 V, REFON = 1 | 3 V | 2.472 | 2.51 | 2.548 | V |
| | REFVSEL = {1} for 2.0 V, REFON = 1 | 3 V | 1.96 | 1.99 | 2.02 | |
| | REFVSEL = {0} for 1.5 V, REFON = 1 | 2.2 V, 3 V | 1.472 | 1.495 | 1.518 | |
| AV _{CC(min)} | REFVSEL = {0} for 1.5 V | | 1.8 | | | V |
| | REFVSEL = {1} for 2.0 V | | 2.2 | | | |
| | REFVSEL = {2} for 2.5 V | | 2.7 | | | |
| I _{REF+} | f _{ADC10CLK} = 5.0 MHz, REFON = 1, REFBURST = 0, REFVSEL = {2} for 2.5 V | 3 V | | 18 | 24 | μA |
| | f _{ADC10CLK} = 5.0 MHz, REFON = 1, REFBURST = 0, REFVSEL = {1} for 2.0 V | 3 V | | 15.5 | 21 | |
| | f _{ADC10CLK} = 5.0 MHz, REFON = 1, REFBURST = 0, REFVSEL = {0} for 1.5 V | 3 V | | 13.5 | 21 | |
| TC _{REF+} | I _{VREF+} = 0 A, REFVSEL = {0, 1, 2}, REFON = 1 | | | 30 | 50 | ppm/ °C |
| I _{SENSOR} | REFON = 0, INCH = 0Ah, ADC10ON = N A, T _A = 30°C | 2.2 V | | 20 | 22 | μA |
| | | 3 V | | 20 | 22 | |
| V _{SENSOR} | See ⁽⁵⁾ | 2.2 V | | 770 | | mV |
| | | 3 V | | 770 | | |
| V _{MID} | ADC10ON = 1, INCH = 0Bh, V _{MID} ≈ 0.5 × V _{AVCC} | 2.2 V | 1.06 | 1.1 | 1.14 | V |
| | | 3 V | 1.46 | 1.5 | 1.54 | |
| t _{SENSOR(sample)} | ADC10ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB | | | 30 | | μs |
| t _{VMID(sample)} | ADC10ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB | | | 1 | | μs |
| PSRR _{DC} | AV _{CC} = AV _{CC(min)} to AV _{CC(max)} , T _A = 25°C, REFVSEL = {0, 1, 2}, REFON = 1 | | | 120 | | μV/V |
| PSRR _{AC} | AV _{CC} = AV _{CC(min)} to AV _{CC(max)} , T _A = 25°C, f = 1 kHz, ΔV _{pp} = 100 mV REFVSEL = {0, 1, 2}, REFON = 1 | | | 6.4 | | mV/V |
| t _{SETTLE} | AV _{CC} = AV _{CC(min)} to AV _{CC(max)} REFVSEL = {0, 1, 2}, REFON = 0 → 1 | | | 75 | | μs |

(1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.

(2) The internal reference current is supplied from terminal AVCC. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an analog-to-digital conversion.

(3) Calculated using the box method: (MAX(−40°C to 85°C) − MIN(−40°C to 85°C)) / MIN(−40°C to 85°C)/(85°C − (−40°C)).

(4) The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is already included in I_{REF+}.

(5) The temperature sensor offset can be significant. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.

(6) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time t_{SENSOR(on)}.

(7) The on-time t_{VMID(on)} is included in the sampling time t_{VMID(sample)}; no additional on time is needed.

(8) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB.

5.46 Comparator_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|------------------------|---|---|------------|--------------------------------------|------------------------------------|--------------------------------------|----|
| V _{CC} | Supply voltage | | 1.8 | | 3.6 | V | |
| I _{AVCC_COMP} | Comparator operating supply current into AVCC, excludes reference resistor ladder | CBPWRMD = 00, CBON = 1, CBRsX = 00 | 1.8 V | | 38 | μA | |
| | | | 2.2 V | | 31 | | |
| | | | 3 V | | 32 | | |
| | | 2.2 V, 3 V | | 10 | 17 | | |
| | CBPWRMD = 10, CBON = 1, CBRsX = 00 | 2.2 V, 3 V | | 0.2 | 0.85 | | |
| V _{REF} | Reference voltage level | CBREFLx = 01, CBREFACC = 0 | ≥ 1.8 V | 1.44 | ±2.5% | V | |
| | | CBREFLx = 10, CBREFACC = 0 | ≥ 2.2 V | 1.92 | ±2.5% | | |
| | | CBREFLx = 11, CBREFACC = 0 | ≥ 3.0 V | 2.39 | ±2.5% | | |
| I _{AVCC_REF} | Quiescent current of resistor ladder into AVCC, including REF module current | CBREFACC = 1, CBREFLx = 01, CBRsX = 10, REFON = 0, CBON = 0 | 2.2 V, 3 V | 17 | 22 | μA | |
| | | CBREFACC = 0, CBREFLx = 01, CBRsX = 10, REFON = 0, CBON = 0 | 2.2 V, 3 V | 33 | 40 | | |
| V _{IC} | Common mode input range | | 0 | | V _{CC} – 1 | V | |
| V _{OFFSET} | Input offset voltage | CBPWRMD = 00 | | –20 | 20 | mV | |
| | | CBPWRMD = 01 or 10 | | –10 | 10 | | |
| C _{IN} | Input capacitance | | | 5 | | pF | |
| R _{SIN} | Series input resistance | On (switch closed) | | 3 | 4 | kΩ | |
| | | Off (switch open) | | 50 | | MΩ | |
| t _{PD} | Propagation delay, response time | CBPWRMD = 00, CBF = 0 | | | 450 | ns | |
| | | CBPWRMD = 01, CBF = 0 | | | 600 | | |
| | | CBPWRMD = 10, CBF = 0 | | | 50 | | μs |
| t _{PD,filter} | Propagation delay with filter active | CBPWRMD = 00, CBON = 1, CBF = 1, CBFdLY = 00 | | 0.35 | 0.6 | 1.5 | μs |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBFdLY = 01 | | 0.6 | 1.0 | 1.8 | |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBFdLY = 10 | | 1.0 | 1.8 | 3.4 | |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBFdLY = 11 | | 1.8 | 3.4 | 6.5 | |
| t _{EN_CMP} | Comparator enable time | CBON = 0 → 1, CBPWRMD = 00 or 01 | | 1 | 2 | μs | |
| | | CBON = 0 → 1, CBPWRMD = 10 | | | 100 | | |
| t _{EN_REF} | Resistor reference enable time | CBON = 0 → 1 | | 1.0 | 1.5 | μs | |
| TC _{CB_REF} | Temperature coefficient reference of V _{CB_REF} | | | | 50 | ppm/°C | |
| V _{CB_REF} | Reference voltage for a given tap | V _{IN} = reference into resistor ladder, n = 0 to 31 | | $\frac{V_{IN} \times (n + 0.5)}{32}$ | $\frac{V_{IN} \times (n + 1)}{32}$ | $\frac{V_{IN} \times (n + 1.5)}{32}$ | V |

5.47 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | T _J | MIN | TYP | MAX | UNIT |
|-----------------------------|--|----------------|-----------------|-----------------|-----|--------|
| DV _{CC(PGM/ERASE)} | Program and erase supply voltage | | 1.8 | | 3.6 | V |
| I _{PGM} | Average supply current from DV _{CC} during program | | | 3 | 5 | mA |
| I _{ERASE} | Average supply current from DV _{CC} during erase | | | 6 | 11 | mA |
| I _{MERASE, IBANK} | Average supply current from DV _{CC} during mass erase or bank erase | | | 6 | 11 | mA |
| t _{CPT} | Cumulative program time ⁽¹⁾ | | | | 16 | ms |
| | Program and erase endurance | | 10 ⁴ | 10 ⁵ | | cycles |
| t _{Retention} | Data retention duration | 25°C | 100 | | | years |
| t _{Word} | Word or byte program time ⁽²⁾ | | 64 | | 85 | μs |
| t _{Block, 0} | Block program time for first byte or word ⁽²⁾ | | 49 | | 65 | μs |
| t _{Block, 1–(N–1)} | Block program time for each additional byte or word, except for last byte or word ⁽²⁾ | | 37 | | 49 | μs |
| t _{Block, N} | Block program time for last byte or word ⁽²⁾ | | 55 | | 73 | μs |
| t _{Erase} | Erase time for segment, mass erase, and bank erase when available ⁽²⁾ | | 23 | | 32 | ms |
| f _{MCLK,MGR} | MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4.MGR1 = 1) | | 0 | | 1 | MHz |

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word or byte write mode and block write mode.

(2) These values are hardwired into the state machine of the flash controller.

5.48 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | V _{CC} | V _{IO} | MIN | TYP | MAX | UNIT |
|-----------------------|--|-----------------|------------------|-------|-----|-----|------|
| f _{SBW} | Spy-Bi-Wire input frequency | 2.2 V, 3 V | 1.62 V to 1.98 V | 0 | | 20 | MHz |
| t _{SBW,Low} | Spy-Bi-Wire low clock pulse duration | 2.2 V, 3 V | 1.62 V to 1.98 V | 0.025 | | 15 | μs |
| t _{SBW,En} | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) ⁽¹⁾ | 2.2 V, 3 V | 1.62 V to 1.98 V | | | 1 | μs |
| t _{SBW,Rst} | Spy-Bi-Wire return to normal operation time | 2.2 V, 3 V | 1.62 V to 1.98 V | 15 | | 100 | μs |
| f _{TCK} | TCK input frequency for 4-wire JTAG ⁽²⁾ | 2.2 V | 1.62 V to 1.98 V | 0 | | 5 | MHz |
| | | 3 V | 1.62 V to 1.98 V | 0 | | 10 | |
| R _{internal} | Internal pulldown resistance on TEST | 2.2 V, 3 V | 1.62 V to 1.98 V | 45 | 60 | 80 | kΩ |

(1) Tools that access the Spy-Bi-Wire interface must wait for the t_{SBW,En} time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.

(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

5.49 DVIO BSL Entry

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | V _{CC} | V _{IO} | MIN | MAX | UNIT |
|----------------------|--|-----------------|------------------|-----|-----|------|
| t _{SU, BSL} | Setup time BSL to $\overline{\text{RST/NMI}}$ ⁽¹⁾ | 2.2 V, 3 V | 1.62 V to 1.98 V | 100 | | ns |
| t _{HO, BSL} | Hold time BSL to $\overline{\text{RST/NMI}}$ ⁽²⁾ | 2.2 V, 3 V | 1.62 V to 1.98 V | 350 | | μs |

(1) AVCC, DVCC, and DVIO stable and within specification.

(2) BSL must remain logic high long enough for the boot code to detect its level and enter the BSL sequence. After the minimum hold time is achieved, BSL is a don't care.

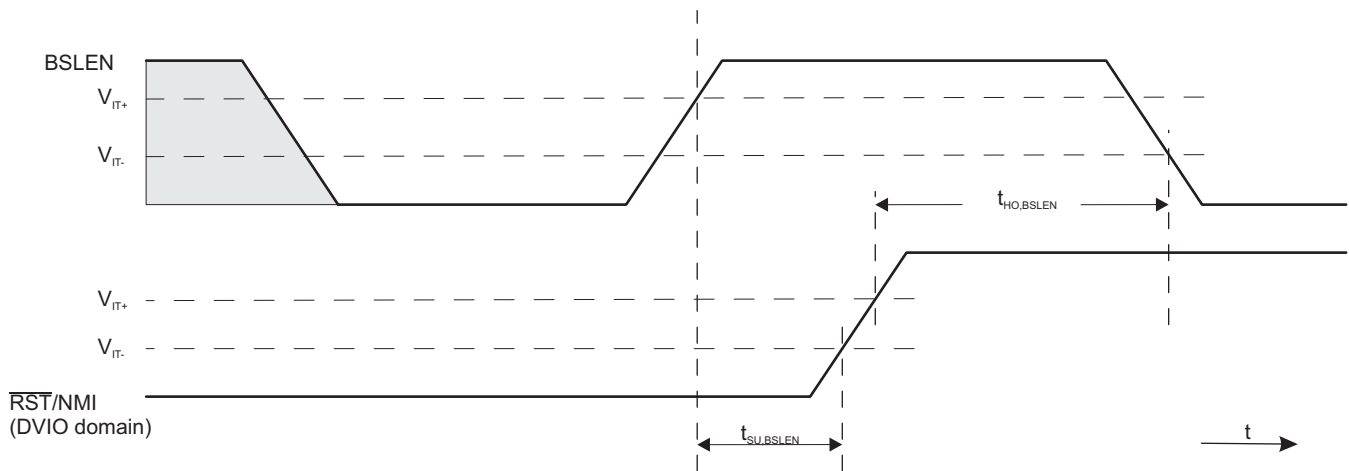


Figure 5-18. DVIO BSL Entry Timing

6 Detailed Description

6.1 CPU ([Link to user's guide](#))

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers (see [Figure 6-1](#)).

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

| | |
|--------------------------|-----------|
| Program Counter | PC/R0 |
| Stack Pointer | SP/R1 |
| Status Register | SR/CG1/R2 |
| Constant Generator | CG2/R3 |
| General-Purpose Register | R4 |
| General-Purpose Register | R5 |
| General-Purpose Register | R6 |
| General-Purpose Register | R7 |
| General-Purpose Register | R8 |
| General-Purpose Register | R9 |
| General-Purpose Register | R10 |
| General-Purpose Register | R11 |
| General-Purpose Register | R12 |
| General-Purpose Register | R13 |
| General-Purpose Register | R14 |
| General-Purpose Register | R15 |

Figure 6-1. CPU Registers

6.2 Operating Modes

These MCUs have one active mode and six software selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

Software can configure the following operating modes:

- Active mode (AM)
 - All clocks are active
- Low-power mode 0 (LPM0)
 - CPU is disabled
 - ACLK and SMCLK remain active, MCLK is disabled
 - FLL loop control remains active
- Low-power mode 1 (LPM1)
 - CPU is disabled
 - FLL loop control is disabled
 - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
 - CPU is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DCO dc-generator remains enabled
 - ACLK remains active
- Low-power mode 3 (LPM3)
 - CPU is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DCO dc generator is disabled
 - ACLK remains active
- Low-power mode 4 (LPM4)
 - CPU is disabled
 - ACLK is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DCO dc generator is disabled
 - Crystal oscillator is stopped
 - Complete data retention
- Low-power mode 4.5 (LPM4.5)
 - Internal regulator disabled
 - No data retention
 - Wake-up signal from $\overline{\text{RST}}/\text{NMI}$, P1, and P2

6.3 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see [Table 6-1](#)). The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 6-1. Interrupt Sources, Flags, and Vectors

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|--|------------------|--------------|-------------|
| System Reset Power up External reset Watchdog time-out, password violation Flash memory password violation PMM password violation | WDTIFG, KEYV (SYSRSTIV) ⁽¹⁾⁽²⁾ | Reset | 0FFFEh | 63, highest |
| System NMI PMM Vacant memory access JTAG mailbox | SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV) ⁽¹⁾ | (Non)maskable | 0FFFCh | 62 |
| User NMI NMI Oscillator fault Flash memory access violation | NMIIFG, OFIFG, ACCVIFG, BUSIFG (SYSUNIV) ⁽¹⁾⁽²⁾ | (Non)maskable | 0FFFAh | 61 |
| COMP_B | Comparator B interrupt flags (CBIV) ⁽¹⁾⁽³⁾ | Maskable | 0FFF8h | 60 |
| TB0 | TB0CCR0 CCIFG0 ⁽³⁾ | Maskable | 0FFF6h | 59 |
| TB0 | TB0CCR1 CCIFG1 to TB0CCR6 CCIFG6, TB0IFG (TB0IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFF4h | 58 |
| Watchdog timer interval timer mode | WDTIFG | Maskable | 0FFF2h | 57 |
| USCI_A0 receive or transmit | UCA0RXIFG, UCA0TXIFG (UCA0IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFF0h | 56 |
| USCI_B0 receive or transmit | UCB0RXIFG, UCB0TXIFG (UCB0IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFEEh | 55 |
| ADC10_A | ADC10IFG0 ⁽¹⁾⁽³⁾⁽⁴⁾ | Maskable | 0FFECCh | 54 |
| TA0 | TA0CCR0 CCIFG0 ⁽³⁾ | Maskable | 0FFEAh | 53 |
| TA0 | TA0CCR1 CCIFG1 to TA0CCR4 CCIFG4, TA0IFG (TA0IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFE8h | 52 |
| Reserved | Reserved | Maskable | 0FFE6h | 51 |
| DMA | DMA0IFG, DMA1IFG, DMA2IFG (DMAIV) ⁽¹⁾⁽³⁾ | Maskable | 0FFE4h | 50 |
| TA1 | TA1CCR0 CCIFG0 ⁽³⁾ | Maskable | 0FFE2h | 49 |
| TA1 | TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFE0h | 48 |
| I/O Port P1 | P1IFG.0 to P1IFG.7 (P1IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFDEh | 47 |
| USCI_A1 receive or transmit | UCA1RXIFG, UCA1TXIFG (UCA1IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFDCh | 46 |
| USCI_B1 receive or transmit | UCB1RXIFG, UCB1TXIFG (UCB1IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFDAh | 45 |
| TA2 | TA2CCR0 CCIFG0 ⁽³⁾ | Maskable | 0FFD8h | 44 |
| TA2 | TA2CCR1 CCIFG1 to TA2CCR2 CCIFG2, TA2IFG (TA2IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFD6h | 43 |
| I/O port P2 | P2IFG.0 to P2IFG.7 (P2IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFD4h | 42 |
| RTC_A | RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV) ⁽¹⁾⁽³⁾ | Maskable | 0FFD2h | 41 |

(1) Multiple source flags

(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.

(Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.

(3) Interrupt flags are located in the module.

(4) Only on devices with ADC, otherwise reserved

Table 6-1. Interrupt Sources, Flags, and Vectors (continued)

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|------------------|-------------------------|------------------|--------------|-----------|
| Reserved | Reserved ⁽⁵⁾ | | 0FFD0h | 40 |
| | | | ⋮ | ⋮ |
| | | | 0FF80h | 0, lowest |

(5) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, TI recommends reserving these locations.

6.4 Memory Organization

Table 6-2 summarizes the memory map.

Table 6-2. Memory Organization⁽¹⁾

| | | MSP430F5227 MSP430F5222 MSP430F5217 MSP430F5212 | MSP430F5229 MSP430F5224 MSP430F5219 MSP430F5214 |
|--|------------|--|--|
| Memory (flash) Main: interrupt vector | Total Size | 64KB 00FFFFh to 00FF80h | 128KB 00FFFFh to 00FF80h |
| Main: code memory | Bank D | N/A | 32KB 0243FFh to 01C400h |
| | Bank C | N/A | 32KB 01C3FFh to 014400h |
| | Bank B | 32KB 0143FFh to 00C400h | 32KB 0143FFh to 00C400h |
| | Bank A | 32KB 00C3FFh to 004400h | 32KB 00C3FFh to 004400h |
| RAM | Sector 3 | 2KB 0043FFh to 003C00h | 2KB 0043FFh to 003C00h |
| | Sector 2 | 2KB 003BFFh to 003400h | 2KB 003BFFh to 003400h |
| | Sector 1 | 2KB 0033FFh to 002C00h | 2KB 0033FFh to 002C00h |
| | Sector 0 | 2KB 002BFFh to 002400h | 2KB 002BFFh to 002400h |
| TI factory memory (ROM) | A | 128 B 001BFFh to 001B80h | 128 B 001BFFh to 001B80h |
| | B | 128 B 001B7Fh to 001B00h | 128 B 001B7Fh to 001B00h |
| | C | 128 B 001AFFh to 001A80h | 128 B 001AFFh to 001A80h |
| | D | 128 B 001A7Fh to 001A00h | 128 B 001A7Fh to 001A00h |
| Information memory (flash) | Info A | 128 B 0019FFh to 001980h | 128 B 0019FFh to 001980h |
| | Info B | 128 B 00197Fh to 001900h | 128 B 00197Fh to 001900h |
| | Info C | 128 B 0018FFh to 001880h | 128 B 0018FFh to 001880h |
| | Info D | 128 B 00187Fh to 001800h | 128 B 00187Fh to 001800h |

(1) N/A = Not available

Table 6-2. Memory Organization⁽¹⁾ (continued)

| | | MSP430F5227 MSP430F5222 MSP430F5217 MSP430F5212 | MSP430F5229 MSP430F5224 MSP430F5219 MSP430F5214 |
|---------------------------------|-------|--|--|
| Bootloader (BSL) memory (flash) | BSL 3 | 512 B 0017FFh to 001600h | 512 B 0017FFh to 001600h |
| | BSL 2 | 512 B 0015FFh to 001400h | 512 B 0015FFh to 001400h |
| | BSL 1 | 512 B 0013FFh to 001200h | 512 B 0013FFh to 001200h |
| | BSL 0 | 512 B 0011FFh to 001000h | 512 B 0011FFh to 001000h |
| Peripherals | Size | 4KB 000FFFh to 0h | 4KB 000FFFh to 0h |

6.5 Bootloader (BSL)

The BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the device memory by the BSL is protected by an user-defined password. Because the F522x and F521x have split I/O power domains, it is possible to interface with the BSL from either the DVCC or DVIO supply domains. This is useful when the MSP430 is interfacing to a host on the DVIO supply domain. The BSL interface on the DVIO supply domain (see [Table 6-3](#)) uses the USCI_A0 module configured as a UART. The BSL interface on the DVCC supply domain (see [Table 6-4](#)) uses a timer-based UART.

NOTE

Devices from TI come factory programmed with the timer-based UART BSL only. If the USCI-based BSL is preferred, it is also available, but it must be programmed by the user.

When using the DVIO supply domain for the BSL, entry to the BSL requires a specific sequence on the $\overline{\text{RST}}/\text{NMI}$ and BSLLEN pins. [Table 6-3](#) shows the required pins and their functions. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For a complete description of the features of the BSL and its implementation, see the [MSP430 Flash Device Bootloader \(BSL\) User's Guide](#). The BSL on the DVIO supply domain uses the USCI_A0 module configured as a UART.

NOTE

To invoke the BSL from the DVIO domain, the $\overline{\text{RST}}/\text{NMI}$ and BSLLEN pins must be used for the entry sequence (see [Section 5.49](#)). It is critical not to confuse the $\overline{\text{RST}}/\text{NMI}$ pin with the $\overline{\text{RSTDVCC}}/\text{SBWTDIO}$ pin. In other MSP430 devices, SBWTDIO is shared with the $\overline{\text{RST}}/\text{NMI}$ pin and $\overline{\text{RSTDVCC}}$ does not exist. Additional information can be found in [Designing With MSP430F522x and MSP430F521x Devices](#).

Table 6-3. DVIO BSL Pin Requirements and Functions

| DEVICE SIGNAL | BSL FUNCTION |
|------------------------------------|---------------------|
| $\overline{\text{RST}}/\text{NMI}$ | External reset |
| BSLEN | Enable BSL |
| P3.3 | Data transmit |
| P3.4 | Data receive |
| DVCC, AVCC | Device power supply |
| DVIO | I/O power supply |
| DVSS | Ground supply |

For applications in which it is desirable to have BSL communication based on the DVCC supply domain, entry to the BSL requires a specific sequence on the $\overline{\text{RSTDVCC}}/\text{SBWTDIO}$ and TEST/SBWTDIO pins. [Table 6-4](#) shows the required pins and their function.

NOTE

To invoke the BSL from the DVCC domain, the $\overline{\text{RSTDVCC}}/\text{SBWTDIO}$ and TEST/SBWTDIO pins must be used for the entry sequence. It is critical not to confuse the $\overline{\text{RST}}/\text{NMI}$ pin with the $\overline{\text{RSTDVCC}}/\text{SBWTDIO}$ pin. In other MSP430 devices, SBWTDIO is shared with the $\overline{\text{RST}}/\text{NMI}$ pin and $\overline{\text{RSTDVCC}}$ does not exist. Additional information can be found in [Designing With MSP430F522x and MSP430F521x Devices](#).

Table 6-4. DVCC BSL Pin Requirements and Functions

| DEVICE SIGNAL | BSL FUNCTION |
|--|---------------------|
| $\overline{\text{RSTDVCC}}/\text{SBWTDIO}$ | External reset |
| TEST/SBWTCK | Enable BSL |
| P1.1 | Data transmit |
| P1.2 | Data receive |
| DVCC, AVCC | Device power supply |
| DVIO | I/O power supply |
| DVSS | Ground supply |

6.6 JTAG Operation

6.6.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RSTDVCC}}/\text{SBWTDIO}$ is required to interface with MSP430 development tools and device programmers. The JTAG pin requirements are shown in [Table 6-5](#). For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For a complete description of the features of the JTAG interface and its implementation, see [MSP430 Programming With the JTAG Interface](#). Additional information can be found in [Designing With MSP430F522x and MSP430F521x Devices](#).

NOTE

All JTAG I/O pins are supplied by DVCC.

NOTE

On other MSP430 devices, the $\overline{\text{RST}}/\text{NMI}$ pin has been used for SBWTDIO, so care must be taken not to mistakenly use the incorrect pin. On the F522x and F521x series of devices, $\overline{\text{RSTDVCC}}$ is used for SBWTDIO as shown in [Table 6-5](#). Additional information can be found in [Designing With MSP430F522x and MSP430F521x Devices](#).

Table 6-5. JTAG Pin Requirements and Functions

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|--|-----------|-----------------------------|
| PJ.3/TCK | IN | JTAG clock input |
| PJ.2/TMS | IN | JTAG state control |
| PJ.1/TDI/TCLK | IN | JTAG data input, TCLK input |
| PJ.0/TDO | OUT | JTAG data output |
| TEST/SBWTCK | IN | Enable JTAG pins |
| $\overline{\text{RSTDVCC}}/\text{SBWTDIO}$ | IN | External reset |
| DVCC, AVCC | | Device power supply |
| DVIO | | I/O power supply |
| DVSS | | Ground supply |

6.6.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the 2-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. The Spy-Bi-Wire interface pin requirements are shown in [Table 6-6](#). For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#). For a complete description of the features of the JTAG interface and its implementation, see [MSP430 Programming With the JTAG Interface](#). Additional information can be found in [Designing With MSP430F522x and MSP430F521x Devices](#).

NOTE

All SBW I/O pins are supplied by DVCC.

NOTE

On other MSP430 devices, the $\overline{\text{RST}}/\text{NMI}$ pin has been used for SBWTDIO, so care must be taken not to mistakenly use the incorrect pin. On the F522x and F521x series of devices, $\overline{\text{RSTDVCC}}$ is used for SBWTDIO as shown in [Table 6-6](#). Additional information can be found in [Designing With MSP430F522x and MSP430F521x Devices](#).

Table 6-6. Spy-Bi-Wire Pin Requirements and Functions

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|--|-----------|-------------------------------|
| TEST/SBWTK | IN | Spy-Bi-Wire clock input |
| $\overline{\text{RSTDVCC}}/\text{SBWTDIO}$ | IN, OUT | Spy-Bi-Wire data input/output |
| DVCC, AVCC | | Device power supply |
| DVIO | | I/O power supply |
| DVSS | | Ground supply |

6.7 Flash Memory ([Link to user's guide](#))

The flash memory can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

6.8 RAM ([Link to user's guide](#))

The RAM is made up of n sectors. Each sector can be completely powered down to reduce leakage; however, all data is lost during power down. Features of the RAM include:

- RAM has n sectors. The sizes of the sectors can be found in [Section 6.4](#).
- Each sector 0 to n can be complete disabled; however, all data in a sector is lost when it is disabled.
- Each sector 0 to n automatically enters low-power retention mode when possible.

6.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be managed using all instructions. For complete module descriptions, see the [MSP430F5xx and MSP430F6xx Family User's Guide](#).

6.9.1 Digital I/O ([Link to user's guide](#))

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Pullup or pulldown on all ports is programmable.
- Drive strength on all ports is programmable.
- Edge-selectable interrupt and LPM4.5 wakeup input capability is available for all bits of ports P1 and P2.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise in pairs.

6.9.2 Port Mapping Controller ([Link to user's guide](#))

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to port P4. [Table 6-7](#) lists the valid settings.

Table 6-7. Port Mapping Mnemonics and Functions

| VALUE | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|-------|-----------------|--|------------------------------|
| 0 | PM_NONE | None | DVSS |
| 1 | PM_CBOUT0 | – | COMP_B output |
| | PM_TB0CLK | TB0 clock input | – |
| 2 | PM_ADC10CLK | – | ADC10CLK |
| | PM_DMAE0 | DMAE0 input | – |
| 3 | PM_SVMOUT | – | SVM output |
| | PM_TB0OUTH | TB0 high-impedance input TB0OUTH | – |
| 4 | PM_TB0CCR0A | TB0 CCR0 capture input CCI0A | TB0 CCR0 compare output Out0 |
| 5 | PM_TB0CCR1A | TB0 CCR1 capture input CCI1A | TB0 CCR1 compare output Out1 |
| 6 | PM_TB0CCR2A | TB0 CCR2 capture input CCI2A | TB0 CCR2 compare output Out2 |
| 7 | PM_TB0CCR3A | TB0 CCR3 capture input CCI3A | TB0 CCR3 compare output Out3 |
| 8 | PM_TB0CCR4A | TB0 CCR4 capture input CCI4A | TB0 CCR4 compare output Out4 |
| 9 | PM_TB0CCR5A | TB0 CCR5 capture input CCI5A | TB0 CCR5 compare output Out5 |
| 10 | PM_TB0CCR6A | TB0 CCR6 capture input CCI6A | TB0 CCR6 compare output Out6 |
| 11 | PM_UCA1RXD | USCI_A1 UART RXD (direction controlled by USCI – input) | |
| | PM_UCA1SOMI | USCI_A1 SPI slave out master in (direction controlled by USCI) | |
| 12 | PM_UCA1TXD | USCI_A1 UART TXD (direction controlled by USCI – output) | |
| | PM_UCA1SIMO | USCI_A1 SPI slave in master out (direction controlled by USCI) | |
| 13 | PM_UCA1CLK | USCI_A1 clock input/output (direction controlled by USCI) | |
| | PM_UCB1STE | USCI_B1 SPI slave transmit enable (direction controlled by USCI) | |
| 14 | PM_UCB1SOMI | USCI_B1 SPI slave out master in (direction controlled by USCI) | |
| | PM_UCB1SCL | USCI_B1 I2C clock (open drain and direction controlled by USCI) | |
| 15 | PM_UCB1SIMO | USCI_B1 SPI slave in master out (direction controlled by USCI) | |
| | PM_UCB1SDA | USCI_B1 I2C data (open drain and direction controlled by USCI) | |
| 16 | PM_UCB1CLK | USCI_B1 clock input/output (direction controlled by USCI) | |
| | PM_UCA1STE | USCI_A1 SPI slave transmit enable (direction controlled by USCI) | |
| 17 | PM_CBOUT1 | None | COMP_B output |
| 18 | PM_MCLK | None | MCLK |

Table 6-7. Port Mapping Mnemonics and Functions (continued)

| VALUE | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|--------------------------|-----------------|---|---------------------|
| 19 | PM_RTCCLK | None | RTCCLK output |
| 20 | PM_UCA0RXD | USCI_A0 UART RXD (direction controlled by USCI - input) | |
| | PM_UCA0SOMI | USCI_A0 SPI slave out master in (direction controlled by USCI) | |
| 21 | PM_UCA0TXD | USCI_A0 UART TXD (direction controlled by USCI - output) | |
| | PM_UCA0SIMO | USCI_A0 SPI slave in master out (direction controlled by USCI) | |
| 22 | PM_UCA0CLK | USCI_A0 clock input/output (direction controlled by USCI) | |
| | PM_UCB0STE | USCI_B0 SPI slave transmit enable (direction controlled by USCI) | |
| 23 | PM_UCB0SOMI | USCI_B0 SPI slave out master in (direction controlled by USCI) | |
| | PM_UCB0SCL | USCI_B0 I2C clock (open drain and direction controlled by USCI) | |
| 24 | PM_UCB0SIMO | USCI_B0 SPI slave in master out (direction controlled by USCI) | |
| | PM_UCB0SDA | USCI_B0 I2C data (open drain and direction controlled by USCI) | |
| 25 | PM_UCB0CLK | USCI_B0 clock input/output (direction controlled by USCI) | |
| | PM_UCA0STE | USCI_A0 SPI slave transmit enable (direction controlled by USCI) | |
| 26 - 30 | Reserved | None | DVSS |
| 31 (0FFh) ⁽¹⁾ | PM_ANALOG | Disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals | |

(1) The value of the PM_ANALOG mnemonic is set to 0FFh. The port mapping registers are only 5 bits wide and the upper bits are ignored, resulting in a read out value of 31.

Table 6-8. Default Mapping

| PIN | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|----------------------------|------------------------|---|---------------------|
| P4.0/P4MAP0 | PM_UCB1STE/PM_UCA1CLK | USCI_B1 SPI slave transmit enable (direction controlled by USCI) USCI_A1 clock input/output (direction controlled by USCI) | |
| P4.1/P4MAP1 | PM_UCB1SIMO/PM_UCB1SDA | USCI_B1 SPI slave in master out (direction controlled by USCI) USCI_B1 I2C data (open drain and direction controlled by USCI) | |
| P4.2/P4MAP2 | PM_UCB1SOMI/PM_UCB1SCL | USCI_B1 SPI slave out master in (direction controlled by USCI) USCI_B1 I2C clock (open drain and direction controlled by USCI) | |
| P4.3/P4MAP3 | PM_UCB1CLK/PM_UCA1STE | USCI_A1 SPI slave transmit enable (direction controlled by USCI) USCI_B1 clock input/output (direction controlled by USCI) | |
| P4.4/P4MAP4 | PM_UCA1TXD/PM_UCA1SIMO | USCI_A1 UART TXD (Direction controlled by USCI - output) USCI_A1 SPI slave in master out (direction controlled by USCI) | |
| P4.5/P4MAP5 | PM_UCA1RXD/PM_UCA1SOMI | USCI_A1 UART RXD (Direction controlled by USCI - input) USCI_A1 SPI slave out master in (direction controlled by USCI) | |
| P4.6/P4MAP6 | PM_NONE | None | DVSS |
| P4.7/P4MAP7 ⁽¹⁾ | PM_NONE | None | DVSS |

(1) Not available on all devices

6.9.3 Oscillator and System Clock ([Link to user's guide](#))

The clock system in the MSP430F522x and MSP430F521x family of devices is supported by the Unified Clock System (UCS) module, which includes support for a 32-kHz watch crystal oscillator (XT1 LF mode) (XT1 HF mode is not supported), an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator (XT2). The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the selected FLL reference frequency. The internal DCO provides a fast turnon clock source and stabilizes in 3.5 μ s (typical). The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (XT1), a high-frequency crystal (XT2), the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally controlled oscillator DCO.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

6.9.4 Power-Management Module (PMM) ([Link to user's guide](#))

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, and brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS and SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

6.9.5 Hardware Multiplier ([Link to user's guide](#))

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

6.9.6 Real-Time Clock (RTC_A) ([Link to user's guide](#))

The RTC_A module can be used as a general-purpose 32-bit counter (counter mode) or as an integrated real-time clock (RTC) (calendar mode). In counter mode, the RTC_A also includes two independent 8-bit timers that can be cascaded to form a 16-bit timer or counter. Both timers can be read and written by software. Calendar mode integrates an internal calendar that compensates for months with less than 31 days and includes leap year correction. The RTC_A also supports flexible alarm functions and offset-calibration hardware.

6.9.7 Watchdog Timer (WDT_A) ([Link to user's guide](#))

The primary function of the WDT_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

6.9.8 System Module (SYS) [\(Link to user's guide\)](#)

The SYS module handles many of the system functions within the device. These include power-on reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootloader (BSL) entry mechanisms, and configuration management (device descriptors). It also includes a data exchange mechanism when using JTAG that is called a JTAG mailbox and that can be used in the application. [Table 6-9](#) lists the SYS module interrupt vector registers.

Table 6-9. System Module Interrupt Vector Registers

| INTERRUPT VECTOR REGISTER | ADDRESS | INTERRUPT EVENT | VALUE | PRIORITY |
|---------------------------|------------|-------------------------------------|------------|----------------------|
| SYSRSTIV, System Reset | 019Eh | No interrupt pending | 00h | |
| | | Brownout (BOR) | 02h | Highest |
| | | $\overline{\text{RST}}$ /NMI (BOR) | 04h | |
| | | PMMSWBOR (BOR) | 06h | |
| | | Wakeup from LPMx.5 | 08h | |
| | | Security violation (BOR) | 0Ah | |
| | | SVSL (POR) | 0Ch | |
| | | SVSH (POR) | 0Eh | |
| | | SVML_OVP (POR) | 10h | |
| | | SVMH_OVP (POR) | 12h | |
| | | PMMSWPOR (POR) | 14h | |
| | | WDT time-out (PUC) | 16h | |
| | | WDT password violation (PUC) | 18h | |
| | | KEYV flash password violation (PUC) | 1Ah | |
| | | Reserved | 1Ch | |
| | | Peripheral area fetch (PUC) | 1Eh | |
| | | PMM password violation (PUC) | 20h | |
| Reserved | 22h to 3Eh | Lowest | | |
| SYSSNIV, System NMI | 019Ch | No interrupt pending | 00h | |
| | | SVMLIFG | 02h | Highest |
| | | SVMHIFG | 04h | |
| | | SVSMLDLYIFG | 06h | |
| | | SVSMHDLYIFG | 08h | |
| | | VMAIFG | 0Ah | |
| | | JMBINIFG | 0Ch | |
| | | JMBOUTIFG | 0Eh | |
| | | SVMLVLRIFG | 10h | |
| | | SVMHVLRFIFG | 12h | |
| | | Reserved | 14h to 1Eh | Lowest |
| | | SYSUNIV, User NMI | 019Ah | No interrupt pending |
| NMIIFG | 02h | | | Highest |
| OFIFG | 04h | | | |
| ACCVIFG | 06h | | | |
| Reserved | 08h | | | |
| Reserved | 0Ah to 1Eh | | | Lowest |

6.9.9 DMA Controller ([Link to user's guide](#))

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC10_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral. [Table 6-10](#) lists the trigger assignments.

Table 6-10. DMA Trigger Assignments⁽¹⁾

| TRIGGER | CHANNEL | | |
|---------|--------------------------|--------------------------|--------------------------|
| | 0 | 1 | 2 |
| 0 | DMAREQ | DMAREQ | DMAREQ |
| 1 | TA0CCR0 CCIFG | TA0CCR0 CCIFG | TA0CCR0 CCIFG |
| 2 | TA0CCR2 CCIFG | TA0CCR2 CCIFG | TA0CCR2 CCIFG |
| 3 | TA1CCR0 CCIFG | TA1CCR0 CCIFG | TA1CCR0 CCIFG |
| 4 | TA1CCR2 CCIFG | TA1CCR2 CCIFG | TA1CCR2 CCIFG |
| 5 | TA2CCR0 CCIFG | TA2CCR0 CCIFG | TA2CCR0 CCIFG |
| 6 | TA2CCR2 CCIFG | TA2CCR2 CCIFG | TA2CCR2 CCIFG |
| 7 | TB0CCR0 CCIFG | TB0CCR0 CCIFG | TB0CCR0 CCIFG |
| 8 | TB0CCR2 CCIFG | TB0CCR2 CCIFG | TB0CCR2 CCIFG |
| 9 | Reserved | Reserved | Reserved |
| 10 | Reserved | Reserved | Reserved |
| 11 | Reserved | Reserved | Reserved |
| 12 | Reserved | Reserved | Reserved |
| 13 | Reserved | Reserved | Reserved |
| 14 | Reserved | Reserved | Reserved |
| 15 | Reserved | Reserved | Reserved |
| 16 | UCA0RXIFG | UCA0RXIFG | UCA0RXIFG |
| 17 | UCA0TXIFG | UCA0TXIFG | UCA0TXIFG |
| 18 | UCB0RXIFG | UCB0RXIFG | UCB0RXIFG |
| 19 | UCB0TXIFG | UCB0TXIFG | UCB0TXIFG |
| 20 | UCA1RXIFG | UCA1RXIFG | UCA1RXIFG |
| 21 | UCA1TXIFG | UCA1TXIFG | UCA1TXIFG |
| 22 | UCB1RXIFG | UCB1RXIFG | UCB1RXIFG |
| 23 | UCB1TXIFG | UCB1TXIFG | UCB1TXIFG |
| 24 | ADC10IFG0 ⁽²⁾ | ADC10IFG0 ⁽²⁾ | ADC10IFG0 ⁽²⁾ |
| 25 | Reserved | Reserved | Reserved |
| 26 | Reserved | Reserved | Reserved |
| 27 | Reserved | Reserved | Reserved |
| 28 | Reserved | Reserved | Reserved |
| 29 | MPY ready | MPY ready | MPY ready |
| 30 | DMA2IFG | DMA0IFG | DMA1IFG |
| 31 | DMAE0 | DMAE0 | DMAE0 |

(1) If a reserved trigger source is selected, no trigger is generated.

(2) Only on devices with ADC; reserved on devices without ADC

6.9.10 **Universal Serial Communication Interface (USCI) (Links to user's guide: [UART Mode](#), [SPI Mode](#), [I²C Mode](#))**

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3- or 4-pin) and I²C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA. Each USCI module contains two portions, A and B.

The USCI_An module provides support for SPI (3- or 4-pin), UART, enhanced UART, or IrDA.

The USCI_Bn module provides support for SPI (3- or 4-pin) or I²C.

The MSP430F522x and MSP430F521x series include two complete USCI modules (n = 0, 1).

6.9.11 TA0 (Link to user's guide)

TA0 is a 16-bit timer/counter (Timer_A type) with five capture/compare registers. TA0 can support multiple captures or compares, PWM outputs, and interval timing (see [Table 6-11](#)). TA0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-11. TA0 Signal Connections

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|------------------|---------|---------------------|---------------------|--------------|----------------------|----------------------|-------------------------------------|-------------------------------------|
| RGC, ZQE, YFF | RGZ | | | | | | RGC, ZQE, YFF | RGZ |
| 18, H2, B7-P1.0 | 13-P1.0 | TA0CLK | TACLK | Timer | NA | NA | | |
| | | ACLK (internal) | ACLK | | | | | |
| | | SMCLK (internal) | SMCLK | | | | | |
| 18, H2, B7-P1.0 | 13-P1.0 | TA0CLK | \overline{TACLK} | | | | | |
| 19, H3, C7-P1.1 | 14-P1.1 | TA0.0 | CCI0A | CCR0 | TA0 | TA0.0 | 19, H3, C7-P1.1 | 14-P1.1 |
| | | DVSS | CCI0B | | | | | |
| | | DVSS | GND | | | | | |
| | | DVCC | V _{CC} | | | | | |
| 20, J3, C8-P1.2 | 15-P1.2 | TA0.1 | CCI1A | CCR1 | TA1 | TA0.1 | 20, J3, C8-P1.2 | 15-P1.2 |
| | | CBOUT (internal) | CCI1B | | | | ADC10 (internal) ADC10SHSx = {1} | ADC10 (internal) ADC10SHSx = {1} |
| | | DVSS | GND | | | | | |
| | | DVCC | V _{CC} | | | | | |
| 21, G4, C6-P1.3 | 16-P1.3 | TA0.2 | CCI2A | CCR2 | TA2 | TA0.2 | 21, G4, C6-P1.3 | 16-P1.3 |
| | | ACLK (internal) | CCI2B | | | | | |
| | | DVSS | GND | | | | | |
| | | DVCC | V _{CC} | | | | | |
| 22, H4, C5-P1.4 | 17-P1.4 | TA0.3 | CCI3A | CCR3 | TA3 | TA0.3 | 22, H4, C5-P1.4 | 17-P1.4 |
| | | DVSS | CCI3B | | | | | |
| | | DVSS | GND | | | | | |
| | | DVCC | V _{CC} | | | | | |
| 23, J4, D8-P1.5 | 18-P1.5 | TA0.4 | CCI4A | CCR4 | TA4 | TA0.4 | 23, J4, D8-P1.5 | 18-P1.5 |
| | | DVSS | CCI4B | | | | | |
| | | DVSS | GND | | | | | |
| | | DVCC | V _{CC} | | | | | |

6.9.12 TA1 (Link to user's guide)

TA1 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA1 can support multiple captures or compares, PWM outputs, and interval timing (see Table 6-12). TA1 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-12. TA1 Signal Connections

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|------------------|---------|---------------------|---------------------------|--------------|----------------------|----------------------|-------------------|---------|
| RGC, ZQE, YFF | RGZ | | | | | | RGC, ZQE, YFF | RGZ |
| 24, G5, D7-P1.6 | 19-P1.6 | TA1CLK | TACLK | Timer | NA | NA | | |
| | | ACLK (internal) | ACLK | | | | | |
| | | SMCLK (internal) | SMCLK | | | | | |
| 24, G5, D7-P1.6 | 19-P1.6 | TA1CLK | $\overline{\text{TACLK}}$ | | | | | |
| 25, H5, D6-P1.7 | 20-P1.7 | TA1.0 | CC10A | CCR0 | TA0 | TA1.0 | 25, H5, D6-P1.7 | 20-P1.7 |
| | | DVSS | CC10B | | | | | |
| | | DVSS | GND | | | | | |
| | | DVCC | V _{CC} | | | | | |
| 26, J5, E8-P2.0 | | TA1.1 | CC11A | CCR1 | TA1 | TA1.1 | 26, J5, E8-P2.0 | |
| | | CBOUT (internal) | CC11B | | | | | |
| | | DVSS | GND | | | | | |
| | | DVCC | V _{CC} | | | | | |
| 27, G6, D5-P2.1 | | TA1.2 | CC12A | CCR2 | TA2 | TA1.2 | 27, G6, D5-P2.1 | |
| | | ACLK (internal) | CC12B | | | | | |
| | | DVSS | GND | | | | | |
| | | DVCC | V _{CC} | | | | | |

6.9.13 TA2 (Link to user's guide)

TA2 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA2 can support multiple captures or compares, PWM outputs, and interval timing (see [Table 6-13](#)). TA2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-13. TA2 Signal Connections

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|------------------|-----|---------------------|---------------------------|--------------|----------------------|----------------------|-------------------|-----|
| RGC, ZQE, YFF | RGZ | | | | | | RGC, ZQE, YFF | RGZ |
| 28, J6, E7-P2.2 | | TA2CLK | TACLK | Timer | NA | NA | | |
| | | ACLK (internal) | ACLK | | | | | |
| | | SMCLK (internal) | SMCLK | | | | | |
| | | TA2CLK | $\overline{\text{TACLK}}$ | | | | | |
| 29, H6, F8-P2.3 | | TA2.0 | CC10A | CCR0 | TA0 | TA2.0 | 29, H6, F8-P2.3 | |
| | | DVSS | CC10B | | | | | |
| | | DVSS | GND | | | | | |
| | | DVCC | V _{CC} | | | | | |
| 30, J7, E6-P2.4 | | TA2.1 | CC11A | CCR1 | TA1 | TA2.1 | 30, J7, E6-P2.4 | |
| | | CBOUT (internal) | CC11B | | | | | |
| | | DVSS | GND | | | | | |
| | | DVCC | V _{CC} | | | | | |
| 31, J8, F7-P2.5 | | TA2.2 | CC12A | CCR2 | TA2 | TA2.2 | 31, J8, F7-P2.5 | |
| | | ACLK (internal) | CC12B | | | | | |
| | | DVSS | GND | | | | | |
| | | DVCC | V _{CC} | | | | | |

6.9.14 TB0 (Link to user's guide)

TB0 is a 16-bit timer/counter (Timer_B type) with seven capture/compare registers. TB0 can support multiple captures or compares, PWM outputs, and interval timing (see Table 6-14). TB0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-14. TB0 Signal Connections

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|---|-----|---------------------|---------------------|--------------|----------------------|----------------------|---|-------------------------------------|
| RGC, ZQE, YFF | RGZ | | | | | | RGC, ZQE, YFF | RGZ |
| (1) | (1) | TB0CLK | TBCLK | Timer | NA | NA | | |
| | | ACLK (internal) | ACLK | | | | | |
| | | SMCLK (internal) | SMCLK | | | | | |
| (1) | (1) | TB0CLK | TBCLK | | | | | |
| 49, B8(9) _i , H1-P7.0 ⁽¹⁾ | (1) | TB0.0 | CCI0A | CCR0 | TB0 | TB0.0 | 49, B8(9) _i , H1-P7.0 ⁽¹⁾ | (1) |
| 49, B8(9) _i , H1-P7.0 ⁽¹⁾ | (1) | TB0.0 | CCI0B | | | | ADC10 (internal) ADC10SHSx = {2} | ADC10 (internal) ADC10SHSx = {2} |
| | | DVSS | GND | | | | | |
| | | DVCC | V _{CC} | | | | | |
| 50, A9, G2-P7.1 ⁽¹⁾ | (1) | TB0.1 | CCI1A | CCR1 | TB1 | TB0.1 | 50, A9, G2-P7.1 ⁽¹⁾ | (1) |
| | | CBOUT (internal) | CCI1B | | | | ADC10 (internal) ADC10SHSx = {3} | ADC10 (internal) ADC10SHSx = {3} |
| | | DVSS | GND | | | | | |
| | | DVCC | V _{CC} | | | | | |
| 51, B7, F3-P7.2 ⁽¹⁾ | (1) | TB0.2 | CCI2A | CCR2 | TB2 | TB0.2 | 51, B7, F3-P7.2 ⁽¹⁾ | (1) |
| 51, B7, F3-P7.2 ⁽¹⁾ | (1) | TB0.2 | CCI2B | | | | | |
| | | DVSS | GND | | | | | |
| | | DVCC | V _{CC} | | | | | |
| 52, A8, G1-P7.3 ⁽¹⁾ | (1) | TB0.3 | CCI3A | CCR3 | TB3 | TB0.3 | 52, A8, G1-P7.3 ⁽¹⁾ | (1) |
| 52, A8, G1-P7.3 ⁽¹⁾ | (1) | TB0.3 | CCI3B | | | | | |
| | | DVSS | GND | | | | | |
| | | DVCC | V _{CC} | | | | | |
| 53, A7, F2-P7.4 ⁽¹⁾ | (1) | TB0.4 | CCI4A | CCR4 | TB4 | TB0.4 | 53, A7, F2-P7.4 ⁽¹⁾ | (1) |
| 53, A7, F2-P7.4 ⁽¹⁾ | (1) | TB0.4 | CCI4B | | | | | |
| | | DVSS | GND | | | | | |
| | | DVCC | V _{CC} | | | | | |
| 54, A6, F1-P7.5 ⁽¹⁾ | (1) | TB0.5 | CCI5A | CCR5 | TB5 | TB0.5 | 54, A6, F1-P7.5 ⁽¹⁾ | (1) |
| 54, A6, F1-P7.5 ⁽¹⁾ | (1) | TB0.5 | CCI5B | | | | | |
| | | DVSS | GND | | | | | |
| | | DVCC | V _{CC} | | | | | |
| (1) | (1) | TB0.6 | CCI6A | CCR6 | TB6 | TB0.6 | (1) | (1) |
| | | ACLK (internal) | CCI6B | | | | | |
| | | DVSS | GND | | | | | |
| | | DVCC | V _{CC} | | | | | |

(1) Timer functions can be assigned by the port mapping controller.

6.9.15 *Comparator_B* ([Link to user's guide](#))

The primary function of the Comparator_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

6.9.16 *ADC10_A* ([Link to user's guide](#))

The ADC10_A module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and a conversion result buffer. A window comparator with lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

6.9.17 *CRC16* ([Link to user's guide](#))

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

6.9.18 *REF Voltage Reference* ([Link to user's guide](#))

The REF is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device.

6.9.19 *Embedded Emulation Module (EEM) (S Version)* ([Link to user's guide](#))

The EEM supports real-time in-system debugging. The S version of the EEM has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

6.9.20 Peripheral File Map

Table 6-15 lists the base address for the registers of each peripheral.

Table 6-15. Peripherals

| MODULE NAME | BASE ADDRESS | OFFSET ADDRESS RANGE |
|--|--------------|----------------------|
| Special Functions (see Table 6-16) | 0100h | 000h-01Fh |
| PMM (see Table 6-17) | 0120h | 000h-010h |
| Flash Control (see Table 6-18) | 0140h | 000h-00Fh |
| CRC16 (see Table 6-19) | 0150h | 000h-007h |
| RAM Control (see Table 6-20) | 0158h | 000h-001h |
| Watchdog (see Table 6-21) | 015Ch | 000h-001h |
| UCS (see Table 6-22) | 0160h | 000h-01Fh |
| SYS (see Table 6-23) | 0180h | 000h-01Fh |
| Shared Reference (see Table 6-24) | 01B0h | 000h-001h |
| Port Mapping Control (see Table 6-25) | 01C0h | 000h-002h |
| Port Mapping Port P4 (see Table 6-25) | 01E0h | 000h-007h |
| Port P1, P2 (see Table 6-26) | 0200h | 000h-01Fh |
| Port P3, P4 (see Table 6-27) | 0220h | 000h-00Bh |
| Port P5, P6 (see Table 6-28) | 0240h | 000h-00Bh |
| Port P7 (see Table 6-29) | 0260h | 000h-00Bh |
| Port PJ (see Table 6-30) | 0320h | 000h-01Fh |
| TA0 (see Table 6-31) | 0340h | 000h-02Eh |
| TA1 (see Table 6-32) | 0380h | 000h-02Eh |
| TB0 (see Table 6-33) | 03C0h | 000h-02Eh |
| TA2 (see Table 6-34) | 0400h | 000h-02Eh |
| Real-Time Clock (RTC_A) (see Table 6-35) | 04A0h | 000h-01Bh |
| 32-Bit Hardware Multiplier (see Table 6-36) | 04C0h | 000h-02Fh |
| DMA General Control (see Table 6-37) | 0500h | 000h-00Fh |
| DMA Channel 0 (see Table 6-37) | 0510h | 000h-00Ah |
| DMA Channel 1 (see Table 6-37) | 0520h | 000h-00Ah |
| DMA Channel 2 (see Table 6-37) | 0530h | 000h-00Ah |
| USCI_A0 (see Table 6-38) | 05C0h | 000h-01Fh |
| USCI_B0 (see Table 6-39) | 05E0h | 000h-01Fh |
| USCI_A1 (see Table 6-40) | 0600h | 000h-01Fh |
| USCI_B1 (see Table 6-41) | 0620h | 000h-01Fh |
| ADC10_A (see Table 6-42) | 0740h | 000h-01Fh |
| Comparator_B (see Table 6-43) | 08C0h | 000h-00Fh |

Table 6-16. Special Function Registers (Base Address: 0100h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-----------------------|----------|--------|
| SFR interrupt enable | SFRIE1 | 00h |
| SFR interrupt flag | SFRIFG1 | 02h |
| SFR reset pin control | SFRRPCR | 04h |

Table 6-17. PMM Registers (Base Address: 0120h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------|----------|--------|
| PMM control 0 | PMMCTL0 | 00h |
| PMM control 1 | PMMCTL1 | 02h |
| SVS high-side control | SVSMHCTL | 04h |
| SVS low-side control | SVSMLCTL | 06h |
| PMM interrupt flags | PMMIFG | 0Ch |
| PMM interrupt enable | PMMIE | 0Eh |
| PMM power mode 5 control | PM5CTL0 | 10h |

Table 6-18. Flash Control Registers (Base Address: 0140h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| Flash control 1 | FCTL1 | 00h |
| Flash control 3 | FCTL3 | 04h |
| Flash control 4 | FCTL4 | 06h |

Table 6-19. CRC16 Registers (Base Address: 0150h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|-----------|--------|
| CRC data input | CRC16DI | 00h |
| CRC data input reverse byte | CRCDIRB | 02h |
| CRC initialization and result | CRCINIRES | 04h |
| CRC result reverse byte | CRCRESR | 06h |

Table 6-20. RAM Control Registers (Base Address: 0158h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| RAM control 0 | RCCTL0 | 00h |

Table 6-21. Watchdog Registers (Base Address: 015Ch)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------|----------|--------|
| Watchdog timer control | WDTCTL | 00h |

Table 6-22. UCS Registers (Base Address: 0160h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| UCS control 0 | UCSCTL0 | 00h |
| UCS control 1 | UCSCTL1 | 02h |
| UCS control 2 | UCSCTL2 | 04h |
| UCS control 3 | UCSCTL3 | 06h |
| UCS control 4 | UCSCTL4 | 08h |
| UCS control 5 | UCSCTL5 | 0Ah |
| UCS control 6 | UCSCTL6 | 0Ch |
| UCS control 7 | UCSCTL7 | 0Eh |

Table 6-22. UCS Registers (Base Address: 0160h) (continued)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| UCS control 8 | UCSCTL8 | 10h |
| UCS control 9 | UCSCTL9 | 12h |

Table 6-23. SYS Registers (Base Address: 0180h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|----------|--------|
| System control | SYSCTL | 00h |
| Bootloader configuration area | SYSBSLC | 02h |
| JTAG mailbox control | SYSJMBC | 06h |
| JTAG mailbox input 0 | SYSJMBIO | 08h |
| JTAG mailbox input 1 | SYSJMBI1 | 0Ah |
| JTAG mailbox output 0 | SYSJMBO0 | 0Ch |
| JTAG mailbox output 1 | SYSJMBO1 | 0Eh |
| User NMI vector generator | SYSUNIV | 1Ah |
| System NMI vector generator | SYSNIV | 1Ch |
| Reset vector generator | SYSRSTIV | 1Eh |

Table 6-24. Shared Reference Registers (Base Address: 01B0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------|----------|--------|
| Shared reference control | REFCTL | 00h |

**Table 6-25. Port Mapping Registers
(Base Address of Port Mapping Control: 01C0h, Port P4: 01E0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|-----------|--------|
| Port mapping key/ID | PMAPKEYID | 00h |
| Port mapping control | PMAPCTL | 02h |
| Port P4.0 mapping | P4MAP0 | 00h |
| Port P4.1 mapping | P4MAP1 | 01h |
| Port P4.2 mapping | P4MAP2 | 02h |
| Port P4.3 mapping | P4MAP3 | 03h |
| Port P4.4 mapping | P4MAP4 | 04h |
| Port P4.5 mapping | P4MAP5 | 05h |
| Port P4.6 mapping | P4MAP6 | 06h |
| Port P4.7 mapping | P4MAP7 | 07h |

Table 6-26. Port P1, P2 Registers (Base Address: 0200h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|----------|--------|
| Port P1 input | P1IN | 00h |
| Port P1 output | P1OUT | 02h |
| Port P1 direction | P1DIR | 04h |
| Port P1 resistor enable | P1REN | 06h |
| Port P1 drive strength | P1DS | 08h |
| Port P1 selection | P1SEL | 0Ah |
| Port P1 interrupt vector word | P1IV | 0Eh |
| Port P1 interrupt edge select | P1IES | 18h |
| Port P1 interrupt enable | P1IE | 1Ah |
| Port P1 interrupt flag | P1IFG | 1Ch |

Table 6-26. Port P1, P2 Registers (Base Address: 0200h) (continued)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|----------|--------|
| Port P2 input | P2IN | 01h |
| Port P2 output | P2OUT | 03h |
| Port P2 direction | P2DIR | 05h |
| Port P2 resistor enable | P2REN | 07h |
| Port P2 drive strength | P2DS | 09h |
| Port P2 selection | P2SEL | 0Bh |
| Port P2 interrupt vector word | P2IV | 1Eh |
| Port P2 interrupt edge select | P2IES | 19h |
| Port P2 interrupt enable | P2IE | 1Bh |
| Port P2 interrupt flag | P2IFG | 1Dh |

Table 6-27. Port P3, P4 Registers (Base Address: 0220h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Port P3 input | P3IN | 00h |
| Port P3 output | P3OUT | 02h |
| Port P3 direction | P3DIR | 04h |
| Port P3 resistor enable | P3REN | 06h |
| Port P3 drive strength | P3DS | 08h |
| Port P3 selection | P3SEL | 0Ah |
| Port P4 input | P4IN | 01h |
| Port P4 output | P4OUT | 03h |
| Port P4 direction | P4DIR | 05h |
| Port P4 resistor enable | P4REN | 07h |
| Port P4 drive strength | P4DS | 09h |
| Port P4 selection | P4SEL | 0Bh |

Table 6-28. Port P5, P6 Registers (Base Address: 0240h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Port P5 input | P5IN | 00h |
| Port P5 output | P5OUT | 02h |
| Port P5 direction | P5DIR | 04h |
| Port P5 resistor enable | P5REN | 06h |
| Port P5 drive strength | P5DS | 08h |
| Port P5 selection | P5SEL | 0Ah |
| Port P6 input | P6IN | 01h |
| Port P6 output | P6OUT | 03h |
| Port P6 direction | P6DIR | 05h |
| Port P6 resistor enable | P6REN | 07h |
| Port P6 drive strength | P6DS | 09h |
| Port P6 selection | P6SEL | 0Bh |

Table 6-29. Port P7 Registers (Base Address: 0260h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| Port P7 input | P7IN | 00h |
| Port P7 output | P7OUT | 02h |
| Port P7 direction | P7DIR | 04h |

Table 6-29. Port P7 Registers (Base Address: 0260h) (continued)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Port P7 resistor enable | P7REN | 06h |
| Port P7 drive strength | P7DS | 08h |
| Port P7 selection | P7SEL | 0Ah |

Table 6-30. Port J Registers (Base Address: 0320h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Port PJ input | PJIN | 00h |
| Port PJ output | PJOUT | 02h |
| Port PJ direction | PJDIR | 04h |
| Port PJ resistor enable | PJREN | 06h |
| Port PJ drive strength | PJDS | 08h |

Table 6-31. TA0 Registers (Base Address: 0340h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA0 control | TAOCTL | 00h |
| Capture/compare control 0 | TAOCTL0 | 02h |
| Capture/compare control 1 | TAOCTL1 | 04h |
| Capture/compare control 2 | TAOCTL2 | 06h |
| Capture/compare control 3 | TAOCTL3 | 08h |
| Capture/compare control 4 | TAOCTL4 | 0Ah |
| TA0 counter | TAOR | 10h |
| Capture/compare 0 | TAOCCR0 | 12h |
| Capture/compare 1 | TAOCCR1 | 14h |
| Capture/compare 2 | TAOCCR2 | 16h |
| Capture/compare 3 | TAOCCR3 | 18h |
| Capture/compare 4 | TAOCCR4 | 1Ah |
| TA0 expansion 0 | TAOEX0 | 20h |
| TA0 interrupt vector | TAOIV | 2Eh |

Table 6-32. TA1 Registers (Base Address: 0380h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA1 control | TA1CTL | 00h |
| Capture/compare control 0 | TA1CTL0 | 02h |
| Capture/compare control 1 | TA1CTL1 | 04h |
| Capture/compare control 2 | TA1CTL2 | 06h |
| TA1 counter | TA1R | 10h |
| Capture/compare 0 | TA1CCR0 | 12h |
| Capture/compare 1 | TA1CCR1 | 14h |
| Capture/compare 2 | TA1CCR2 | 16h |
| TA1 expansion 0 | TA1EX0 | 20h |
| TA1 interrupt vector | TA1IV | 2Eh |

Table 6-33. TB0 Registers (Base Address: 03C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TB0 control | TBOCTL | 00h |
| Capture/compare control 0 | TBOCTL0 | 02h |

Table 6-33. TB0 Registers (Base Address: 03C0h) (continued)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------|----------|--------|
| Capture/compare control 1 | TB0CTL1 | 04h |
| Capture/compare control 2 | TB0CTL2 | 06h |
| Capture/compare control 3 | TB0CTL3 | 08h |
| Capture/compare control 4 | TB0CTL4 | 0Ah |
| Capture/compare control 5 | TB0CTL5 | 0Ch |
| Capture/compare control 6 | TB0CTL6 | 0Eh |
| TB0 counter | TB0R | 10h |
| Capture/compare 0 | TB0CCR0 | 12h |
| Capture/compare 1 | TB0CCR1 | 14h |
| Capture/compare 2 | TB0CCR2 | 16h |
| Capture/compare 3 | TB0CCR3 | 18h |
| Capture/compare 4 | TB0CCR4 | 1Ah |
| Capture/compare 5 | TB0CCR5 | 1Ch |
| Capture/compare 6 | TB0CCR6 | 1Eh |
| TB0 expansion 0 | TB0EX0 | 20h |
| TB0 interrupt vector | TB0IV | 2Eh |

Table 6-34. TA2 Registers (Base Address: 0400h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA2 control | TA2CTL | 00h |
| Capture/compare control 0 | TA2CTL0 | 02h |
| Capture/compare control 1 | TA2CTL1 | 04h |
| Capture/compare control 2 | TA2CTL2 | 06h |
| TA2 counter | TA2R | 10h |
| Capture/compare 0 | TA2CCR0 | 12h |
| Capture/compare 1 | TA2CCR1 | 14h |
| Capture/compare 2 | TA2CCR2 | 16h |
| TA2 expansion 0 | TA2EX0 | 20h |
| TA2 interrupt vector | TA2IV | 2Eh |

Table 6-35. Real-Time Clock Registers (Base Address: 04A0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------|----------------|--------|
| RTC control 0 | RTCCTL0 | 00h |
| RTC control 1 | RTCCTL1 | 01h |
| RTC control 2 | RTCCTL2 | 02h |
| RTC control 3 | RTCCTL3 | 03h |
| RTC prescaler 0 control | RTCPS0CTL | 08h |
| RTC prescaler 1 control | RTCPS1CTL | 0Ah |
| RTC prescaler 0 | RTCPS0 | 0Ch |
| RTC prescaler 1 | RTCPS1 | 0Dh |
| RTC interrupt vector word | RTCIV | 0Eh |
| RTC seconds/counter 1 | RTCSEC/RTCNT1 | 10h |
| RTC minutes/counter 2 | RTCMIN/RTCNT2 | 11h |
| RTC hours/counter 3 | RTCHOUR/RTCNT3 | 12h |
| RTC day of week/counter 4 | RTCADOW/RTCNT4 | 13h |
| RTC days | RTCDAW | 14h |
| RTC month | RTCMON | 15h |

Table 6-35. Real-Time Clock Registers (Base Address: 04A0h) (continued)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-----------------------|----------|--------|
| RTC year low | RTCYEARL | 16h |
| RTC year high | RTCYEARH | 17h |
| RTC alarm minutes | RTCAMIN | 18h |
| RTC alarm hours | RTCAHOUR | 19h |
| RTC alarm day of week | RTCADOW | 1Ah |
| RTC alarm days | RTCADAY | 1Bh |

Table 6-36. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|-----------|--------|
| 16-bit operand 1 – multiply | MPY | 00h |
| 16-bit operand 1 – signed multiply | MPYS | 02h |
| 16-bit operand 1 – multiply accumulate | MAC | 04h |
| 16-bit operand 1 – signed multiply accumulate | MACS | 06h |
| 16-bit operand 2 | OP2 | 08h |
| 16 × 16 result low word | RESLO | 0Ah |
| 16 × 16 result high word | RESHI | 0Ch |
| 16 × 16 sum extension | SUMEXT | 0Eh |
| 32-bit operand 1 – multiply low word | MPY32L | 10h |
| 32-bit operand 1 – multiply high word | MPY32H | 12h |
| 32-bit operand 1 – signed multiply low word | MPYS32L | 14h |
| 32-bit operand 1 – signed multiply high word | MPYS32H | 16h |
| 32-bit operand 1 – multiply accumulate low word | MAC32L | 18h |
| 32-bit operand 1 – multiply accumulate high word | MAC32H | 1Ah |
| 32-bit operand 1 – signed multiply accumulate low word | MACS32L | 1Ch |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H | 1Eh |
| 32-bit operand 2 – low word | OP2L | 20h |
| 32-bit operand 2 – high word | OP2H | 22h |
| 32 × 32 result 0 – least significant word | RES0 | 24h |
| 32 × 32 result 1 | RES1 | 26h |
| 32 × 32 result 2 | RES2 | 28h |
| 32 × 32 result 3 – most significant word | RES3 | 2Ah |
| MPY32 control 0 | MPY32CTL0 | 2Ch |

Table 6-37. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|----------|--------|
| DMA channel 0 control | DMA0CTL | 00h |
| DMA channel 0 source address low | DMA0SAL | 02h |
| DMA channel 0 source address high | DMA0SAH | 04h |
| DMA channel 0 destination address low | DMA0DAL | 06h |
| DMA channel 0 destination address high | DMA0DAH | 08h |
| DMA channel 0 transfer size | DMA0SZ | 0Ah |
| DMA channel 1 control | DMA1CTL | 00h |
| DMA channel 1 source address low | DMA1SAL | 02h |
| DMA channel 1 source address high | DMA1SAH | 04h |
| DMA channel 1 destination address low | DMA1DAL | 06h |
| DMA channel 1 destination address high | DMA1DAH | 08h |

**Table 6-37. DMA Registers (Base Address DMA General Control: 0500h,
DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|----------|--------|
| DMA channel 1 transfer size | DMA1SZ | 0Ah |
| DMA channel 2 control | DMA2CTL | 00h |
| DMA channel 2 source address low | DMA2SAL | 02h |
| DMA channel 2 source address high | DMA2SAH | 04h |
| DMA channel 2 destination address low | DMA2DAL | 06h |
| DMA channel 2 destination address high | DMA2DAH | 08h |
| DMA channel 2 transfer size | DMA2SZ | 0Ah |
| DMA module control 0 | DMACTL0 | 00h |
| DMA module control 1 | DMACTL1 | 02h |
| DMA module control 2 | DMACTL2 | 04h |
| DMA module control 3 | DMACTL3 | 06h |
| DMA module control 4 | DMACTL4 | 08h |
| DMA interrupt vector | DMAIV | 0Eh |

Table 6-38. USCI_A0 Registers (Base Address: 05C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|------------|--------|
| USCI control 1 | UCA0CTL1 | 00h |
| USCI control 0 | UCA0CTL0 | 01h |
| USCI baud rate 0 | UCA0BR0 | 06h |
| USCI baud rate 1 | UCA0BR1 | 07h |
| USCI modulation control | UCA0MCTL | 08h |
| USCI status | UCA0STAT | 0Ah |
| USCI receive buffer | UCA0RXBUF | 0Ch |
| USCI transmit buffer | UCA0TXBUF | 0Eh |
| USCI LIN control | UCA0ABCTL | 10h |
| USCI IrDA transmit control | UCA0IRTCTL | 12h |
| USCI IrDA receive control | UCA0IRRCTL | 13h |
| USCI interrupt enable | UCA0IE | 1Ch |
| USCI interrupt flags | UCA0IFG | 1Dh |
| USCI interrupt vector word | UCA0IV | 1Eh |

Table 6-39. USCI_B0 Registers (Base Address: 05E0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------------|-----------|--------|
| USCI synchronous control 1 | UCB0CTL1 | 00h |
| USCI synchronous control 0 | UCB0CTL0 | 01h |
| USCI synchronous bit rate 0 | UCB0BR0 | 06h |
| USCI synchronous bit rate 1 | UCB0BR1 | 07h |
| USCI synchronous status | UCB0STAT | 0Ah |
| USCI synchronous receive buffer | UCB0RXBUF | 0Ch |
| USCI synchronous transmit buffer | UCB0TXBUF | 0Eh |
| USCI I2C own address | UCB0I2COA | 10h |
| USCI I2C slave address | UCB0I2CSA | 12h |
| USCI interrupt enable | UCB0IE | 1Ch |
| USCI interrupt flags | UCB0IFG | 1Dh |
| USCI interrupt vector word | UCB0IV | 1Eh |

Table 6-40. USCI_A1 Registers (Base Address: 0600h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|------------|--------|
| USCI control 1 | UCA1CTL1 | 00h |
| USCI control 0 | UCA1CTL0 | 01h |
| USCI baud rate 0 | UCA1BR0 | 06h |
| USCI baud rate 1 | UCA1BR1 | 07h |
| USCI modulation control | UCA1MCTL | 08h |
| USCI status | UCA1STAT | 0Ah |
| USCI receive buffer | UCA1RXBUF | 0Ch |
| USCI transmit buffer | UCA1TXBUF | 0Eh |
| USCI LIN control | UCA1ABCTL | 10h |
| USCI IrDA transmit control | UCA1IRTCTL | 12h |
| USCI IrDA receive control | UCA1IRRCTL | 13h |
| USCI interrupt enable | UCA1IE | 1Ch |
| USCI interrupt flags | UCA1IFG | 1Dh |
| USCI interrupt vector word | UCA1IV | 1Eh |

Table 6-41. USCI_B1 Registers (Base Address: 0620h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------------|-----------|--------|
| USCI synchronous control 1 | UCB1CTL1 | 00h |
| USCI synchronous control 0 | UCB1CTL0 | 01h |
| USCI synchronous bit rate 0 | UCB1BR0 | 06h |
| USCI synchronous bit rate 1 | UCB1BR1 | 07h |
| USCI synchronous status | UCB1STAT | 0Ah |
| USCI synchronous receive buffer | UCB1RXBUF | 0Ch |
| USCI synchronous transmit buffer | UCB1TXBUF | 0Eh |
| USCI I2C own address | UCB1I2COA | 10h |
| USCI I2C slave address | UCB1I2CSA | 12h |
| USCI interrupt enable | UCB1IE | 1Ch |
| USCI interrupt flags | UCB1IFG | 1Dh |
| USCI interrupt vector word | UCB1IV | 1Eh |

Table 6-42. ADC10_A Registers (Base Address: 0740h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|------------|--------|
| ADC10_A control 0 | ADC10CTL0 | 00h |
| ADC10_A control 1 | ADC10CTL1 | 02h |
| ADC10_A control 2 | ADC10CTL2 | 04h |
| ADC10_A window comparator low threshold | ADC10LO | 06h |
| ADC10_A window comparator high threshold | ADC10HI | 08h |
| ADC10_A memory control 0 | ADC10MCTL0 | 0Ah |
| ADC10_A conversion memory | ADC10MEM0 | 12h |
| ADC10_A interrupt enable | ADC10IE | 1Ah |
| ADC10_A interrupt flags | ADC10IGH | 1Ch |
| ADC10_A interrupt vector word | ADC10IV | 1Eh |

Table 6-43. Comparator_B Registers (Base Address: 08C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------|----------|--------|
| Comp_B control 0 | CBCTL0 | 00h |
| Comp_B control 1 | CBCTL1 | 02h |
| Comp_B control 2 | CBCTL2 | 04h |
| Comp_B control 3 | CBCTL3 | 06h |
| Comp_B interrupt | CBINT | 0Ch |
| Comp_B interrupt vector word | CBIV | 0Eh |

6.10 Input/Output Diagrams

6.10.1 Port P1 (P1.0 to P1.7) Input/Output With Schmitt Trigger

Figure 6-2 shows the port diagram. Table 6-44 summarizes the selection of the port function.

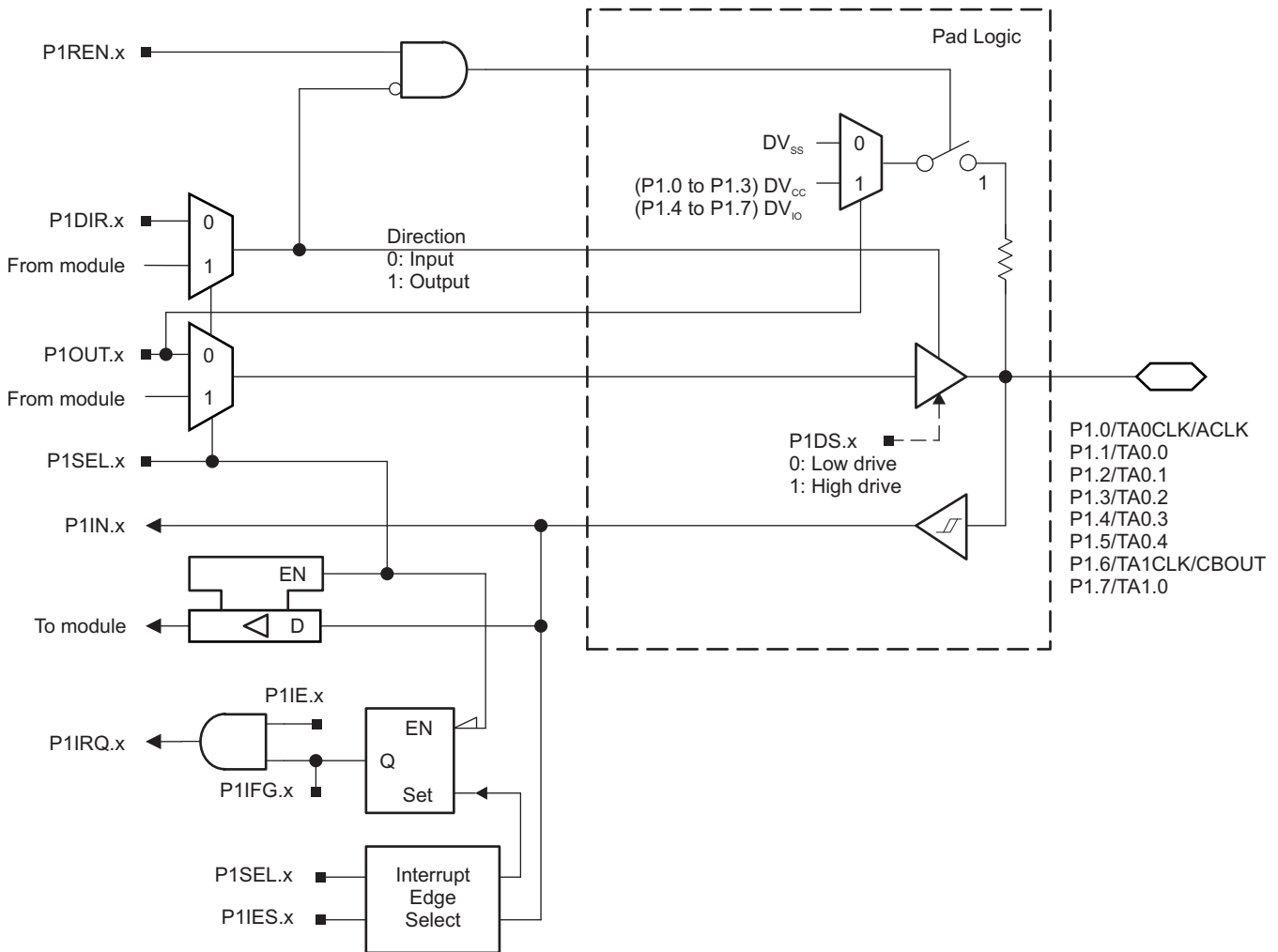


Figure 6-2. Port P1 (P1.0 to P1.7) Diagram

Table 6-44. Port P1 (P1.0 to P1.7) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | |
|-------------------|---|--------------------|-------------------------|---------|
| | | | P1DIR.x | P1SEL.x |
| P1.0/TA0CLK/ACLK | 0 | P1.0 (I/O) | I: 0; O: 1 | 0 |
| | | TA0CLK | 0 | 1 |
| | | ACLK | 1 | 1 |
| P1.1/TA0.0 | 1 | P1.1 (I/O) | I: 0; O: 1 | 0 |
| | | TA0.CCI0A | 0 | 1 |
| | | TA0.0 | 1 | 1 |
| P1.2/TA0.1 | 2 | P1.2 (I/O) | I: 0; O: 1 | 0 |
| | | TA0.CCI1A | 0 | 1 |
| | | TA0.1 | 1 | 1 |
| P1.3/TA0.2 | 3 | P1.3 (I/O) | I: 0; O: 1 | 0 |
| | | TA0.CCI2A | 0 | 1 |
| | | TA0.2 | 1 | 1 |
| P1.4/TA0.3 | 4 | P1.4 (I/O) | I: 0; O: 1 | 0 |
| | | TA0.CCI3A | 0 | 1 |
| | | TA0.3 | 1 | 1 |
| P1.5/TA0.4 | 5 | P1.5 (I/O) | I: 0; O: 1 | 0 |
| | | TA0.CCI4A | 0 | 1 |
| | | TA0.4 | 1 | 1 |
| P1.6/TA1CLK/CBOUT | 6 | P1.6 (I/O) | I: 0; O: 1 | 0 |
| | | TA1CLK | 0 | 1 |
| | | CBOUT comparator B | 1 | 1 |
| P1.7/TA1.0 | 7 | P1.7 (I/O) | I: 0; O: 1 | 0 |
| | | TA1.CCI0A | 0 | 1 |
| | | TA1.0 | 1 | 1 |

6.10.2 Port P2 (P2.0 to P2.7) Input/Output With Schmitt Trigger

Figure 6-3 shows the port diagram. Table 6-45 summarizes the selection of the port function.

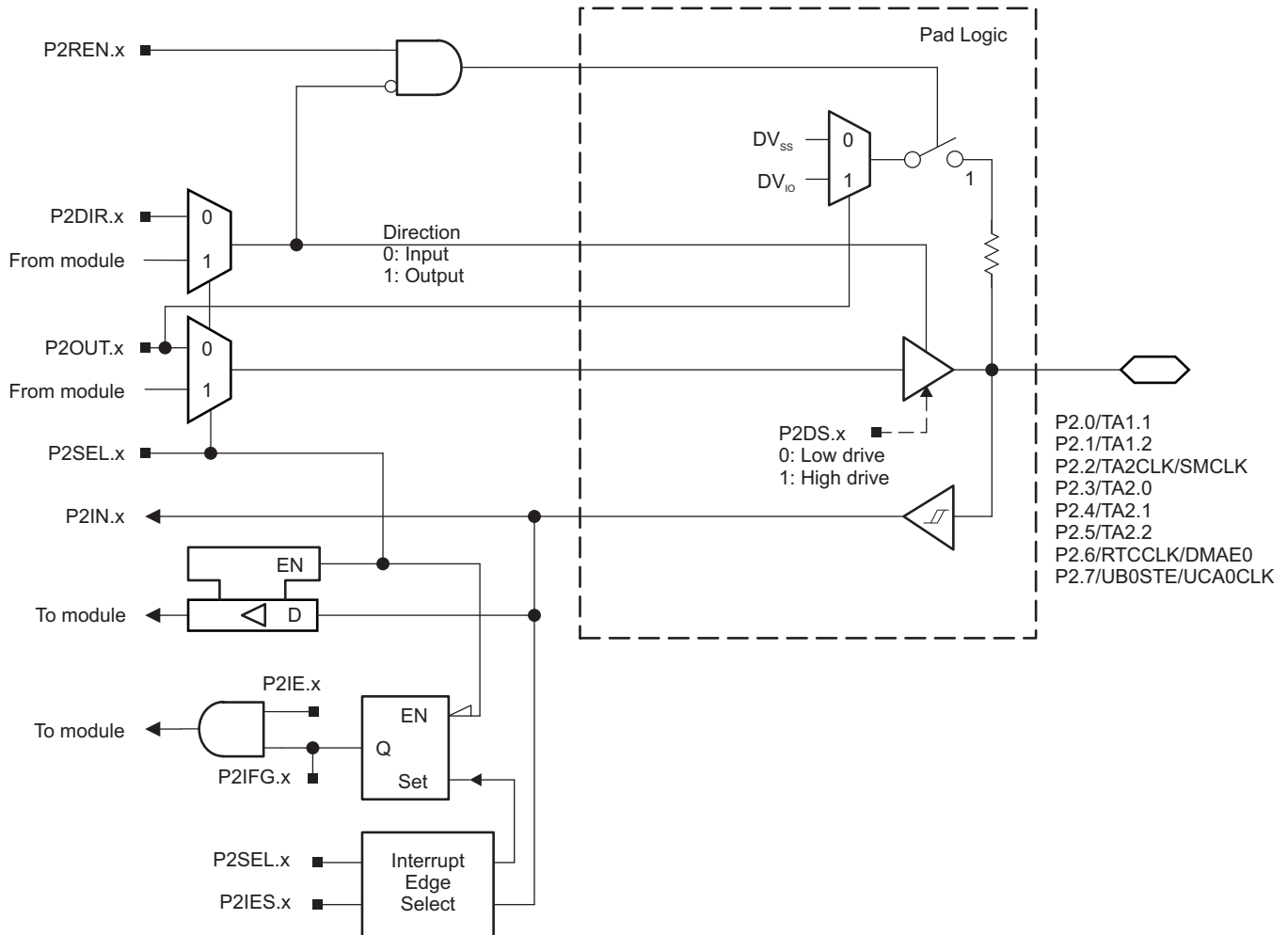


Figure 6-3. Port P2 (P2.0 to P2.7) Diagram

Table 6-45. Port P2 (P2.0 to P2.7) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | |
|----------------------------------|---|------------------------------------|--|---------|
| | | | P2DIR.x | P2SEL.x |
| P2.0/TA1.1 ⁽²⁾ | 0 | P2.0 (I/O) | I: 0; O: 1 | 0 |
| | | TA1.CCI1A | 0 | 1 |
| | | TA1.1 | 1 | 1 |
| P2.1/TA1.2 ⁽²⁾ | 1 | P2.1 (I/O) | I: 0; O: 1 | 0 |
| | | TA1.CCI2A | 0 | 1 |
| | | TA1.2 | 1 | 1 |
| P2.2/TA2CLK/SMCLK ⁽²⁾ | 2 | P2.2 (I/O) | I: 0; O: 1 | 0 |
| | | TA2CLK | 0 | 1 |
| | | SMCLK | 1 | 1 |
| P2.3/TA2.0 ⁽²⁾ | 3 | P2.3 (I/O) | I: 0; O: 1 | 0 |
| | | TA2.CCI0A | 0 | 1 |
| | | TA2.0 | 1 | 1 |
| P2.4/TA2.1 ⁽²⁾ | 4 | P2.4 (I/O) | I: 0; O: 1 | 0 |
| | | TA2.CCI1A | 0 | 1 |
| | | TA2.1 | 1 | 1 |
| P2.5/TA2.2 ⁽²⁾ | 5 | P2.5 (I/O) | I: 0; O: 1 | 0 |
| | | TA2.CCI2A | 0 | 1 |
| | | TA2.2 | 1 | 1 |
| P2.6/RTCCLK/DMAE0 ⁽²⁾ | 6 | P2.6 (I/O) | I: 0; O: 1 | 0 |
| | | DMAE0 | 0 | 1 |
| | | RTCCLK | 1 | 1 |
| P2.7/UCB0STE/UCA0CLK | 7 | P2.7 (I/O) | I: 0; O: 1 | 0 |
| | | UCB0STE/UCA0CLK ^{(3) (4)} | X | 1 |

(1) X = Don't care

(2) Not available on RGZ package types.

(3) The pin direction is controlled by the USCI module.

(4) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI_B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

6.10.3 Port P3 (P3.0 to P3.4) Input/Output With Schmitt Trigger

Figure 6-4 shows the port diagram. Table 6-46 summarizes the selection of the port function.

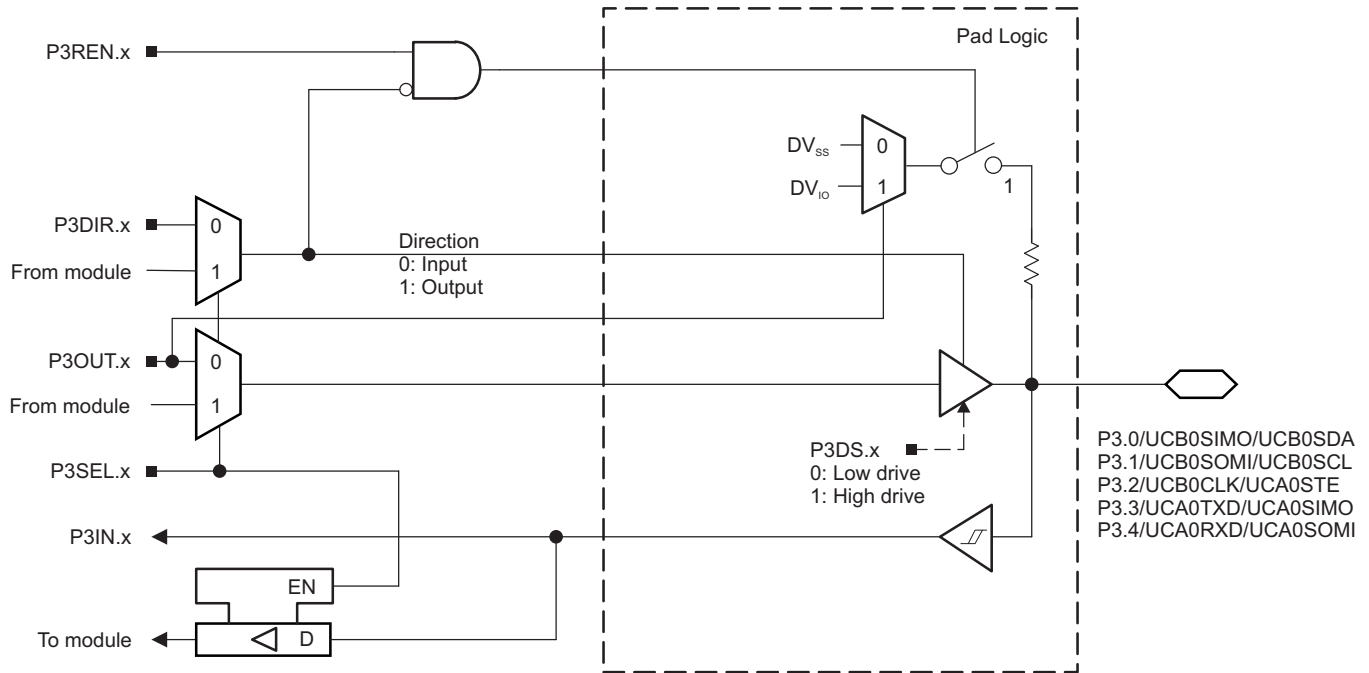


Figure 6-4. Port P3 (P3.0 to P3.4) Diagram

Table 6-46. Port P3 (P3.0 to P3.4) Pin Functions

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | |
|-----------------------|---|-------------------------------------|--|---------|
| | | | P3DIR.x | P3SEL.x |
| P3.0/UCB0SIMO/UCB0SDA | 0 | P3.0 (I/O) | I: 0; O: 1 | 0 |
| | | UCB0SIMO/UCB0SDA ^{(2) (3)} | X | 1 |
| P3.1/UCB0SOMI/UCB0SCL | 1 | P3.1 (I/O) | I: 0; O: 1 | 0 |
| | | UCB0SOMI/UCB0SCL ^{(2) (3)} | X | 1 |
| P3.2/UCB0CLK/UCA0STE | 2 | P3.2 (I/O) | I: 0; O: 1 | 0 |
| | | UCB0CLK/UCA0STE ^{(2) (4)} | X | 1 |
| P3.3/UCA0TXD/UCA0SIMO | 3 | P3.3 (I/O) | I: 0; O: 1 | 0 |
| | | UCA0TXD/UCA0SIMO ⁽²⁾ | X | 1 |
| P3.4/UCA0RXD/UCA0SOMI | 4 | P3.4 (I/O) | I: 0; O: 1 | 0 |
| | | UCA0RXD/UCA0SOMI ⁽²⁾ | X | 1 |

(1) X = Don't care

(2) The pin direction is controlled by the USCI module.

(3) If the I2C functionality is selected, the output drives only the logical 0 to V_{SS} level.

(4) UCB0CLK function takes precedence over UCA0STE function. If the pin is required as UCB0CLK input or output, USCI_A0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

6.10.4 Port P4 (P4.0 to P4.7) Input/Output With Schmitt Trigger

Figure 6-5 shows the port diagram. Table 6-47 summarizes the selection of the port function.

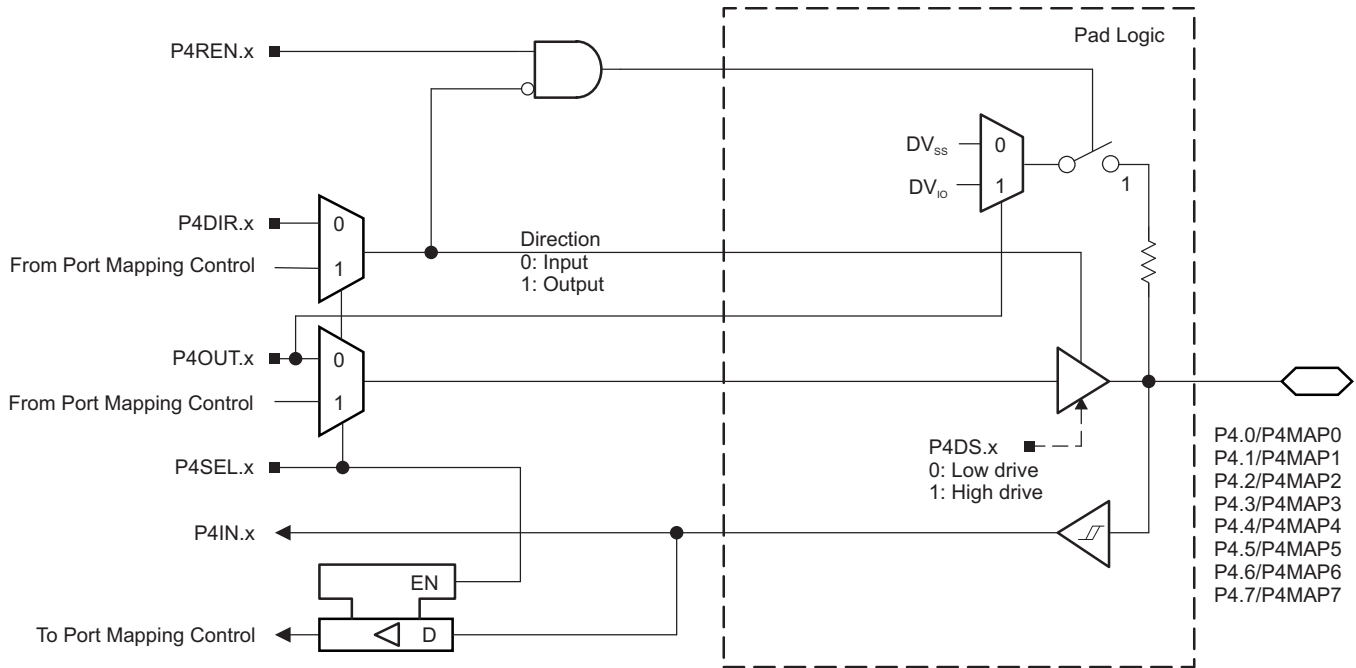


Figure 6-5. Port P4 (P4.0 to P4.7) Diagram

Table 6-47. Port P4 (P4.0 to P4.7) Pin Functions

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|----------------------------|---|-----------------------------------|--|---------|--------|
| | | | P4DIR.x ⁽²⁾ | P4SEL.x | P4MAPx |
| P4.0/P4MAP0 | 0 | P4.0 (I/O) | I: 0; O: 1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| P4.1/P4MAP1 | 1 | P4.1 (I/O) | I: 0; O: 1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| P4.2/P4MAP2 | 2 | P4.2 (I/O) | I: 0; O: 1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| P4.3/P4MAP3 | 3 | P4.3 (I/O) | I: 0; O: 1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| P4.4/P4MAP4 | 4 | P4.4 (I/O) | I: 0; O: 1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| P4.5/P4MAP5 | 5 | P4.5 (I/O) | I: 0; O: 1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| P4.6/P4MAP6 | 6 | P4.6 (I/O) | I: 0; O: 1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| P4.7/P4MAP7 ⁽³⁾ | 7 | P4.7 (I/O) | I: 0; O: 1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |

(1) X = Don't care

(2) The direction of some mapped secondary functions are controlled directly by the module. See Table 6-7 for specific direction control information of mapped secondary functions.

(3) Not available on RGZ package types.

6.10.5 Port P5 (P5.0 and P5.1) Input/Output With Schmitt Trigger

Figure 6-6 shows the port diagram. Table 6-48 summarizes the selection of the port function.

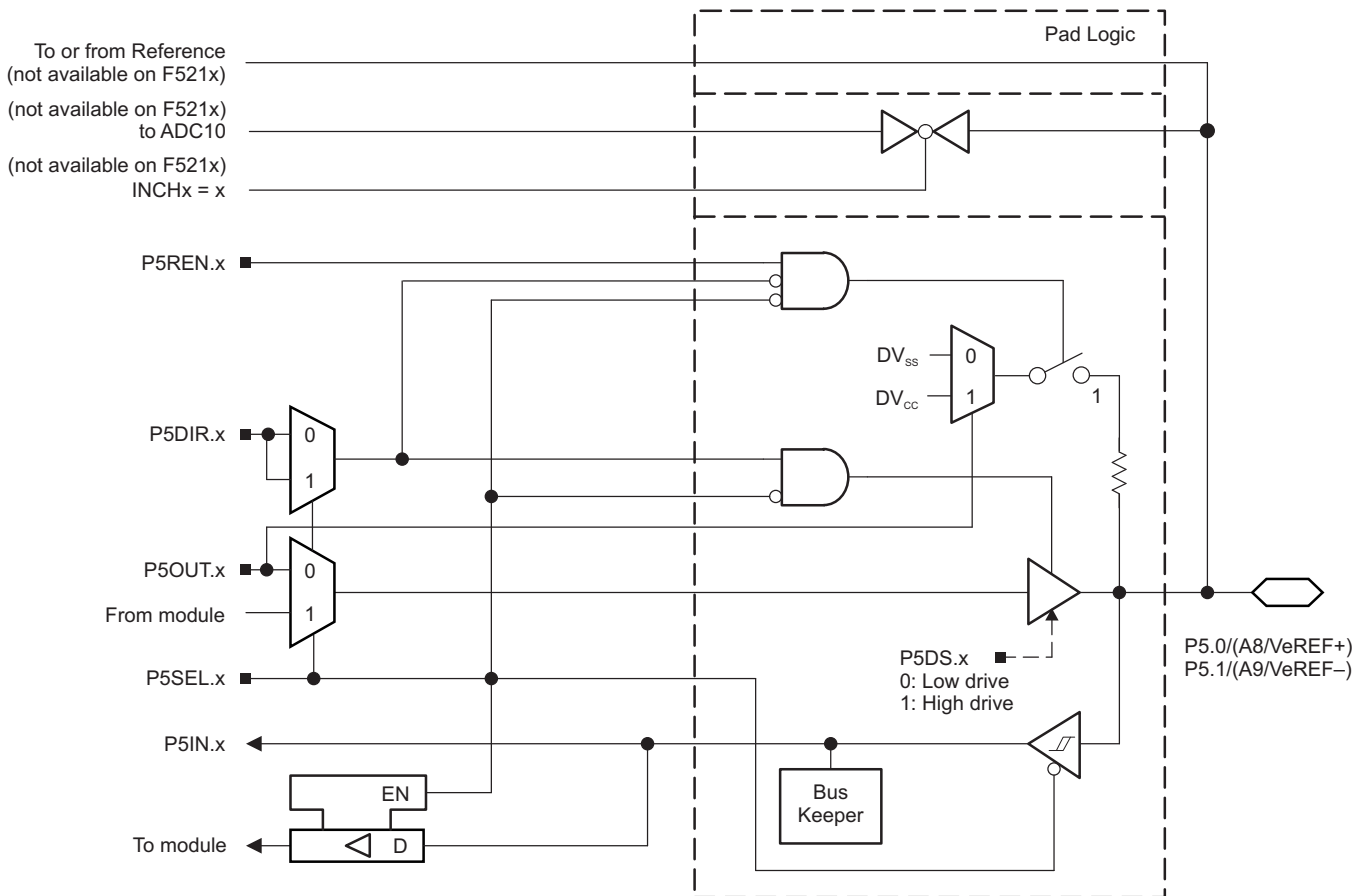


Figure 6-6. Port P5 (P5.0 and P5.1) Diagram

Table 6-48. Port P5 (P5.0 and P5.1) Pin Functions

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------|---|---------------------------|--|---------|-----------------------|
| | | | P5DIR.x | P5SEL.x | REFOUT ⁽²⁾ |
| P5.0/A8/VeREF+ | 0 | P5.0 (I/O) ⁽³⁾ | I: 0; O: 1 | 0 | X |
| | | A8/VeREF+ ⁽⁴⁾ | X | 1 | 0 |
| P5.1/A9/VeREF- | 1 | P5.1 (I/O) ⁽³⁾ | I: 0; O: 1 | 0 | X |
| | | A9/VeREF- ⁽⁵⁾ | X | 1 | 0 |

(1) X = Don't care

(2) REFOUT resides in the REF module.

(3) Default condition

(4) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF+ and used as the reference for the ADC10_A. Channel A8, when selected with the INCHx bits, is connected to the VeREF+ pin.

(5) Setting the P5SEL.1 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF- and used as the reference for the ADC10_A. Channel A9, when selected with the INCHx bits, is connected to the VeREF- pin.

6.10.6 Port P5 (P5.2) Input/Output With Schmitt Trigger

Figure 6-7 shows the port diagram. Table 6-49 summarizes the selection of the port function.

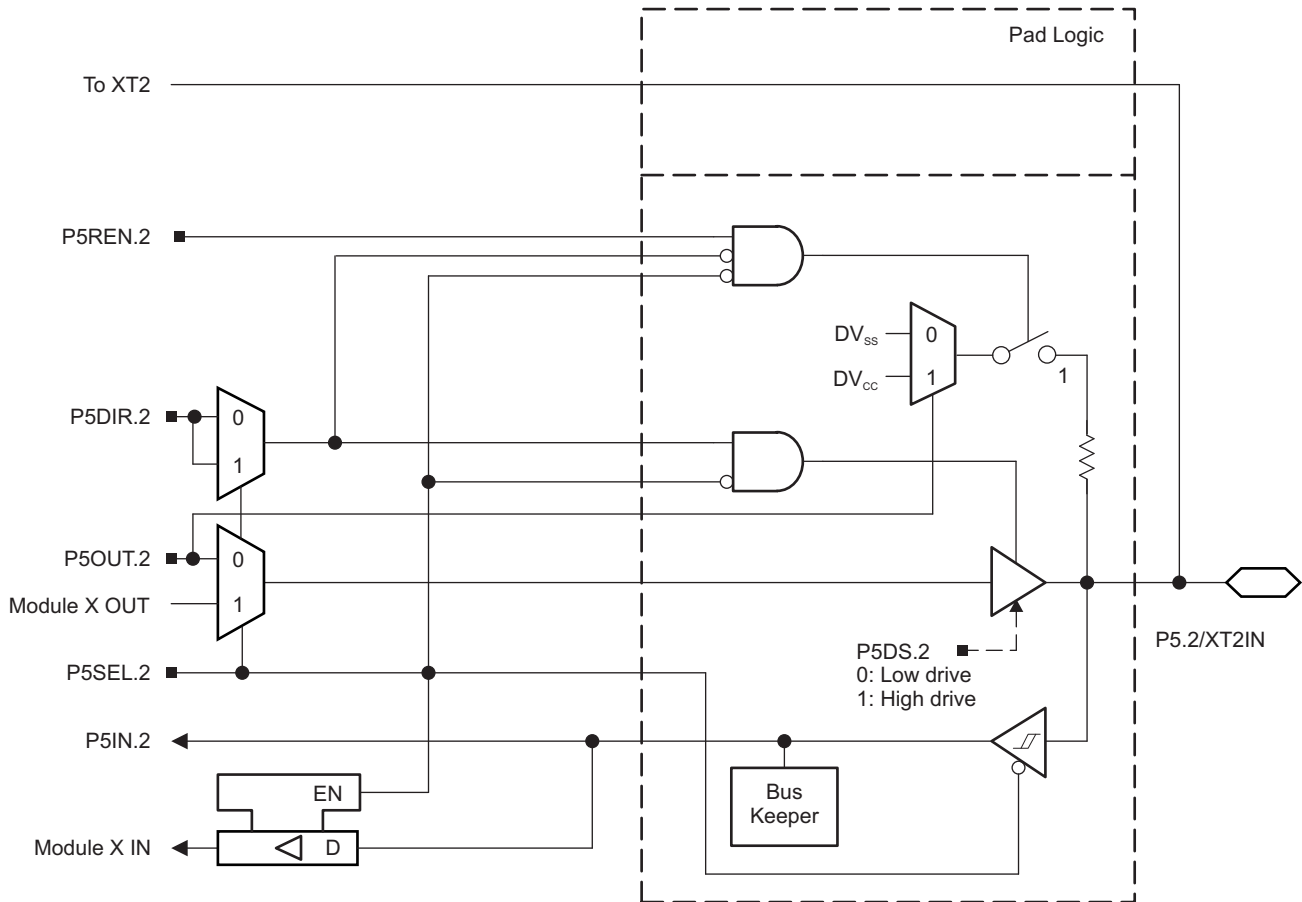


Figure 6-7. Port P5 (P5.2) Diagram

6.10.7 Port P5 (P5.3) Input/Output With Schmitt Trigger

Figure 6-8 shows the port diagram. Table 6-49 summarizes the selection of the port function.

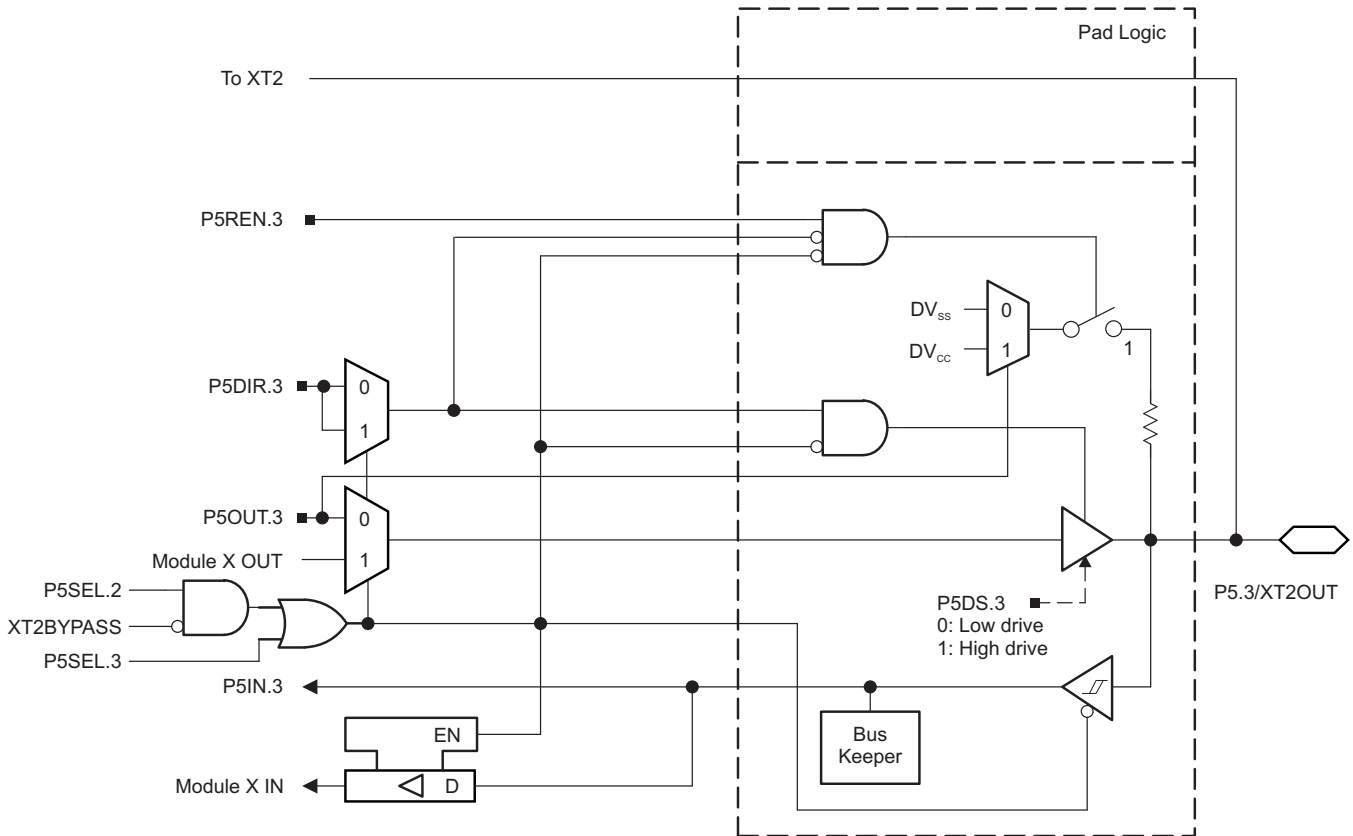


Figure 6-8. Port P5 (P5.3) Diagram

Table 6-49. Port P5 (P5.2 and P5.3) Pin Functions

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|-----------------|---|------------------------------------|--|---------|---------|-----------|
| | | | P5DIR.x | P5SEL.2 | P5SEL.3 | XT2BYPASS |
| P5.2/XT2IN | 2 | P5.2 (I/O) | I: 0; O: 1 | 0 | X | X |
| | | XT2IN crystal mode ⁽²⁾ | X | 1 | X | 0 |
| | | XT2IN bypass mode ⁽²⁾ | X | 1 | X | 1 |
| P5.3/XT2OUT | 3 | P5.3 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | XT2OUT crystal mode ⁽³⁾ | X | 1 | X | 0 |
| | | P5.3 (I/O) ⁽³⁾ | X | 1 | 0 | 1 |

(1) X = Don't care

(2) Setting P5SEL.2 causes the general-purpose I/O to be disabled. Pending the setting of XT2BYPASS, P5.2 is configured for crystal mode or bypass mode.

(3) Setting P5SEL.2 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.3 can be used as general-purpose I/O.

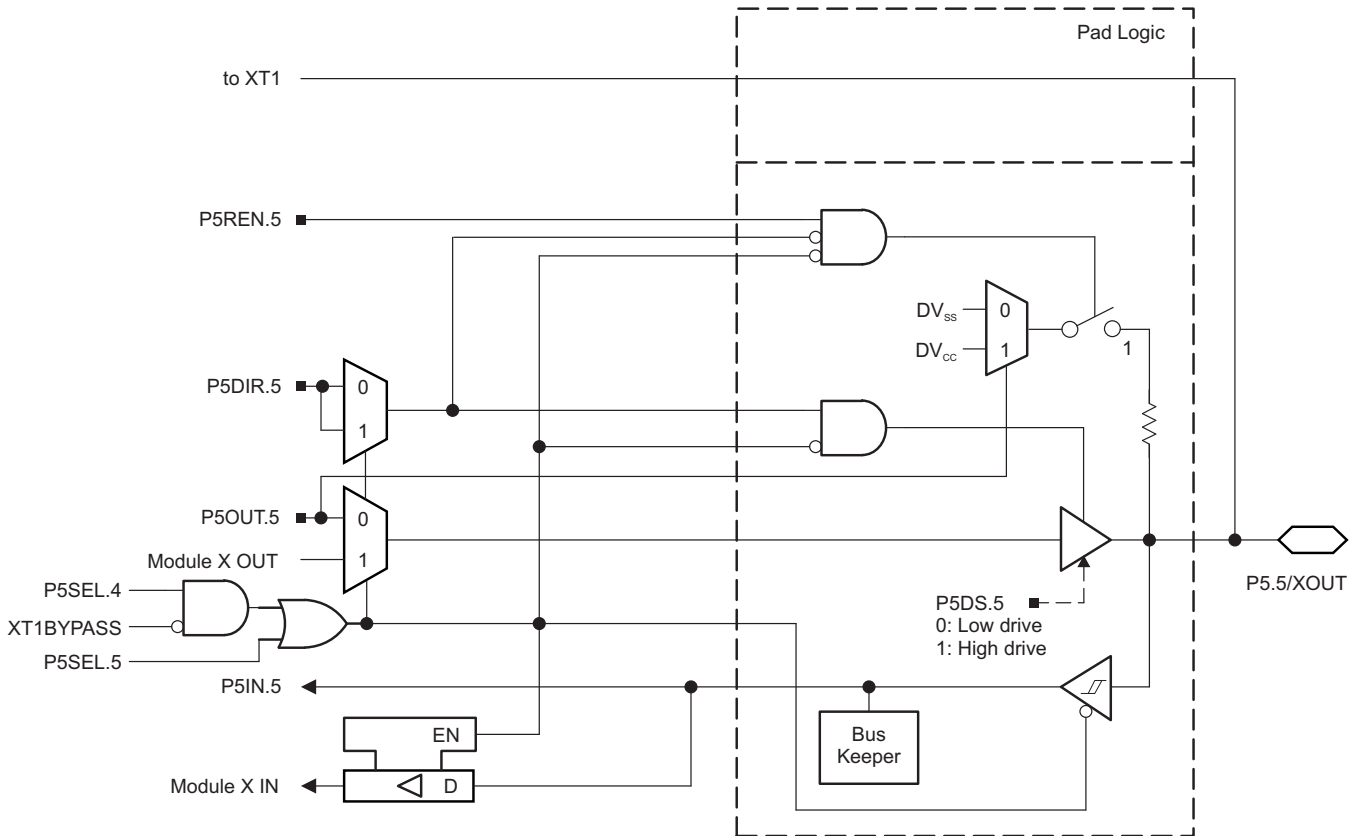


Figure 6-10. Port P5 (P5.5) Diagram

Table 6-50. Port P5 (P5.4 and P5.5) Pin Functions

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|-----------------|---|----------------------------------|--|---------|---------|-----------|
| | | | P5DIR.x | P5SEL.4 | P5SEL.5 | XT1BYPASS |
| P5.4/XIN | 4 | P5.4 (I/O) | I: 0; O: 1 | 0 | X | X |
| | | XIN crystal mode ⁽²⁾ | X | 1 | X | 0 |
| | | XIN bypass mode ⁽²⁾ | X | 1 | X | 1 |
| P5.5/XOUT | 5 | P5.5 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | XOUT crystal mode ⁽³⁾ | X | 1 | X | 0 |
| | | P5.5 (I/O) ⁽³⁾ | X | 1 | 0 | 1 |

- (1) X = Don't care
(2) Setting P5SEL.4 causes the general-purpose I/O to be disabled. Pending the setting of XT1BYPASS, P5.4 is configured for crystal mode or bypass mode.
(3) Setting P5SEL.4 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.5 can be used as general-purpose I/O.

6.10.9 Port P6 (P6.0 to P6.7) Input/Output With Schmitt Trigger

Figure 6-11 shows the port diagram. Table 6-51 summarizes the selection of the port function.

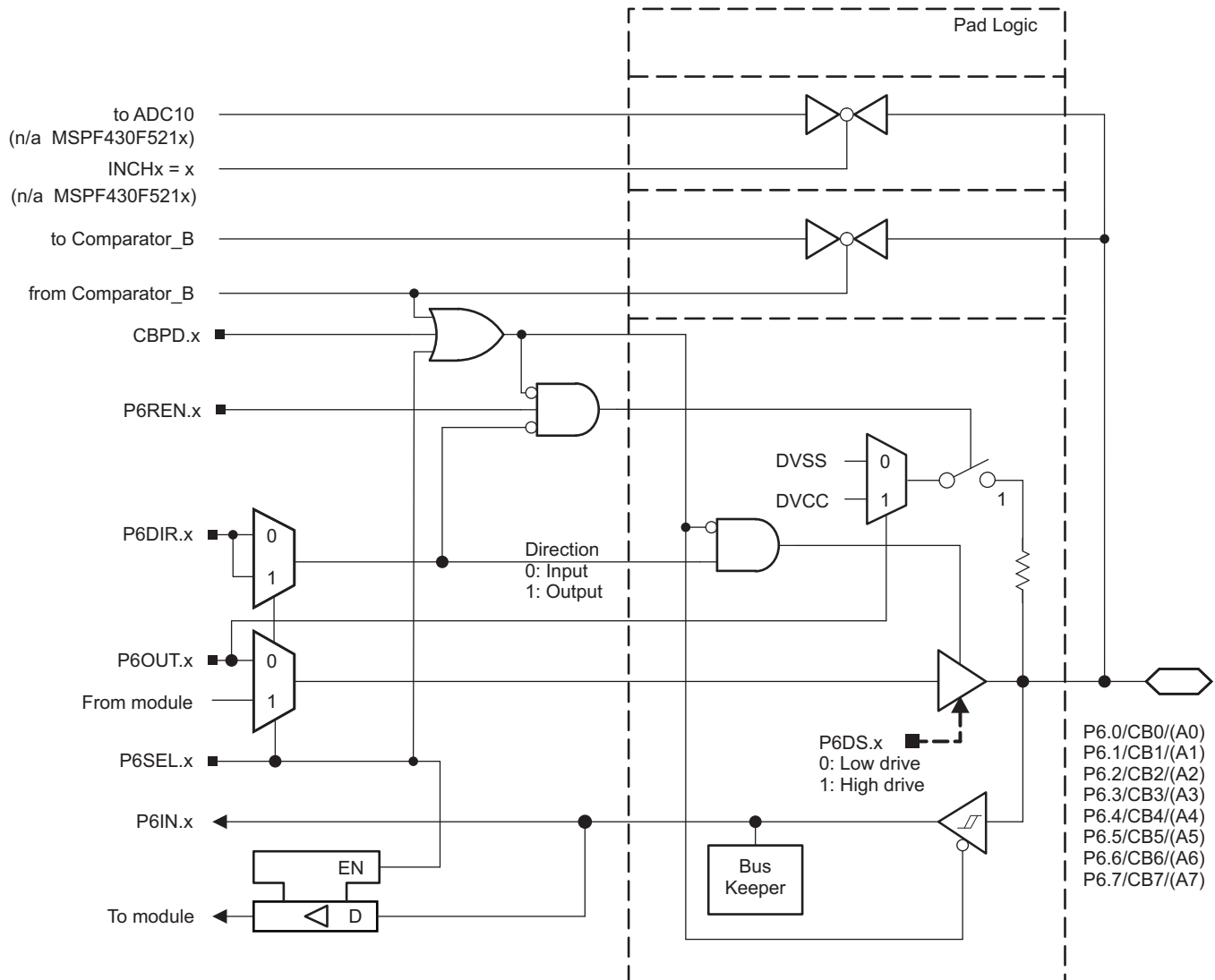


Figure 6-11. Port P6 (P6.0 to P6.7) Diagram

Table 6-51. Port P6 (P6.0 to P6.7) Pin Functions

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | | |
|------------------------------|---|--------------------|-------------------------|---------|------|
| | | | P6DIR.x | P6SEL.x | CBPD |
| P6.0/CB0/(A0) | 0 | P6.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A0 | X | 1 | X |
| | | CB0 ⁽¹⁾ | X | X | 1 |
| P6.1/CB1/(A1) | 1 | P6.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A1 | X | 1 | X |
| | | CB1 ⁽¹⁾ | X | X | 1 |
| P6.2/CB2/(A2) | 2 | P6.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A2 | X | 1 | X |
| | | CB2 ⁽¹⁾ | X | X | 1 |
| P6.3/CB3/(A3) | 3 | P6.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A3 | X | 1 | X |
| | | CB3 ⁽¹⁾ | X | X | 1 |
| P6.4/CB4/(A4) | 4 | P6.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A4 | X | 1 | X |
| | | CB4 ⁽¹⁾ | X | X | 1 |
| P6.5/CB5/(A5) | 5 | P6.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A5 | X | 1 | X |
| | | CB5 ⁽¹⁾ | X | X | 1 |
| P6.6/CB6/(A6) ⁽²⁾ | 6 | P6.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A6 | X | 1 | X |
| | | CB6 ⁽¹⁾ | X | X | 1 |
| P6.7/CB7/(A7) ⁽²⁾ | 7 | P6.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A7 | X | 1 | X |
| | | CB7 ⁽¹⁾ | X | X | 1 |

(1) Setting the CBPD.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CBx input pin to the comparator multiplexer with the CBx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CBPD.x bit.

(2) Not available on RGZ package types.

6.10.10 Port P7 (P7.0 to P7.5) Input/Output With Schmitt Trigger

Figure 6-12 shows the port diagram. Table 6-52 summarizes the selection of the port function.

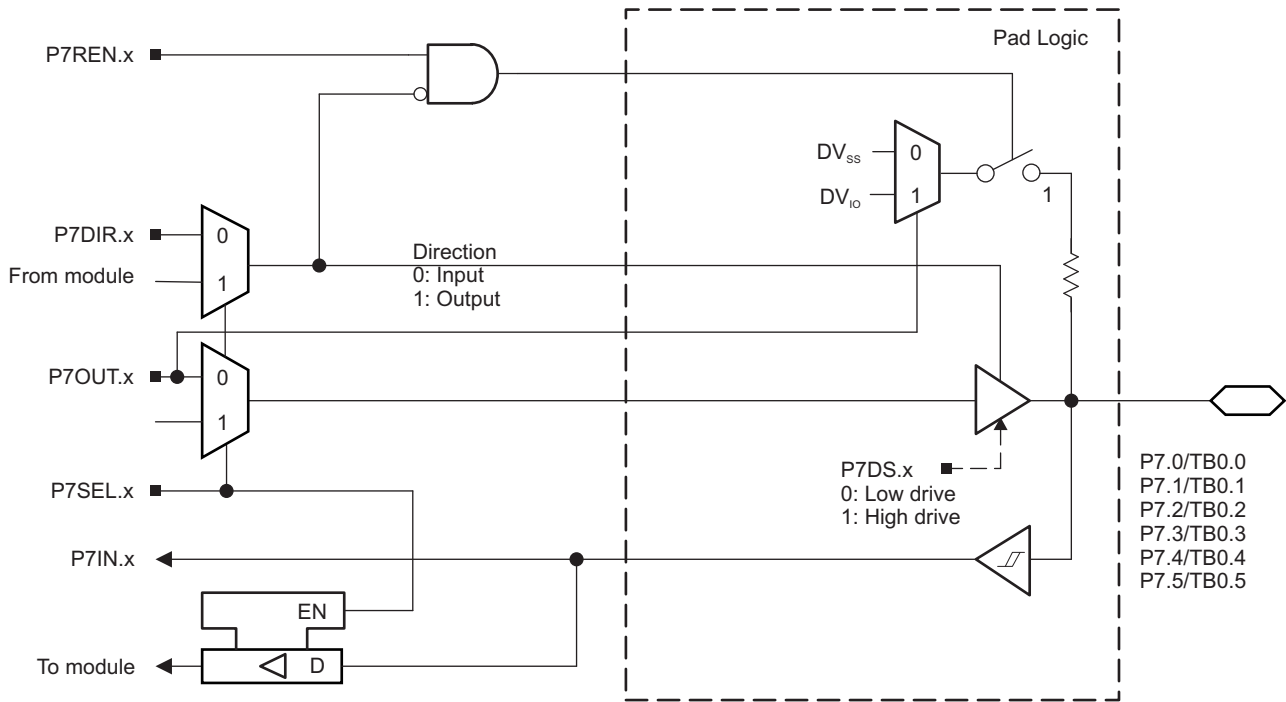


Figure 6-12. Port P7 (P7.0 to P7.5) Diagram

Table 6-52. Port P7 (P7.0 to P7.5) Pin Functions

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | |
|---------------------------|---|------------|-------------------------|---------|
| | | | P7DIR.x | P7SEL.x |
| P7.0/TB0.0 ⁽¹⁾ | 0 | P7.0 (I/O) | I: 0; O: 1 | 0 |
| | | TB0.CCI0A | 0 | 1 |
| | | TB0.0 | 1 | 1 |
| P7.1/TB0.1 ⁽¹⁾ | 1 | P7.1 (I/O) | I: 0; O: 1 | 0 |
| | | TB0.CCI1A | 0 | 1 |
| | | TB0.1 | 1 | 1 |
| P7.2/TB0.2 ⁽¹⁾ | 2 | P7.2 (I/O) | I: 0; O: 1 | 0 |
| | | TB0.CCI2A | 0 | 1 |
| | | TB0.2 | 1 | 1 |
| P7.3/TB0.3 ⁽¹⁾ | 3 | P7.3 (I/O) | I: 0; O: 1 | 0 |
| | | TB0.CCI3A | 0 | 1 |
| | | TB0.3 | 1 | 1 |
| P7.4/TB0.4 ⁽¹⁾ | 4 | P7.4 (I/O) | I: 0; O: 1 | 0 |
| | | TB0.CCI4A | 0 | 1 |
| | | TB0.4 | 1 | 1 |
| P7.5/TB0.5 ⁽¹⁾ | 5 | P7.5 (I/O) | I: 0; O: 1 | 0 |
| | | TB0.CCI5A | 0 | 1 |
| | | TB0.5 | 1 | 1 |

(1) Not available on RGZ package types.

6.10.11 Port PJ (PJ.0) JTAG Pin TDO, Input/Output With Schmitt Trigger or Output

Figure 6-13 shows the port diagram. Table 6-53 summarizes the selection of the port function.

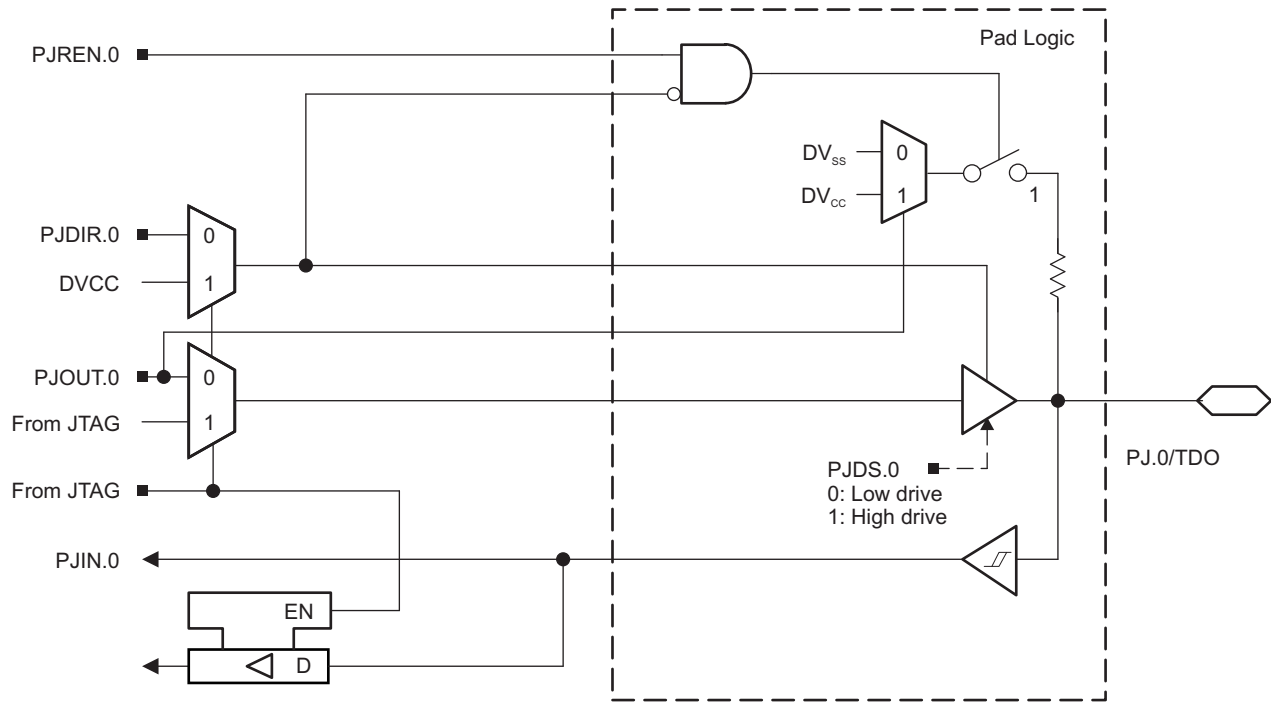


Figure 6-13. Port PJ (PJ.0) Diagram

6.10.12 Port PJ (PJ.1 to PJ.3) JTAG Pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

Figure 6-14 shows the port diagram. Table 6-53 summarizes the selection of the port function.

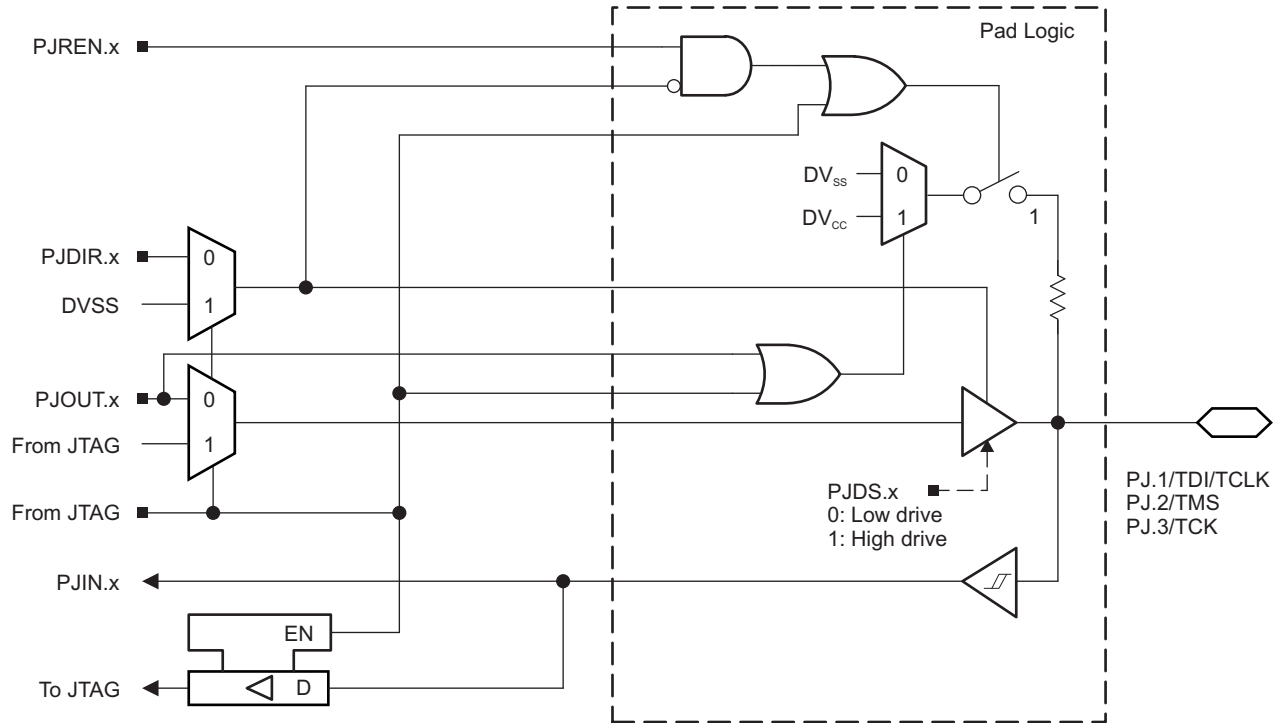


Figure 6-14. Port PJ (PJ.1 to PJ.3) Diagram

Table 6-53. Port PJ (PJ.0 to PJ.3) Pin Functions

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ |
|-----------------|---|-----------------------------|--|
| | | | PJDIR.x |
| PJ.0/TDO | 0 | PJ.0 (I/O) ⁽²⁾ | I: 0; O: 1 |
| | | TDO ⁽³⁾ | X |
| PJ.1/TDI/TCLK | 1 | PJ.1 (I/O) ⁽²⁾ | I: 0; O: 1 |
| | | TDI/TCLK ^{(3) (4)} | X |
| PJ.2/TMS | 2 | PJ.2 (I/O) ⁽²⁾ | I: 0; O: 1 |
| | | TMS ^{(3) (4)} | X |
| PJ.3/TCK | 3 | PJ.3 (I/O) ⁽²⁾ | I: 0; O: 1 |
| | | TCK ^{(3) (4)} | X |

- (1) X = Don't care
- (2) Default condition
- (3) The pin direction is controlled by the JTAG module.
- (4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are do not care.

6.11 Device Descriptors

Table 6-54 and Table 6-55 list the contents of the device descriptor tag-length-value (TLV) structure for each device type.

Table 6-54. MSP430F522x Device Descriptor Table⁽¹⁾

| DESCRIPTION | ADDRESS | SIZE (BYTES) | VALUE | | | | |
|-------------------|--|-----------------|-------|----------|----------|----------|----------|
| | | | F5229 | F5227 | F5224 | F5222 | |
| Info Block | Info length | 01A00h | 1 | 06h | 06h | 06h | 06h |
| | CRC length | 01A01h | 1 | 06h | 06h | 06h | 06h |
| | CRC value | 01A02h | 2 | Per unit | Per unit | Per unit | Per unit |
| | Device ID | 01A04h | 1 | 51h | 4Fh | 4Ch | 4Ah |
| | Device ID | 01A05h | 1 | 81h | 81h | 81h | 81h |
| | Hardware revision | 01A06h | 1 | Per unit | Per unit | Per unit | Per unit |
| | Firmware revision | 01A07h | 1 | Per unit | Per unit | Per unit | Per unit |
| Die Record | Die record tag | 01A08h | 1 | 08h | 08h | 08h | 08h |
| | Die record length | 01A09h | 1 | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot/wafer ID | 01A0Ah | 4 | Per unit | Per unit | Per unit | Per unit |
| | Die X position | 01A0Eh | 2 | Per unit | Per unit | Per unit | Per unit |
| | Die Y position | 01A10h | 2 | Per unit | Per unit | Per unit | Per unit |
| | Test results | 01A12h | 2 | Per unit | Per unit | Per unit | Per unit |
| ADC10 Calibration | ADC10 calibration tag | 01A14h | 1 | 13h | 13h | 13h | 13h |
| | ADC10 calibration length | 01A15h | 1 | 10h | 10h | 10h | 10h |
| | ADC gain factor | 01A16h | 2 | Per unit | Per unit | Per unit | Per unit |
| | ADC offset | 01A18h | 2 | Per unit | Per unit | Per unit | Per unit |
| | ADC 1.5-V reference Temperature sensor 30°C | 01A1Ah | 2 | Per unit | Per unit | Per unit | Per unit |
| | ADC 1.5-V reference Temperature sensor 85°C | 01A1Ch | 2 | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.0-V reference Temperature sensor 30°C | 01A1Eh | 2 | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.0-V reference Temperature sensor 85°C | 01A20h | 2 | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.5-V reference Temperature sensor 30°C | 01A22h | 2 | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.5-V reference Temperature sensor 85°C | 01A24h | 2 | Per unit | Per unit | Per unit | Per unit |
| REF Calibration | REF calibration tag | 01A26h | 1 | 12h | 12h | 12h | 12h |
| | REF calibration length | 01A27h | 1 | 06h | 06h | 06h | 06h |
| | REF 1.5-V reference factor | 01A28h | 2 | Per unit | Per unit | Per unit | Per unit |
| | REF 2.0-V reference factor | 01A2Ah | 2 | Per unit | Per unit | Per unit | Per unit |
| | REF 2.5-V reference factor | 01A2Ch | 2 | Per unit | Per unit | Per unit | Per unit |

(1) NA = Not applicable

Table 6-54. MSP430F522x Device Descriptor Table⁽¹⁾ (continued)

| DESCRIPTION | ADDRESS | SIZE (BYTES) | VALUE | | | |
|------------------------------|---------|-----------------|------------|------------|------------|------------|
| | | | F5229 | F5227 | F5224 | F5222 |
| Peripheral descriptor tag | 01A2Eh | 1 | 02h | 02h | 02h | 02h |
| Peripheral descriptor length | 01A2Fh | 1 | 5Fh | 5Fh | 5Dh | 5Dh |
| Memory 1 | | 2 | 08h 8Ah | 08h 8Ah | 08h 8Ah | 08h 8Ah |
| Memory 2 | | 2 | 0Ch 86h | 0Ch 86h | 0Ch 86h | 0Ch 86h |
| Memory 3 | | 2 | 12h 2Eh | 12h 2Eh | 12h 2Eh | 12h 2Eh |
| Memory 4 | | 2 | 22h 96h | 22h 94h | 22h 96h | 22h 94h |
| Memory 5 | | 2 | N/A | N/A | N/A | N/A |
| Memory 6 | | 1/2 | N/A | N/A | N/A | N/A |
| Delimiter | | 1 | 00h | 00h | 00h | 00h |
| Peripheral count | | 1 | 20h | 20h | 1Fh | 1Fh |
| MSP430CPUXV2 | | 2 | 00h 23h | 00h 23h | 00h 23h | 00h 23h |
| JTAG | | 2 | 00h 09h | 00h 09h | 00h 09h | 00h 09h |
| SBW | | 2 | 00h 0Fh | 00h 0Fh | 00h 0Fh | 00h 0Fh |
| EEM-S | | 2 | 00h 03h | 00h 03h | 00h 03h | 00h 05h |
| TI BSL | | 2 | 00h FCh | 00h FCh | 00h FCh | 00h FCh |
| SFR | | 2 | 10h 41h | 10h 41h | 10h 41h | 10h 41h |
| PMM | | 2 | 02h 30h | 02h 30h | 02h 30h | 02h 30h |
| FCTL | | 2 | 02h 38h | 02h 38h | 02h 38h | 02h 38h |
| CRC16 | | 2 | 01h 3Ch | 01h 3Ch | 01h 3Ch | 01h 3Ch |
| CRC16_RB | | 2 | 00h 3Dh | 00h 3Dh | 00h 3Dh | 00h 3Dh |
| RAMCTL | | 2 | 00h 44h | 00h 44h | 00h 44h | 00h 44h |
| WDT_A | | 2 | 00h 40h | 00h 40h | 00h 40h | 00h 40h |
| UCS | | 2 | 01h 48h | 01h 48h | 01h 48h | 01h 48h |
| SYS | | 2 | 02h 42h | 02h 42h | 02h 42h | 02h 42h |
| REF | | 2 | 03h A0h | 03h A0h | 03h A0h | 03h A0h |
| Port mapping | | 2 | 01h 10h | 01h 10h | 01h 10h | 01h 10h |
| Port 1/2 | | 2 | 04h 51h | 04h 51h | 04h 51h | 04h 51h |
| Port 3/4 | | 2 | 02h 52h | 02h 52h | 02h 52h | 02h 52h |
| Port 5/6 | | 2 | 02h 53h | 02h 53h | 02h 53h | 02h 53h |

Peripheral
Descriptor

Table 6-54. MSP430F522x Device Descriptor Table⁽¹⁾ (continued)

| DESCRIPTION | ADDRESS | SIZE (BYTES) | VALUE | | | | |
|---|---------------|-----------------|-------|------------|------------|------------|------------|
| | | | F5229 | F5227 | F5224 | F5222 | |
| Peripheral Descriptor (continued) | Port 7/8 | | 2 | 02h 54h | 02h 54h | N/A | N/A |
| | JTAG | | 2 | 0Ch 5Fh | 0Ch 5Fh | 0Eh 5Fh | 0Eh 5Fh |
| | TA0 | | 2 | 02h 62h | 02h 62h | 02h 62h | 02h 62h |
| | TA1 | | 2 | 04h 61h | 04h 61h | 04h 61h | 04h 61h |
| | TB0 | | 2 | 04h 67h | 04h 67h | 04h 67h | 04h 67h |
| | TA2 | | 2 | 04h 61h | 04h 61h | 04h 61h | 04h 61h |
| | RTC | | 2 | 0Ah 68h | 0Ah 68h | 0Ah 68h | 0Ah 68h |
| | MPY32 | | 2 | 02h 85h | 02h 85h | 02h 85h | 02h 85h |
| | DMA-3 | | 2 | 04h 47h | 04h 47h | 04h 47h | 04h 47h |
| | USCI_A/B | | 2 | 0Ch 90h | 0Ch 90h | 0Ch 90h | 0Ch 90h |
| | USCI_A/B | | 2 | 04h 90h | 04h 90h | 04h 90h | 04h 90h |
| | ADC10_A | | 2 | 14h D3h | 14h D3h | 14h D3h | 14h D3h |
| | COMP_B | | 2 | 18h A8h | 18h A8h | 18h A8h | 18h A8h |
| Interrupts | COMP_B | | 1 | A8h | A8h | A8h | A8h |
| | TB0.CCIFG0 | | 1 | 64h | 64h | 64h | 64h |
| | TB0.CCIFG1..6 | | 1 | 65h | 65h | 65h | 65h |
| | WDTIFG | | 1 | 40h | 40h | 40h | 40h |
| | USCI_A0 | | 1 | 90h | 90h | 90h | 90h |
| | USCI_B0 | | 1 | 91h | 91h | 91h | 91h |
| | ADC10_A | | 1 | D0h | D0h | D0h | D0h |
| | TA0.CCIFG0 | | 1 | 60h | 60h | 60h | 60h |
| | TA0.CCIFG1..4 | | 1 | 61h | 61h | 61h | 61h |
| | Reserved | | 1 | 01h | 01h | 01h | 01h |
| | DMA | | 1 | 46h | 46h | 46h | 46h |
| | TA1.CCIFG0 | | 1 | 62h | 62h | 62h | 62h |
| | TA1.CCIFG1..2 | | 1 | 63h | 63h | 63h | 63h |
| | P1 | | 1 | 50h | 50h | 50h | 50h |
| | USCI_A1 | | 1 | 92h | 92h | 92h | 92h |
| | USCI_B1 | | 1 | 93h | 93h | 93h | 93h |
| | TA1.CCIFG0 | | 1 | 66h | 66h | 66h | 66h |
| | TA1.CCIFG1..2 | | 1 | 67h | 67h | 67h | 67h |
| | P2 | | 1 | 51h | 51h | 51h | 51h |
| | RTC_A | | 1 | 68h | 68h | 68h | 68h |
| Delimiter | | 1 | 00h | 00h | 00h | 00h | |

Table 6-55. MSP430F521x Device Descriptor Table⁽¹⁾

| DESCRIPTION | ADDRESS | SIZE (BYTES) | VALUE | | | | |
|-------------------|---|--------------|-------|----------|----------|----------|----------|
| | | | F5219 | F5217 | F5214 | F5212 | |
| Info Block | Info length | 01A00h | 1 | 06h | 06h | 06h | 06h |
| | CRC length | 01A01h | 1 | 06h | 06h | 06h | 06h |
| | CRC value | 01A02h | 2 | Per unit | Per unit | Per unit | Per unit |
| | Device ID | 01A04h | 1 | 47h | 45h | 42h | 40h |
| | Device ID | 01A05h | 1 | 81h | 81h | 81h | 81h |
| | Hardware revision | 01A06h | 1 | Per unit | Per unit | Per unit | Per unit |
| | Firmware revision | 01A07h | 1 | Per unit | Per unit | Per unit | Per unit |
| Die Record | Die record tag | 01A08h | 1 | 08h | 08h | 08h | 08h |
| | Die record length | 01A09h | 1 | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot/wafer ID | 01A0Ah | 4 | Per unit | Per unit | Per unit | Per unit |
| | Die X position | 01A0Eh | 2 | Per unit | Per unit | Per unit | Per unit |
| | Die Y position | 01A10h | 2 | Per unit | Per unit | Per unit | Per unit |
| | Test results | 01A12h | 2 | Per unit | Per unit | Per unit | Per unit |
| ADC10 Calibration | ADC10 calibration tag | 01A14h | 1 | 13h | 13h | 13h | 13h |
| | ADC10 calibration length | 01A15h | 1 | 10h | 10h | 10h | 10h |
| | ADC gain factor | 01A16h | 2 | Blank | Blank | Blank | Blank |
| | ADC offset | 01A18h | 2 | Blank | Blank | Blank | Blank |
| | ADC 1.5-V reference Temperature sensor 30°C | 01A1Ah | 2 | Blank | Blank | Blank | Blank |
| | ADC 1.5-V Reference Temperature sensor 85°C | 01A1Ch | 2 | Blank | Blank | Blank | Blank |
| | ADC 2.0-V reference Temperature sensor 30°C | 01A1Eh | 2 | Blank | Blank | Blank | Blank |
| | ADC 2.0-V reference Temperature sensor 85°C | 01A20h | 2 | Blank | Blank | Blank | Blank |
| | ADC 2.5-V reference Temperature sensor 30°C | 01A22h | 2 | Blank | Blank | Blank | Blank |
| | ADC 2.5-V reference Temperature sensor 85°C | 01A24h | 2 | Blank | Blank | Blank | Blank |
| REF Calibration | REF calibration tag | 01A26h | 1 | 12h | 12h | 12h | 12h |
| | REF calibration length | 01A27h | 1 | 06h | 06h | 06h | 06h |
| | REF 1.5-V reference factor | 01A28h | 2 | Per unit | Per unit | Per unit | Per unit |
| | REF 2.0-V reference factor | 01A2Ah | 2 | Per unit | Per unit | Per unit | Per unit |
| | REF 2.5-V reference factor | 01A2Ch | 2 | Per unit | Per unit | Per unit | Per unit |

(1) NA = Not applicable, Blank = unused and reads FFh

Table 6-55. MSP430F521x Device Descriptor Table⁽¹⁾ (continued)

| DESCRIPTION | ADDRESS | SIZE (BYTES) | VALUE | | | |
|------------------------------|---------|-----------------|------------|------------|------------|------------|
| | | | F5219 | F5217 | F5214 | F5212 |
| Peripheral descriptor tag | 01A2Eh | 1 | 02h | 02h | 02h | 02h |
| Peripheral descriptor length | 01A2Fh | 1 | 5Dh | 5Dh | 5Bh | 5Bh |
| Memory 1 | | 2 | 08h 8Ah | 08h 8Ah | 08h 8Ah | 08h 8Ah |
| Memory 2 | | 2 | 0Ch 86h | 0Ch 86h | 0Ch 86h | 0Ch 86h |
| Memory 3 | | 2 | 12h 2Eh | 12h 2Eh | 12h 2Eh | 12h 2Eh |
| Memory 4 | | 2 | 22h 96h | 22h 94h | 22h 96h | 22h 94h |
| Memory 5 | | 2 | N/A | N/A | N/A | N/A |
| Memory 6 | | 1/2 | N/A | N/A | N/A | N/A |
| Delimiter | | 1 | 00h | 00h | 00h | 00h |
| Peripheral count | | 1 | 1Fh | 1Fh | 1Eh | 1Eh |
| MSP430CPUXV2 | | 2 | 00h 23h | 00h 23h | 00h 23h | 00h 23h |
| JTAG | | 2 | 00h 09h | 00h 09h | 00h 09h | 00h 09h |
| SBW | | 2 | 00h 0Fh | 00h 0Fh | 00h 0Fh | 00h 0Fh |
| EEM-S | | 2 | 00h 03h | 00h 03h | 00h 03h | 00h 05h |
| TI BSL | | 2 | 00h FCh | 00h FCh | 00h FCh | 00h FCh |
| SFR | | 2 | 10h 41h | 10h 41h | 10h 41h | 10h 41h |
| PMM | | 2 | 02h 30h | 02h 30h | 02h 30h | 02h 30h |
| FCTL | | 2 | 02h 38h | 02h 38h | 02h 38h | 02h 38h |
| CRC16 | | 2 | 01h 3Ch | 01h 3Ch | 01h 3Ch | 01h 3Ch |
| CRC16_RB | | 2 | 00h 3Dh | 00h 3Dh | 00h 3Dh | 00h 3Dh |
| RAMCTL | | 2 | 00h 44h | 00h 44h | 00h 44h | 00h 44h |
| WDT_A | | 2 | 00h 40h | 00h 40h | 00h 40h | 00h 40h |
| UCS | | 2 | 01h 48h | 01h 48h | 01h 48h | 01h 48h |
| SYS | | 2 | 02h 42h | 02h 42h | 02h 42h | 02h 42h |
| REF | | 2 | 03h A0h | 03h A0h | 03h A0h | 03h A0h |
| Port mapping | | 2 | 01h 10h | 01h 10h | 01h 10h | 01h 10h |
| Port 1/2 | | 2 | 04h 51h | 04h 51h | 04h 51h | 04h 51h |
| Port 3/4 | | 2 | 02h 52h | 02h 52h | 02h 52h | 02h 52h |
| Port 5/6 | | 2 | 02h 53h | 02h 53h | 02h 53h | 02h 53h |

Peripheral
Descriptor

Table 6-55. MSP430F521x Device Descriptor Table⁽¹⁾ (continued)

| DESCRIPTION | ADDRESS | SIZE (BYTES) | VALUE | | | |
|---|---------------|-----------------|------------|------------|------------|------------|
| | | | F5219 | F5217 | F5214 | F5212 |
| Peripheral Descriptor (continued) | Port 7/8 | 2 | 02h 54h | 02h 54h | N/A | N/A |
| | JTAG | 2 | 0Ch 5Fh | 0Ch 5Fh | 0Eh 5Fh | 0Eh 5Fh |
| | TA0 | 2 | 02h 62h | 02h 62h | 02h 62h | 02h 62h |
| | TA1 | 2 | 04h 61h | 04h 61h | 04h 61h | 04h 61h |
| | TB0 | 2 | 04h 67h | 04h 67h | 04h 67h | 04h 67h |
| | TA2 | 2 | 04h 61h | 04h 61h | 04h 61h | 04h 61h |
| | RTC | 2 | 0Ah 68h | 0Ah 68h | 0Ah 68h | 0Ah 68h |
| | MPY32 | 2 | 02h 85h | 02h 85h | 02h 85h | 02h 85h |
| | DMA-3 | 2 | 04h 47h | 04h 47h | 04h 47h | 04h 47h |
| | USCI_A/B | 2 | 0Ch 90h | 0Ch 90h | 0Ch 90h | 0Ch 90h |
| | USCI_A/B | 2 | 04h 90h | 04h 90h | 04h 90h | 04h 90h |
| | ADC10_A | 2 | N/A | N/A | N/A | N/A |
| | COMP_B | 2 | 2Ch A8h | 2Ch A8h | 2Ch A8h | 2Ch A8h |
| Interrupts | COMP_B | 1 | A8h | A8h | A8h | A8h |
| | TB0.CCIFG0 | 1 | 64h | 64h | 64h | 64h |
| | TB0.CCIFG1..6 | 1 | 65h | 65h | 65h | 65h |
| | WDTIFG | 1 | 40h | 40h | 40h | 40h |
| | USCI_A0 | 1 | 90h | 90h | 90h | 90h |
| | USCI_B0 | 1 | 91h | 91h | 91h | 91h |
| | Reserved | 1 | 01h | 01h | 01h | 01h |
| | TA0.CCIFG0 | 1 | 60h | 60h | 60h | 60h |
| | TA0.CCIFG1..4 | 1 | 61h | 61h | 61h | 61h |
| | Reserved | 1 | 01h | 01h | 01h | 01h |
| | DMA | 1 | 46h | 46h | 46h | 46h |
| | TA1.CCIFG0 | 1 | 62h | 62h | 62h | 62h |
| | TA1.CCIFG1..2 | 1 | 63h | 63h | 63h | 63h |
| | P1 | 1 | 50h | 50h | 50h | 50h |
| | USCI_A1 | 1 | 92h | 92h | 92h | 92h |
| | USCI_B1 | 1 | 93h | 93h | 93h | 93h |
| | TA2.CCIFG0 | 1 | 66h | 66h | 66h | 66h |
| | TA2.CCIFG1..2 | 1 | 67h | 67h | 67h | 67h |
| P2 | 1 | 51h | 51h | 51h | 51h | |
| RTC_A | 1 | 68h | 68h | 68h | 68h | |
| Delimiter | 1 | 00h | 00h | 00h | 00h | |

7 Device and Documentation Support

7.1 Getting Started

For more information on the MSP430 family of devices and the tools and libraries that are available to help with your development, visit the [MSP430 ultra-low-power sensing and measurement MCUs overview](#).

7.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. [Figure 7-1](#) provides a legend for reading the complete device name.



Figure 7-1. Device Nomenclature

7.3 Tools and Software

All MSP microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at [MSP430 Ultra-Low-Power MCUs – Tools & software](#).

Table 7-1 lists the debug features of the MSP430F522x and MSP430F521x MCUs. See the [Code Composer Studio for MSP430 User's Guide](#) for details on the available features.

Table 7-1. Hardware Debug Features

| MSP430 ARCHITECTURE | 4-WIRE JTAG | 2-WIRE JTAG | BREAK-POINTS (N) | RANGE BREAK-POINTS | CLOCK CONTROL | STATE SEQUENCER | TRACE BUFFER | LPMx.5 DEBUGGING SUPPORT | EnergyTrace++ Technology |
|---------------------|-------------|-------------|------------------|--------------------|---------------|-----------------|--------------|--------------------------|--------------------------|
| MSP430Xv2 | Yes | Yes | 3 | Yes | Yes | No | No | Yes | Yes |

Design Kits and Evaluation Modules

MSP-TS430RGC64C - 64-pin Target Development Board for MSP430F5x MCUs The MSP-TS430RGC64C is a stand-alone 64-pin ZIF socket target board used to program and debug the MSP430 MCU in system through the JTAG interface or the Spy-Bi-Wire (2-wire JTAG) protocol.

Bluetooth® and MSP430 Audio Source Reference Design Board The Bluetooth and MSP430 Audio Source reference design can be used by customers to create a variety of applications for low-end, low-power audio source solutions for applications including toys, projectors, smart remotes and any audio streaming accessories.

Dual-Mode Bluetooth CC2564 Module With Integrated Antenna Evaluation Board The CC2564MODAEM evaluation board contains the Bluetooth BR/EDR/LE HCI solution. Based on TI's CC2564B dual-mode Bluetooth single-chip device, the bCC2564MODA is intended for evaluation and design purposes, reducing design effort and enabling fast time to market.

Software

MSP430Ware™ Software MSP430Ware software is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 MCU design resources, MSP430Ware software also includes a high-level API called MSP Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware software is available as a component of CCS or as a stand-alone package.

MSP430F522x, MSP430F521x Code Examples C code examples that configure each of the integrated peripherals for various application needs.

MSP Driver Library The abstracted API of MSP Driver Library provides easy-to-use function calls that free you from directly manipulating the bits and bytes of the MSP430 hardware. Thorough documentation is delivered through a helpful API Guide, which includes details on each function call and the recognized parameters. Developers can use Driver Library functions to write complete projects with minimal overhead.

MSP EnergyTrace™ Technology EnergyTrace technology for MSP430 microcontrollers is an energy-based code analysis tool that measures and displays the energy profile of the application and helps to optimize it for ultra-low-power consumption.

ULP (Ultra-Low Power) Advisor ULP Advisor™ software is a tool for guiding developers to write more efficient code to fully use the unique ultra-low-power features of MSP and MSP432 microcontrollers. Aimed at both experienced and new microcontroller developers, ULP Advisor checks your code against a thorough ULP checklist to help minimize the energy consumption of your application. At build time, ULP Advisor provides notifications and remarks to highlight areas of your code that can be further optimized for lower power.

IEC60730 Software Package The IEC60730 MSP430 software package was developed to help customers comply with IEC 60730-1:2010 (Automatic Electrical Controls for Household and Similar Use – Part 1: General Requirements) for up to Class B products, which includes home appliances, arc detectors, power converters, power tools, e-bikes, and many others. The IEC60730 MSP430 software package can be embedded in customer applications running on MSP430s to help simplify the customer's certification efforts of functional safety-compliant consumer devices to IEC 60730-1:2010 Class B.

Fixed Point Math Library for MSP The MSP IQmath and Qmath Libraries are a collection of highly optimized and high-precision mathematical functions for C programmers to seamlessly port a floating-point algorithm into fixed-point code on MSP430 and MSP432 devices. These routines are typically used in computationally intensive real-time applications where optimal execution speed, high accuracy, and ultra-low energy are critical. By using the IQmath and Qmath libraries, it is possible to achieve execution speeds considerably faster and energy consumption considerably lower than equivalent code written using floating-point math.

Floating Point Math Library for MSP430 Continuing to innovate in the low-power and low-cost microcontroller space, TI provides MSPMATHLIB. Leveraging the intelligent peripherals of our devices, this floating-point math library of scalar functions that are up to 26 times faster than the standard MSP430 math functions. Mathlib is easy to integrate into your designs. This library is free and is integrated in both Code Composer Studio IDE and IAR Embedded Workbench IDE.

Development Tools

Code Composer Studio™ Integrated Development Environment for MSP Microcontrollers Code Composer Studio (CCS) integrated development environment (IDE) supports all MSP microcontroller devices. CCS comprises a suite of embedded software utilities used to develop and debug embedded applications. CCS includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features.

Command-Line Programmer MSP Flasher is an open-source shell-based interface for programming MSP microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP Flasher can download binary files (.txt or .hex) directly to the MSP microcontroller without an IDE.

MSP MCU Programmer and Debugger The MSP-FET is a powerful emulation development tool – often called a debug probe – which lets users quickly begin application development on MSP low-power MCUs. Creating MCU software usually requires downloading the resulting binary program to the MSP device for validation and debugging.

MSP-GANG Production Programmer The MSP Gang Programmer is an MSP430 or MSP432 device programmer that can program up to eight identical MSP430 or MSP432 flash or FRAM devices at the same time. The MSP Gang Programmer connects to a host PC using a standard RS-232 or USB connection and provides flexible programming options that let the user fully customize the process.

7.4 Documentation Support

The following documents describe the MSP430F522x and MSP430F521x MCUs. Copies of these documents are available on the Internet at www.ti.com.

Receiving Notification of Document Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (see [Section 7.5](#) for links to product folders). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

Errata

MSP430F5229 Device Erratasheet Describes the known exceptions to the functional specifications for the MSP430F5229 device.

MSP430F5227 Device Erratasheet Describes the known exceptions to the functional specifications for the MSP430F5227 device.

MSP430F5224 Device Erratasheet Describes the known exceptions to the functional specifications for the MSP430F5224 device.

MSP430F5222 Device Erratasheet Describes the known exceptions to the functional specifications for the MSP430F5222 device.

MSP430F5219 Device Erratasheet Describes the known exceptions to the functional specifications for the MSP430F5219 device.

MSP430F5217 Device Erratasheet Describes the known exceptions to the functional specifications for the MSP430F5217 device.

MSP430F5214 Device Erratasheet Describes the known exceptions to the functional specifications for the MSP430F5214 device.

MSP430F5212 Device Erratasheet Describes the known exceptions to the functional specifications for the MSP430F5212 device.

User's Guides

MSP430F5xx and MSP430F6xx Family User's Guide Detailed information on the modules and peripherals available in this device family.

MSP430 Flash Device Bootloader (BSL) User's Guide The MSP430 bootloader (BSL) (formerly known as the bootstrap loader) lets users communicate with embedded memory in the MSP430 microcontroller during the prototyping phase, final production, and in service. Both the programmable memory (flash memory) and the data memory (RAM) can be modified as required. Do not confuse the bootloader with the bootstrap loader programs found in some digital signal processors (DSPs) that automatically load program code (and data) from external memory to the internal memory of the DSP.

MSP430 Programming With the JTAG Interface This document describes the functions that are required to erase, program, and verify the memory module of the MSP430 flash-based and FRAM-based microcontroller families using the JTAG communication port. In addition, it describes how to program the JTAG access security fuse that is available on all MSP430 devices. This document describes device access using both the standard 4-wire JTAG interface and the 2-wire JTAG interface, which is also referred to as Spy-Bi-Wire (SBW).

MSP430 Hardware Tools User's Guide This manual describes the hardware of the TI MSP-FET430 Flash Emulation Tool (FET). The FET is the program development tool for the MSP430 ultra-low-power microcontroller.

Application Reports

Designing with MSP430F522x and MSP430F521x Devices The MSP430F522x and MSP430F521x devices support a split supply I/O system that is essential in systems in which the MCU is required to interface with external devices (such as sensors or other processors) that operate at different voltage level compared to the MCU device supply. Additionally, the split supply input voltage range of the F522x and F521x devices starts as low as 1.62 V (see the device data sheet specifications), and this allows for nominal 1.8-V I/O interface without the need for external level translation. This application report describes the various design considerations to keep in mind while designing the F522x and F521x devices in an application.

General Oversampling of MSP ADCs for Higher Resolution Multiple MSP ultra-low-power microcontrollers offer analog-to-digital converters (ADCs) to convert physical quantities into digital numbers, a function that is widely used across numerous applications. There are times, however, when a customer design demands a higher resolution than the ADC of the selected MSP can offer. This application report, which is based on the previously-published Oversampling the ADC12 for Higher Resolution (SLAA323), therefore describes how an oversampling method can be incorporated to increase ADC resolution past the currently available number of bits.

MSP430 32-kHz Crystal Oscillators Selection of the correct crystal, correct load circuit, and proper board layout are important for a stable crystal oscillator. This application report summarizes crystal oscillator function and explains the parameters to select the correct crystal for MSP430 ultra-low-power operation. In addition, hints and examples for correct board layout are given. The document also contains detailed information on the possible oscillator tests to ensure stable oscillator operation in mass production.

MSP430 System-Level ESD Considerations System-Level ESD has become increasingly demanding as silicon technology scales to lower voltages and the need for designing cost-effective and ultra-low-power components. This application report addresses three ESD topics to help board designers and OEMs understand and design robust system-level designs: (1) Component-level ESD testing and system-level ESD testing; (2) General design guidelines for system-level ESD protection; (3) Introduction to System Efficient ESD Design (SEED), a co-design methodology of on-board and on-chip ESD protection. A few real-world system-level ESD protection design examples and their results are discussed.

7.5 Related Links

Table 7-2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7-2. Related Links

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|-------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| MSP430F5229 | Click here | Click here | Click here | Click here | Click here |
| MSP430F5227 | Click here | Click here | Click here | Click here | Click here |
| MSP430F5224 | Click here | Click here | Click here | Click here | Click here |
| MSP430F5222 | Click here | Click here | Click here | Click here | Click here |
| MSP430F5219 | Click here | Click here | Click here | Click here | Click here |
| MSP430F5217 | Click here | Click here | Click here | Click here | Click here |
| MSP430F5214 | Click here | Click here | Click here | Click here | Click here |
| MSP430F5212 | Click here | Click here | Click here | Click here | Click here |

7.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

[TI E2E™ Community](#)

TI's *Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

[TI Embedded Processors Wiki](#)

Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.7 Trademarks

MSP430, MSP430Ware, EnergyTrace, ULP Advisor, Code Composer Studio, E2E are trademarks of Texas Instruments.

Bluetooth is a registered trademark of Bluetooth SIG.

All other trademarks are the property of their respective owners.

7.8 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.9 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|----------------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430F5212IRGZT | ACTIVE | VQFN | RGZ | 48 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F5212 | Samples |
| MSP430F5214IRGZR | ACTIVE | VQFN | RGZ | 48 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F5214 | Samples |
| MSP430F5217IRGCT | ACTIVE | VQFN | RGC | 64 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F5217 | Samples |
| MSP430F52171YFFR | ACTIVE | DSBGA | YFF | 64 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | M430F5217 | Samples |
| MSP430F52191YFFT | ACTIVE | DSBGA | YFF | 64 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | M430F5219 | Samples |
| MSP430F5219IZQE | LIFEBUY | BGA MICROSTAR JUNIOR | ZQE | 80 | 490 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 85 | F5219 | |
| MSP430F5222IRGZR | ACTIVE | VQFN | RGZ | 48 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F5222 | Samples |
| MSP430F5222IRGZT | ACTIVE | VQFN | RGZ | 48 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F5222 | Samples |
| MSP430F5224IRGZR | ACTIVE | VQFN | RGZ | 48 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F5224 | Samples |
| MSP430F5227IZQE | LIFEBUY | BGA MICROSTAR JUNIOR | ZQE | 80 | 490 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 85 | F5227 | |
| MSP430F5229IRGCR | ACTIVE | VQFN | RGC | 64 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F5229 | Samples |
| MSP430F5229IRGCT | ACTIVE | VQFN | RGC | 64 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F5229 | Samples |
| MSP430F52291YFFR | ACTIVE | DSBGA | YFF | 64 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | M430F5229 | Samples |
| MSP430F52291YFFT | ACTIVE | DSBGA | YFF | 64 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | M430F5229 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430F5212IRGZT | VQFN | RGZ | 48 | 250 | 180.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430F5214IRGZR | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430F5217IRGCT | VQFN | RGC | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430F5217IYFFR | DSBGA | YFF | 64 | 2500 | 330.0 | 12.4 | 3.54 | 3.66 | 0.81 | 8.0 | 12.0 | Q2 |
| MSP430F5219IYFFT | DSBGA | YFF | 64 | 250 | 180.0 | 12.4 | 3.54 | 3.66 | 0.81 | 8.0 | 12.0 | Q2 |
| MSP430F5222IRGZR | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430F5222IRGZT | VQFN | RGZ | 48 | 250 | 180.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430F5224IRGZR | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430F5229IRGCR | VQFN | RGC | 64 | 2000 | 330.0 | 16.4 | 9.3 | 9.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430F5229IRGCT | VQFN | RGC | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430F5229IYFFR | DSBGA | YFF | 64 | 2500 | 330.0 | 12.4 | 3.54 | 3.66 | 0.81 | 8.0 | 12.0 | Q2 |
| MSP430F5229IYFFT | DSBGA | YFF | 64 | 250 | 180.0 | 12.4 | 3.54 | 3.66 | 0.81 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430F5212IRGZT | VQFN | RGZ | 48 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F5214IRGZR | VQFN | RGZ | 48 | 2500 | 367.0 | 367.0 | 38.0 |
| MSP430F5217IRGCT | VQFN | RGC | 64 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F5217IYFFR | DSBGA | YFF | 64 | 2500 | 335.0 | 335.0 | 25.0 |
| MSP430F5219IYFFT | DSBGA | YFF | 64 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F5222IRGZR | VQFN | RGZ | 48 | 2500 | 367.0 | 367.0 | 38.0 |
| MSP430F5222IRGZT | VQFN | RGZ | 48 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F5224IRGZR | VQFN | RGZ | 48 | 2500 | 367.0 | 367.0 | 38.0 |
| MSP430F5229IRGCR | VQFN | RGC | 64 | 2000 | 367.0 | 367.0 | 38.0 |
| MSP430F5229IRGCT | VQFN | RGC | 64 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F5229IYFFR | DSBGA | YFF | 64 | 2500 | 335.0 | 335.0 | 25.0 |
| MSP430F5229IYFFT | DSBGA | YFF | 64 | 250 | 182.0 | 182.0 | 20.0 |

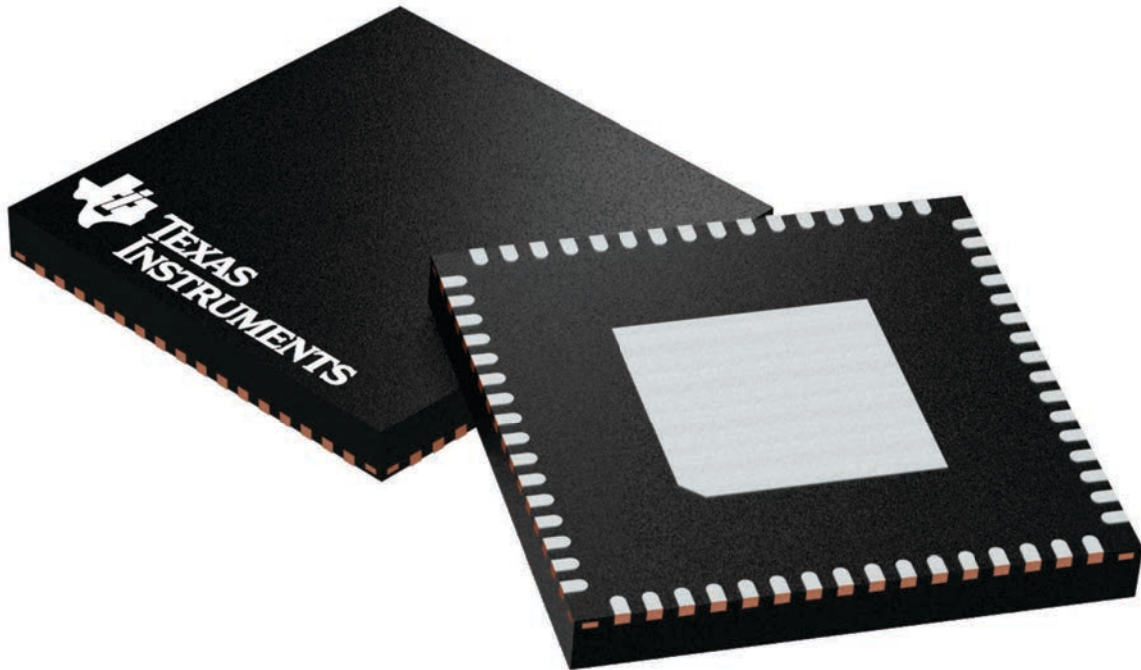
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

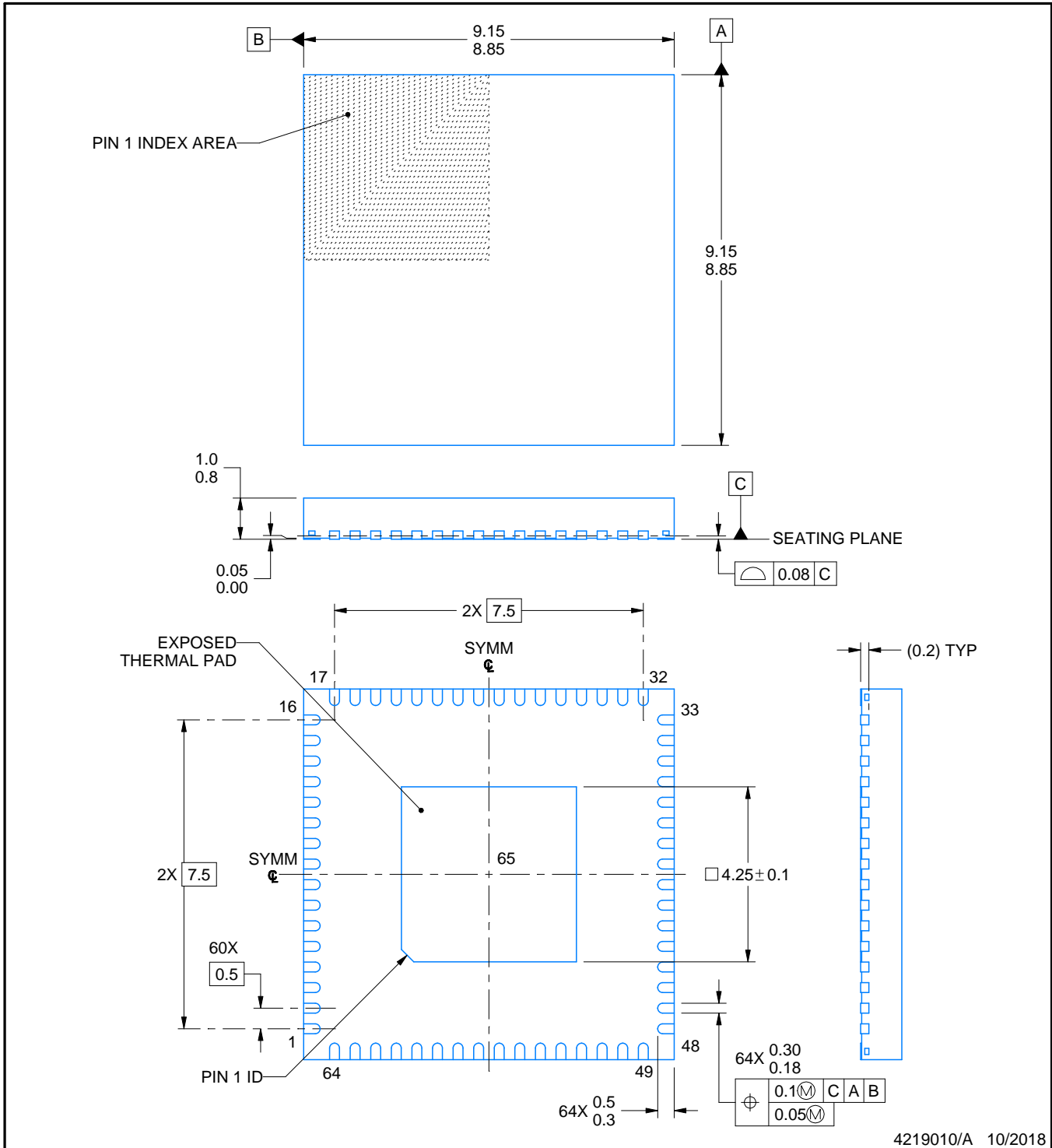
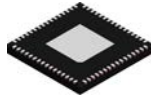
9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224597/A



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RGC0064B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219010/A 10/2018

NOTES: (continued)

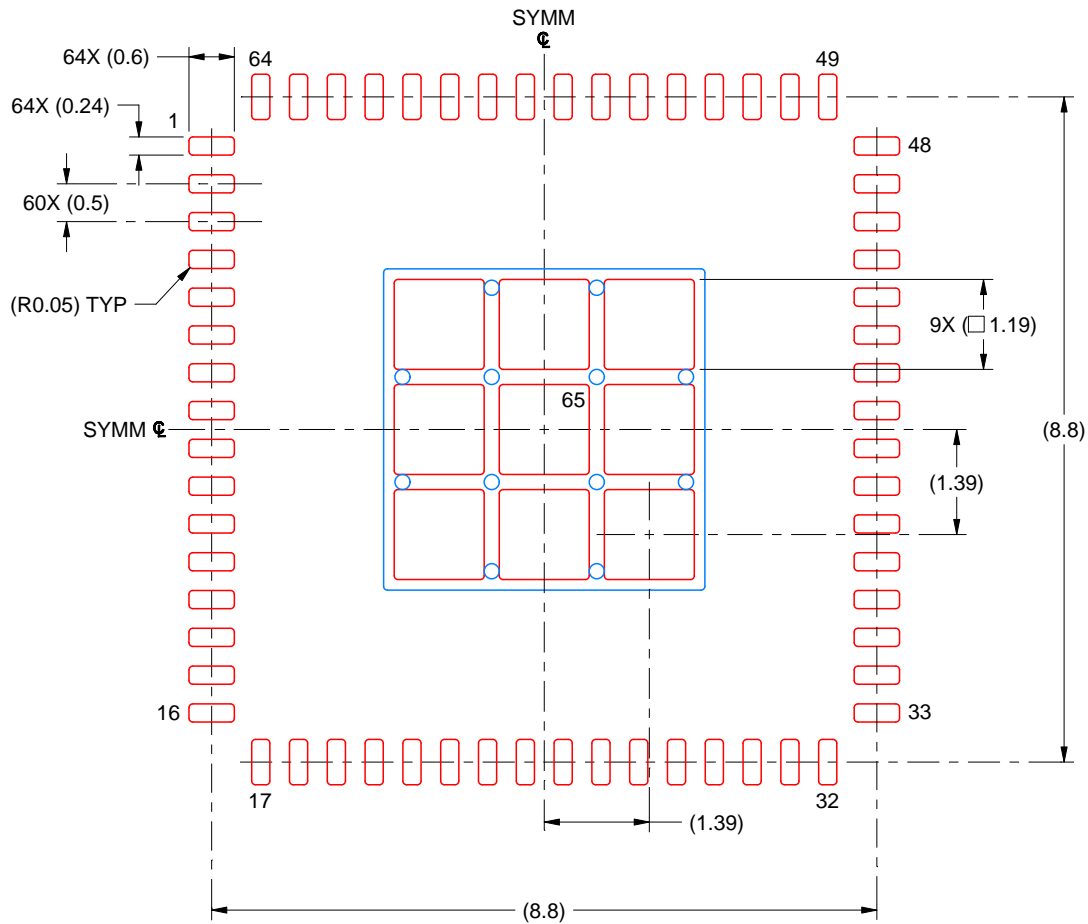
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGC0064B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 MM THICK STENCIL
 SCALE: 10X

EXPOSED PAD 65
 71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219010/A 10/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

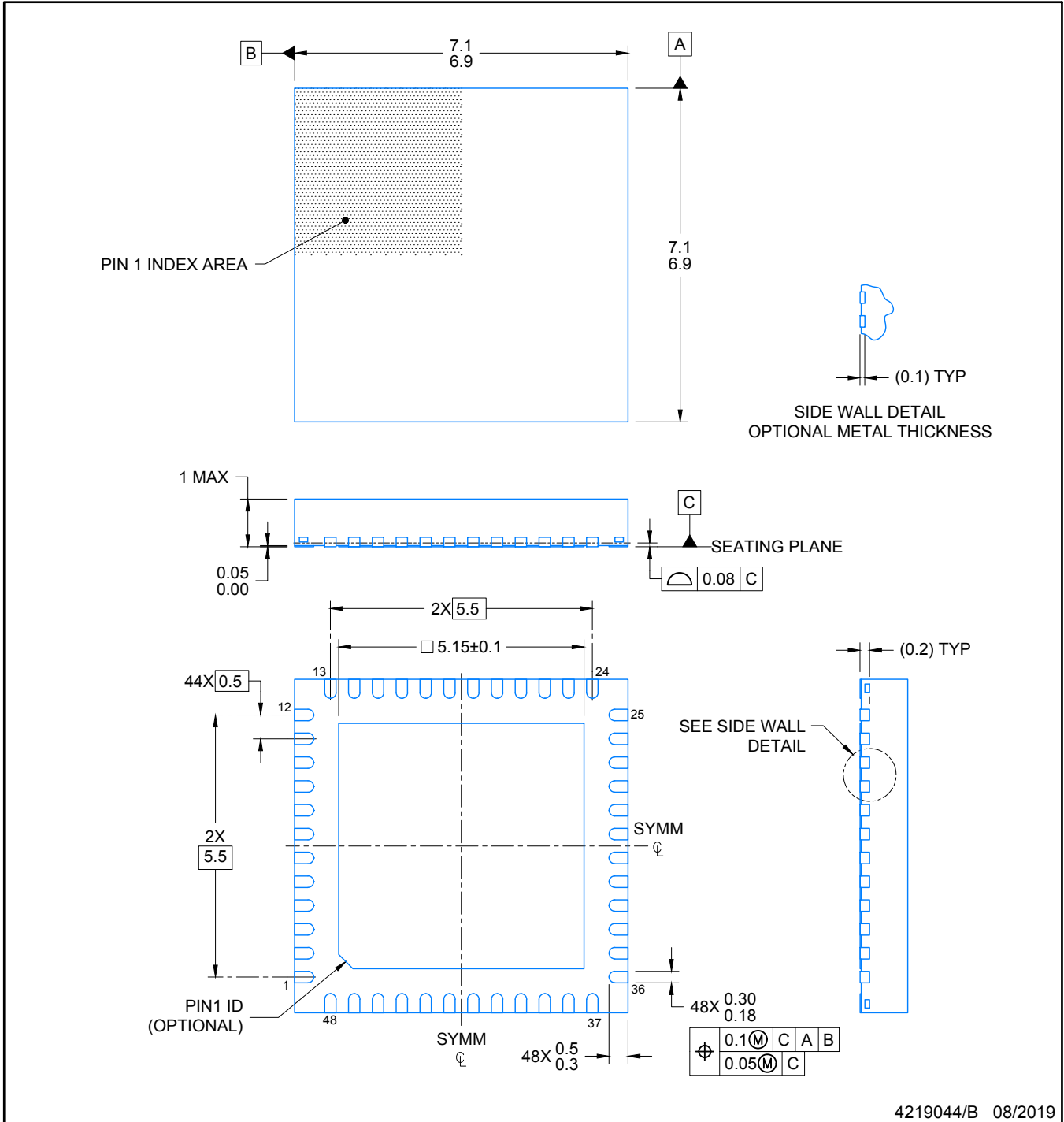
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



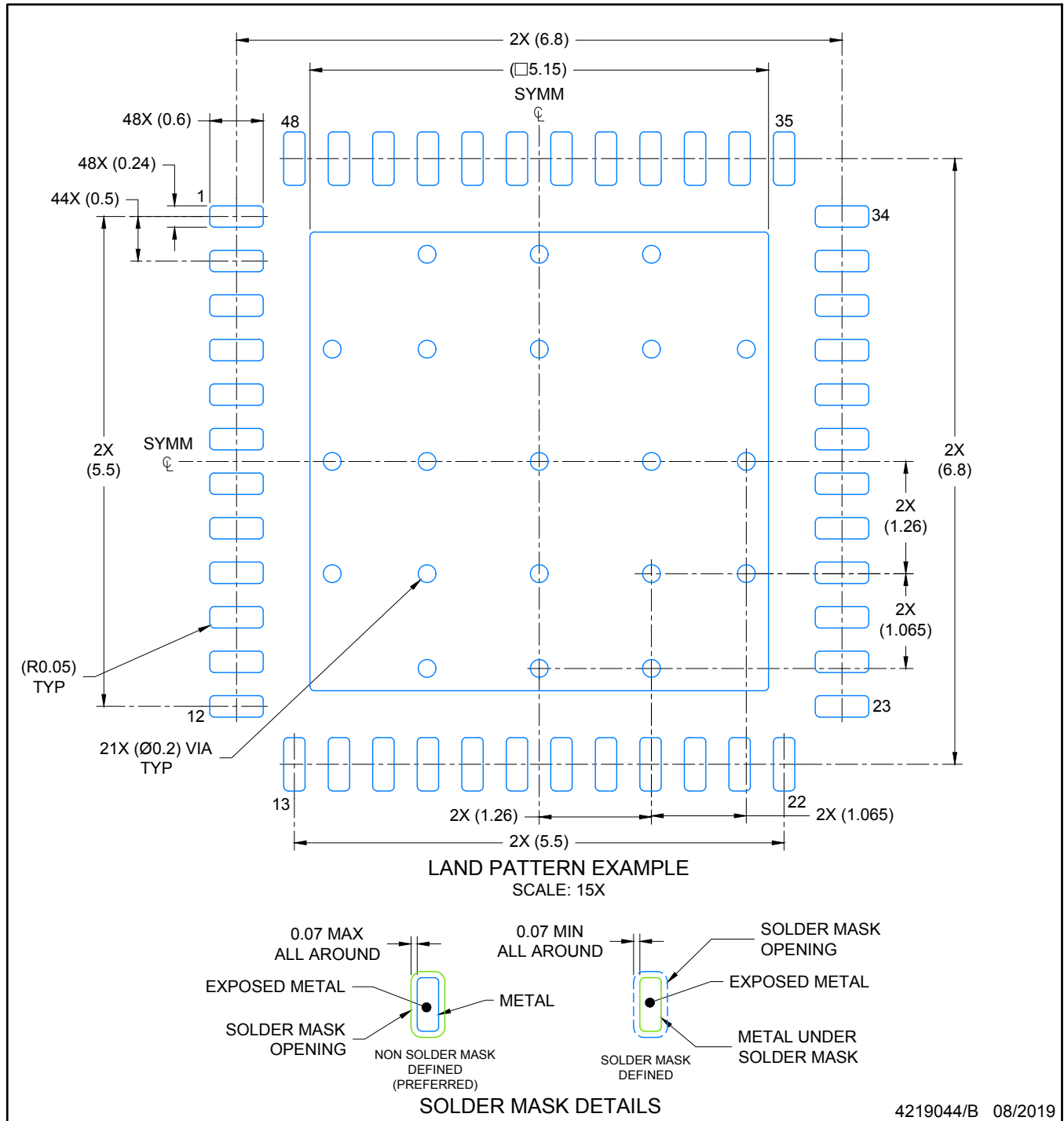
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

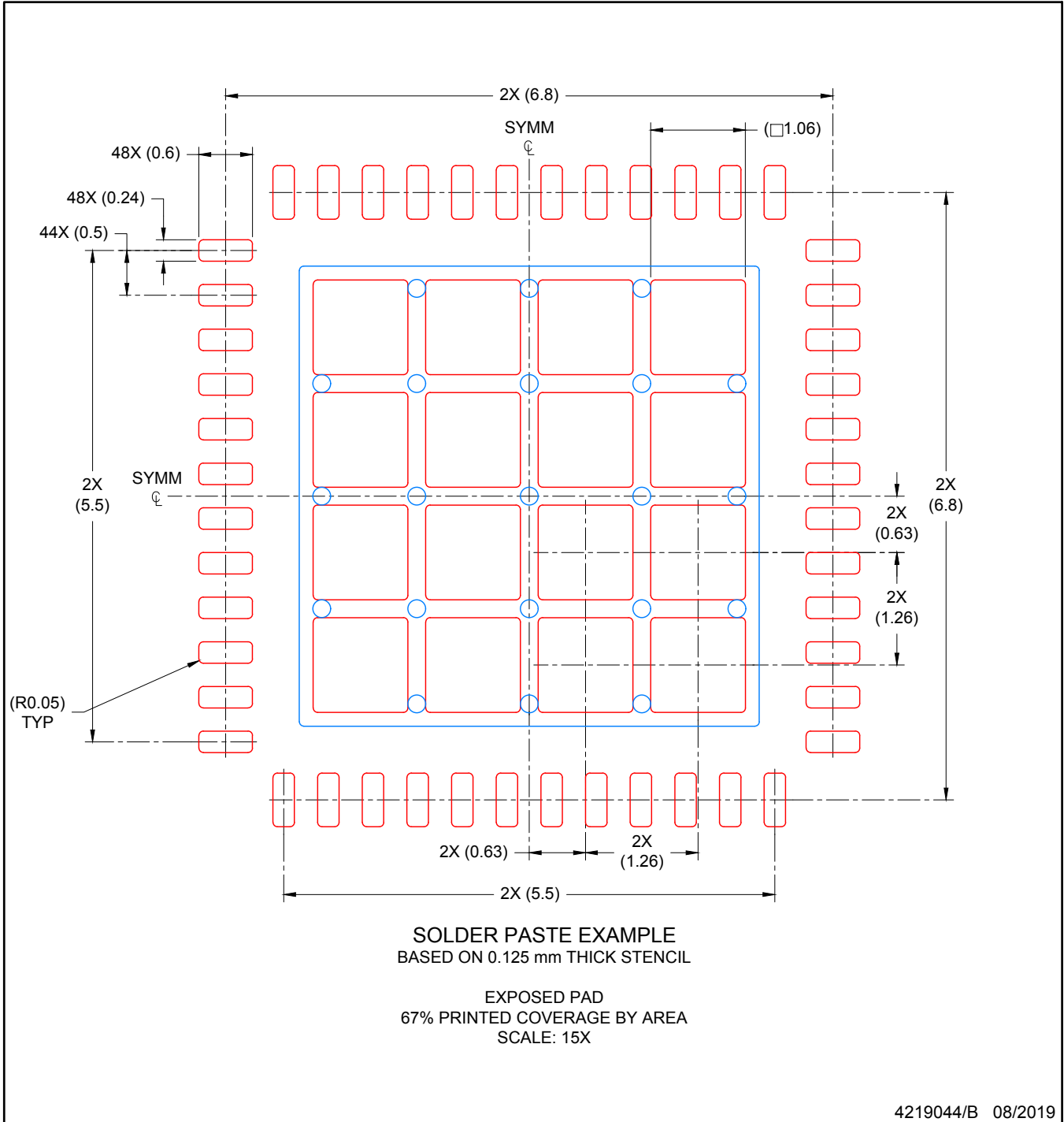
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGZ0048A

VQFN - 1 mm max height

PLASTIC QUADFLAT PACK- NO LEAD



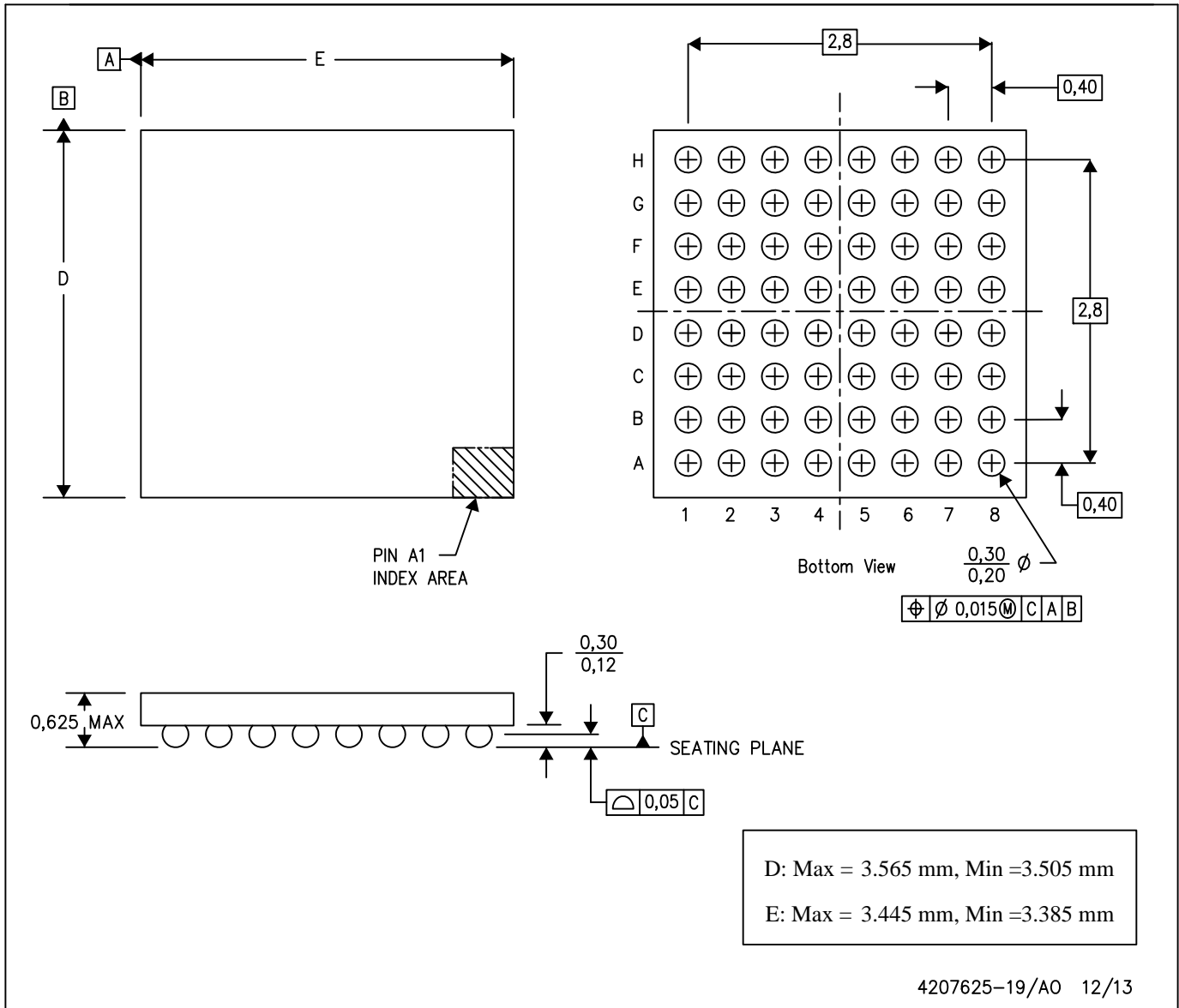
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

YFF (R-XBGA-N64)

DIE-SIZE BALL GRID ARRAY



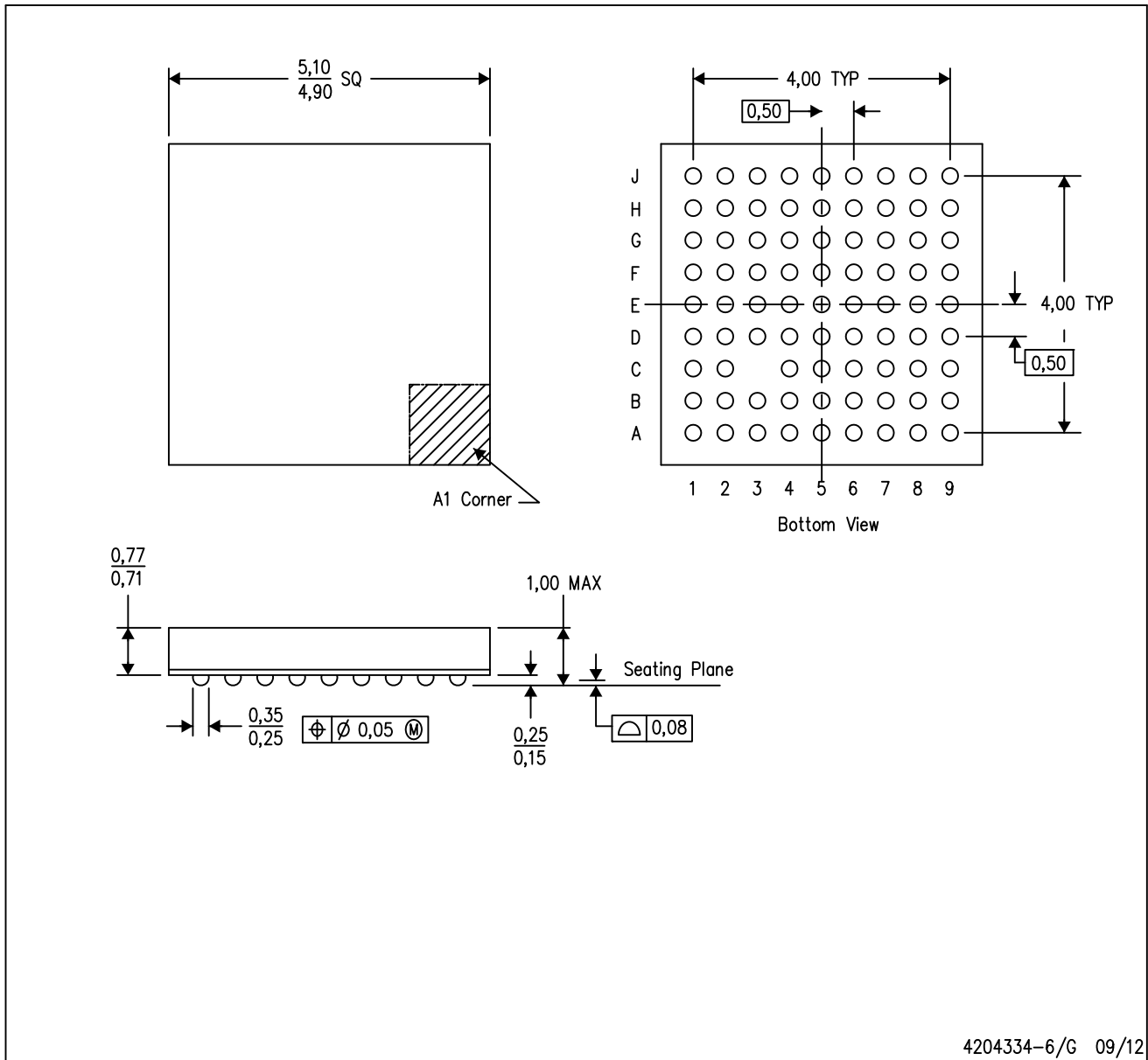
- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 B. This drawing is subject to change without notice.
 C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

MECHANICAL DATA

ZQE (S-PBGA-N80)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225
 - D. This is a Pb-free solder ball design.

MicroStar Junior is a trademark of Texas Instruments.

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