

## N-channel 600 V, 0.168 $\Omega$ typ., 18 A MDmesh™ M2 Power MOSFET in a TO-220FP ultra narrow leads package

Datasheet - production data

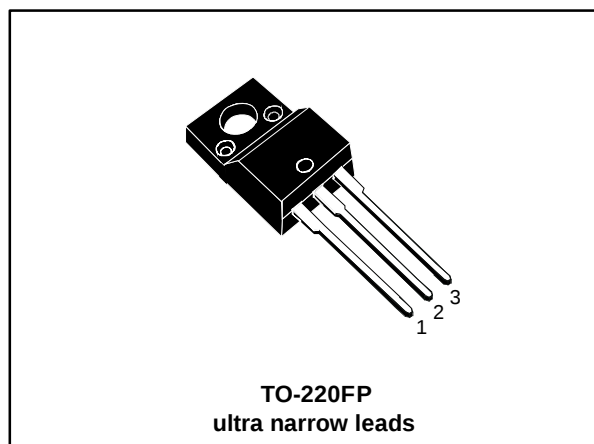
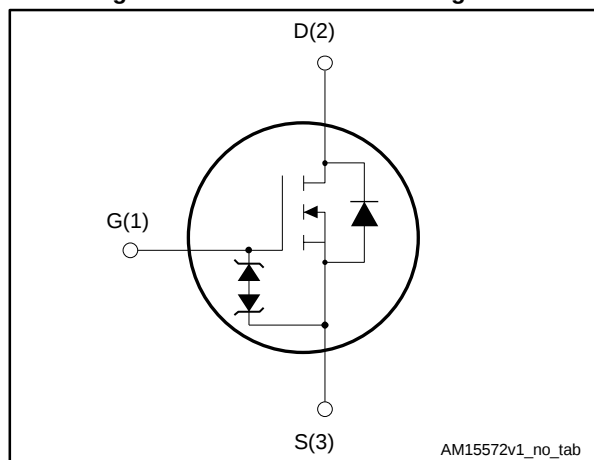


Figure 1: Internal schematic diagram



### Features

| Order code  | V <sub>DS</sub> | R <sub>DS(on)</sub> max | I <sub>D</sub> |
|-------------|-----------------|-------------------------|----------------|
| STFU24N60M2 | 600 V           | 0.19 $\Omega$           | 18 A           |

- Extremely low gate charge
- Lower R<sub>DS(on)</sub> x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications
- LLC converters, resonant converters

### Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

| Order code  | Marking | Package                     | Packing |
|-------------|---------|-----------------------------|---------|
| STFU24N60M2 | 24N60M2 | TO-220FP ultra narrow leads | Tube    |

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## Contents

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol                  | Parameter                                                                                                                               | Value             | Unit               |
|-------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|-------------------|--------------------|
| $V_{GS}$                | Gate-source voltage                                                                                                                     | $\pm 25$          | V                  |
| $I_D$                   | Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$                                                                        | 18 <sup>(1)</sup> | A                  |
| $I_D$                   | Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$                                                                       | 12 <sup>(1)</sup> | A                  |
| $I_{DM}$ <sup>(2)</sup> | Drain current (pulsed)                                                                                                                  | 72 <sup>(1)</sup> | A                  |
| $P_{TOT}$               | Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$                                                                                 | 30                | W                  |
| $V_{ISO}$               | Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t = 1\text{ s}$ ; $T_C = 25\text{ }^{\circ}\text{C}$ ) | 2500              | V                  |
| $dv/dt$ <sup>(3)</sup>  | Peak diode recovery voltage slope                                                                                                       | 15                | V/ns               |
| $dv/dt$ <sup>(4)</sup>  | MOSFET $dv/dt$ ruggedness                                                                                                               | 50                |                    |
| $T_{stg}$               | Storage temperature                                                                                                                     | - 55 to 150       | $^{\circ}\text{C}$ |
| $T_j$                   | Max. operating junction temperature                                                                                                     |                   |                    |

**Notes:**<sup>(1)</sup>Limited by maximum junction temperature.<sup>(2)</sup>Pulse width limited by safe operating area.<sup>(3)</sup> $I_{SD} \leq 18\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DSpeak} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .<sup>(4)</sup> $V_{DS} \leq 480\text{ V}$ .

Table 3: Thermal data

| Symbol         | Parameter                               | Value | Unit                        |
|----------------|-----------------------------------------|-------|-----------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case max    | 4.2   | $^{\circ}\text{C}/\text{W}$ |
| $R_{thj-amb}$  | Thermal resistance junction-ambient max | 62.5  |                             |

Table 4: Avalanche characteristics

| Symbol   | Parameter                                                                                                      | Value | Unit |
|----------|----------------------------------------------------------------------------------------------------------------|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )                           | 3.5   | A    |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_j = 25^{\circ}\text{C}$ , $I_D = I_{AR}$ ; $V_{DD} = 50\text{ V}$ ) | 180   | mJ   |

## 2 Electrical characteristics

(T<sub>C</sub> = 25 °C unless otherwise specified)

**Table 5: On /off states**

| Symbol               | Parameter                                             | Test conditions                                             | Min. | Typ.  | Max. | Unit |
|----------------------|-------------------------------------------------------|-------------------------------------------------------------|------|-------|------|------|
| V <sub>(BR)DSS</sub> | Drain-source breakdown voltage                        | I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0 V                | 600  |       |      | V    |
| I <sub>DSS</sub>     | Zero gate voltage drain current (V <sub>GS</sub> = 0) | V <sub>DS</sub> = 600 V                                     |      |       | 1    | μA   |
|                      |                                                       | V <sub>DS</sub> = 600 V, T <sub>C</sub> = 125 °C            |      |       | 100  | μA   |
| I <sub>GSS</sub>     | Gate-body leakage current (V <sub>DS</sub> = 0)       | V <sub>GS</sub> = ± 25 V                                    |      |       | ±10  | μA   |
| V <sub>GS(th)</sub>  | Gate threshold voltage                                | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA | 2    | 3     | 4    | V    |
| R <sub>DS(on)</sub>  | Static drain-source on-resistance                     | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 9 A                |      | 0.168 | 0.19 | Ω    |

**Table 6: Dynamic**

| Symbol                   | Parameter                     | Test conditions                                                                                                                                      | Min. | Typ. | Max. | Unit |
|--------------------------|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| C <sub>iss</sub>         | Input capacitance             | V <sub>DS</sub> = 100 V, f = 1 MHz,<br>V <sub>GS</sub> = 0 V                                                                                         | -    | 1060 | -    | pF   |
| C <sub>oss</sub>         | Output capacitance            |                                                                                                                                                      | -    | 55   | -    | pF   |
| C <sub>rss</sub>         | Reverse transfer capacitance  |                                                                                                                                                      | -    | 2.2  | -    | pF   |
| C <sub>oss eq. (1)</sub> | Equivalent output capacitance | V <sub>DS</sub> = 0 to 480 V, V <sub>GS</sub> = 0 V                                                                                                  | -    | 258  | -    | pF   |
| R <sub>G</sub>           | Intrinsic gate resistance     | f = 1 MHz, I <sub>D</sub> = 0                                                                                                                        | -    | 7    | -    | Ω    |
| Q <sub>g</sub>           | Total gate charge             | V <sub>DD</sub> = 480 V, I <sub>D</sub> = 18 A,<br>V <sub>GS</sub> = 10 V ( see <a href="#">Figure 15: "Test circuit for gate charge behavior"</a> ) | -    | 29   | -    | nC   |
| Q <sub>gs</sub>          | Gate-source charge            |                                                                                                                                                      | -    | 6    | -    | nC   |
| Q <sub>gd</sub>          | Gate-drain charge             |                                                                                                                                                      | -    | 12   | -    | nC   |

**Notes:**

(1)C<sub>oss eq.</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>.

**Table 7: Switching times**

| Symbol              | Parameter           | Test conditions                                                                                                                                                                                                                                | Min. | Typ. | Max. | Unit |
|---------------------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| t <sub>d(on)</sub>  | Turn-on delay time  | V <sub>DD</sub> = 300 V, I <sub>D</sub> = 9 A,<br>R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V ( see <a href="#">Figure 14: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 19: "Switching time waveform"</a> ) | -    | 14   | -    | ns   |
| t <sub>r</sub>      | Rise time           |                                                                                                                                                                                                                                                | -    | 9    | -    | ns   |
| t <sub>d(off)</sub> | Turn-off delay time |                                                                                                                                                                                                                                                | -    | 60   | -    | ns   |
| t <sub>f</sub>      | Fall time           |                                                                                                                                                                                                                                                | -    | 15   | -    | ns   |

Table 8: Source drain diode

| Symbol             | Parameter                     | Test conditions                                                                                                                                                                                                                      | Min. | Typ. | Max. | Unit          |
|--------------------|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{SD}^{(1)}$     | Source-drain current          |                                                                                                                                                                                                                                      | -    |      | 18   | A             |
| $I_{SDM}^{(1)(2)}$ | Source-drain current (pulsed) |                                                                                                                                                                                                                                      | -    |      | 72   | A             |
| $V_{SD}^{(3)}$     | Forward on voltage            | $I_{SD} = 18\text{ A}$ , $V_{GS} = 0\text{ V}$                                                                                                                                                                                       | -    |      | 1.6  | V             |
| $t_{rr}$           | Reverse recovery time         | $I_{SD} = 18\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60\text{ V}$ ( see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> )                                      | -    | 332  |      | ns            |
| $Q_{rr}$           | Reverse recovery charge       |                                                                                                                                                                                                                                      | -    | 4    |      | $\mu\text{C}$ |
| $I_{RRM}$          | Reverse recovery current      |                                                                                                                                                                                                                                      | -    | 24   |      | A             |
| $t_{rr}$           | Reverse recovery time         | $I_{SD} = 18\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ , (see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> ) | -    | 450  |      | ns            |
| $Q_{rr}$           | Reverse recovery charge       |                                                                                                                                                                                                                                      | -    | 5.5  |      | $\mu\text{C}$ |
| $I_{RRM}$          | Reverse recovery current      |                                                                                                                                                                                                                                      | -    | 25   |      | A             |

**Notes:**

<sup>(1)</sup>The value is rated according to  $R_{thj-case}$  and limited by package.

<sup>(2)</sup>Pulse width limited by safe operating area.

<sup>(3)</sup>Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

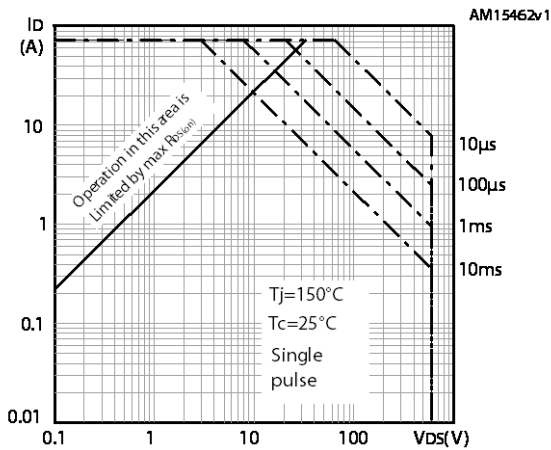


Figure 3: Thermal impedance

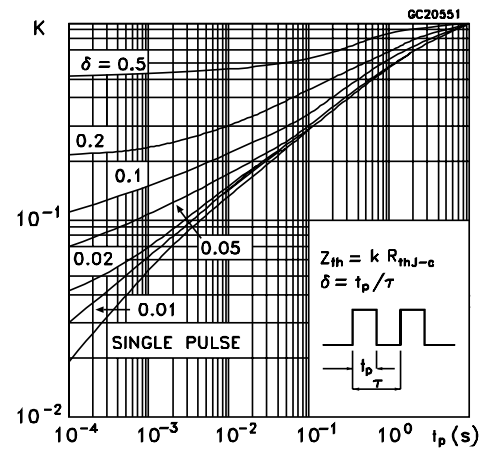


Figure 4: Output characteristics

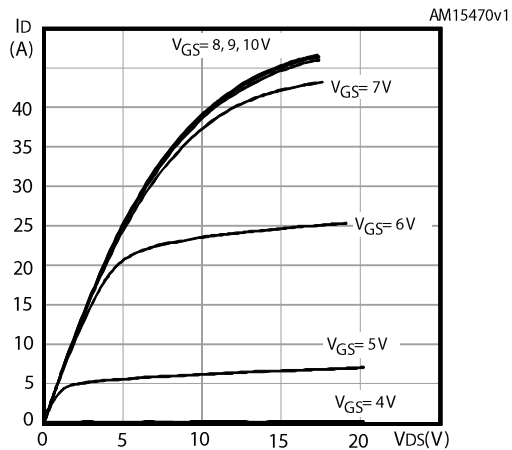


Figure 5: Transfer characteristics

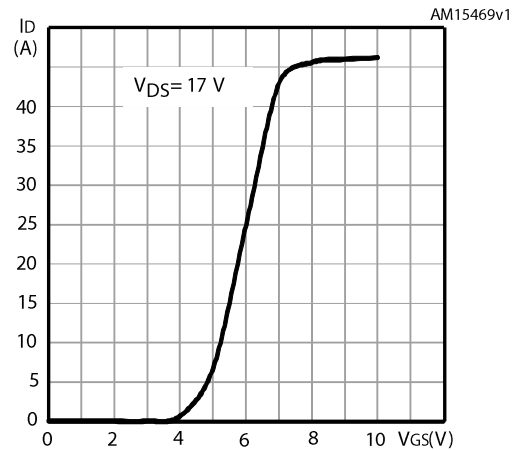


Figure 6: Gate charge vs gate-source voltage

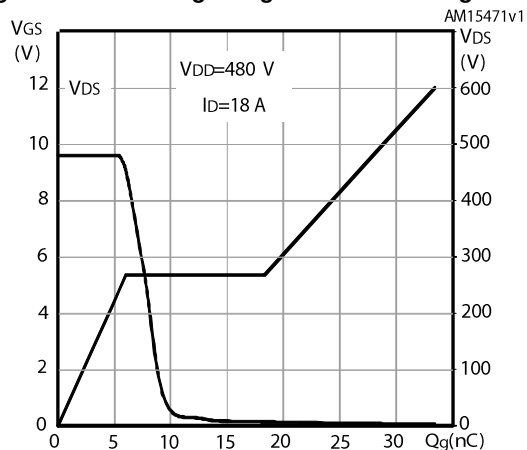


Figure 7: Static drain-source on-resistance

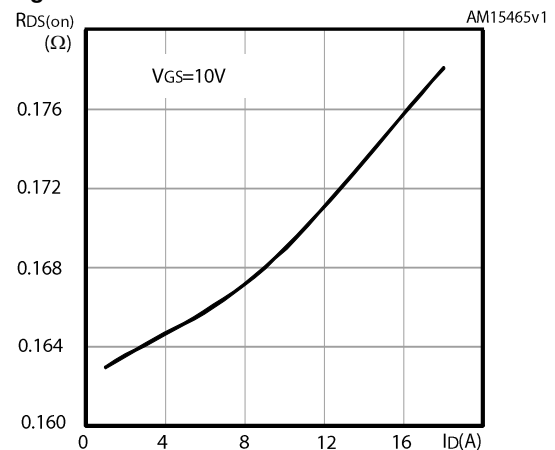


Figure 8: Capacitance variations

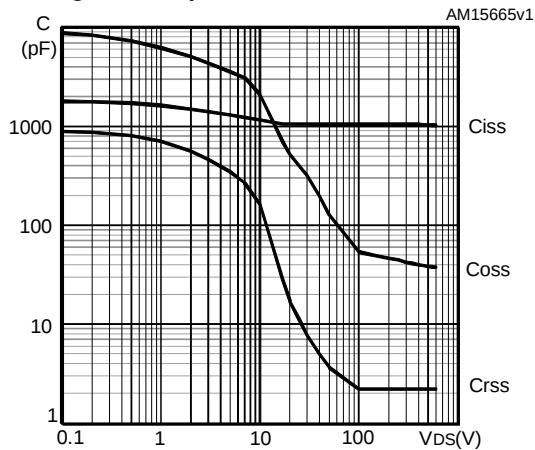


Figure 9: Normalized gate threshold voltage vs. temperature

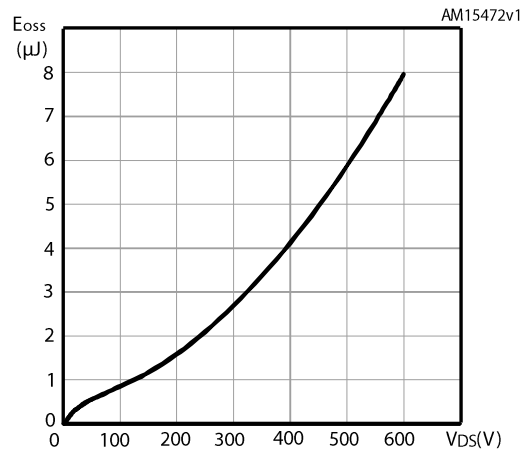


Figure 10: Normalized on-resistance vs temperature

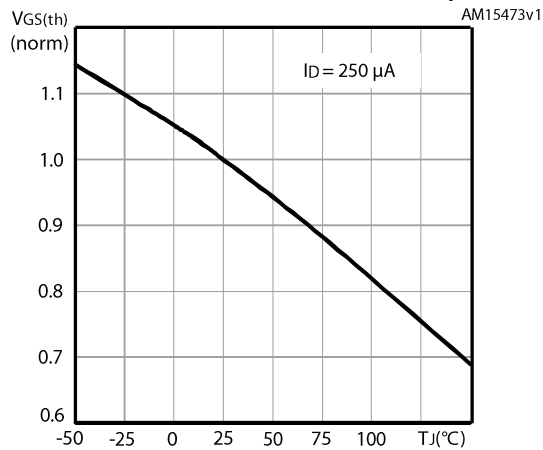


Figure 11: Source-drain diode forward characteristics

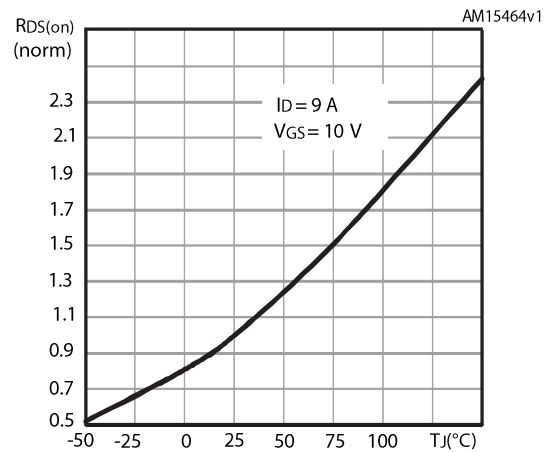


Figure 12: Normalized V(BR)DSS vs temperature

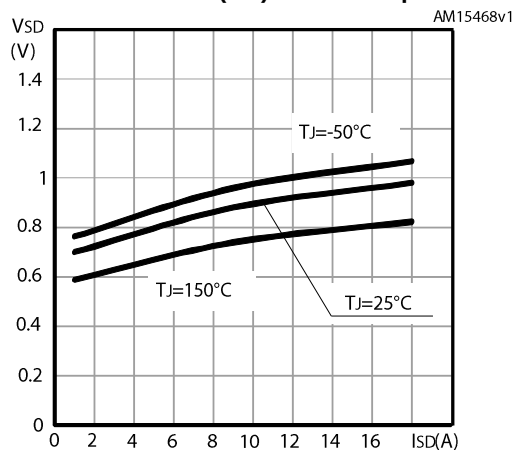
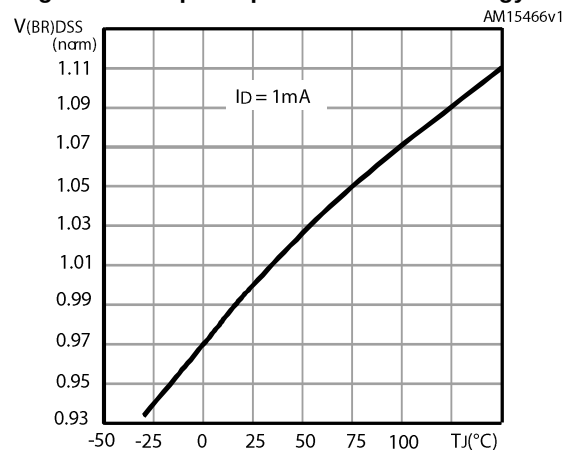
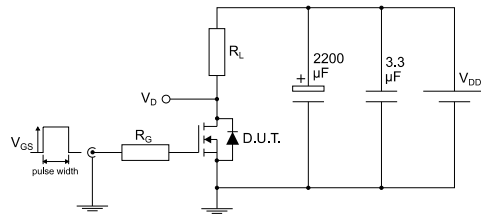


Figure 13: Output capacitance stored energy



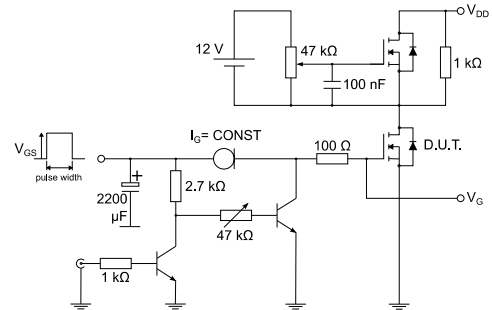
### 3 Test circuit

**Figure 14: Test circuit for resistive load switching times**



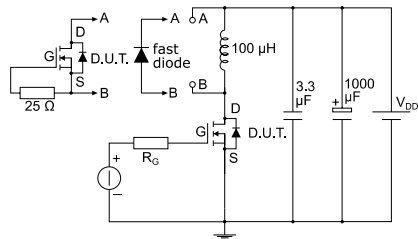
AM01468v1

**Figure 15: Test circuit for gate charge behavior**



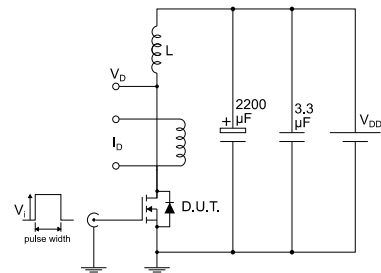
AM01468v1

**Figure 16: Test circuit for inductive load switching and diode recovery times**



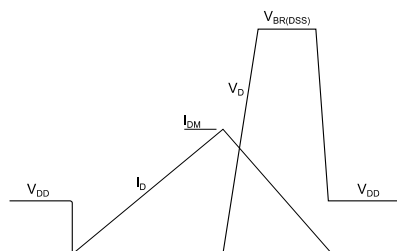
AM01470v1

**Figure 17: Unclamped inductive load test circuit**



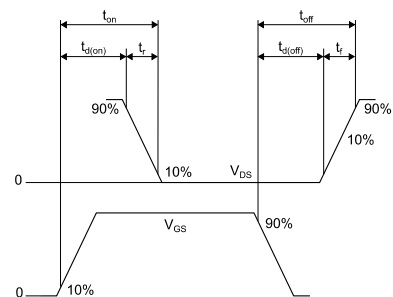
AM01471v1

**Figure 18: Unclamped inductive waveform**



AM01472v1

**Figure 19: Switching time waveform**



AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 TO-220FP package information

Figure 20: TO-220FP ultra narrow leads package outline

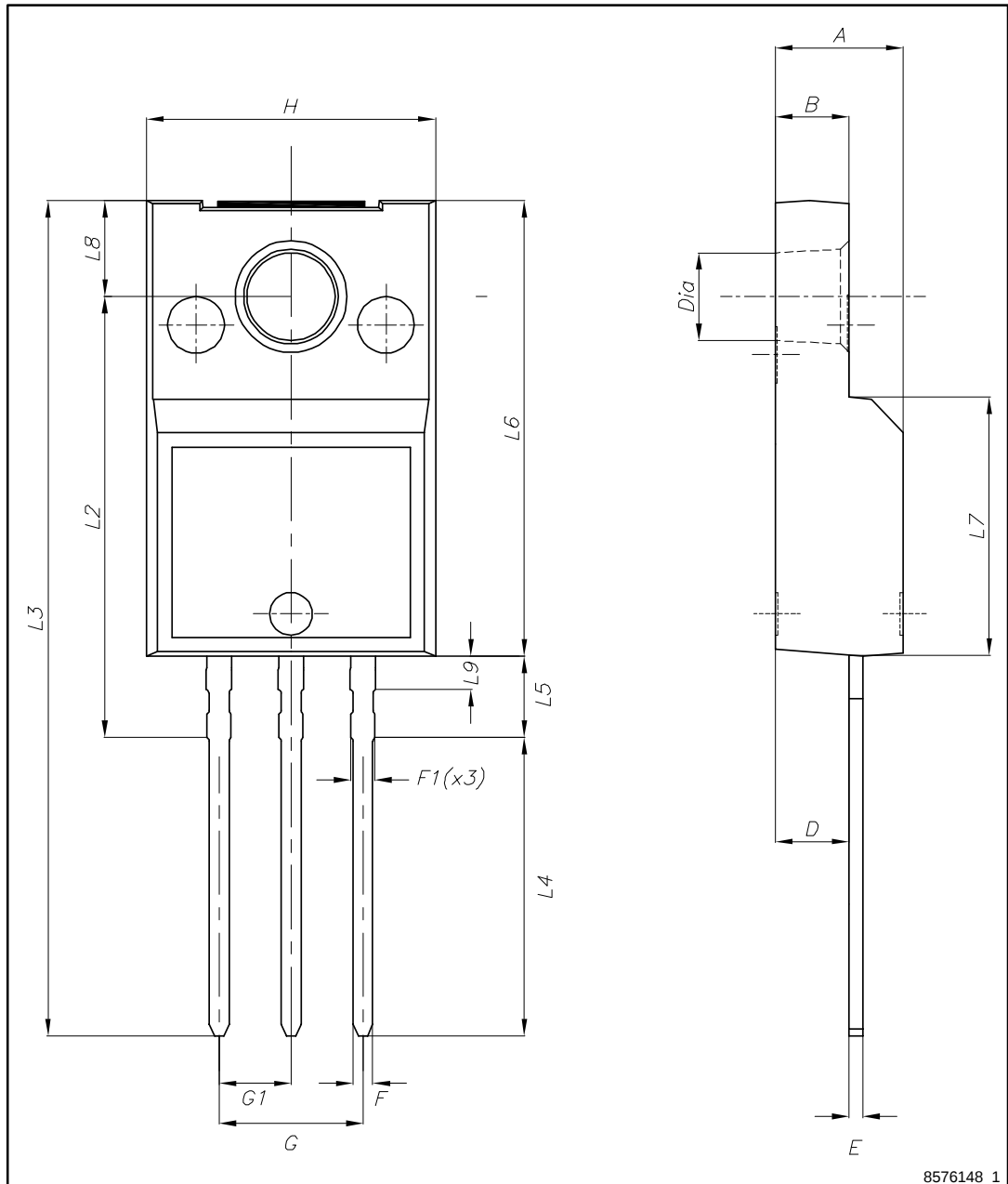


Table 9: TO-220FP ultra narrow leads mechanical data

| Dim. | mm    |      |       |
|------|-------|------|-------|
|      | Min.  | Typ. | Max.  |
| A    | 4.40  |      | 4.60  |
| B    | 2.50  |      | 2.70  |
| D    | 2.50  |      | 2.75  |
| E    | 0.45  |      | 0.60  |
| F    | 0.65  |      | 0.75  |
| F1   | -     |      | 0.90  |
| G    | 4.95  |      | 5.20  |
| G1   | 2.40  | 2.54 | 2.70  |
| H    | 10.00 |      | 10.40 |
| L2   | 15.10 |      | 15.90 |
| L3   | 28.50 |      | 30.50 |
| L4   | 10.20 |      | 11.00 |
| L5   | 2.50  |      | 3.10  |
| L6   | 15.60 |      | 16.40 |
| L7   | 9.00  |      | 9.30  |
| L8   | 3.20  |      | 3.60  |
| L9   | -     |      | 1.30  |
| Dia. | 3.00  |      | 3.20  |

## 5 Revision history

**Table 10: Document revision history**

| Date         | Revision | Changes                                                       |
|--------------|----------|---------------------------------------------------------------|
| 12-Mar-2015  | 1        | Initial release                                               |
| 08-Sept-2015 | 2        | Datasheet status promoted from preliminary to production data |

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