# bq24133 1.6-MHz Synchronous Switched-Mode Li-Ion and Li-Polymer Stand-Alone Battery Charger With Integrated MOSFETs and Power Path Selector

## 1 Features

- 1.6-MHz Synchronous Switched-Mode Charger With 2.5-A Integrated N-MOSFETs
- Up to 92% Efficiency
- 30-V Input Rating With Adjustable Overvoltage Protection
  - 4.5-V to 17-V Input Operating Voltage
- Battery Charge Voltage
  - 1-Cell, 2-Cell, or 3-Cell With 4.2 V/Cell
- High Integration
  - Automatic Power Path Selector Between Adapter and Battery
  - Dynamic Power Management
  - Integrated 20-V Switching MOSFETs
  - Integrated Bootstrap Diode
  - Internal Digital Soft Start
- Safety
  - Thermal Regulation Loop Throttles Back Current to Limit $T_J$ = 120°C
  - Thermal Shutdown
  - Battery Thermistor Sense Hot/Cold Charge Suspend and Battery Detect
  - Adjustable Input Overvoltage Protection
  - Cycle-by-Cycle Current Limit
- Accuracy
  - ±0.5% Charge Voltage Regulation
  - ±5% Charge Current Regulation
  - ±6% Input Current Regulation
- <15-µA Battery Current With Adapter Removed
- <1.5-mA Input Current With Adapter Present and Charge Disabled Package

## 2 Applications

- Tablet PCs
- Netbooks and Ultra-Mobile Computers
- Portable Data Capture Terminals
- Portable Printers
- Medical Diagnostics Equipment
- Battery Bay Chargers
- Battery Backup Systems

## 3 Description

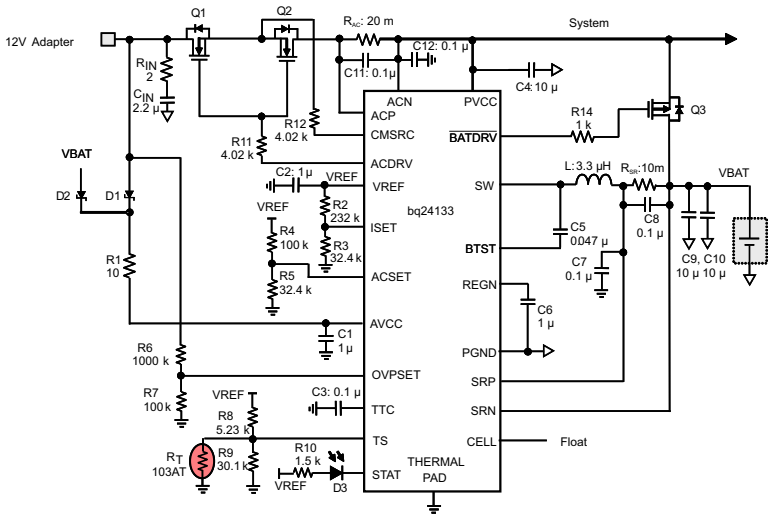
The bq24133 device is a highly integrated stand-alone Li-Ion and Li-Polymer switched-mode battery charger with two integrated N-channel power MOSFETs. The device offers a constant-frequency synchronous PWM controller with high accuracy regulation of input current, charge current, and voltage. The bq24133 closely monitors the battery pack temperature to allow charge only in a preset temperature window. The bq24133 charges one, two, or three cells (selected by CELL pin) at a fixed 4.2 V/cell.

**Device Information**[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| bq24133 | VQFN (24) | 5.50 mm × 3.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Typical Application Schematic**



## Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision B (March 2011) to Revision C** — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

**Changes from Revision A (March 2011) to Revision B** — **Page**

- Added 30-V Input Rating with Adjustable Overvoltage Protection ... 1
- Added new paragraph to Description (Continued) ... 3
- Changed Voltage range (with respect to AGND) pins in ABSOLUTE MAXIMUM RATINGS table ... 6
- Added paragraph at the end of INPUT FILTER DESIGN section ... 27

## 5 Description (continued)

The bq24133 charges the battery in three phases: preconditioning, constant current, and constant voltage.

The bq24133 provides power path selector gate driver ACDRV/CMSRC on input NMOS pair ACFET (Q1) and RBFET (Q2), and BATDRV on a battery PMOS device (Q3). When the qualified adapter is present, the system is directly connected to the adapter. Otherwise, the system is connected to the battery. In addition, the power path prevents battery from boosting back to the input.

The bq24133 charges the battery from a DC source as high as 17 V, including a car battery. The input overvoltage limit is adjustable through the OVPSET pin. The AVCC, ACP, and ACN pins have a 30-V rating. When a high-voltage DC source is inserted, Q1 and Q2 remain off to avoid high-voltage damage to the system.

For 1-cell applications where the battery is not removable, the system can be directly connected to the battery to simplify the power path design and reduce the cost. With this configuration, the battery can automatically supplement the system load if the adapter is overloaded.

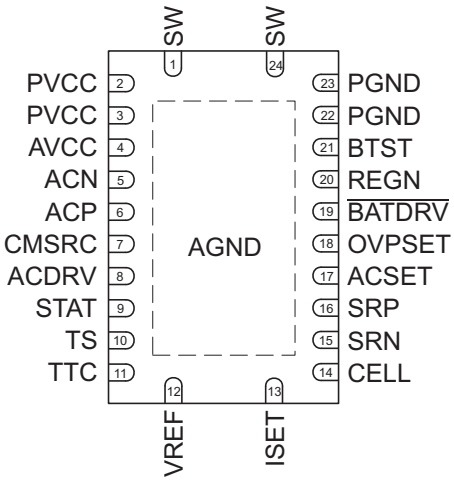
The bq24133 is available in a 24-pin, 5.5-mm × 3.5-mm thin VQFN package.

## 6 Device Comparison Table

| | INPUT VOLTAGE | MAX CHARGE RATE | BATTERY VOLTAGE | JEITA |
|---|---|---|---|---|
| bq24133 | 4.5 V to 17 V | 2.5 A | 4.2 V/cell | No |
| bq24170 | | 4 A | 4.2 V/cell | No |
| bq24171 | | | Adjustable | Yes |
| bq24172 | | | Adjustable | No |

# 7 Pin Configuration and Functions

**RGY Package**
**24-Pin VQFN**
**Top View**




**Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| ACDRV | 8 | O | AC adapter to system switch driver output. Connect to 4-kΩ resistor then to the gate of the ACFET N-channel power MOSFET and the reverse conduction blocking N-channel power MOSFET. Connect both FETs as common-source. The internal gate drive is asymmetrical, allowing a quick turnoff and slower turnon in addition to the internal break-before-make logic with respect to the $\overline{\text{BATDRV}}$. |
| ACN | 5 | I | Adapter current sense resistor negative input. A 0.1-µF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. An optional 0.1-µF ceramic capacitor is placed from ACN pin to AGND for common-mode filtering. |
| ACP | 6 | P/I | Adapter current sense resistor positive input. A 0.1-µF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. A 0.1-µF ceramic capacitor is placed from ACP pin to AGND for common-mode filtering. |
| ACSET | 17 | I | Input current set point. Use a voltage divider from VREF to ACSET to AGND to set this value: $I_{DPM} = \frac{V_{ACSET}}{20 \times R_{AC}}$ |
| AGND | Thermal Pad | P | Exposed pad beneath the IC. Always solder Thermal Pad to the board, and have vias on the Thermal Pad plane star-connecting to AGND and ground plane for high-current power converter. It dissipates the heat from the IC. |
| AVCC | 4 | P | IC power positive supply. Place a 1-µF ceramic capacitor from AVCC to AGND and place it as close as possible to IC. Place a 10-Ω resistor from input side to AVCC pin to filter the noise. For 5-V input, a 5-Ω resistor is recommended. |
| $\overline{\text{BATDRV}}$ | 19 | O | Battery discharge MOSFET gate driver output. Connect to 1-kΩ resistor to the gate of the BATFET P-channel power MOSFET. Connect the source of the BATFET to the system load voltage node. Connect the drain of the BATFET to the battery pack positive node. The internal gate drive is asymmetrical to allow a quick turnoff and slower turnon, in addition to the internal break-before-make logic with respect to ACDRV. |
| BTST | 21 | P | PWM high-side driver positive supply. Connect the 0.047-µF bootstrap capacitor from SW to BTST. |
| CELL | 14 | I | Cell selection pin. Set CELL pin LOW for 1-cell, Float for 2-cell (0.8 V - 1.8 V), and HIGH for 3-cell with a fixed 4.2 V per cell. |
| CMSRC | 7 | O | Connect to common source of N-channel ACFET and reverse blocking MOSFET (RBFET). Place 4-kΩ resistor from CMSRC pin to the common source of ACFET and RBFET to control the turnon speed. The resistance between ACDRV and CMSRC should be 500 kΩ or bigger. |

## Pin Functions (continued)

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| ISET | 13 | I | Fast charge current set point. Use a voltage divider from VREF to ISET to AGND to set the fast charge current: $$I_{CHG} = \frac{V_{ISET}}{20 \times R_{SR}}$$ The precharge and termination current is internally as one tenth of the charge current. The charger is disabled when ISET pin voltage is below 40 mV and enabled when ISET pin voltage is above 120 mV. |
| OVPSET | 18 | I | Valid input voltage set point. Use a voltage divider from input to OVPSET to AGND to set this voltage. The voltage above internal 1.6-V reference indicates input overvoltage, and the voltage below internal 0.5-V reference indicates input undervoltage. In either condition, charge terminates, and input NMOS pair ACFET/RBFET turn off. LED driven by STAT pin keeps blinking, reporting fault condition. |
| PGND | 22, 23 | P | Power ground. Ground connection for high-current power converter node. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. Only connect to AGND through the Thermal Pad underneath the IC. |
| PVCC | 2, 3 | P | Charger input voltage. Connect at least 10-µF ceramic capacitor from PVCC to PGND and place it as close as possible to IC. |
| REGN | 20 | P | PWM low-side driver positive 6-V supply output. Connect a 1-µF ceramic capacitor from REGN to PGND pin, close to the IC. Generate high-side driver bootstrap voltage by integrated diode from REGN to BTST. |
| SRN | 15 | I | Charge current sense resistor negative input. A 0.1-µF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. A 0.1-µF ceramic capacitor is placed from SRN pin to AGND for common-mode filtering. |
| SRP | 16 | I/P | Charge current sense resistor, positive input. A 0.1-µF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. A 0.1-µF ceramic capacitor is placed from SRP pin to AGND for common-mode filtering. |
| STAT | 9 | O | Open-drain charge status pin with 10-kΩ pullup to power rail. The STAT pin can be used to drive LED or communicate with the host processor. It indicates various charger operations: LOW when charge in progress. HIGH when charge is complete or in SLEEP mode. Blinking at 0.5 Hz when fault occurs, including charge suspend, input overvoltage, timer fault and battery absent. |
| SW | 1, 24 | P | Switching node, charge current output inductor connection. Connect the 0.047-µF bootstrap capacitor from SW to BTST. |
| TS | 10 | I | Temperature qualification voltage input. Connect a negative temperature coefficient thermistor. Program the hot and cold temperature window with a resistor divider from VREF to TS to AGND. The temperature qualification window can be set to 5-40°C or wider. The 103AT thermistor is recommended. |
| TTC | 11 | I | Safety Timer and termination control. Connect a capacitor from this node to AGND to set the fast charge safety timer(5.6 min/nF). Precharge timer is internally fixed to 30 minutes. Pull the TTC to LOW to disable the charge termination and safety timer. Pull the TTC to HIGH to disable the safety timer but allow the charge termination. |
| VREF | 12 | P | 3.3-V reference voltage output. Place a 1-µF ceramic capacitor from VREF to AGND pin close to the IC. This voltage could be used for programming ISET and ACSET and TS pins. It may also serve as the pullup rail of STAT pin and CELL pin. |

# 8 Specifications

## 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage (with respect to AGND) | AVCC, ACP, ACN, ACDRV, CMSRC, STAT | –0.3 | 30 | V |
| | PVCC | –0.3 | 20 | |
| | BTST | –0.3 | 26 | |
| | $\overline{\text{BATDRV}}$, SRP, SRN | –0.3 | 20 | |
| | SW | –2 | 20 | |
| | OVPSET, REGN, TS, TTC, CELL | –0.3 | 7 | |
| | VREF, ISET, ACSET | –0.3 | 3.6 | |
| | PGND | –0.3 | 0.3 | |
| Maximum difference voltage | SRP–SRN, ACP-ACN | –0.5 | 0.5 | V |
| Junction temperature, $T_J$ | | –40 | 155 | °C |
| Storage temperature, $T_{stg}$ | | –55 | 155 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND if not specified. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages.

## 8.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | 1000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101 (2) | 250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 8.3 Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage | $V_{IN}$ | 4.5 | 17 | V |
| Output voltage | $V_{OUT}$ | | 13.5 | V |
| Output current ($R_{SR}$ 10 mΩ) | $I_{OUT}$ | 0.6 | 2.5 | A |
| Maximum difference voltage | ACP – ACN | –200 | 200 | mV |
| | SRP – SRN | –200 | 200 | |
| Operation free-air temperature range, $T_A$ | | –40 | 85 | °C |

## 8.4 Thermal Information

| THERMAL METRIC (1) | | bq24133 RGY [VQFN] 24 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 35.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.4 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 31.2 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 8.5 Electrical Characteristics

4.5 V ≤ V(PVCC, AVCC) ≤ 17 V, –40°C < $T_J$ + 125°C, typical values are at $T_A$ = 25°C, with respect to AGND (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OPERATING CONDITIONS** | | | | | | |
| $V_{AVCC\_OP}$ | AVCC input voltage operating range during charging | | 4.5 | | 17 | V |
| **QUIESCENT CURRENTS** | | | | | | |
| $I_{BAT}$ | Battery discharge current (sum of currents into AVCC, PVCC, ACP, ACN) | $V_{AVCC}$ > $V_{UVLO}$, $V_{SRN}$ > $V_{AVCC}$ (SLEEP), $T_J$ = 0°C to 85°C | | | 15 | µA |
| | | BTST, SW, SRP, SRN, $V_{AVCC}$ > $V_{UVLO}$, $V_{AVCC}$ > $V_{SRN}$, ISET < 40 mV, $V_{BAT}$=12.6 V, Charge disabled | | | 25 | |
| | | BTST, SW, SRP, SRN, $V_{AVCC}$ > $V_{UVLO}$, $V_{AVCC}$ > $V_{SRN}$, ISET > 120 mV, $V_{BAT}$=12.6 V, Charge done | | | 25 | |
| $I_{AC}$ | Adapter supply current (sum of current into AVCC,ACP, ACN) | $V_{AVCC}$ > $V_{UVLO}$, $V_{AVCC}$ > $V_{SRN}$, ISET < 40 mV, $V_{BAT}$=12.6 V, Charge disabled | | 1.2 | 1.5 | mA |
| | | $V_{AVCC}$ > $V_{UVLO}$, $V_{AVCC}$ > $V_{SRN}$, ISET > 120 mV, Charge enabled, no switching | | 2.5 | 5 | |
| | | $V_{AVCC}$ > $V_{UVLO}$, $V_{AVCC}$ > $V_{SRN}$, ISET > 120 mV, Charge enabled, switching | | 15(1) | | |
| **CHARGE VOLTAGE REGULATION** | | | | | | |
| $V_{BAT\_REG}$ | SRN regulation voltage | CELL to AGND, 1 cell, measured on SRN | | 4.2 | | V |
| | | CELL floating, 2 cells, measured on SRN | | 8.4 | | V |
| | | CELL to VREF, 3 cells, measured on SRN | | 12.6 | | V |
| | Charge voltage regulation accuracy | $T_J$ = 0°C to 85°C | –0.5% | | 0.5% | |
| | | $T_J$ = –40°C to 125°C | -0.7% | | 0.7% | |
| **CURRENT REGULATION – FAST CHARGE** | | | | | | |
| $V_{ISET}$ | ISET Voltage Range | $R_{SENSE}$ = 10 mΩ | 0.12 | | 0.5 | V |
| $K_{ISET}$ | Charge Current Set Factor (Amps of Charge Current per Volt on ISET pin) | $R_{SENSE}$ = 10 mΩ | | 5 | | A/V |
| | Charge Current Regulation Accuracy | $V_{SRP-SRN}$ = 40 mV | –5% | | 5% | |
| | | $V_{SRP-SRN}$ = 20 mV | –8% | | 8% | |
| | | $V_{SRP-SRN}$ = 5 mV | –25% | | 25% | |
| $V_{ISET\_CD}$ | Charge Disable Threshold | ISET falling | 40 | 50 | | mV |
| $V_{ISET\_CE}$ | Charge Enable Threshold | ISET rising | | 100 | 120 | mV |
| $I_{ISET}$ | Leakage Current into ISET | VISET = 2 V | | | 100 | nA |
| **INPUT CURRENT REGULATION** | | | | | | |
| $K_{DPM}$ | Input DPM Current Set Factor (Amps of Input Current per Volt on ACSET) | $R_{SENSE}$ = 20 mΩ | | 2.5 | | A/V |
| | Input DPM Current Regulation Accuracy | $V_{ACP-ACN}$ = 80 mV | –6% | | 6% | |
| | | $V_{ACP-ACN}$ = 40 mV | –10% | | 10% | |
| | | $V_{ACP-ACN}$ = 20 mV | –15% | | 15% | |
| | | $V_{ACP-ACN}$ = 5 mV | –20% | | 20% | |
| $I_{ACSET}$ | Leakage Current into ACSET pin | $V_{ACSET}$ = 2 V | | | 100 | nA |
| **CURRENT REGULATION – PRECHARGE** | | | | | | |
| $K_{IPRECHG}$ | Precharge current set factor | Percentage of fast charge current | | 10%(2) | | |
| | Precharge current regulation accuracy | $V_{SRP-SRN}$ = 4 mV | –25% | | 25% | |
| | | $V_{SRP-SRN}$ = 2 mV | –40% | | 40% | |

(1) Specified by design.
(2) The minimum current is 120 mA on 10 mΩ sense resistor.

## Electrical Characteristics (continued)

4.5 V ≤ V(PVCC, AVCC) ≤ 17 V, –40°C < $T_J$ + 125°C, typical values are at $T_A$ = 25°C, with respect to AGND (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CHARGE TERMINATION** | | | | | | |
| $K_{TERM}$ | Termination current set factor | Percentage of fast charge current | | 10%(2) | | |
| | Termination current regulation accuracy | $V_{SRP-SRN}$ = 4 mV | –25% | | 25% | |
| | | $V_{SRP-SRN}$ = 2 mV | –40% | | 40% | |
| $t_{TERM\_DEG}$ | Deglitch time for termination (both edges) | | | 100 | | ms |
| $t_{QUAL}$ | Termination qualification time | $V_{SRN}$ > $V_{RECH}$ and $I_{CHG}$ < $I_{TERM}$ | | 250 | | ms |
| $I_{QUAL}$ | Termination qualification current | Discharge current once termination is detected | | 2 | | mA |
| **INPUT UNDERVOLTAGE LOCKOUT COMPARATOR (UVLO)** | | | | | | |
| $V_{UVLO}$ | AC undervoltage rising threshold | Measure on AVCC | 3.4 | 3.6 | 3.8 | V |
| $V_{UVLO\_HYS}$ | AC undervoltage hysteresis, falling | Measure on AVCC | | 300 | | mV |
| **SLEEP COMPARATOR (REVERSE DISCHARGING PROTECTION)** | | | | | | |
| $V_{SLEEP}$ | SLEEP mode threshold | $V_{AVCC}$ – $V_{SRN}$ falling | 50 | 90 | 150 | mV |
| $V_{SLEEP\_HYS}$ | SLEEP mode hysteresis | $V_{AVCC}$ – $V_{SRN}$ rising | | 200 | | mV |
| $t_{SLEEP\_FALL\_CD}$ | SLEEP deglitch to disable charge | $V_{AVCC}$ – $V_{SRN}$ falling | | 1 | | ms |
| $t_{SLEEP\_FALL\_FETOFF}$ | SLEEP deglitch to turn off input FETs | $V_{AVCC}$ – $V_{SRN}$ falling | | 5 | | ms |
| $t_{SLEEP\_FALL}$ | Deglitch to enter SLEEP mode, disable VREF and enter low quiescent mode | $V_{AVCC}$ – $V_{SRN}$ falling | | 100 | | ms |
| $t_{SLEEP\_PWRUP}$ | Deglitch to exit SLEEP mode, and enable VREF | $V_{AVCC}$ – $V_{SRN}$ rising | | 30 | | ms |
| **ACN-SRN COMPARATOR** | | | | | | |
| $V_{ACN-SRN}$ | Threshold to turn on BATFET | $V_{ACN-SRN}$ falling | 150 | 220 | 300 | mV |
| $V_{ACN-SRN\_HYS}$ | Hysteresis to turn off BATFET | $V_{ACN-SRN}$ rising | | 100 | | mV |
| $t_{BATFETOFF\_DEG}$ | Deglitch to turn on BATFET | $V_{ACN-SRN}$ falling | | 2 | | ms |
| $t_{BATFETON\_DEG}$ | Deglitch to turn off BATFET | $V_{ACN-SRN}$ rising | | 50 | | µs |
| **BAT LOWV COMPARATOR** | | | | | | |
| $V_{LOWV}$ | Precharge to fast charge transition | CELL to AGND, 1 cell, measure on SRN | 2.87 | 2.9 | 2.93 | V |
| | | CELL floating, 2 cells, measure on SRN | 5.74 | 5.8 | 5.86 | |
| | | CELL to VREF, 3 cells, measure on SRN | 8.61 | 8.7 | 8.79 | |
| $V_{LOWV\_HYS}$ | Fast charge to precharge hysteresis | CELL to AGND, 1 cell, measure on SRN | | 200 | | mV |
| | | CELL floating, 2 cells, measure on SRN | | 400 | | |
| | | CELL to VREF, 3 cells, measure on SRN | | 600 | | |
| $t_{pre2fas}$ | $V_{LOWV}$ rising deglitch | Delay to start fast charge current | | 25 | | ms |
| $t_{fast2pre}$ | $V_{LOWV}$ falling deglitch | Delay to start precharge current | | 25 | | ms |
| **RECHARGE COMPARATOR** | | | | | | |
| $V_{RECHG}$ | Recharge Threshold, below regulation voltage limit, $V_{BAT\_REG}$-$V_{SRN}$ | CELL to AGND, 1 cell, measure on SRN | 70 | 100 | 130 | mV |
| | | CELL floating, 2 cells, measure on SRN | 140 | 200 | 260 | |
| | | CELL to VREF, 3 cells, measure on SRN | 210 | 300 | 390 | |
| $t_{RECH\_RISE\_DEG}$ | $V_{RECHG}$ rising deglitch | SRN decreasing below $V_{RECHG}$ | | 10 | | ms |
| $t_{RECH\_FALL\_DEG}$ | $V_{RECHG}$ falling deglitch | SRN increasing above $V_{RECHG}$ | | 10 | | ms |

## Electrical Characteristics (continued)

4.5 V ≤ V(PVCC, AVCC) ≤ 17 V, –40°C < $T_J$ + 125°C, typical values are at $T_A$ = 25°C, with respect to AGND (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **BAT OVERVOLTAGE COMPARATOR** | | | | | | |
| $V_{OV\_RISE}$ | Overvoltage rising threshold | As percentage of $V_{BAT\_REG}$ | | 104% | | |
| $V_{OV\_FALL}$ | Overvoltage falling threshold | As percentage of $V_{SRN}$ | | 102% | | |
| **INPUT OVERVOLTAGE COMPARATOR (ACOV)** | | | | | | |
| $V_{ACOV}$ | AC Overvoltage Rising Threshold to turn off ACFET | OVPSET rising | 1.55 | 1.6 | 1.65 | V |
| $V_{ACOV\_HYS}$ | AC overvoltage falling hysteresis | OVPSET falling | | 50 | | mV |
| $t_{ACOV\_RISE\_DEG}$ | AC Overvoltage Rising Deglitch to turn off ACFET and Disable Charge | OVPSET rising | | 1 | | µs |
| $t_{ACOV\_FALL\_DEG}$ | AC Overvoltage Falling Deglitch to turn on ACFET | OVPSET falling | | 30 | | ms |
| **INPUT UNDERVOLTAGE COMPARATOR (ACUV)** | | | | | | |
| $V_{ACUV}$ | AC Undervoltage Falling Threshold to turn off ACFET | OVPSET falling | 0.45 | 0.5 | 0.55 | V |
| $V_{ACUV\_HYS}$ | AC Undervoltage Rising Hysteresis | OVPSET rising | | 100 | | mV |
| $t_{ACOV\_FALL\_DEG}$ | AC Undervoltage Falling Deglitch to turn off ACFET and Disable Charge | OVPSET falling | | 1 | | µs |
| $t_{ACOV\_RISE\_DEG}$ | AC Undervoltage Rising Deglitch to turn on ACFET | OVPSET rising | | 30 | | ms |
| **THERMAL REGULATION** | | | | | | |
| $T_{J\_REG}$ | Junction Temperature Regulation Accuracy | ISET > 120 mV, Charging | | 120 | | °C |
| **THERMAL SHUTDOWN COMPARATOR** | | | | | | |
| $T_{SHUT}$ | Thermal shutdown rising temperature | Temperature rising | | 150 | | °C |
| $T_{SHUT\_HYS}$ | Thermal shutdown hysteresis | Temperature falling | | 20 | | °C |
| $t_{SHUT\_RISE\_DEG}$ | Thermal shutdown rising deglitch | Temperature rising | | 100 | | µs |
| $t_{SHUT\_FALL\_DEG}$ | Thermal shutdown falling deglitch | Temperature falling | | 10 | | ms |
| **THERMISTOR COMPARATOR** | | | | | | |
| $V_{LTF}$ | Cold Temperature Threshold, TS pin Voltage Rising Threshold | Charger suspends charge. As percentage to $V_{VREF}$ | 72.5% | 73.5% | 74.5% | |
| $V_{LTF\_HYS}$ | Cold Temperature Hysteresis, TS pin Voltage Falling | As percentage to $V_{VREF}$ | 0.2% | 0.4% | 0.6% | |
| $V_{HTF}$ | Hot Temperature TS pin voltage rising Threshold | As percentage to $V_{VREF}$ | 46.6% | 47.2% | 48.8% | |
| $V_{TCO}$ | Cut-off Temperature TS pin voltage falling Threshold | As percentage to $V_{VREF}$ | 44.2% | 44.7% | 45.2% | |
| $t_{TS\_CHG\_SUS}$ | Deglitch time for Temperature Out of Range Detection | $V_{TS} > V_{LTF}$, or $V_{TS} < V_{TCO}$, or $V_{TS} < V_{HTF}$ | | 20 | | ms |
| $t_{TS\_CHG\_RESUME}$ | Deglitch time for Temperature in Valid Range Detection | $V_{TS} < V_{LTF} – V_{LTF\_HYS}$ or $V_{TS} > V_{TCO}$, or $V_{TS} > V_{HTF}$ | | 400 | | ms |
| **CHARGE OVERCURRENT COMPARATOR (CYCLE-BY-CYCLE)** | | | | | | |
| $V_{OCP\_CHRG}$ | Charge Overcurrent Rising Threshold, $V_{SRP}$ > 2.2 V | Current as percentage of fast charge current | | 160% | | |
| $V_{OCP\_MIN}$ | Charge Overcurrent Limit Min, $V_{SRP}$ < 2.2 V | Measure $V_{SRP-SRN}$ | | 45 | | mV |
| $V_{OCP\_MAX}$ | Charge Overcurrent Limit Max, $V_{SRP}$ > 2.2 V | Measure $V_{SRP-SRN}$ | | 75 | | mV |
| **HSFET OVERCURRENT COMPARATOR (CYCLE-BY-CYCLE)** | | | | | | |
| $I_{OCP\_HSFET}$ | Current limit on HSFET | Measure on HSFET | 6 | | | A |
| **CHARGE UNDERCURRENT COMPARATOR (CYCLE-BY-CYCLE)** | | | | | | |
| $V_{UCP}$ | Charge undercurrent falling threshold | Measure on $V_{(SRP-SRN)}$ | 1 | 5 | 9 | mV |

## Electrical Characteristics (continued)

4.5 V ≤ V(PVCC, AVCC) ≤ 17 V, –40°C < $T_J$ + 125°C, typical values are at $T_A$ = 25°C, with respect to AGND (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **BAT SHORT COMPARATOR** | | | | | | |
| $V_{BATSHT}$ | Battery short falling threshold | Measure on SRN | | 2 | | V |
| $V_{BATSHT\_HYS}$ | Battery short rising hysteresis | Measure on SRN | | 200 | | mV |
| $t_{BATSHT\_DEG}$ | Deglitch on both edges | | | 1 | | µs |
| $V_{BATSHT}$ | Charge Current during BATSHORT | Percentage of fast charge current | | 10%(2) | | |
| **VREF REGULATOR** | | | | | | |
| $V_{VREF\_REG}$ | VREF regulator voltage | $V_{AVCC}$ > $V_{UVLO}$, No load | 3.267 | 3.3 | 3.333 | V |
| $I_{VREF\_LIM}$ | VREF current limit | $V_{VREF}$ = 0 V, $V_{AVCC}$ > $V_{UVLO}$ | 35 | | 90 | mA |
| **REGN REGULATOR** | | | | | | |
| $V_{REGN\_REG}$ | REGN regulator voltage | $V_{AVCC}$ > 10 V, ISET > 120 mV | 5.7 | 6 | 6.3 | V |
| $I_{REGN\_LIM}$ | REGN current limit | $V_{REGN}$ = 0 V, $V_{AVCC}$ > 10 v, ISET > 120 mV | 40 | | 120 | mA |
| **TTC INPUT** | | | | | | |
| $t_{prechrg}$ | Precharge Safety Timer | Precharge time before fault occurs | 1620 | 1800 | 1980 | s |
| $t_{fastchrg}$ | Fast Charge Timer Range | $T_{chg}$=$C_{TTC}$*$K_{TTC}$ | 1 | | 10 | hr |
| | Fast Charge Timer Accuracy | | –10% | | 10% | |
| $K_{TTC}$ | Timer Multiplier | | | 5.6 | | min/nF |
| $V_{TTC\_LOW}$ | TTC Low Threshold | TTC falling | | | 0.4 | V |
| $I_{TTC}$ | TTC Source/Sink Current | | 45 | 50 | 55 | µA |
| $V_{TTC\_OSC\_HI}$ | TTC oscillator high threshold | | | 1.5 | | V |
| $V_{TTC\_OSC\_LO}$ | TTC oscillator low threshold | | | 1 | | V |
| **BATTERY SWITCH (BATFET) DRIVER** | | | | | | |
| $R_{DS\_BAT\_OFF}$ | BATFET Turnoff Resistance | $V_{AVCC}$ > 5 V | | | 100 | Ω |
| $R_{DS\_BAT\_ON}$ | BATFET Turnon Resistance | $V_{AVCC}$ > 5 V | | | 20 | kΩ |
| $V_{BATDRV\_REG}$ | BATFET Drive Voltage | $V_{BATDRV\_REG}$ =$V_{ACN}$ - $V_{BATDRV}$ when $V_{AVCC}$ > 5 V and BATFET is on | 4.2 | | 7 | V |
| $t_{BATFET\_DEG}$ | BATFET Power-up Delay to turn off BATFET after adapter is detected | | | 30 | | ms |
| **AC SWITCH (ACFET) DRIVER** | | | | | | |
| $I_{ACFET}$ | ACDRV Charge Pump Current Limit | $V_{ACDRV}$ - $V_{CMSRC}$ = 5 V | | 60 | | µA |
| $V_{ACDRV\_REG}$ | Gate Drive Voltage on ACFET | $V_{ACDRV}$ - $V_{CMSRC}$ when $V_{AVCC}$ > $V_{UVLO}$ | 4.2 | 6 | | V |
| $R_{ACDRV\_LOAD}$ | Maximum load between ACDRV and CMSRC | | 500 | | | kΩ |
| **AC/BAT SWITCH DRIVER TIMING** | | | | | | |
| $t_{DRV\_DEAD}$ | Driver Dead Time | Dead Time when switching between ACFET and BATFET | | 10 | | µs |
| **BATTERY DETECTION** | | | | | | |
| $t_{WAKE}$ | Wake timer | Max time charge is enabled | | 500 | | ms |
| $I_{WAKE}$ | Wake current | $R_{SENSE}$ = 10 mΩ | 50 | 125 | 200 | mA |
| $t_{DISCHARGE}$ | Discharge timer | Max time discharge current is applied | | 1 | | s |
| $I_{DISCHARGE}$ | Discharge current | | | 8 | | mA |
| $I_{FAULT}$ | Fault current after a time-out fault | | | 2 | | mA |
| $V_{WAKE}$ | Wake threshold with respect to $V_{REG}$ To detect battery absent during WAKE | Measure on SRN | | 100 | | mV/cell |
| $V_{DISCH}$ | Discharge Threshold to detect battery absent during discharge | Measure on SRN | | 2.9 | | V/cell |

## Electrical Characteristics (continued)

4.5 V ≤ V(PVCC, AVCC) ≤ 17 V, –40°C < $T_J$ + 125°C, typical values are at $T_A$ = 25°C, with respect to AGND (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INTERNAL PWM** | | | | | | |
| fsw | PWM Switching Frequency | | 1360 | 1600 | 1840 | kHz |
| $t_{SW\_DEAD}$ | Driver Dead Time(1) | Dead time when switching between LSFET and HSFET no load | | 30 | | ns |
| $R_{DS\_HI}$ | High-Side MOSFET ON-Resistance | $V_{BTST} – V_{SW}$ = 4.5 V | | 80 | 150 | mΩ |
| $R_{DS\_LO}$ | Low-Side MOSFET ON-Resistance | | | 95 | 160 | mΩ |
| $V_{BTST\_REFRESH}$ | Bootstrap Refresh Comparator Threshold Voltage | $V_{BTST} – V_{SW}$ when low-side refresh pulse is requested, $V_{AVCC}$ = 4.5 V | 3 | | | V |
| | | $V_{BTST} – V_{SW}$ when low-side refresh pulse is requested, $V_{AVCC}$ > 6 V | 4 | | | |
| **INTERNAL SOFT START (8 steps to regulation current ICHG)** | | | | | | |
| SS_STEP | Soft start steps | | | 8 | | step |
| $T_{SS\_STEP}$ | Soft start step time | | | 1.6 | 3 | ms |
| **CHARGER SECTION POWER-UP SEQUENCING** | | | | | | |
| $t_{CE\_DELAY}$ | Delay from ISET above 120 mV to start charging battery | | | 1.5 | | s |
| **INTEGRATED BTST DIODE** | | | | | | |
| $V_F$ | Forward Bias Voltage | $I_F$=120 mA at 25°C | | 0.85 | | V |
| $V_R$ | Reverse breakdown voltage | $I_R$=2 µA at 25°C | | | 20 | V |
| **LOGIC IO PIN CHARACTERISTICS** | | | | | | |
| $V_{OUT\_LO}$ | STAT Output Low Saturation Voltage | Sink Current = 5 mA | | | 0.5 | V |
| $V_{CELL\_LO}$ | CELL pin input low threshold, 1 cell | CELL pin voltage falling edge | | | 0.5 | V |
| $V_{CELL\_MID}$ | CELL pin input mid threshold, 2 cells | CELL pin voltage rising for MIN, falling for MAX | 0.8 | | 1.8 | V |
| $V_{CELL\_HI}$ | CELL pin input high threshold, 3 cells | CELL pin voltage rising edge | 2.5 | | | V |

## 8.6 Typical Characteristics

**Table 1. Table of Graphs (1)**

| FIGURE | DESCRIPTION |
|---|---|
| Figure 1 | AVCC, VREF, ACDRV and STAT Power Up (ISET=0) |
| Figure 2 | Charge Enable by ISET |
| Figure 3 | Current Soft Start |
| Figure 4 | Charge Disable by ISET |
| Figure 5 | Continuous Conduction Mode Switching |
| Figure 6 | Discontinuous Conduction Mode Switching |
| Figure 7 | BATFET to ACFET Transition during Power Up |
| Figure 8 | System Load Transient (Input Current DPM) |
| Figure 9 | Battery Insertion and Removal |
| Figure 10 | Battery to Ground Short Protection |
| Figure 11 | Battery to Ground Short Transition |
| Figure 12 | Efficiency vs Output Current ($V_{OUT}$ = 3.8 V) |
| Figure 21 | Efficiency vs Output Current (2-3 cell) |

(1) All waveforms and data are measured on HPA715 EVM.

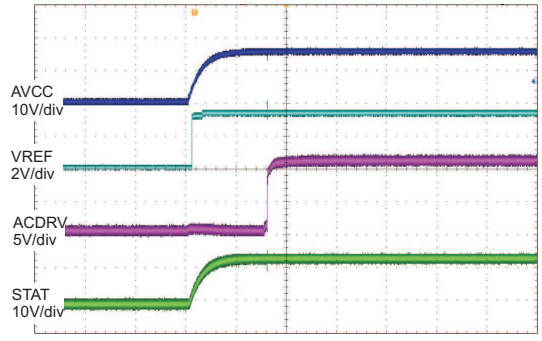



**Figure 1. Power Up (ISET = 0)**

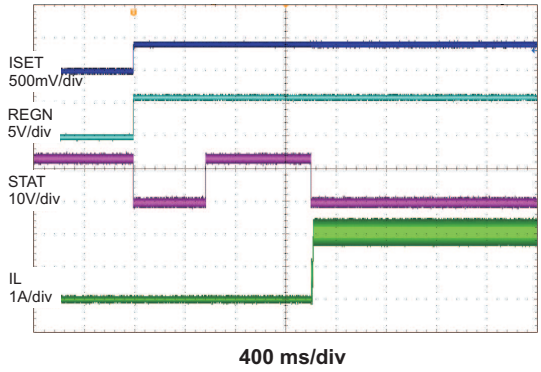



**Figure 2. Charge Enable by ISET**

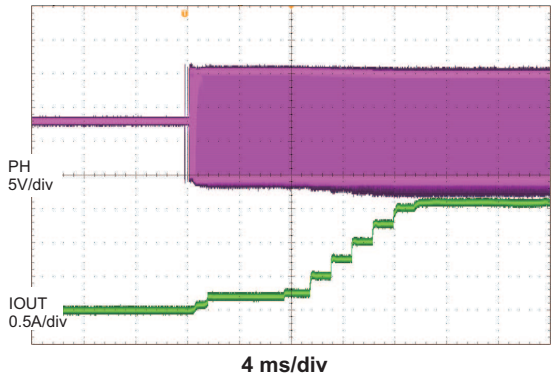



**Figure 3. Current Soft Start**

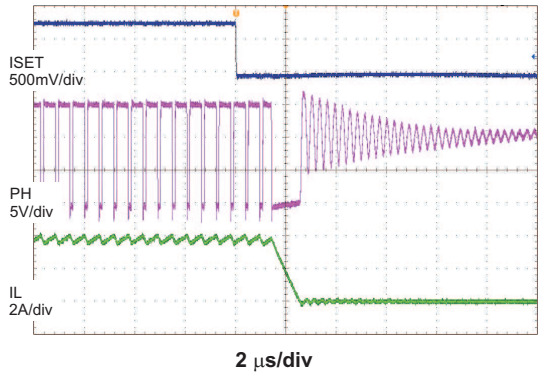



**Figure 4. Charge Disable by ISET**

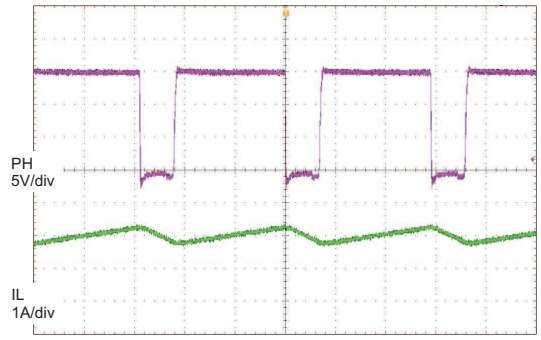



Figure 5. Continuous Conduction Mode Switching

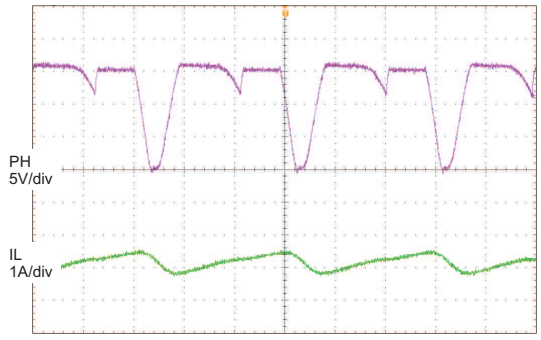



Figure 6. Discontinuous Conduction Mode Switching

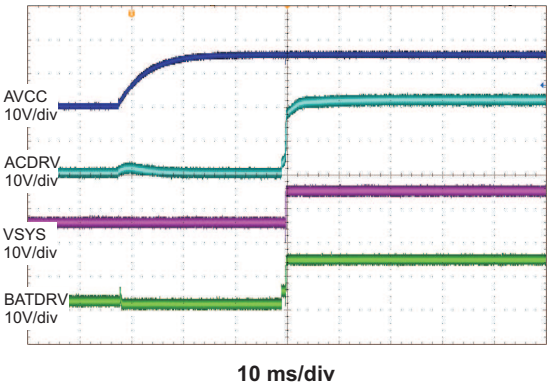



Figure 7. BATFET to ACFET Transition During Power Up

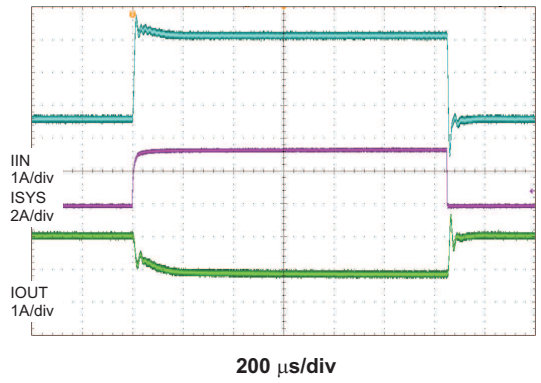



Figure 8. System Load Transient (Input current DPM)

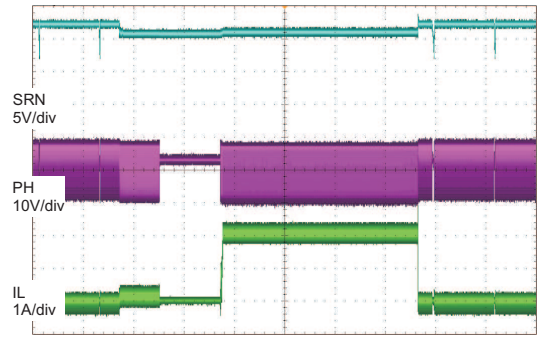



Figure 9. Battery Insertion and Removal

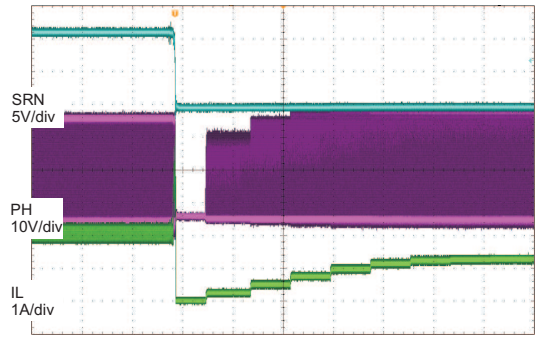



Figure 10. Battery to Ground Short Protection

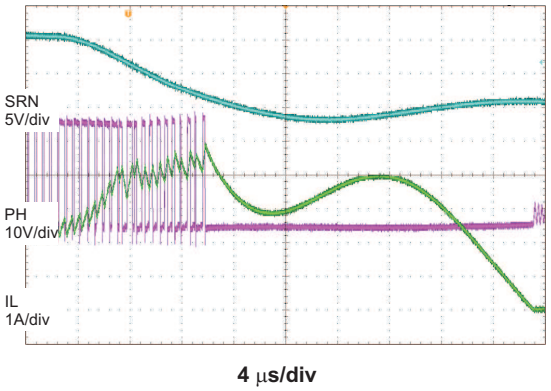



**Figure 11. Battery to Ground Short Transition**

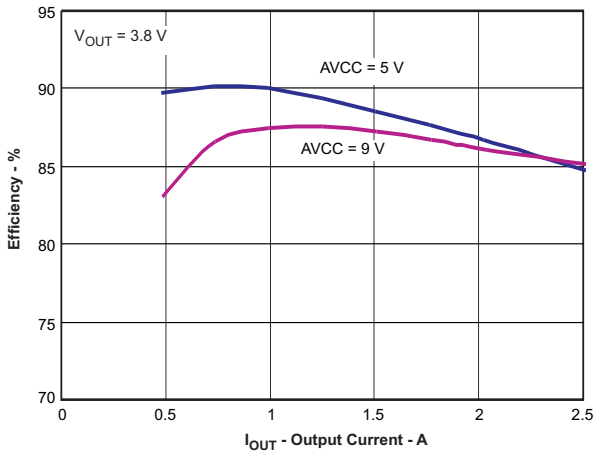


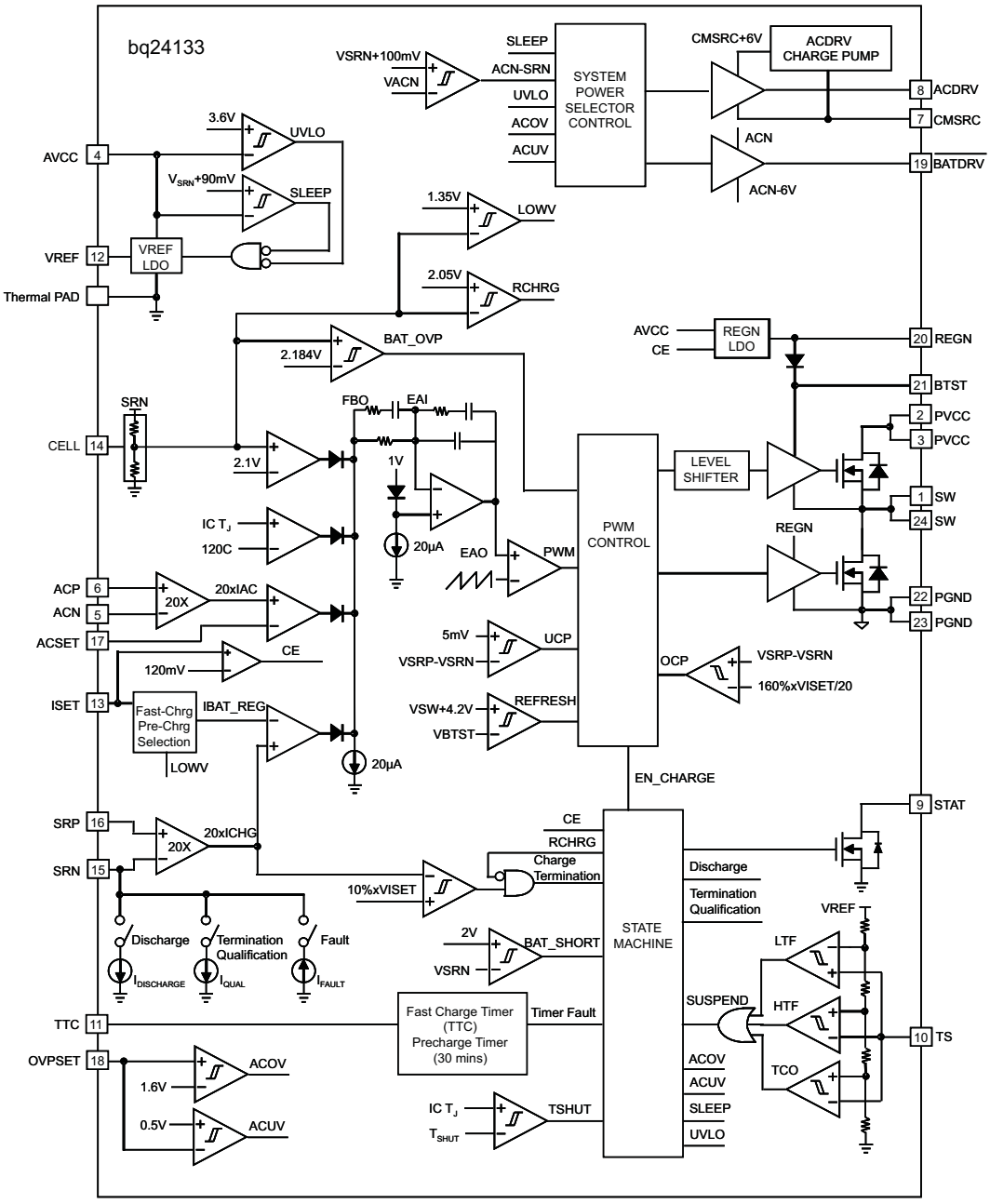

**Figure 12. Efficiency vs Output Current**

# 9 Detailed Description

## 9.1 Overview

The bq24133 device is a stand-alone switched-mode battery charger for Li-ion and Li-Polymer batteries with power path management and integrated N-channel power MOSFETs. This fixed-frequency synchronous PWM charger offers high accuracy regulation of input current charge current and battery regulation voltage.

## 9.2 Functional Block Diagram



## 9.3 Feature Description

Figure 13 shows a typical charging profile.

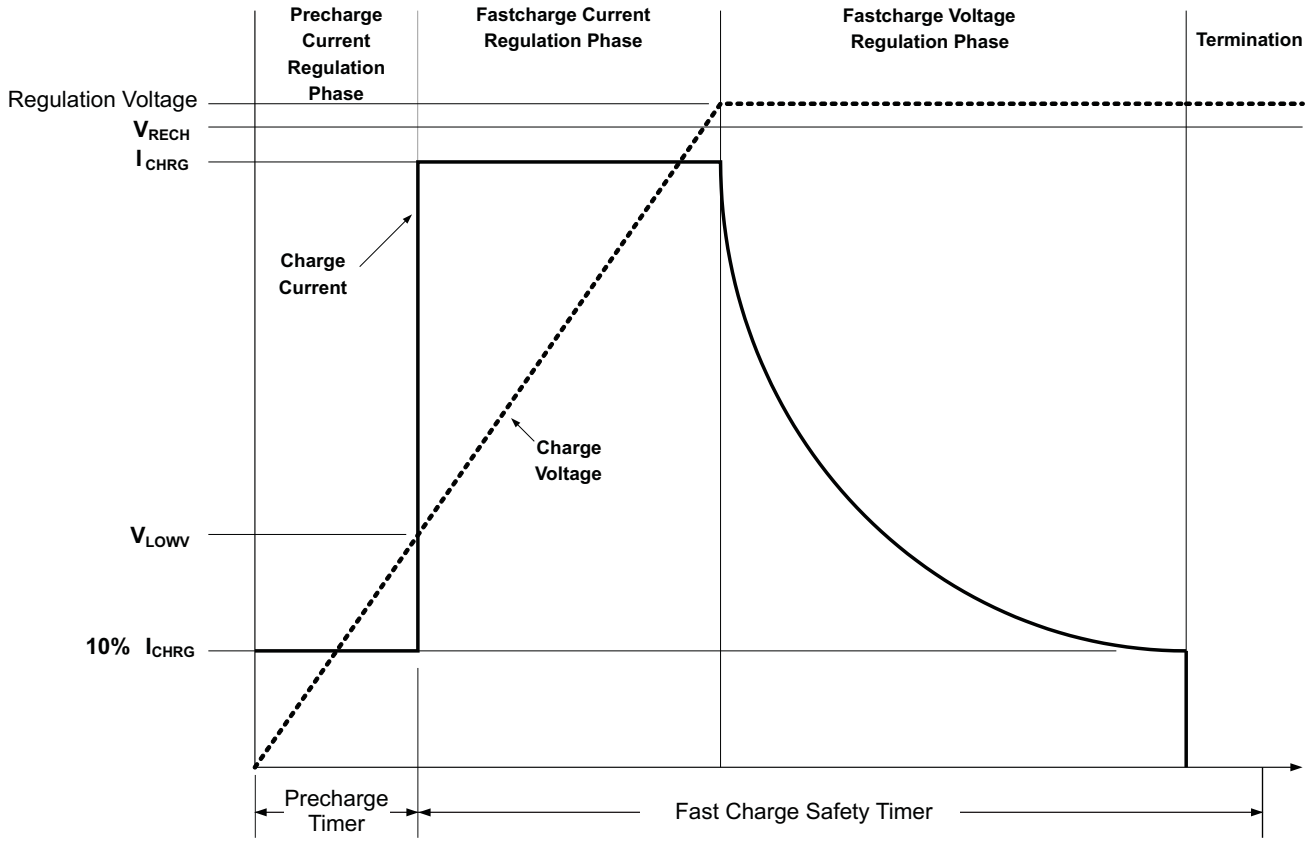



**Figure 13. Typical Charging Profile**

### 9.3.1 Battery Voltage Regulation

The bq24133 offers a high accuracy voltage regulator on for the charging voltage. The bq24133 uses CELL pin to select number of cells with a fixed 4.2 V/cell. Connecting CELL to AGND sets 1-cell output, floating CELL pin sets 2-cell output, and connecting to VREF sets 3-cell output.

**Table 2. bq24133 CELL Pin Settings**

| CELL PIN | VOLTAGE REGULATION |
|---|---|
| AGND | 4.2 V |
| Floating | 8.4 V |
| VREF | 12.6 V |

### 9.3.2 Battery Current Regulation

The ISET input sets the maximum charging current. Battery current is sensed by current sensing resistor RSR connected between SRP and SRN. The equation for charge current is:

$$I_{CHARGE} = \frac{V_{ISET}}{20 \times R_{SR}} \quad (1)$$

The valid input voltage range of ISET is up to 0.5 V. With 10-mΩ sense resistor, the maximum output current is 2.5 A.

The charger is disabled when ISET pin voltage is below 40 mV and is enabled when the ISET pin voltage is above 120 mV. For 10-mΩ current sensing resistor, the minimum fast charge current must be higher than 600 mA.

Under high ambient temperature, the charge current will fold back to keep IC temperature not exceeding 120°C.

### 9.3.3 Battery Precharge Current Regulation

On power up, if the battery voltage is below the $V_{LOWV}$ threshold, the bq24133 applies the precharge current to the battery. This precharge feature is intended to revive deeply discharged cells. If the $V_{LOWV}$ threshold is not reached within 30 minutes of initiating precharge, the charger turns off and a fault is indicated on the status pin.

For bq24133, the precharge current is set as 10% of the fast charge rate set by ISET voltage.

$$I_{PRECHARGE} = \frac{V_{ISET}}{200 \times R_{SR}} \quad (2)$$

### 9.3.4 Input Current Regulation

The total input current from an AC adapter or other DC sources is a function of the system supply current and the battery charging current. System current normally fluctuated as portions of the systems are powered up or down. Without Dynamic Power Management (DPM), the source must be able to supply the maximum system current and the maximum available charger input current simultaneously. By using DPM, the input current regulator reduces the charging current when the summation of system power and charge power exceeds the maximum input power. Therefore, the current capability of the AC adapter can be lowered, reducing system cost.

Input current is set by the voltage on ACSET pin using the following equation:

$$I_{DPM} = \frac{V_{ACSET}}{20 \times R_{AC}} \quad (3)$$

The ACP and ACN pins are used to sense across RAC with default value of 20 mΩ. However, resistors of other values can also be used. A larger sense resistor will give a larger sense voltage and higher regulation accuracy, at the expense of higher conduction loss.

### 9.3.5 Charge Termination, Recharge, And Safety Timers

The charger monitors the charging current during the voltage regulation phase. Termination is detected when the SRN voltage is higher than recharge threshold and the charge current is less than the termination current threshold, as calculated below:

$$I_{TERM} = \frac{V_{ISET}}{200 \times R_{SR}}$$

where

- $V_{ISET}$ is the voltage on the ISET pin.
- $R_{SR}$ is the sense resistor. (4)

There is a 25-ms deglitch time during transition between fast charge and precharge.

As a safety backup, the charger also provides an internal fixed 30 minutes precharge safety timer and a programmable fast charge timer. The fast charge time is programmed by the capacitor connected between the TTC pin and AGND, and is given by the formula:

$$t_{TTC} = C_{TTC} \times K_{TTC}$$

where

- $C_{TTC}$ is the capacitor connected to TTC.
- $K_{TTC}$ is the constant multiplier. (5)

A new charge cycle is initiated when one of the following conditions occurs:

- The battery voltage falls below the recharge threshold
- A power-on-reset (POR) event occurs
- ISET pin toggled below 40 mV (disable charge) and above 120 mV (enable charge)

Pull the TTC pin to AGND to disable both termination and fast charge safety timer (reset timer). Pull the TTC pin to VREF to disable the safety timer, but allow charge termination.

### 9.3.6 Power Up

The charge uses a SLEEP comparator to determine the source of power on the AVCC pin because AVCC can be supplied either from the battery or the adapter. With the adapter source present, if the AVCC voltage is greater than the SRN voltage, the charger exits SLEEP mode. If all conditions are met for charging, the charger then starts charge the battery (see *Enable and Disable Charging*). If SRN voltage is greater than AVCC, the charger enters low quiescent current SLEEP mode to minimize current drain from the battery. During SLEEP mode, the VREF output turns off and the STAT pin goes to high impedance.

If AVCC is below the UVLO threshold, the device is disabled.

### 9.3.7 Input Undervoltage Lockout (UVLO)

The system must have a minimum AVCC voltage to allow proper operation. This AVCC voltage could come from either input adapter or battery because a conduction path exists from the battery to AVCC through the high-side NMOS body diode. When AVCC is below the UVLO threshold, all circuits on the IC are disabled.

### 9.3.8 Input Overvoltage/Undervoltage Protection

ACOV provides protection to prevent system damage due to high input voltage. In bq24133, once the voltage on OVPSET is above the 1.6-V ACOV threshold or below the 0.5-V ACUV threshold, charge is disabled and input MOSFETs turn off. The bq24133 provides flexibility to set the input qualification threshold.

### 9.3.9 Enable and Disable Charging

The following conditions have to be valid before charging is enabled:

- ISET pin above 120 mV.
- Device is not in UVLO mode (that is, $V_{AVCC} > V_{UVLO}$).
- Device is not in SLEEP mode (that is, $V_{AVCC} > V_{SRN}$).
- OVPSET voltage is from 0.5 V to 1.6 V to qualify the adapter.
- 1.5-s delay is complete after initial power up.
- REGN LDO and VREF LDO voltages are at correct levels.
- Thermal Shut down (TSHUT) is not valid.
- TS fault is not detected.
- ACFET turns on (see *System Power Selector* for details).

One of the following conditions stops ongoing charging:

- ISET pin voltage is below 40 mV.
- Device is in UVLO mode.
- Adapter is removed, causing the device to enter SLEEP mode.
- OVPSET voltage indicates the adapter is not valid.
- REGN or VREF LDO voltage is overloaded.
- TSHUT temperature threshold is reached.
- TS voltage goes out of range, indicating the battery temperature is too hot or too cold.
- ACFET turns off.
- TTC timer expires or precharge timer expires.

### 9.3.10 System Power Selector

The IC automatically switches adapter or battery power to the system load. The battery is connected to the system by default during power up or during SLEEP mode. When the adapter plugs in and the voltage is above the battery voltage, the IC exits SLEEP mode. The battery is disconnected from the system and the adapter is connected to the system after exiting SLEEP. An automatic break-before-make logic prevents shoot-through currents when the selectors switch.

The ACDRV is used to drive a pair of back-to-back N-channel power MOSFETs between adapter and ACP with sources connected together to CMSRC. The N-channel FET with the drain connected to the ACP (Q2, RBFET) provides reverse battery discharge protection, and minimizes system power dissipation with its low-$RDS_{ON}$. The other N-channel FET with drain connected to adapter input (Q1, ACFET) separates battery from adapter, and provides a limited dI/dt when connecting the adapter to the system by controlling the FET turnon time. The /BATDRV controls a P-channel power MOSFET (Q3, BATFET) placed between battery and system with drain connected to battery.

Before the adapter is detected, the ACDRV is pulled to CMSRC to keep ACFET off, disconnecting the adapter from system. /BATDRV stays at ACN - 6 V (clamp to ground) to connect battery to system if all the following conditions are valid:

- $V_{AVCC} > V_{UVLO}$ (battery supplies AVCC)
- $V_{ACN} < V_{SRN} + 200$ mV

After the device comes out of SLEEP mode, the system begins to switch from battery to adapter. The AVCC voltage has to be 300 mV above SRN to enable the transition. The break-before-make logic keeps both ACFET and BATFET off for 10 µs before ACFET turns on. This prevents shoot-through current or any large discharging current from going into the battery. The /BATDRV is pulled up to ACN and the ACDRV pin is set to CMSRC + 6 V by an internal charge pump to turn on N-channel ACFET, connecting the adapter to the system if all the following conditions are valid:

- $V_{ACUV} < V_{OVPSET} < V_{ACOV}$
- $V_{AVCC} > V_{SRN} + 300$ mV

When the adapter is removed, the IC turns off ACFET and enters SLEEP mode.

BATFET keeps off until the system drops close to SRN. The $\overline{\text{BATDRV}}$ pin is driven to ACN - 6V by an internal regulator to turn on P-channel BATFET, connecting the battery to the system.

Asymmetrical gate drive provides fast turnoff and slow turnon of the ACFET and BATFET to help the break-before-make logic and to allow a soft-start at turnon of both MOSFETs. The delay time can be further increased, by putting a capacitor from gate to source of the power MOSFETs.

### 9.3.11 Converter Operation

The bq24133 employs a 1.6-MHz constant frequency step-down switching regulator. The fixed-frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current, and temperature, simplifying output filter design and keeping it out of the audible noise region.

A type III compensation network allows using ceramic capacitors at the output of the converter. An internal saw-tooth ramp is compared to the internal error control signal to vary the duty cycle of the converter. The ramp height is proportional to the AVCC voltage to cancel out any loop gain variation due to a change in input voltage, and simplifies the loop compensation. Internal gate drive logic allows achieving 97% duty cycle before pulse skipping starts.

### 9.3.12 Automatic Internal Soft-Start Charger Current

The charger automatically soft-starts the charger regulation current every time the charger goes into fast charge to ensure there is no overshoot or stress on the output capacitors or the power converter. The soft-start consists of stepping up the charge regulation current into eight evenly divided steps up to the programmed charge current. Each step lasts around 1.6 ms, for a typical rise time of 12.8 ms. No external components are needed for this function.

### 9.3.13 Charge Overcurrent Protection

The charger monitors top side MOSFET current by high-side sense FET. When peak current exceeds MOSFET limit, the charger turns off the top side MOSFET and keeps it off until the next cycle. The charger has a secondary cycle-to-cycle overcurrent protection. The charger monitors the charge current, and prevents the current from exceeding 160% of the programmed charge current. The high-side gate drive turns off when either overcurrent condition is detected, and automatically resumes when the current falls below the overcurrent threshold.

### 9.3.14 Charge Undercurrent Protection

After the recharge, if the SRP-SRN voltage decreases below 5 mV, then the low-side FET is turned off for the rest of the switching cycle. During discontinuous conduction mode (DCM), the low-side FET turns on for a short period of time when the boostrap capacitor voltage drops below 4 V to provide refresh charge for the capacitor. This is important to prevent negative inductor current from causing any boost effect in which the input voltage increases as power is transferred from the battery to the input capacitors. This can lead to an overvoltage on the AVCC node and potentially cause damage to the system.

### 9.3.15 Battery Detection

For applications with removable battery packs, IC provides a battery absent detection scheme to reliably detect insertion or removal of battery packs. The battery detection routine runs on power up, or if battery voltage falls below recharge threshold voltage due to removing a battery or discharging a battery.

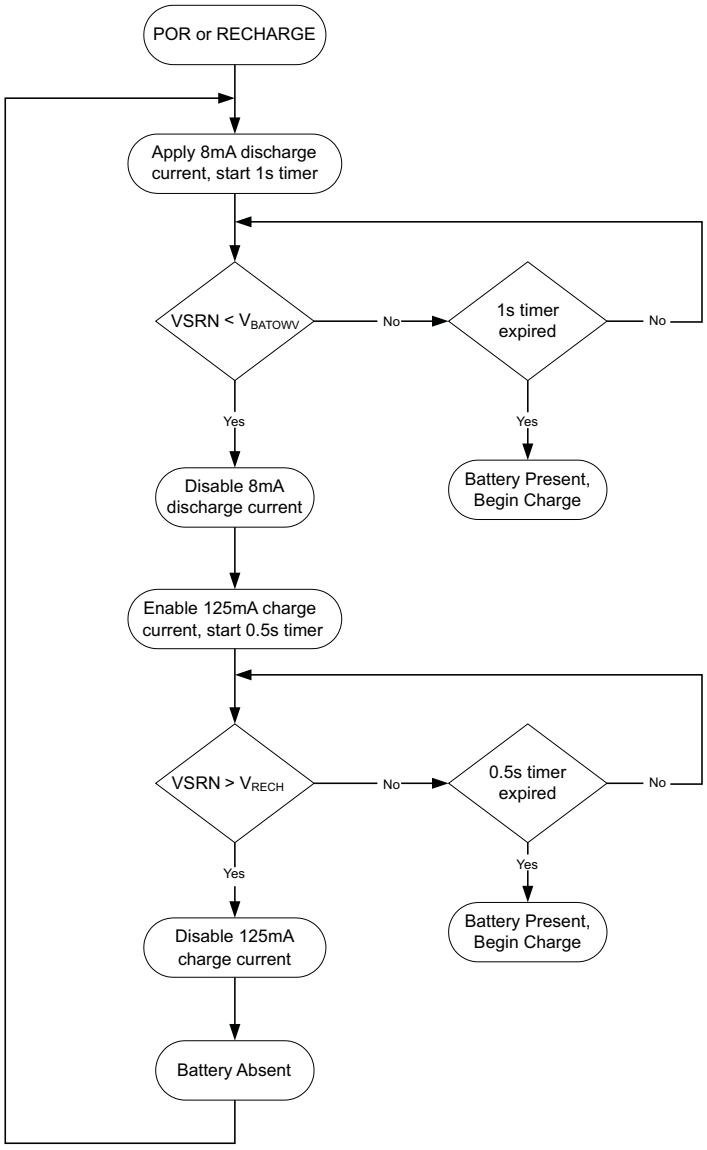



**Figure 14. Battery Detection Flow Chart**

Once the device has powered up, an 8-mA discharge current is applied to the SRN terminal. If the battery voltage falls below the LOWV threshold within 1 second, the discharge source is turned off, and the charger is turned on at low charge current (125 mA). If the battery voltage gets up above the recharge threshold within 500 ms, there is no battery present and the cycle restarts. If either the 500 ms or 1 second timer times out before the respective thresholds are hit, a battery is detected and a charge cycle is initiated.

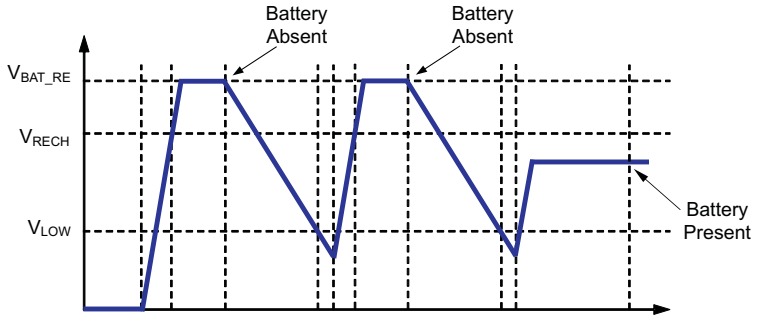



**Figure 15. Battery Detect Timing Diagram**

Ensure that the total output capacitance at the battery node is not so large that the discharge current source cannot pull the voltage below the LOWV threshold during the 1 second discharge time. The maximum output capacitances can be calculated according to the following equations:

$$C_{MAX} = \frac{I_{DISCH} \times t_{DISCH}}{(4.1\ V - 2.9\ V) \times \text{Number of cells}} \quad (6)$$

where

- $C_{MAX}$ is the maximum output capacitance.
- $I_{DISCH}$ is the discharge current.
- $t_{DISCH}$ is the discharge time.

#### *9.3.15.1 Example*

For a 3-cell Li+ charger, $I_{DISCH}$ = 8 mA, $t_{DISCH}$ = 1 second.

$$C_{MAX} = \frac{8\ mA \times 1\ sec}{1.2\ V \times 3} = 2.2\ mF \quad (7)$$

Based on these calculations, no more than 2200 µF should be allowed on the battery node for proper operation of the battery detection circuit.

### 9.3.16 Battery Short Protection

When SRN pin voltage is lower than 2 V, it is considered as battery short condition during charging period. The charger will shut down immediately for 1 ms, then soft start back to the charging current the same as precharge current. This prevents high current may build in output inductor and cause inductor saturation when battery terminal is shorted during charging. The converter works in nonsynchronous mode during battery short.

### 9.3.17 Battery Overvoltage Protection

The converter will not allow the high-side FET to turn on until the battery voltage goes below 102% of the regulation voltage. This allows 1-cycle response to an overvoltage condition – such as occurs when the load is removed or the battery is disconnected. A total 6 mA current sink from SRP/SRN to AGND allows discharging the stored output inductor energy that is transferred to the output capacitors. If battery overvoltage condition lasts for more than 30 ms, charge is disabled.

### 9.3.18 Temperature Qualification

The controller continuously monitors battery temperature by measuring the voltage between the TS pin and AGND. A negative temperature coefficient thermistor (NTC) and an external voltage divider typically develop this voltage. The controller compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the battery temperature must be within the $V_{LTF}$ to $V_{HTF}$ thresholds. If battery temperature is outside of this range, the controller suspends charge and waits until the battery temperature is within the $V_{LTF}$ to $V_{HTF}$ range. During the charge cycle the battery temperature must be within the $V_{LTF}$ to $V_{TCO}$ thresholds. If battery temperature is outside of this range, the controller suspends charge and waits until the battery temperature is within the $V_{LTF}$ to $V_{HTF}$ range. The controller suspends charge by turning off the PWM charge MOSFETs. Figure 16 summarizes the operation.

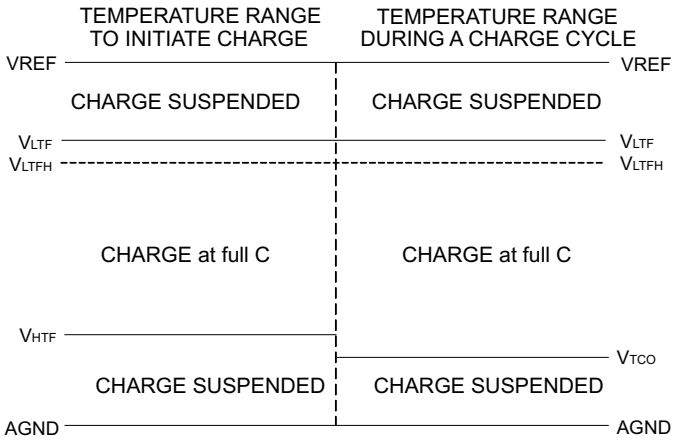



**Figure 16. TS Pin, Thermistor Sense Thresholds**

Assuming a 103AT NTC thermistor on the battery pack as shown in Figure 17, the values of RT1 and RT2 can be determined by using Equation 8 and Equation 9:

$$RT2 = \frac{V_{VREF} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{V_{LTF}} - \frac{1}{V_{TCO}}\right)}{RTH_{HOT} \times \left(\frac{V_{VREF}}{V_{TCO}} - 1\right) - RTH_{COLD} \times \left(\frac{V_{VREF}}{V_{LTF}} - 1\right)} \quad (8)$$

$$RT1 = \frac{\frac{V_{VREF}}{V_{LTF}} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}} \quad (9)$$

Select 0°C to 45°C range for Li-ion or Li-polymer battery,

$RTH_{COLD}$ = 27.28 kΩ
$RTH_{HOT}$ = 4.911 kΩ
RT1 = 5.23 kΩ
RT2 = 30.1 kΩ

After select closest standard resistor value, by calculating the thermistor resistance at temperature threshold, the final temperature range can be gotten from thermistor data sheet temperature resistance table.

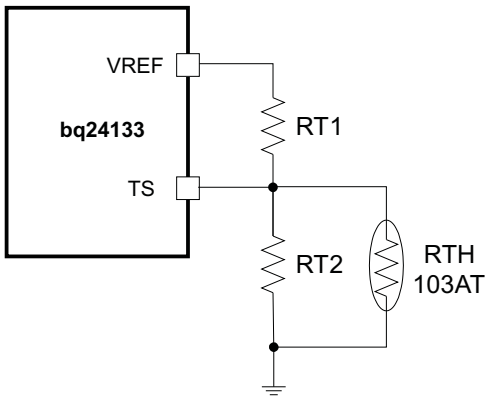



**Figure 17. TS Resistor Network**

### 9.3.19 MOSFET Short Circuit and Inductor Short Circuit Protection

The IC has a short circuit protection feature. Its cycle-by-cycle current monitoring feature is achieved through monitoring the voltage drop across Rdson of the MOSFETs. The charger will be latched off, but the ACFET keep on to power the system. The only way to reset the charger from latch-off status is remove adapter then plug adapter in again. Meanwhile, STAT is blinking to report the fault condition.

### 9.3.20 Thermal Regulation and Shutdown Protection

The VQFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junctions temperatures low. The internal thermal regulation loop will fold back the charge current to keep the junction temperature from exceeding 120°C. As added level of protection, the charger converter turns off and self-protects whenever the junction temperature exceeds the TSHUT threshold of 150°C. The charger stays off until the junction temperature falls below 130°C.

### 9.3.21 Timer Fault Recovery

The IC provides a recovery method to deal with timer fault conditions. The following summarizes this method:

Condition 1: The battery voltage is above the recharge threshold and a time-out fault occurs.

Recovery Method: The timer fault will clear when the battery voltage falls below the recharge threshold, and battery detection will begin. A POR or taking ISET below 40 mV will also clear the fault.

Condition 2: The battery voltage is below the recharge threshold and a time-out fault occurs.

Recovery Method: Under this scenario, the IC applies the fault current to the battery. This small current is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, the IC disabled the fault current and executes the recovery method described in Condition 1. A POR or taking ISET below 40 mV will also clear the fault.

### 9.3.22 Charge Status Outputs

The open-drain STAT outputs indicate various charger operations as listed in Table 3. These status pins can be used to drive LEDs or communicate with the host processor. OFF indicates that the open-drain transistor is turned off.

**Table 3. STAT Pin Definition**

| CHARGE STATE | STAT |
|---|---|
| Charge in progress (including recharging) | ON |
| Charge complete, Sleep mode, Charge disabled | OFF |
| Charge suspend, Input overvoltage, Battery overvoltage, timer fault, , battery absent | BLINK |

## 9.4 Device Functional Modes

The bq24133 is a stand-alone switched-mode charger with power path selector. The device can operate from either a qualified adapter or supply system power from the battery. Dynamic Power Management (DPM) mode allows for a smaller adapter to be used effectively in systems with more dynamic system loads.

The bq2433 device provides power path selector gate driver ACDRV/CMSRC on input NMOS pair ACFET (Q1) and RBFET (Q2), and BATDRV on a battery PMOS device (Q3). When the qualified adapter is present, the system is directly connected to the adapter. Otherwise, the system is connected to the battery. In addition, the power path prevents battery from boosting back to the input.

The bq24133 features DPM to reduce the charge current when the input power limit is reached to avoid overloading the adapter. A highly accurate current-sense amplifier enables precise measurement of input current from adapter to monitor overall system power.

The total input current from an AC adapter or other DC sources is a function of the system supply current and the battery charging current. System current normally fluctuated as portions of the systems are powered up or down. Without DPM, the source must be able to supply the maximum system current and the maximum available charger input current simultaneously. By using DPM, the input current regulator reduces the charging current when the summation of system power and charge power exceeds the maximum input power. Therefore, the current capability of the AC adapter can be lowered, thus reducing system cost.

Although the bq24133 is a stand-alone charger, external control circuitry can effectively be used to change pin settings such as ISET, ACSET, and enable Battery Learn mode to accommodated for dynamic charging conditions.

# 10 Application and Implementation

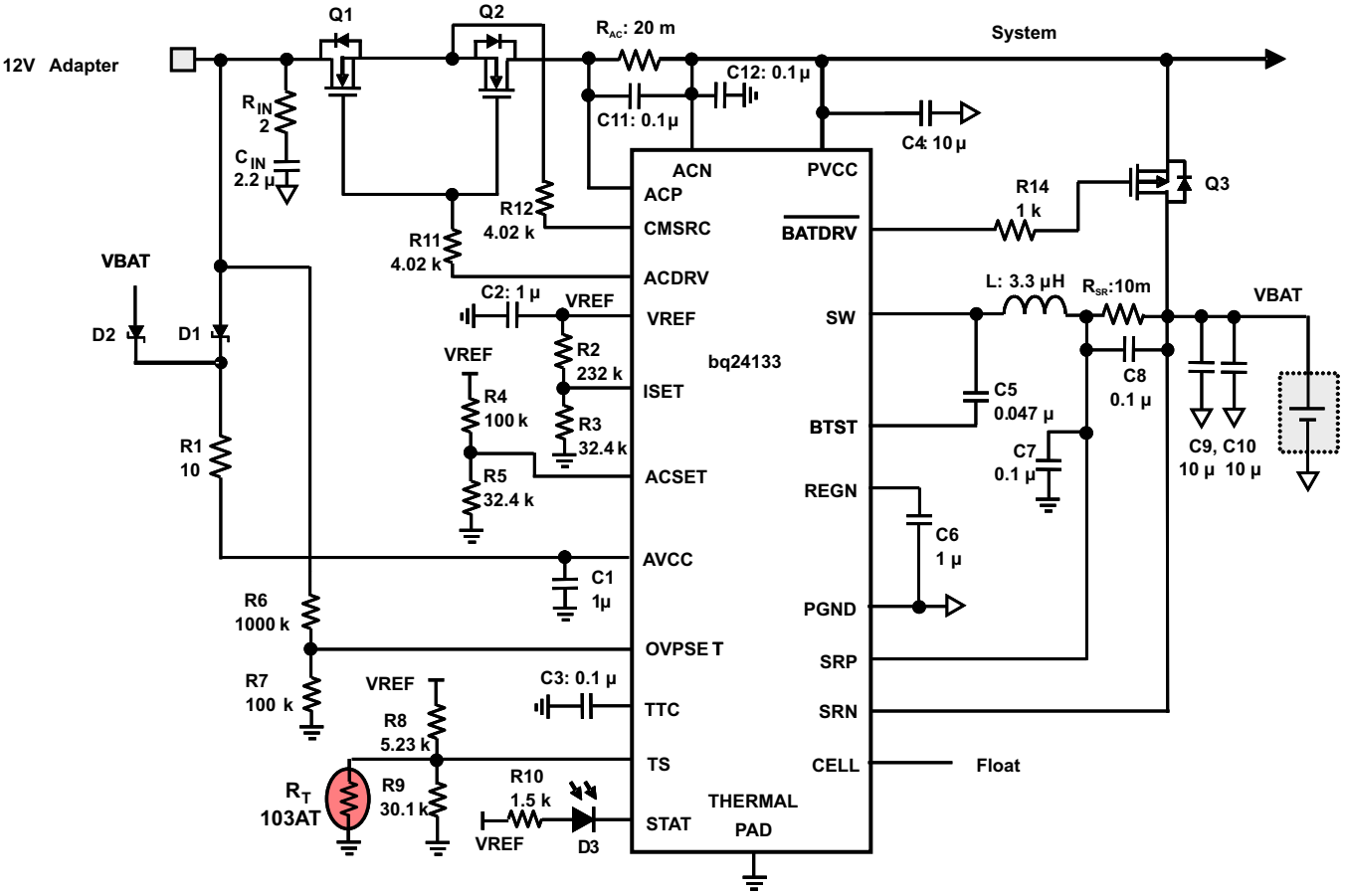
**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

A typical application consists of a bq24133 with power path management and from 1- to 3-cell series Li-ion or Li-polymer battery in a wide variety of cost sensitive portable applications with charge current requirements up to 2.5 A. The bq24133 provides a fixed 4.2 V/cell (programmable through CELL pin) with high accuracy and low leakage.

## 10.2 Typical Application




12-V input, 2-cell battery 8.4 V, 2-A charge current, 0.2-A precharge/termination current, 2-A DPM current, 18-V input OVP, 0 – 45°C TS

**Figure 18. Typical Application Schematic**

## Typical Application (continued)

### 10.2.1 Design Requirements

For this design example, use the parameters listed in Table 4 as the input parameters.

**Table 4. Design Parameters**

| PARAMETER | EXAMPLE VALUE |
|---|---|
| Input Voltage Range | 4.5 V - 17 V |
| Input DPM Current Limit | 600 mA min |
| Battery Voltage | 13.5 V max |
| Charge Current | 2.5 A max |

### 10.2.2 Detailed Design Procedure

#### *10.2.2.1 Inductor Selection*

The bq24133 has a 1600-kHz switching frequency to allow the use of small inductor and capacitor values. Inductor saturation current should be higher than the charging current ($I_{CHG}$) plus half the ripple current ($I_{RIPPLE}$):

$$I_{SAT} \geq I_{CHG} + (1/2) I_{RIPPLE} \tag{10}$$

Inductor ripple current depends on input voltage ($V_{IN}$), duty cycle ($D = V_{OUT}/V_{IN}$), switching frequency (fs), and inductance (L):

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1-D)}{fs \times L} \tag{11}$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. Usually inductor ripple is designed in the range of 20% to 40% of the maximum charging current as a trade-off between inductor size and efficiency for a practical design.

#### *10.2.2.2 Input Capacitor*

The input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current $I_{CIN}$ occurs where the duty cycle is closest to 50% and can be estimated by the following equation:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \tag{12}$$

A low ESR ceramic capacitor such as X7R or X5R is preferred for the input decoupling capacitor and should be placed as close as possible to the drain of the high-side MOSFET and source of the low-side MOSFET. The voltage rating of the capacitor must be higher than the normal input voltage level. A 25-V rating or higher capacitor is preferred for a 15-V input voltage. A 20-µF capacitance is suggested for a typical 2.5-A charging current.

#### *10.2.2.3 Output Capacitor*

The output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current $I_{COUT}$ is given as:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \tag{13}$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LCfs^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{14}$$

At certain input/output voltages and switching frequencies, the voltage ripple can be reduced by increasing the output filter LC.

The bq24133 has an internal loop compensator. To achieve good loop stability, the resonant frequency of the output inductor and output capacitor should be designed from 15 kHz to 25 kHz. The preferred ceramic capacitor has a 25-V or higher rating, X7R or X5R.

#### *10.2.2.4 Input Filter Design*

During adapter hot plug-in, the parasitic inductance and the input capacitor from the adapter cable form a second-order system. The voltage spike at the AVCC pin may be beyond the IC maximum voltage rating and damage the IC. The input filter must be carefully designed and tested to prevent an overvoltage event on the AVCC pin.

There are several methods to damping or limiting the overvoltage spike during adapter hot plug-in. An electrolytic capacitor with high ESR as an input capacitor can damp the overvoltage spike well below the IC maximum pin voltage rating. A high-current capability TVS Zener diode can also limit the overvoltage level to an IC safe level. However, these two solutions may not be lowest cost or smallest size.

A cost-effective and small-size solution is shown in Figure 19. R1 and C1 are composed of a damping RC network to damp the hot plug-in oscillation. As a result, the overvoltage spike is limited to a safe level. D1 is used for reverse voltage protection for the AVCC pin. C2 is the AVCC pin decoupling capacitor and it should be placed as close as possible to the AVCC pin. R2 and C2 form a damping RC network to further protect the IC from high dv/dt and high voltage spike. The C2 value should be less than the C1 value so R1 can dominant the equivalent ESR value to get enough damping effect for hot plug-in. R1 and R2 must be sized enough to handle in-rush current power loss according to the resistor manufacturer's data sheet. The filter component values always need to be verified with a real application and minor adjustments may be needed to fit in the real application circuit.

If the input is 5 V (USB host or USB adapter), then D1 can be saved. R2 has to be 5 Ω or higher to limit the current if the input is reversely inserted.

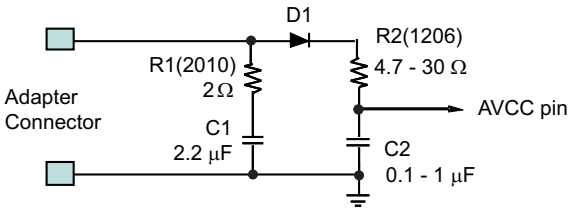



**Figure 19. Input Filter**

#### *10.2.2.5 Input ACFET and RBFET Selection*

N-type MOSFETs are used as input ACFET(Q1) and RBFET(Q2) for better cost-effective and small-size solution, as shown in Figure 22. Normally, there is a total capacitance of 50 µH connected at PVCC node: 10-µF capacitor for buck converter of bq24133 and 40-µF capacitor for system side. There is a surge current during Q1 turnon period when a valid adapter is inserted. Decreasing the turnon speed of Q1 can limit this surge current in desirable range by selecting a MOSFET with relative bigger $C_{GD}$ and/or $C_{GS}$. If Q1 turns on too fast, we must add external $C_{GD}$ and/or $C_{GS}$. For example, 4.7-nF $C_{GD}$ and 47-nF $C_{GS}$ are adopted on EVM while using NexFET CSD17313 as Q1.

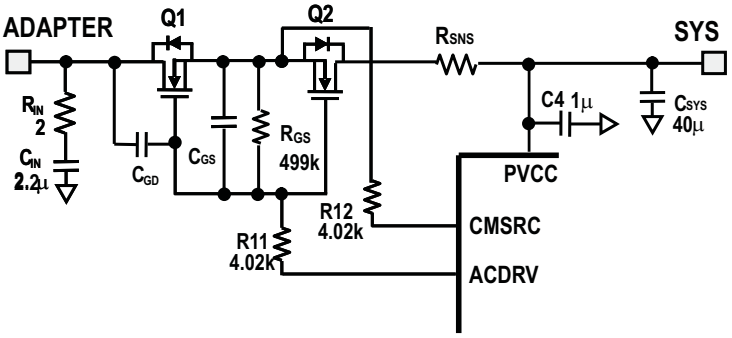



**Figure 20. Input ACFET and RBFET**

#### 10.2.2.6 Inductor, Capacitor, and Sense Resistor Selection Guidelines

The IC provides internal loop compensation. With this scheme, the best stability occurs when the LC resonant frequency, $f_o$, is approximately 15 kHz to 25 kHz for the IC.

$$f_o = \frac{1}{2\pi\sqrt{LC}} \quad (15)$$

Table 5 summarizes typical LC components for various charge currents.

**Table 5. Typical Values as a Function of Charge Current**

| CHARGE CURRENT | 1 A | 2 A |
|---|---|---|
| Output inductor L | 6.8 µH | 3.3 µH |
| Output capacitor C | 10 µF | 20 µF |

### 10.2.3 Application Curve

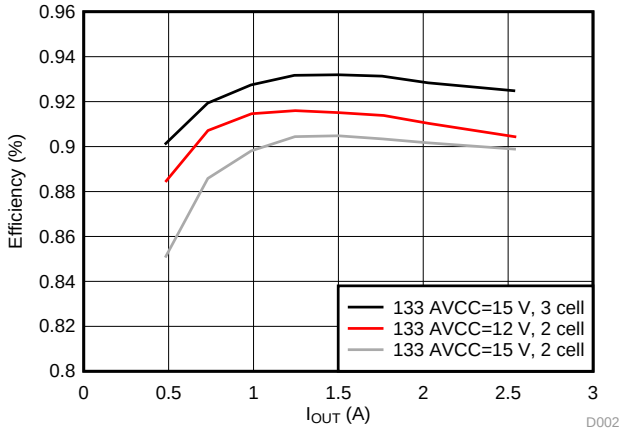
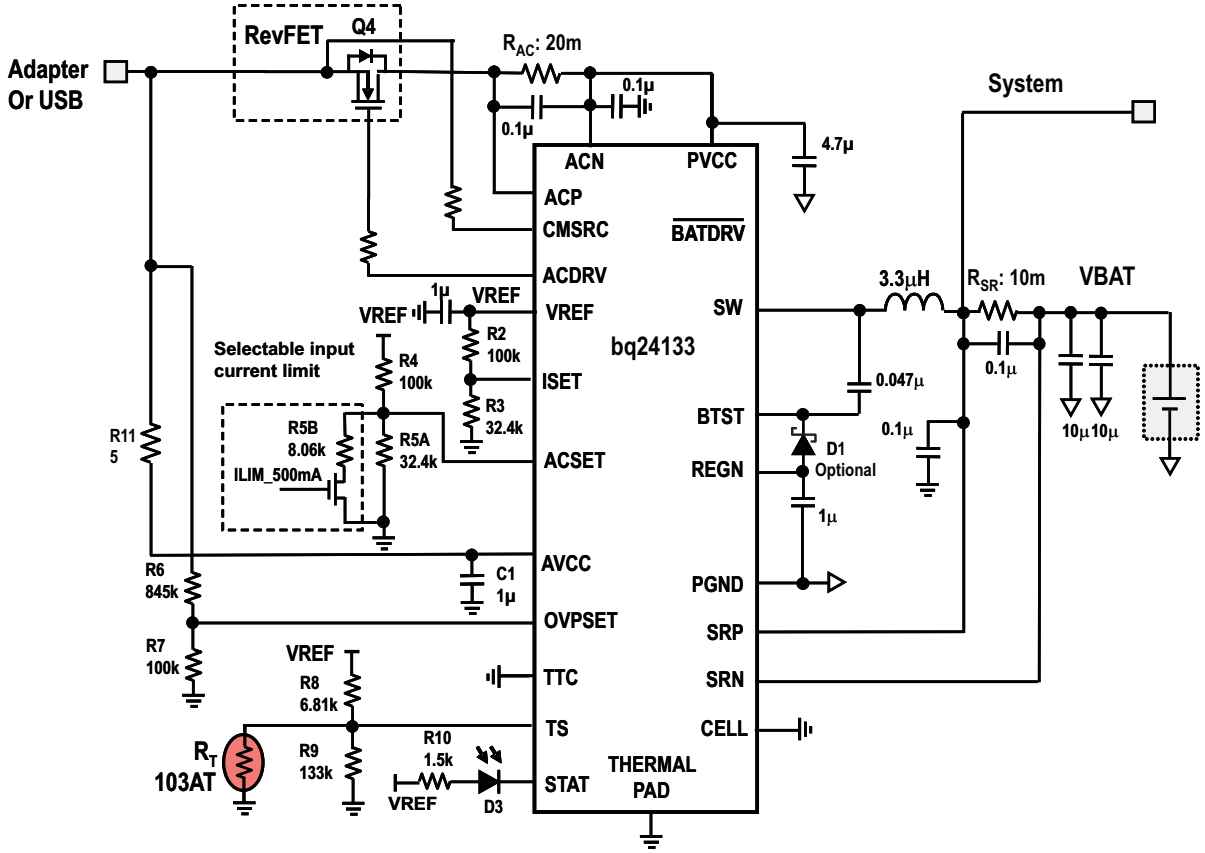



**Figure 21. Efficiency vs Output Current**

## 10.3 System Examples




USB or adapter with input OVP 15 V, up to 2-A charge current, 0.2-A precharge current, 2-A adapter current or 500-mA USB current, 5 – 40°C TS, system connected before sense resistor

**Figure 22. Typical Application Schematic With Single-Cell Unremovable Battery**

# 11 Power Supply Recommendations

In order to provide an output voltage on SYS, the bq24133 require a power supply from 4.5-V to 17-V input with ideally more than 500-mA current rating connected to VBUS; or, a single-cell Li-Ion battery with voltage > VBATUVLO connected to BAT.

# 12 Layout

## 12.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize the high frequency current path loop (see Figure 23) is important to prevent electrical and magnetic field radiation and high-frequency resonant problems. The following is a PCB layout priority list for proper layout. Layout of the PCB according to this specific order is essential.

1. Place the input capacitor as close as possible to the PVCC supply and ground connections and use the shortest copper trace connection. These parts should be placed on the same layer of the PCB instead of on different layers and using vias to make this connection.
2. Place the inductor input terminal as close as possible to the SW terminal. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. The charging current sensing resistor should be placed right next to the inductor output. Route the sense leads connected across the sensing resistor back to the IC in the same layer, close to each other (minimize loop area) and do not route the sense leads through a high-current path (see Figure 24 for Kelvin connection for best current accuracy). Place decoupling capacitor on these traces next to the IC.
4. Place the output capacitor next to the sensing resistor output and ground.
5. Output capacitor ground connections must be tied to the same copper that connects to the input capacitor ground before connecting to system ground.
6. Route analog ground separately from power ground and use a single ground connection to tie charger power ground to charger analog ground. Just beneath the IC use analog ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling. Use the thermal pad as a single ground connection point to connect analog ground and power ground together, or use a 0-Ω resistor to tie analog ground to power ground. A star-connection under the thermal pad is highly recommended.
7. It is critical to solder the exposed thermal pad on the backside of the IC package to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. Decoupling capacitors must be placed next to the IC pins and make trace connection as short as possible.
9. The number and physical size of the vias must be enough for a given current path.

## 12.2 Layout Examples

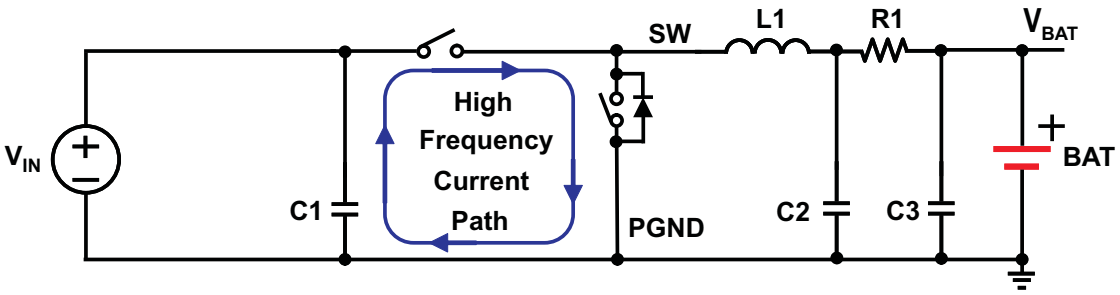



**Figure 23. High-Frequency Current Path**

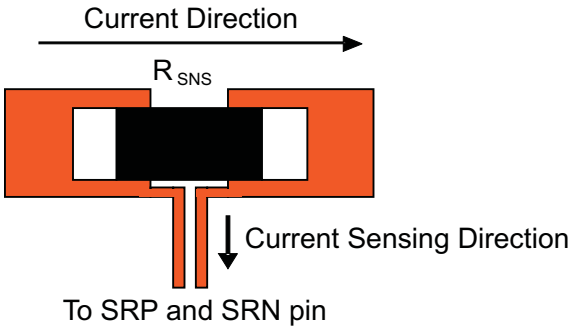



**Figure 24. Sensing Resistor PCB Layout**

# 13 Device and Documentation Support

## 13.1 Trademarks

All trademarks are the property of their respective owners.

## 13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ24133RGYR | ACTIVE | VQFN | RGY | 24 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BQ24133 | Samples |
| BQ24133RGYT | ACTIVE | VQFN | RGY | 24 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | BQ24133 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

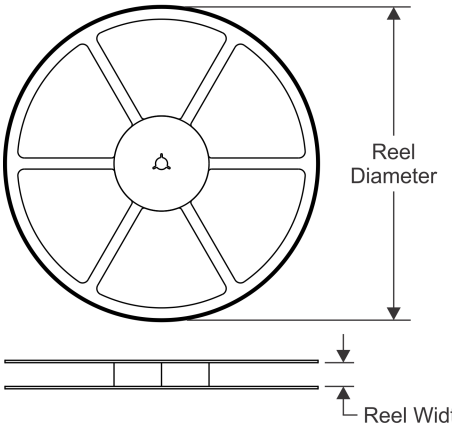
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

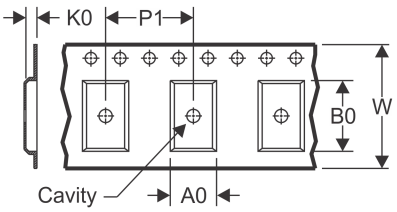
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

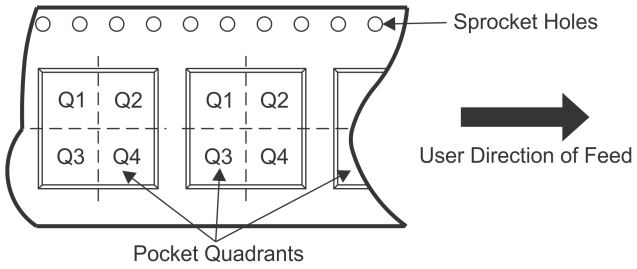



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

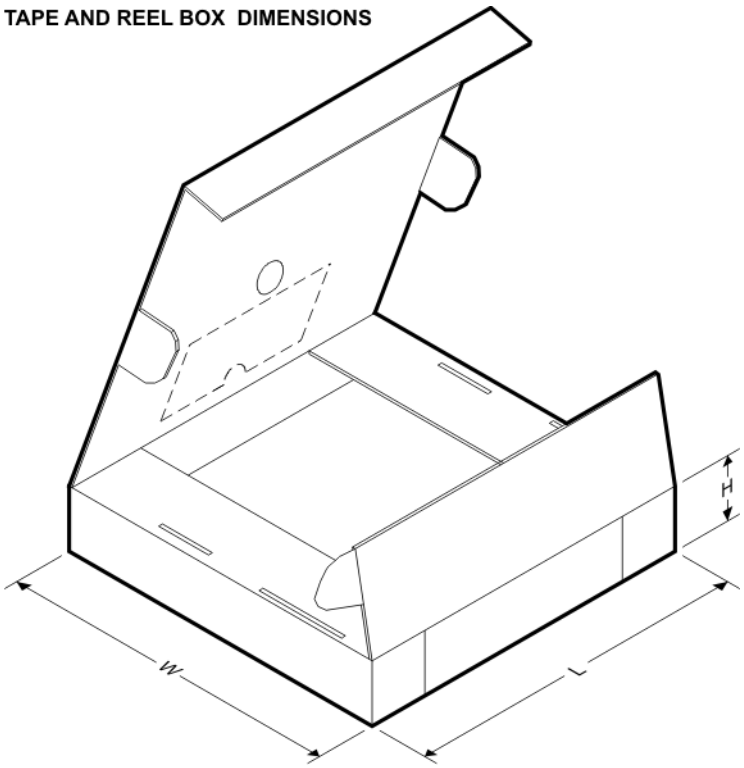
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ24133RGYR | VQFN | RGY | 24 | 3000 | 330.0 | 12.4 | 3.8 | 5.8 | 1.2 | 8.0 | 12.0 | Q1 |
| BQ24133RGYT | VQFN | RGY | 24 | 250 | 180.0 | 12.4 | 3.8 | 5.8 | 1.2 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

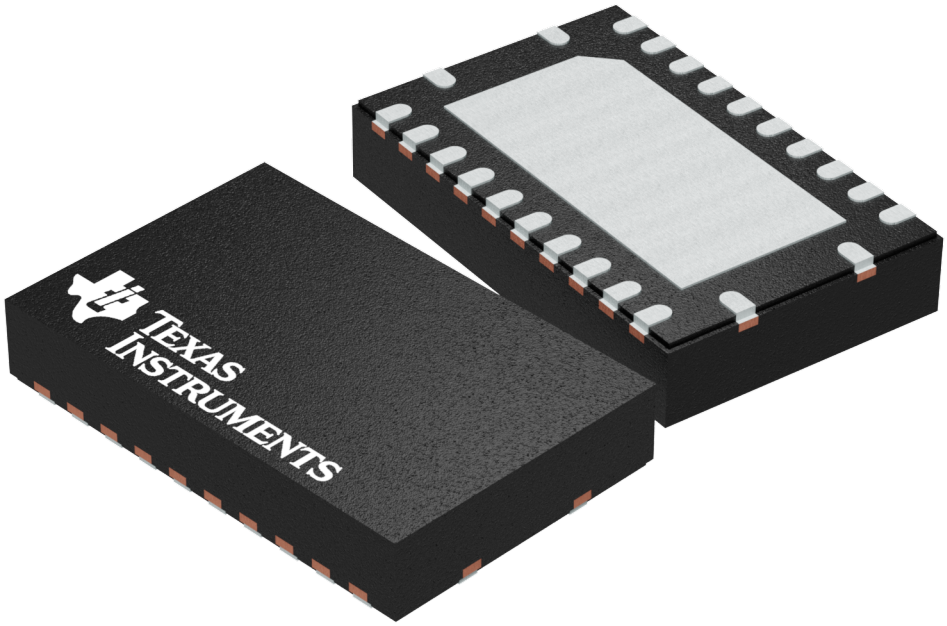
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| BQ24133RGYR | VQFN | RGY | 24 | 3000 | 367.0 | 367.0 | 35.0 |
| BQ24133RGYT | VQFN | RGY | 24 | 250 | 210.0 | 185.0 | 35.0 |

# RGY 24

# VQFN - 1 mm max height

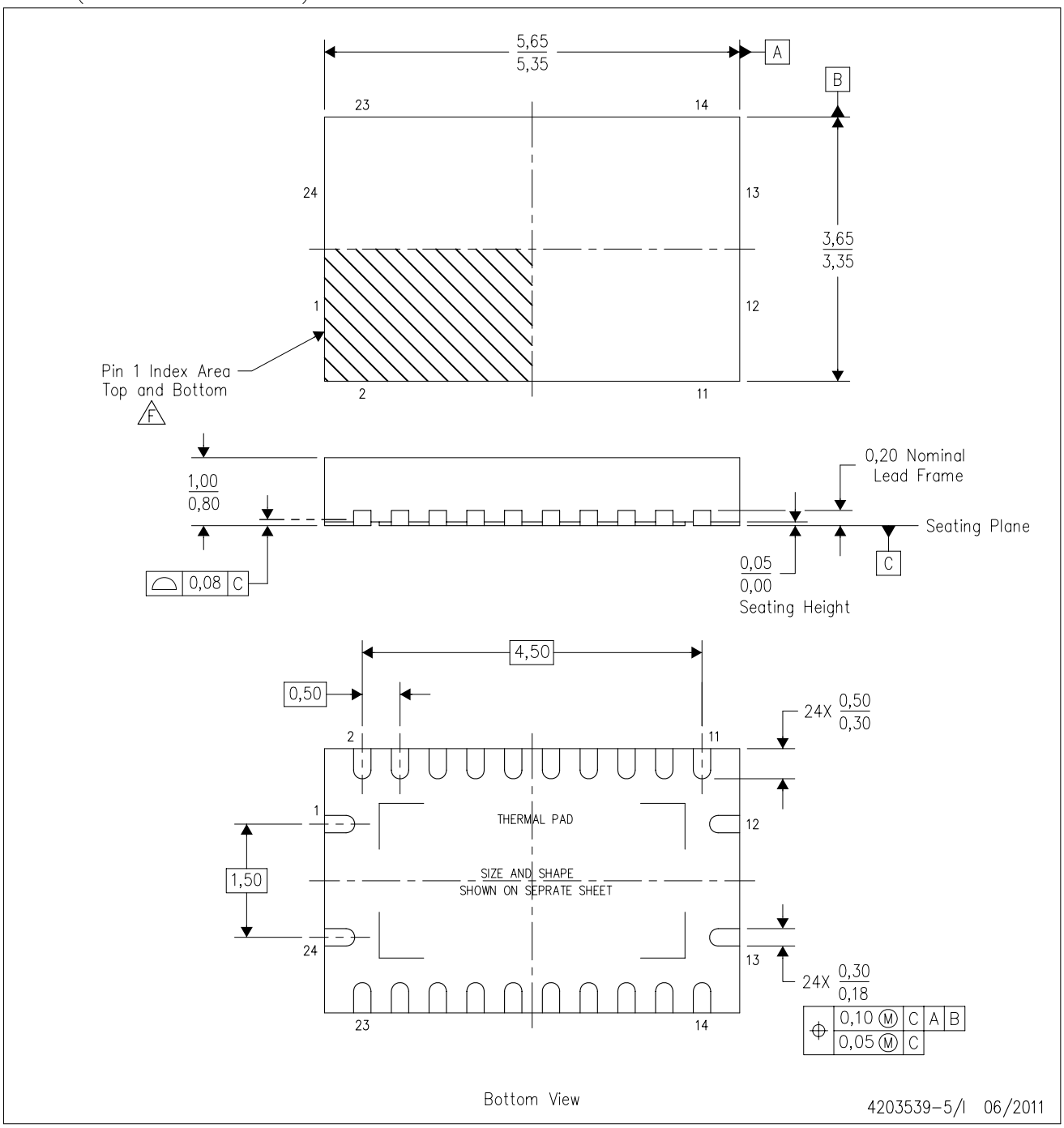
**5.5 x 3.5 mm, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGY (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

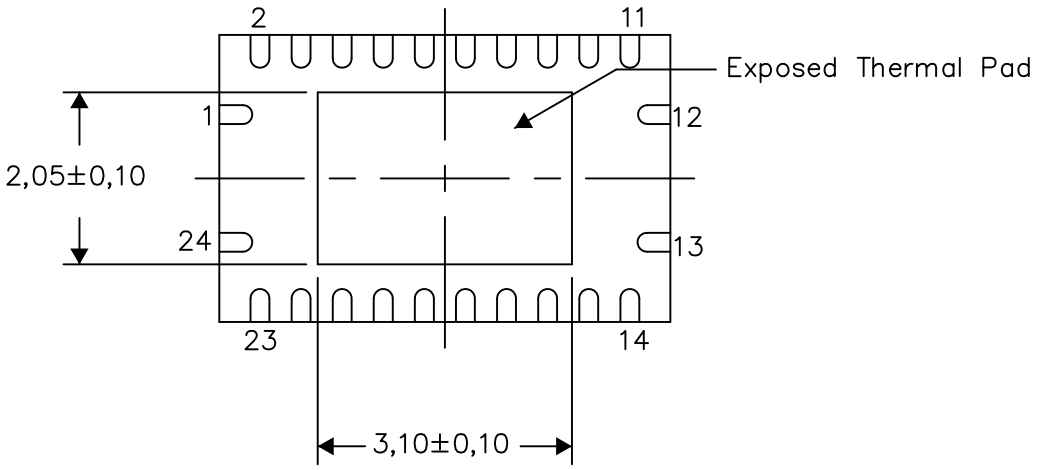
RGY (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



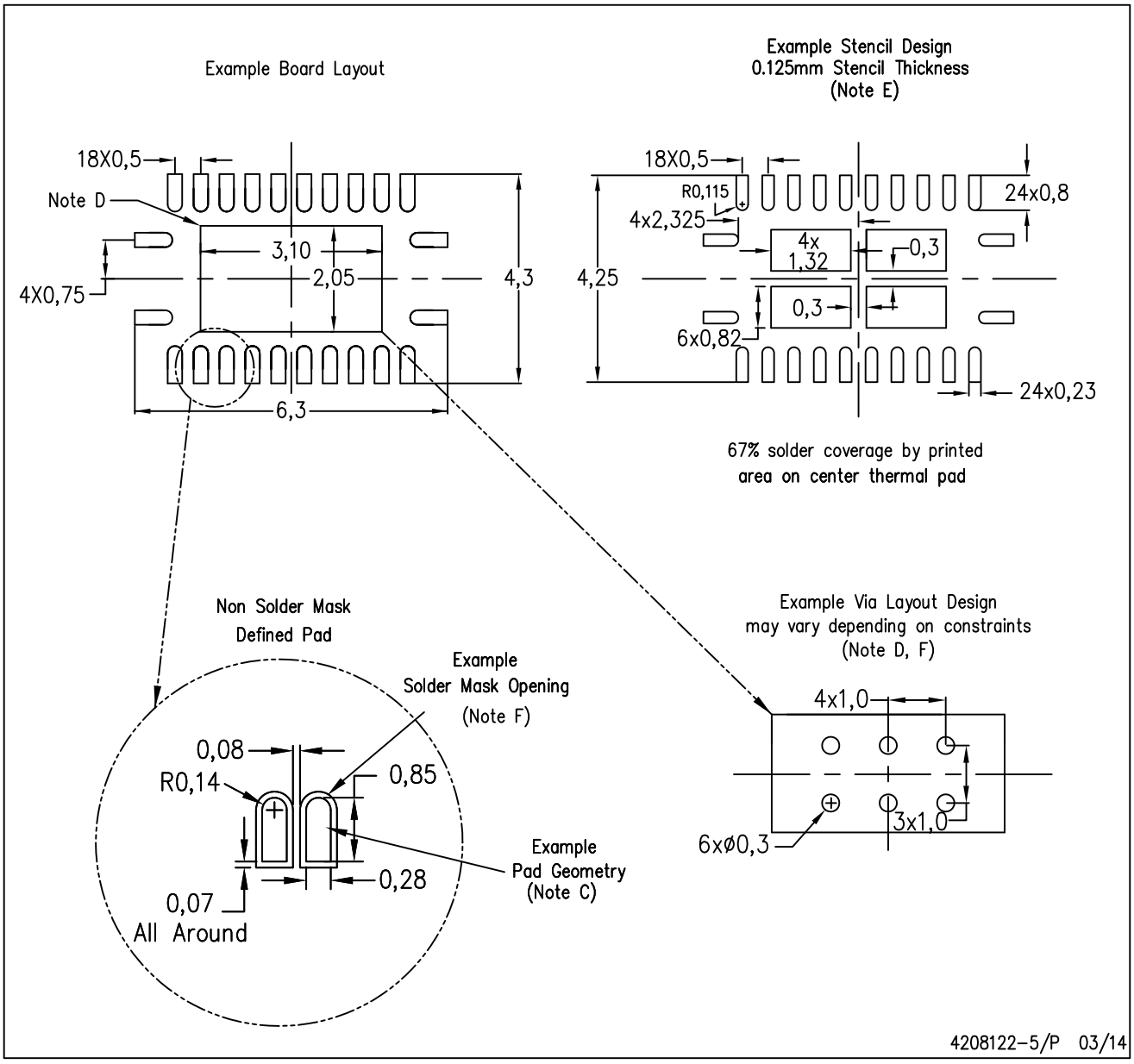

Bottom View

Exposed Thermal Pad Dimensions

4206353–6/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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