

SINGLE-SUPPLY, *microPower* CMOS OPERATIONAL AMPLIFIERS *microAmplifier™* Series

FEATURES

- SINGLE-SUPPLY OPERATION
- RAIL-TO-RAIL OUTPUT (within 3mV)
- *microPOWER*: $I_Q = 20\mu\text{A}/\text{Amplifier}$
- *microSIZE* PACKAGES
- LOW OFFSET VOLTAGE: $125\mu\text{V max}$
- SPECIFIED FROM $V_S = 2.3\text{V to } 5.5\text{V}$
- SINGLE, DUAL, AND QUAD VERSIONS

APPLICATIONS

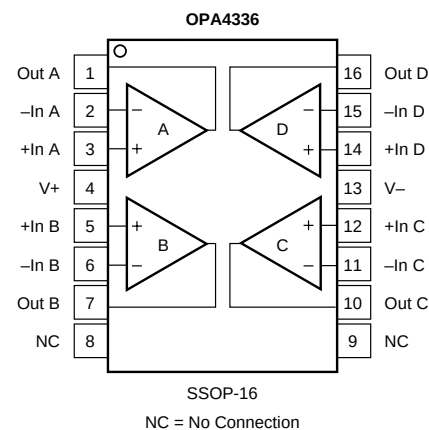
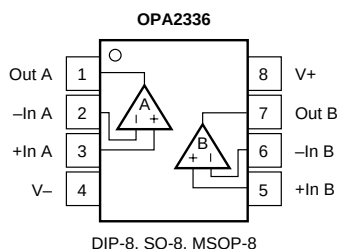
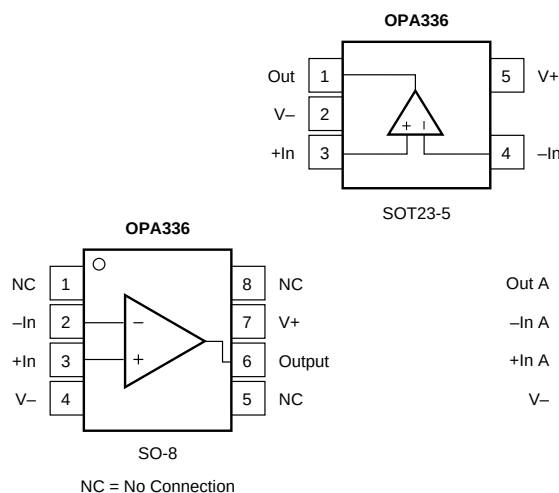
- BATTERY-POWERED INSTRUMENTS
- PORTABLE DEVICES
- HIGH-IMPEDANCE APPLICATIONS
- PHOTODIODE PRE-AMPS
- PRECISION INTEGRATORS
- MEDICAL INSTRUMENTS
- TEST EQUIPMENT

DESCRIPTION

OPA336 series *microPower* CMOS operational amplifiers are designed for battery-powered applications. They operate on a single supply with operation as low as 2.1V. The output is rail-to-rail and swings to within 3mV of the supplies with a $100\text{k}\Omega$ load. The common-mode range extends to the negative supply—ideal for single-supply applications. Single, dual, and quad versions have identical specifications for maximum design flexibility.

In addition to small size and low quiescent current ($20\mu\text{A}/\text{amplifier}$), they feature low offset voltage ($125\mu\text{V max}$), low input bias current (1pA), and high open-loop gain (115dB). Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

OPA336 packages are the tiny SOT23-5 surface mount and SO-8 surface-mount. OPA2336 come in the miniature MSOP-8 surface-mount, SO-8 surface-mount, and DIP-8 packages. The OPA4336 package is the space-saving SSOP-16 surface-mount. All are specified from -40°C to $+85^\circ\text{C}$ and operate from -55°C to $+125^\circ\text{C}$. A macromodel is available for download (at www.ti.com) for design analysis.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PACKAGE/ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE-LEAD	PACKAGE DRAWING DESIGNATOR	PACKAGE MARKING
Single OPA336N OPA336NA OPA336NJ OPA336U OPA336UA OPA336UJ	SOT23-5 SOT23-5 SOT23-5 SO-8 Surface-Mount SO-8 Surface-Mount SO-8 Surface-Mount	DBV DBV DBV D D D	A36 ⁽²⁾ A36 ⁽²⁾ J36 OPA336U OPA336UA OPA336UJ
Dual OPA2336E OPA2336EA OPA2336P OPA2336PA OPA2336U OPA2336UA	MSOP-8 Surface-Mount MSOP-8 Surface-Mount DIP-8 DIP-8 SO-8 Surface-Mount SO-8 Surface-Mount	DGK DGK P P D D	B36 ⁽²⁾ B36 ⁽²⁾ OPA2336P OPA2336PA OPA2336U OPA2336UA
Quad OPA4336EA	SSOP-16 Surface-Mount	DBQ	OPA4336EA

NOTES: (1) For the most current package and ordering information, see the package option addendum at the end of this data sheet. (2) Grade will be marked on the Reel.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage	7.5V
Signal Input Terminals, Voltage ⁽²⁾	(V-) -0.3V to (V+) +0.3V
Current ⁽²⁾	10mA
Output Short-Circuit ⁽³⁾	Continuous
Operating Temperature	-55°C to +125°C
Storage Temperature	-55°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C
ESD Rating:	
Charged Device Model, OPA336 NJ and UJ only (CDM) ⁽⁴⁾	1000V
Human Body Model (HBM) ⁽⁴⁾	500V
Machine Model (MM) ⁽⁴⁾	100V

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only. Functional operation of the device at these conditions, or beyond the specified operating conditions, is not implied. (2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package. (4) OPA336 NJ and UJ have been tested to CDM of 1000V. All other previous package versions have been tested using HBM and MM. Results are shown.

**ELECTROSTATIC
DISCHARGE SENSITIVITY**

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS: $V_S = 2.3V$ to $5.5V$

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.

At $T_A = +25^{\circ}C$, $V_S = +5V$, and $R_L = 25k\Omega$ connected to $V_S/2$, unless otherwise noted.

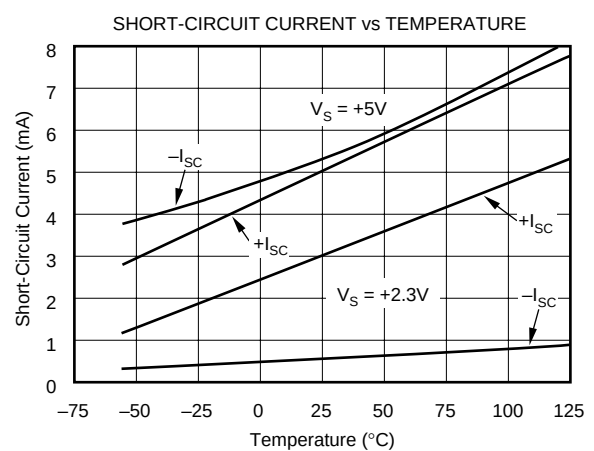
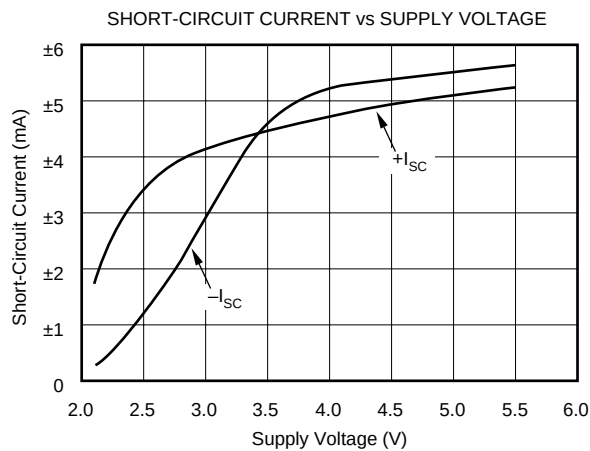
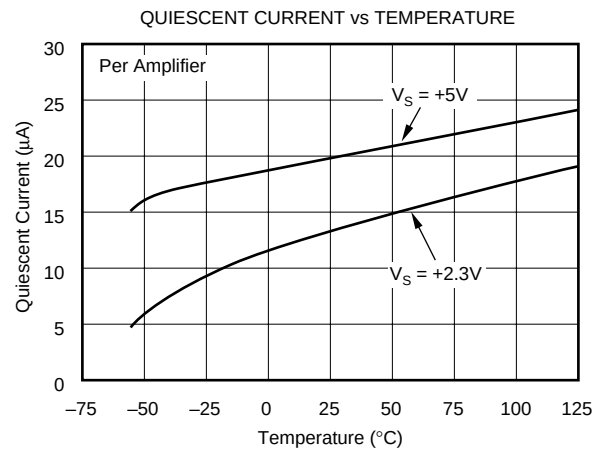
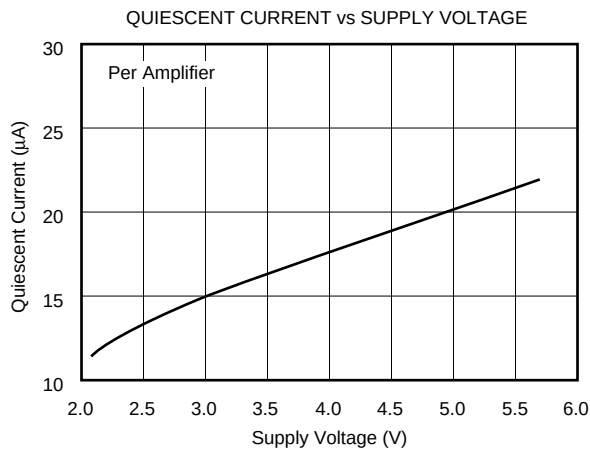
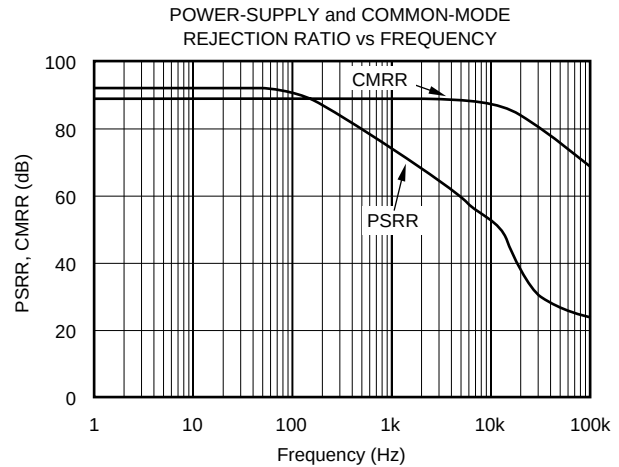
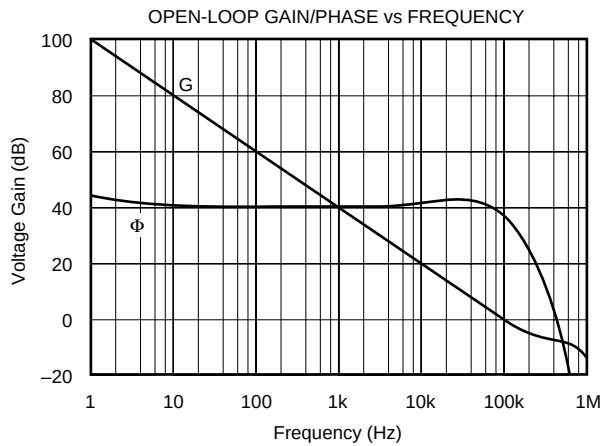
PARAMETER	CONDITION	OPA336N, U OPA2336E, P, U			OPA336NA, UA OPA2336EA, PA, UA OPA4336EA			OPA336NJ, UJ			UNITS
		MIN	TYP ⁽¹⁾	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage vs Temperature vs Power Supply Over Temperature Channel Separation, dc	V_{OS} dV_{OS}/dT PSRR		± 60 ± 1.5 25 0.1	± 125 100 130		*	± 500 *		± 500 *	± 2500 *	μV $\mu V/^{\circ}C$ $\mu V/V$ $\mu V/V$
INPUT BIAS CURRENT Input Bias Current Over Temperature Input Offset Current	I_B I_{OS}		± 1 ± 1	± 10 ± 60 ± 10		*	*		*	*	pA pA pA
NOISE Input Voltage Noise, $f = 0.1$ to $10Hz$ Input Voltage Noise Density, $f = 1kHz$ e_n Current Noise Density, $f = 1kHz$ i_n			3 40 30			*	*		*	*	$\mu Vp-p$ $nV/\sqrt{Hz}$ $fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection Ratio Over Temperature	V_{CM} CMRR	$-0.2V$ 80 76	90	$(V+) - 1$	*	86 74	*	*	86 74	*	V dB dB
INPUT IMPEDANCE Differential Common-Mode			$10^{13} \parallel 2$ $10^{13} \parallel 4$			*	*		*	*	$\Omega \parallel pF$ $\Omega \parallel pF$
OPEN-LOOP GAIN Open-Loop Voltage Gain Over Temperature Over Temperature	A_{OL}	$R_L = 25k\Omega, 100mV < V_O < (V+) - 100mV$ $R_L = 25k\Omega, 100mV < V_O < (V+) - 100mV$ $R_L = 5k\Omega, 500mV < V_O < (V+) - 500mV$ $R_L = 5k\Omega, 500mV < V_O < (V+) - 500mV$	100 100 90 90	115 106		90 90 *	*		90 90 *	*	dB dB dB dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Overload Recovery Time	GBW SR	$V_S = 5V, G = 1$ $V_S = 5V, G = 1$ $V_{IN} \cdot G = V_S$	100 0.03 100			*	*		*	*	kHz V/ μs μs
OUTPUT Voltage Output Swing from Rail ⁽²⁾ Over Temperature Over Temperature Short-Circuit Current Capacitive Load Drive	I_{SC} C_{LOAD}	$R_L = 100k\Omega, A_{OL} \geq 70dB$ $R_L = 25k\Omega, A_{OL} \geq 90dB$ $R_L = 25k\Omega, A_{OL} \geq 90dB$ $R_L = 5k\Omega, A_{OL} \geq 90dB$ $R_L = 5k\Omega, A_{OL} \geq 90dB$	3 20 100 70 500 ± 5 See Text	100 100 500		*	*		*	*	mV mV mV mV mA pF
POWER SUPPLY Specified Voltage Range Minimum Operating Voltage Quiescent Current (per amplifier) Over Temperature	V_S I_Q	2.3	2.1 20	5.5 32 36	*	*	*	*	*	*	V V μA μA
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance SOT-23-5 Surface-Mount MSOP-8 Surface-Mount SO-8 Surface-Mount DIP-8 SSOP-16 Surface-Mount DIP-14	θ_{JA}	-40 -55 -55		$+85$ $+125$ $+125$	*	*	*	*	*	*	$^{\circ}C$ $^{\circ}C$ $^{\circ}C$ $^{\circ}C/W$ $^{\circ}C/W$ $^{\circ}C/W$ $^{\circ}C/W$ $^{\circ}C/W$ $^{\circ}C/W$

*Specifications same as OPA2336E, P, U.

NOTES: (1) $V_S = +5V$. (2) Output voltage swings are measured between the output and positive and negative power-supply rails.

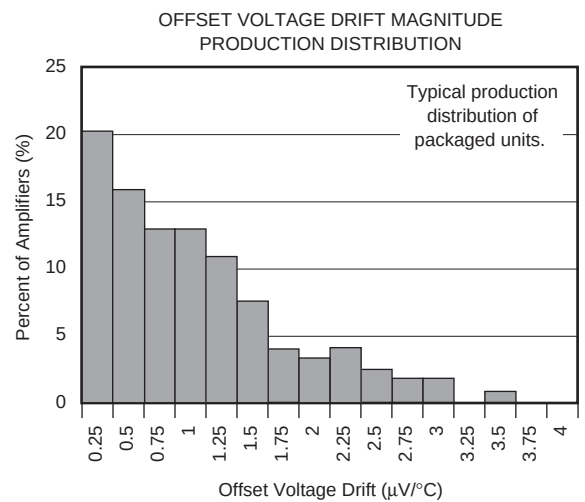
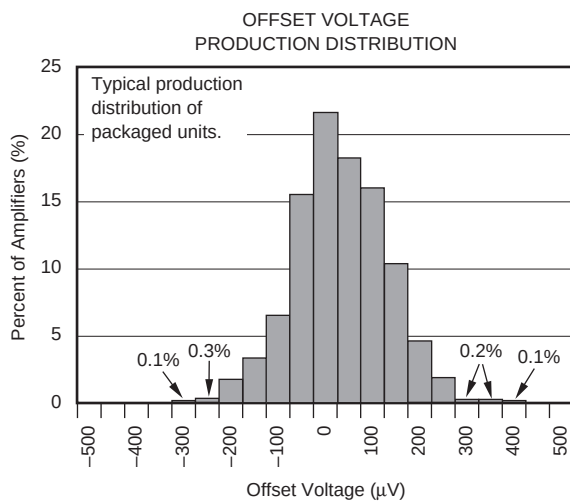
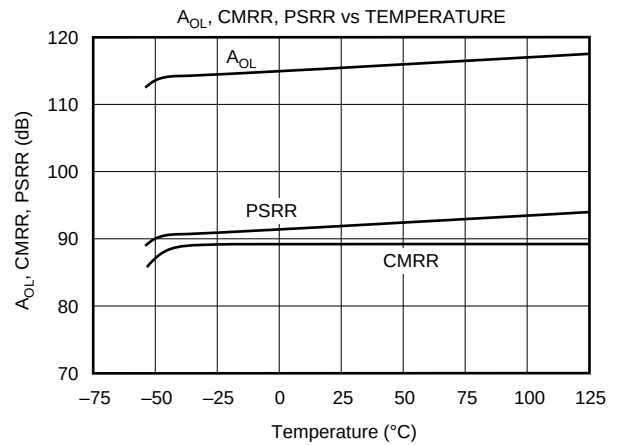
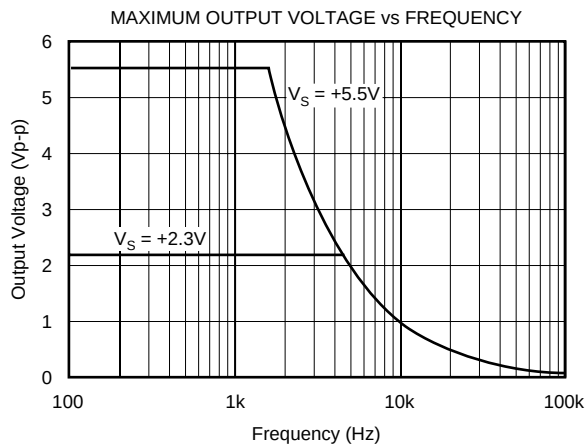
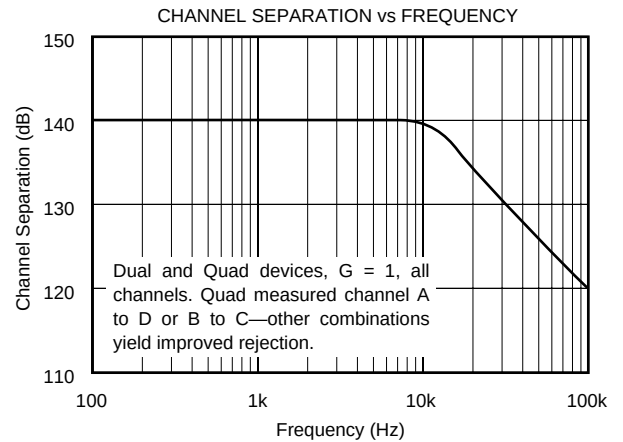
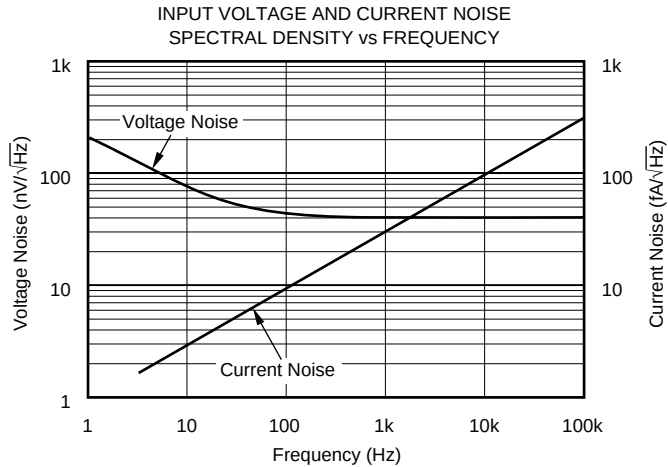
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, and $R_L = 25\text{k}\Omega$ connected to $V_S/2$, unless otherwise noted.



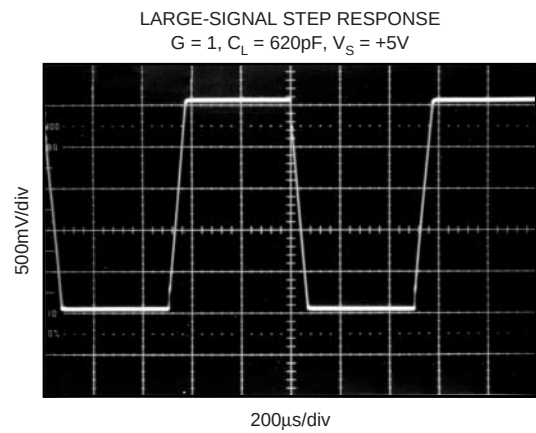
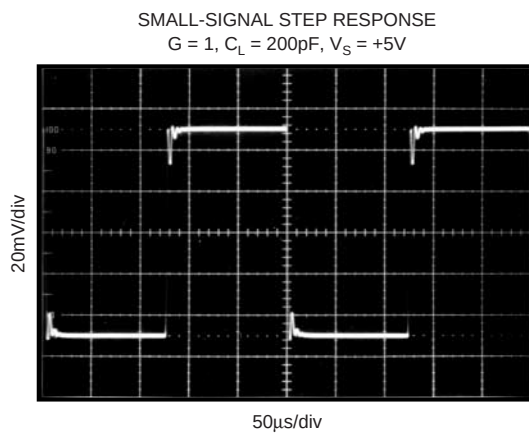
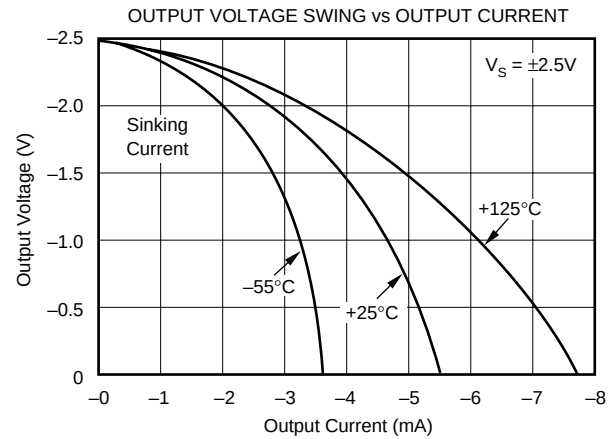
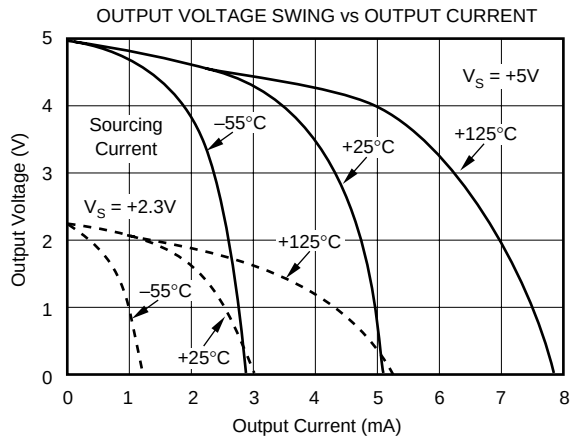
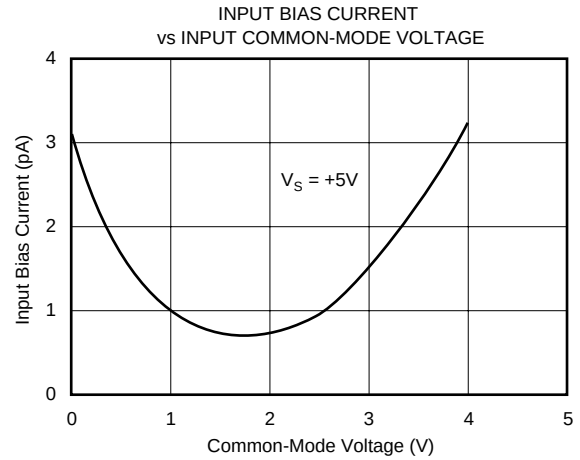
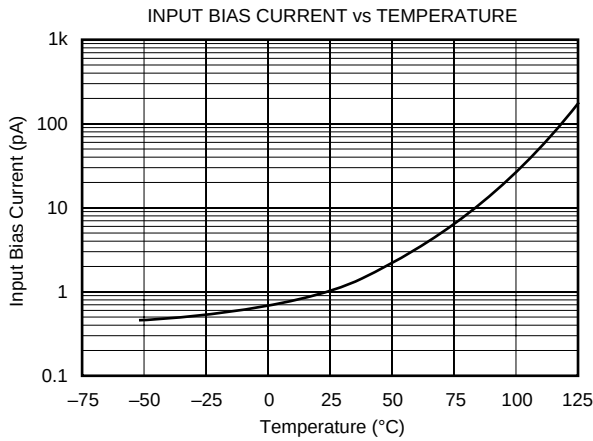
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, and $R_L = 25\text{k}\Omega$ connected to $V_S/2$, unless otherwise noted.



TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, and $R_L = 25\text{k}\Omega$ connected to $V_S/2$, unless otherwise noted.



APPLICATIONS INFORMATION

OPA336 series op amps are fabricated on a state-of-the-art 0.6 micron CMOS process. They are unity-gain stable and suitable for a wide range of general-purpose applications. Power-supply pins should be bypassed with 0.01 μ F ceramic capacitors. OPA336 series op amps are protected against reverse battery voltages.

OPERATING VOLTAGE

OPA336 series op amps can operate from a +2.1V to +5.5V single supply with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the typical characteristics. OPA336 series op amps are fully specified for operation from +2.3V to +5.5V; a single limit applies over the supply range. In addition, many parameters are ensured over the specified temperature range, -40°C to $+85^{\circ}\text{C}$.

INPUT VOLTAGE

The input common-mode range of OPA336 series op amps extends from $(V-) - 0.2\text{V}$ to $(V+) - 1\text{V}$. For normal operation, inputs should be limited to this range. The absolute maximum input voltage is 300mV beyond the supplies. Thus, inputs greater than the input common-mode range but less than maximum input voltage, while not valid, will not cause any damage to the op amp. Furthermore, the inputs may go beyond the power supplies without phase inversion, as shown in Figure 1, unlike some other op amps.

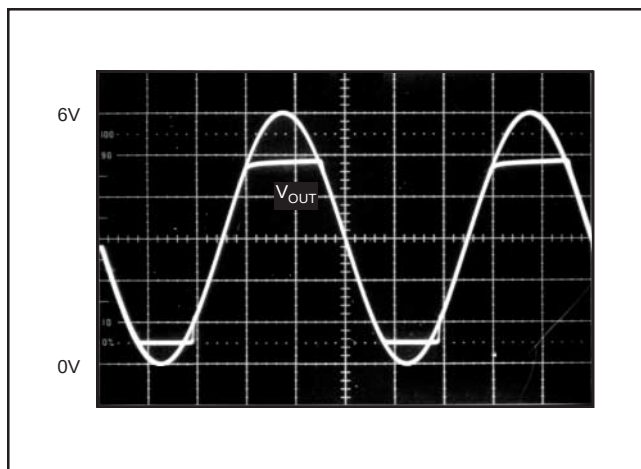


FIGURE 1. No Phase Inversion with Inputs Greater than the Power-Supply Voltage.

Normally, input bias current is approximately 1pA. However, input voltages exceeding the power supplies can cause excessive current to flow in or out of the input pins. Momentary voltages greater than the power supply can be tolerated as long as the current on the input pins is limited to 10mA. This is easily accomplished with an input resistor, as shown in Figure 2.

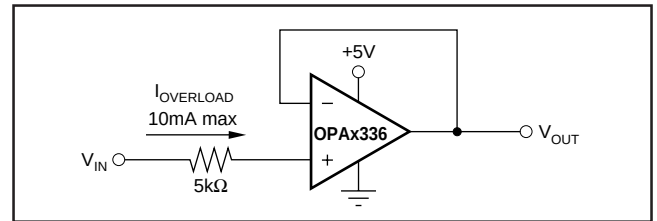


FIGURE 2. Input Current Protection for Voltages Exceeding the Supply Voltage.

CAPACITIVE LOAD AND STABILITY

OPA336 series op amps can drive a wide range of capacitive loads. However, all op amps under certain conditions may become unstable. Op-amp configuration, gain, and load value are just a few of the factors to consider when determining stability.

When properly configured, OPA336 series op amps can drive approximately 10,000pF. An op amp in unity-gain configuration is the most vulnerable to capacitive load. The capacitive load reacts with the op amp's output resistance, along with any additional load resistance, to create a pole in the response which degrades the phase margin. In unity gain, OPA336 series op amps perform well with a pure capacitive load up to about 300pF. Increasing gain enhances the amplifier's ability to drive loads beyond this level.

One method of improving capacitive load drive in the unity-gain configuration is to insert a 50 Ω to 100 Ω resistor inside the feedback loop, as shown in Figure 3. This reduces ringing with large capacitive loads while maintaining DC

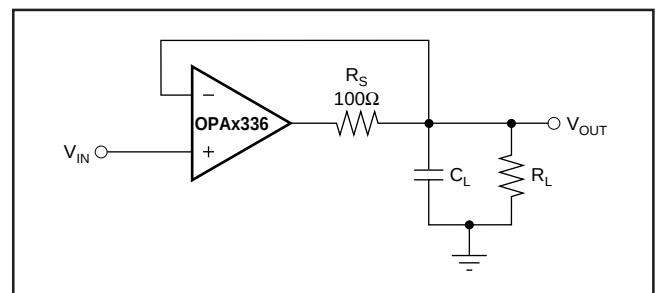


FIGURE 3. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive.

accuracy. For example, with $R_L = 25\text{k}\Omega$, OPA336 series op amps perform well with capacitive loads in excess of 1000pF , as shown in Figure 4. Without R_S , capacitive load drive is typically 350pF for these conditions, as shown in Figure 5.

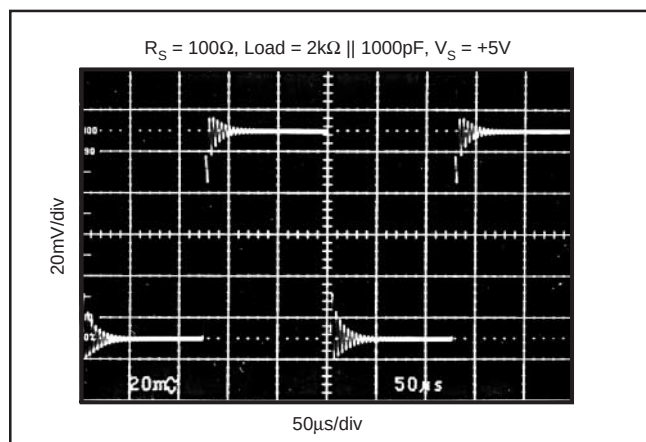


FIGURE 4. Small-Signal Step Response Using Series Resistor to Improve Capacitive Load Drive.

Alternatively, the resistor may be connected in series with the output outside of the feedback loop. However, if there is a resistive load parallel to the capacitive load, it and the series resistor create a voltage divider. This introduces a

Direct Current (DC) error at the output; however, this error may be insignificant. For instance, with $R_L = 100\text{k}\Omega$ and $R_S = 100\Omega$, there is only about a 0.1% error at the output.

Figure 5 shows the recommended operating regions for the OPA336. Decreasing the load resistance generally improves capacitive load drive. Figure 5 also illustrates how stability differs depending on where the resistive load is connected. With $G = +1$ and $R_L = 10\text{k}\Omega$ connected to $V_S/2$, the OPA336 can typically drive 500pF . Connecting the same load to ground improves capacitive load drive to 1000pF .

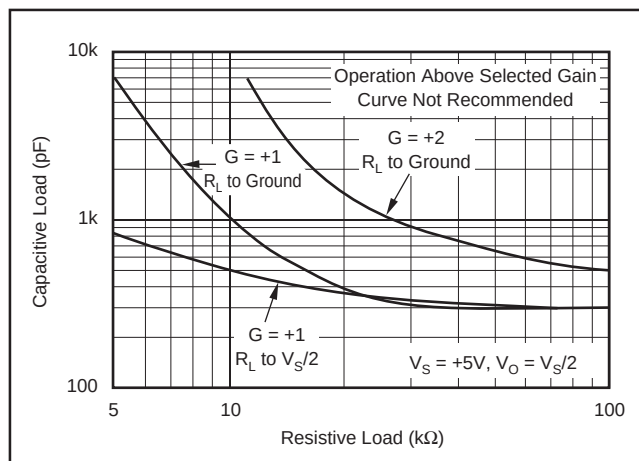


FIGURE 5. Stability—Capacitive Load vs Resistive Load.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA00779NA/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA2336E/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B36	Samples
OPA2336E/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B36	Samples
OPA2336E/2K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B36	Samples
OPA2336EA/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B36	Samples
OPA2336EA/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B36	Samples
OPA2336EA/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B36	Samples
OPA2336P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	OPA2336P	Samples
OPA2336PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	OPA2336P A	Samples
OPA2336U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2336U	Samples
OPA2336U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2336U	Samples
OPA2336U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2336U	Samples
OPA2336UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2336U A	Samples
OPA2336UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2336U A	Samples
OPA2336UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2336U A	Samples
OPA2336UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2336U	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA336N/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336N/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336N/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336N/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336NA/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336NA/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336NA/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336NA/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		A36	Samples
OPA336NJ/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	J36	Samples
OPA336NJ/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	J36	Samples
OPA336NJ/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	J36	Samples
OPA336U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR		OPA 336U	Samples
OPA336U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR		OPA 336U	Samples
OPA336UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR		OPA 336U A	Samples
OPA336UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR		OPA 336U A	Samples
OPA4336EA/250	ACTIVE	SSOP	DBQ	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4336EA	Samples
OPA4336EA/250G4	ACTIVE	SSOP	DBQ	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4336EA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4336EA/2K5	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4336EA	Samples
OPA4336EA/2K5G4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4336EA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

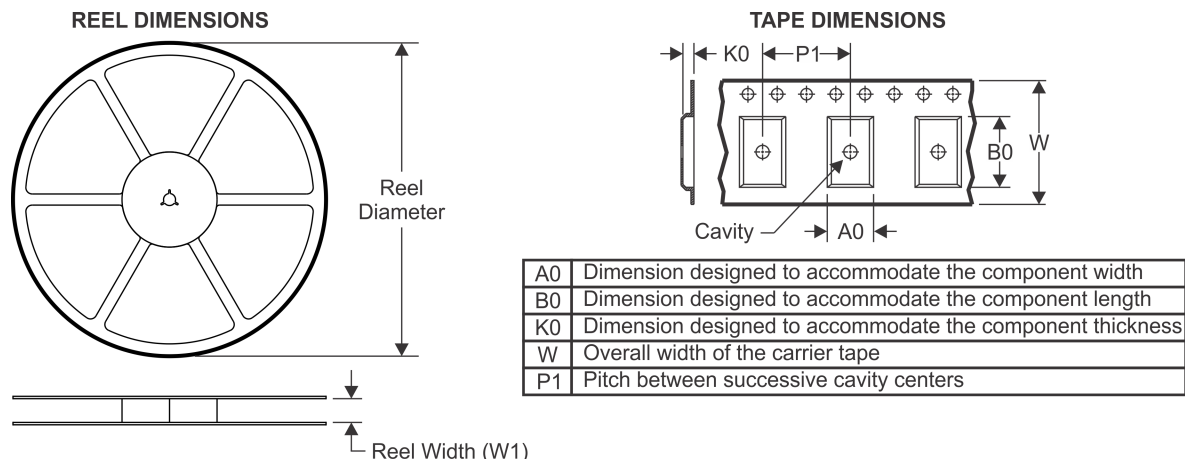
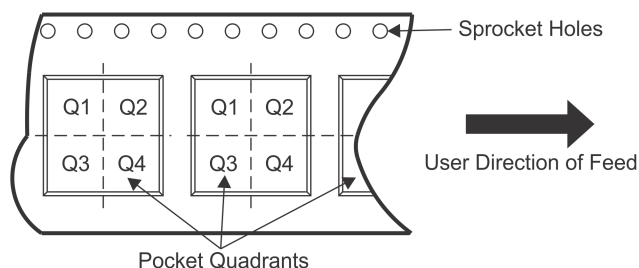
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA336 :

-
- Enhanced Product: [OPA336-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

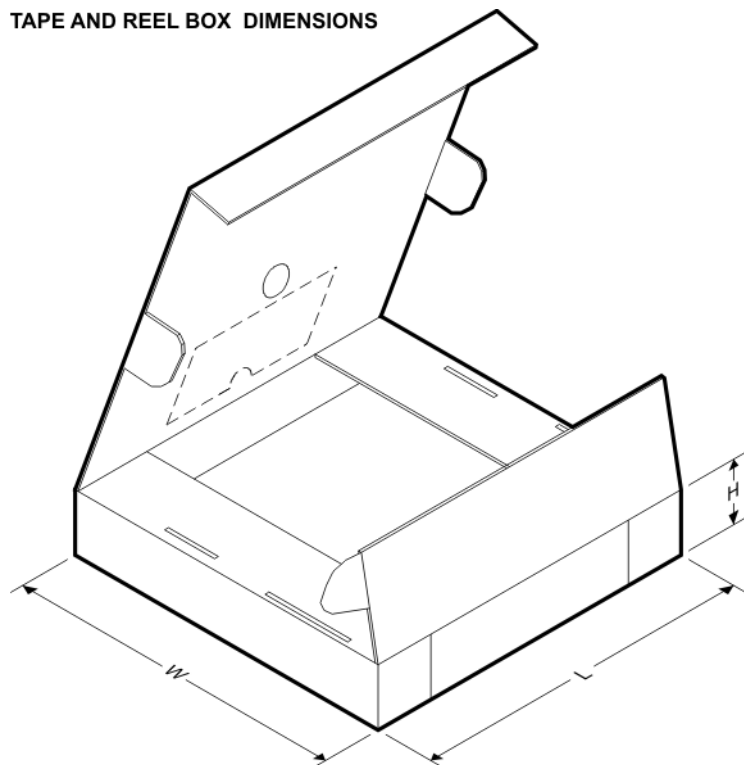
TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2336E/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2336E/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2336EA/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2336EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2336U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2336UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA336N/250	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA336N/3K	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA336N/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA336NA/250	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA336NA/3K	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA336NA/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA336NJ/250	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA336NJ/3K	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA336NJ/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA336U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA336UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4336EA/250	SSOP	DBQ	16	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA4336EA/2K5	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2336E/250	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2336E/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA2336EA/250	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2336EA/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA2336U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA2336UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA336N/250	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA336N/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA336N/3K	SOT-23	DBV	5	3000	203.0	203.0	35.0
OPA336NA/250	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA336NA/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA336NA/3K	SOT-23	DBV	5	3000	203.0	203.0	35.0
OPA336NJ/250	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA336NJ/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA336NJ/3K	SOT-23	DBV	5	3000	203.0	203.0	35.0
OPA336U/2K5	SOIC	D	8	2500	367.0	367.0	35.0

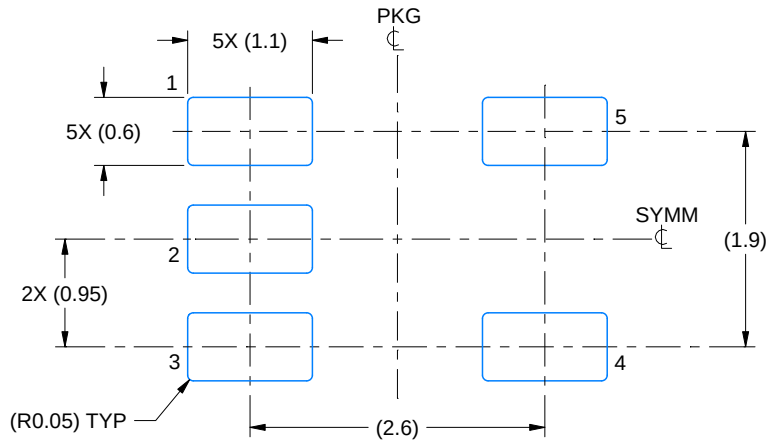
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA336UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA4336EA/250	SSOP	DBQ	16	250	210.0	185.0	35.0
OPA4336EA/2K5	SSOP	DBQ	16	2500	367.0	367.0	35.0

EXAMPLE BOARD LAYOUT

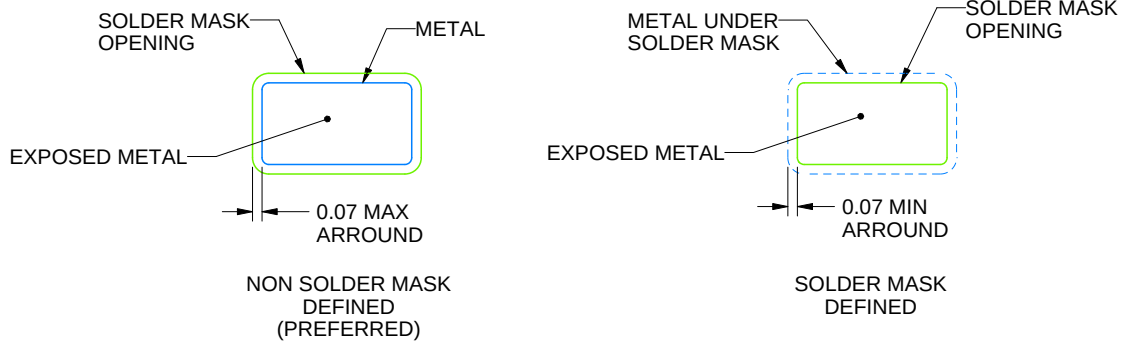
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

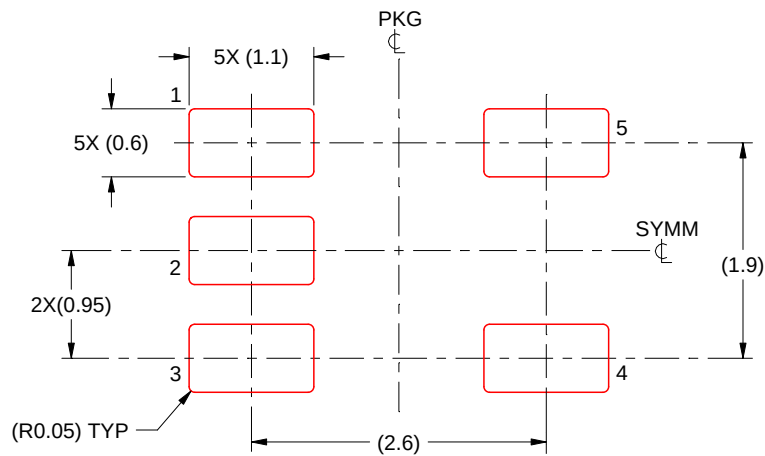
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

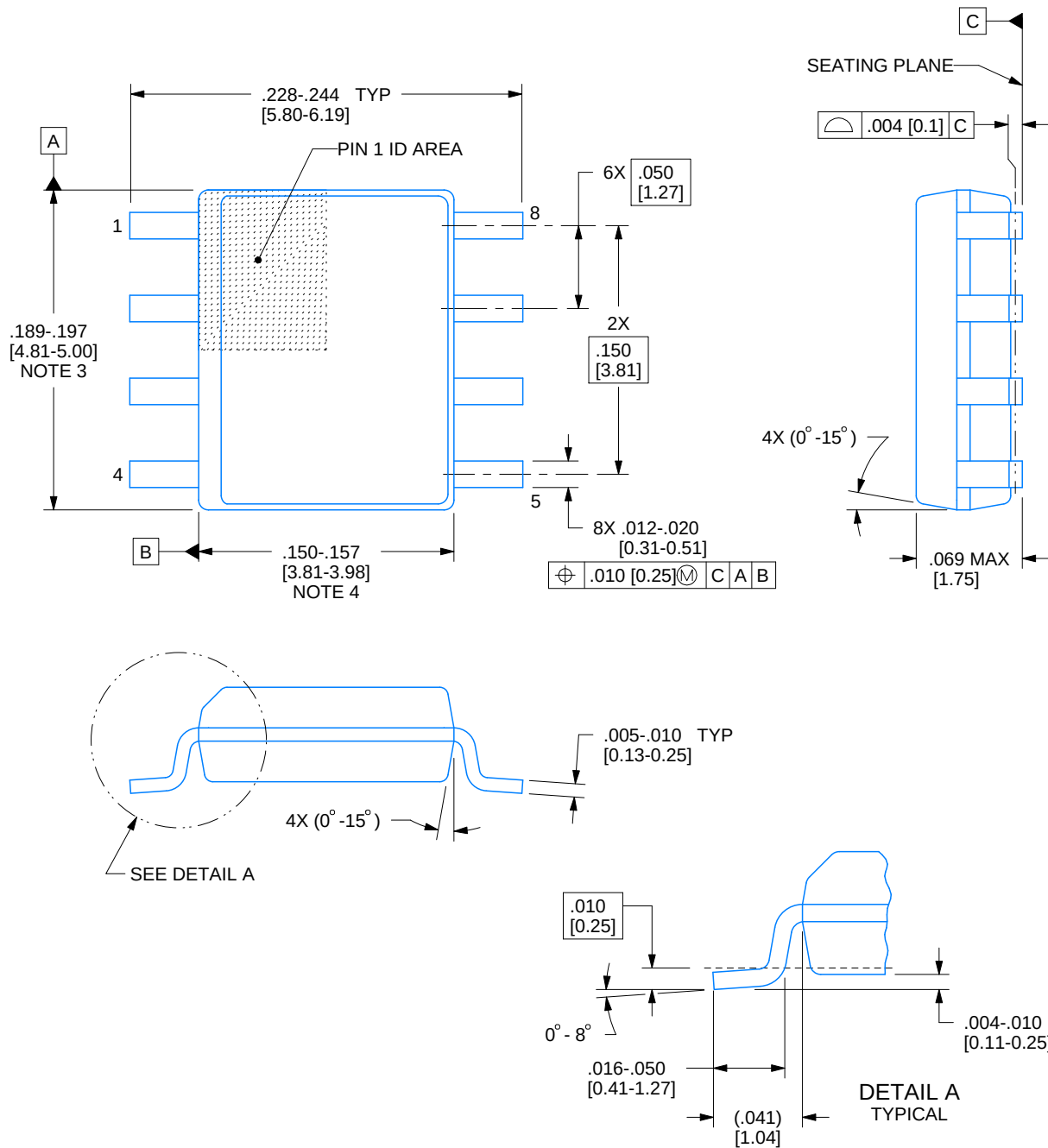
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

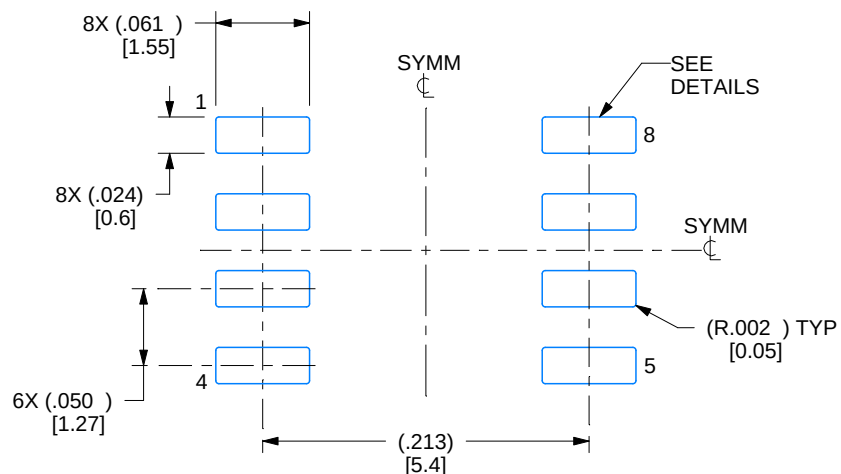
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

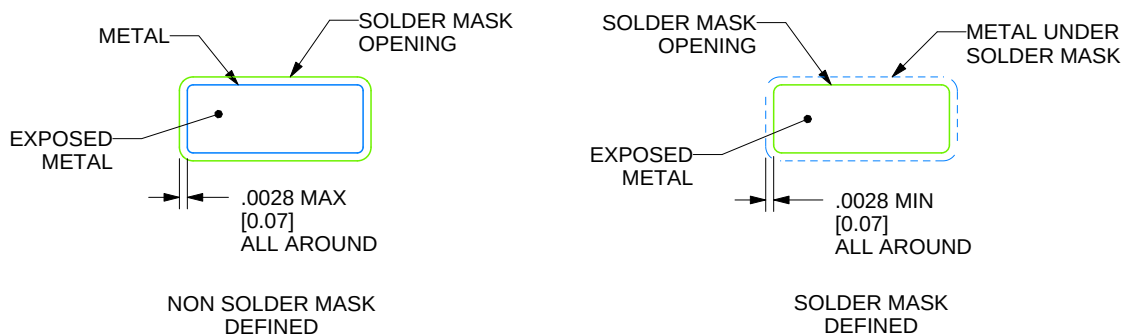
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

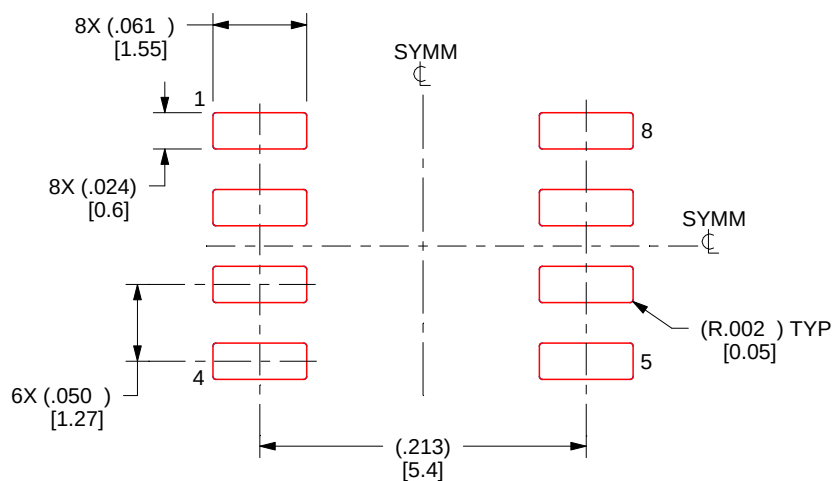
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

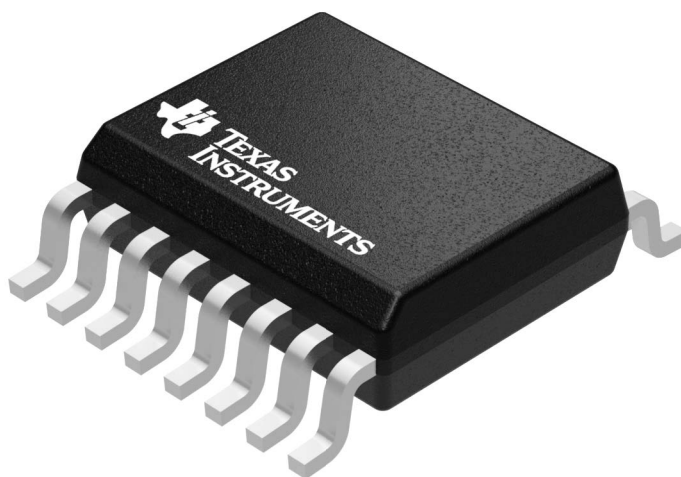


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

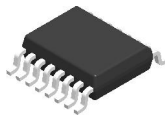
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

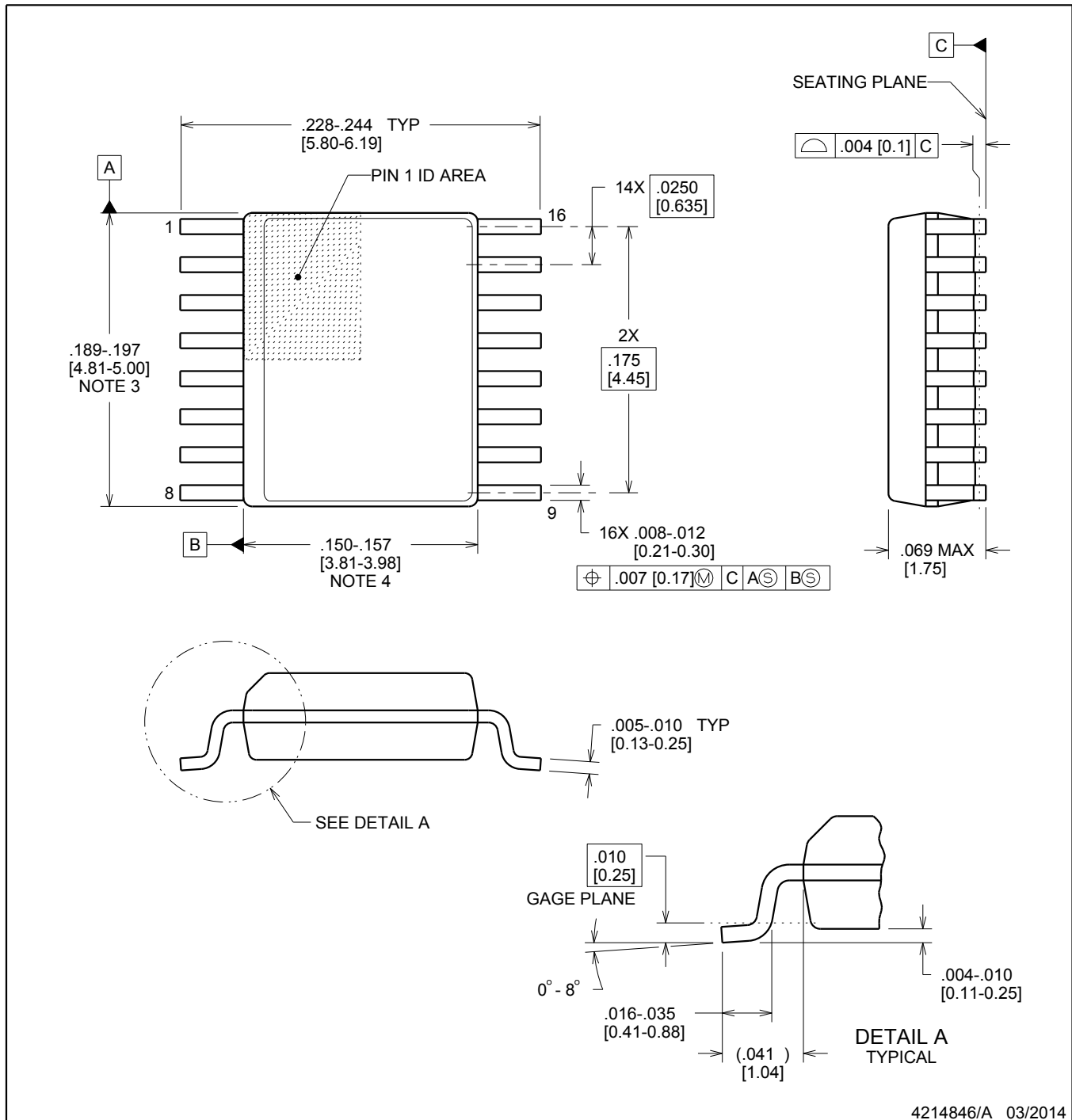


DBQ0016A

PACKAGE OUTLINE

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



4214846/A 03/2014

NOTES:

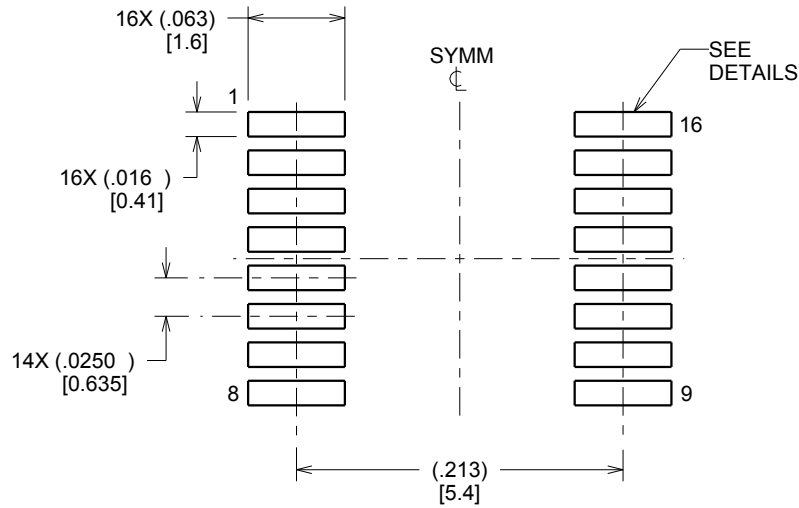
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

EXAMPLE BOARD LAYOUT

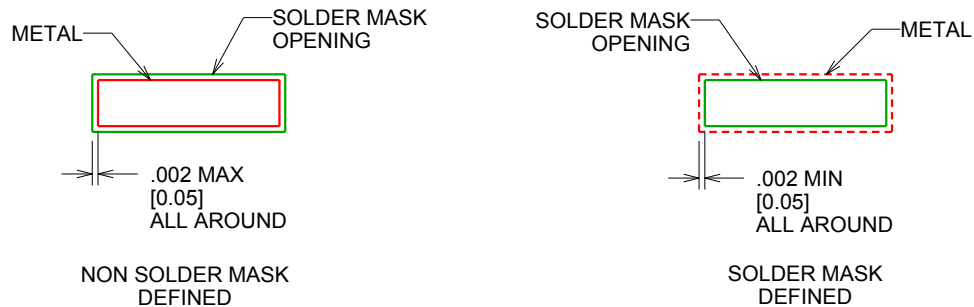
DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

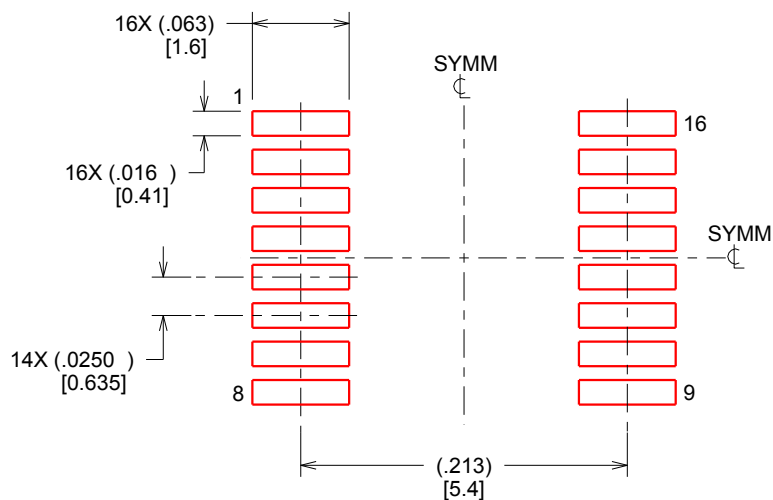
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

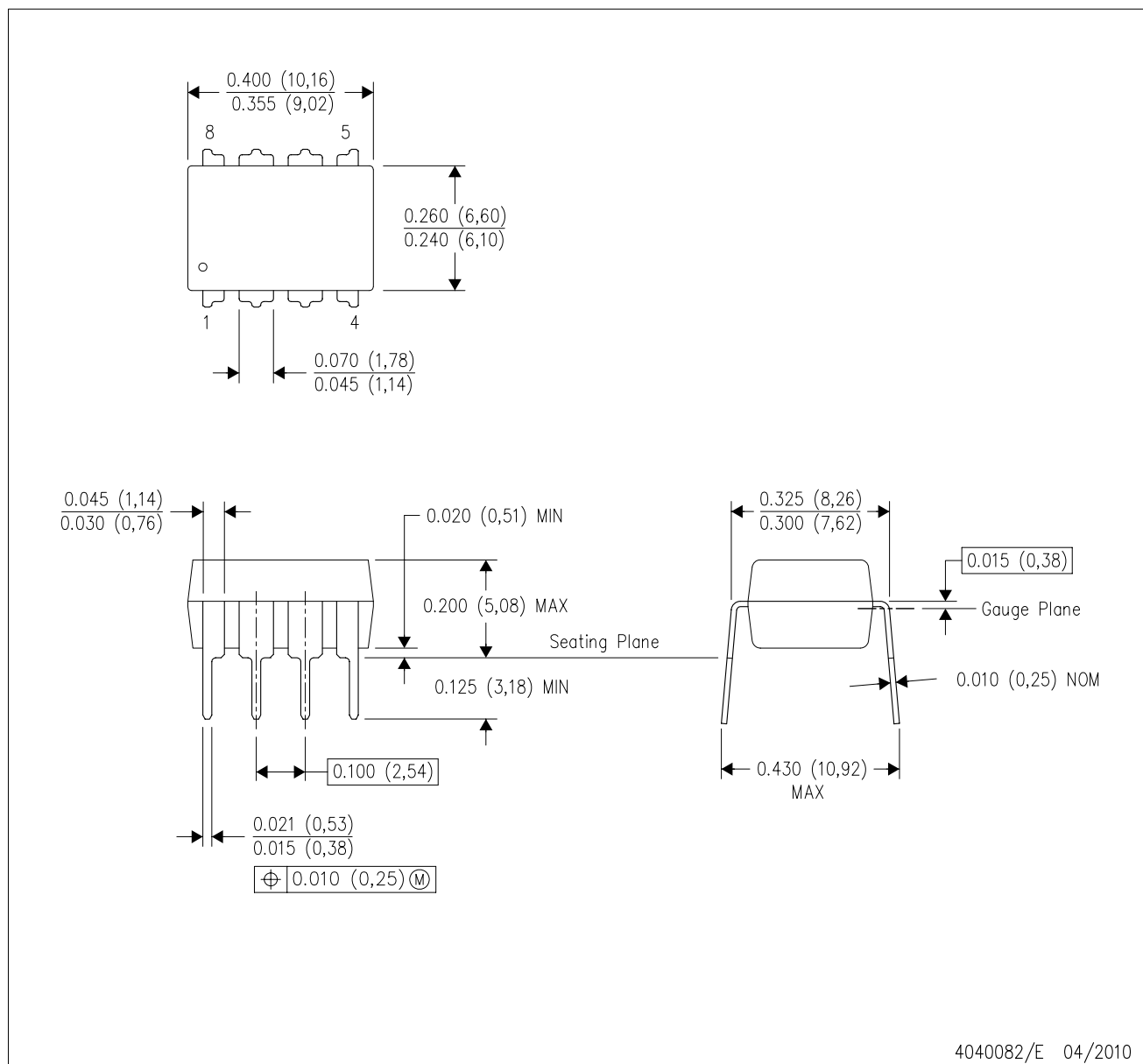
4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

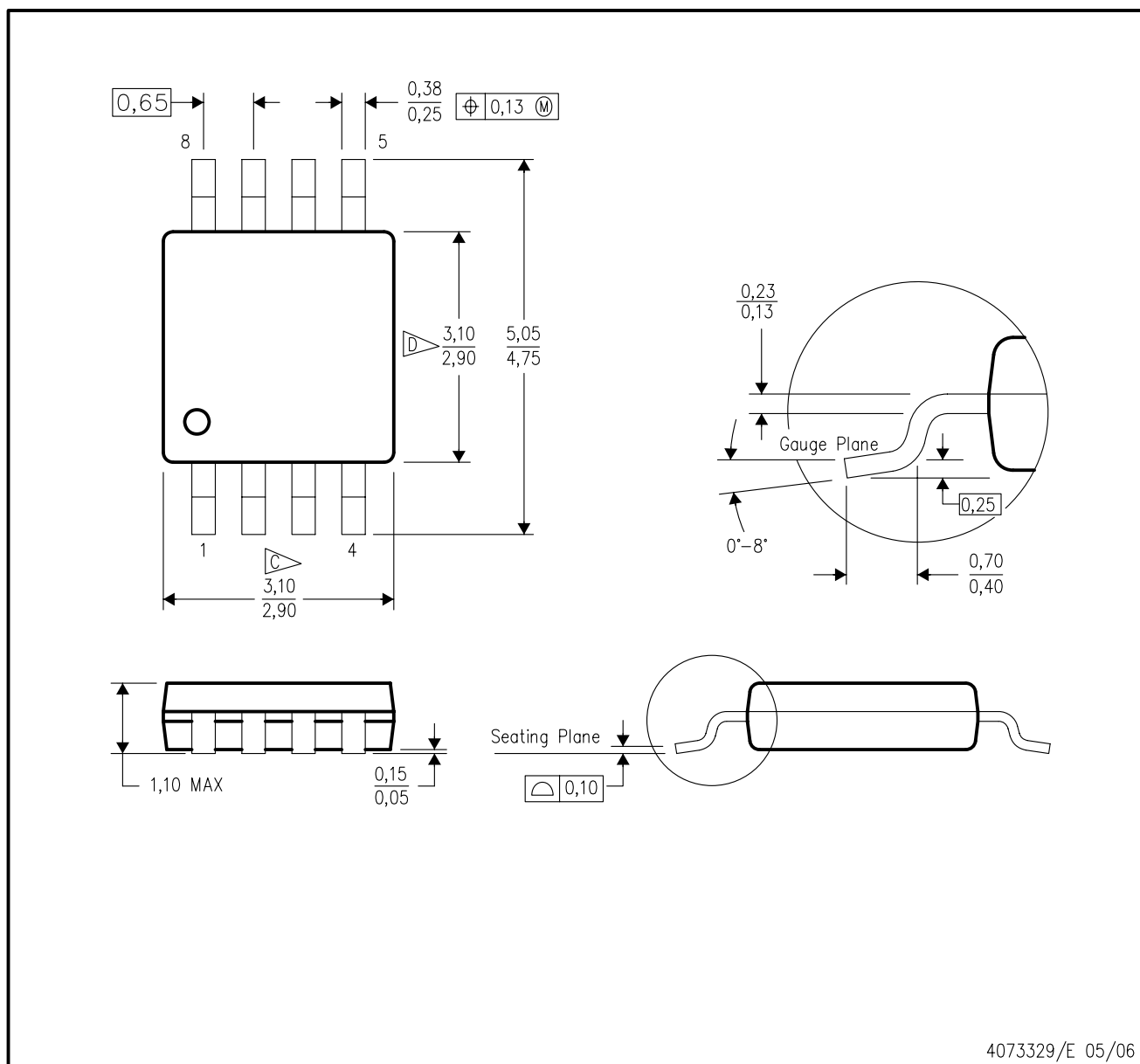
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

DGK (S-PDSO-G8)

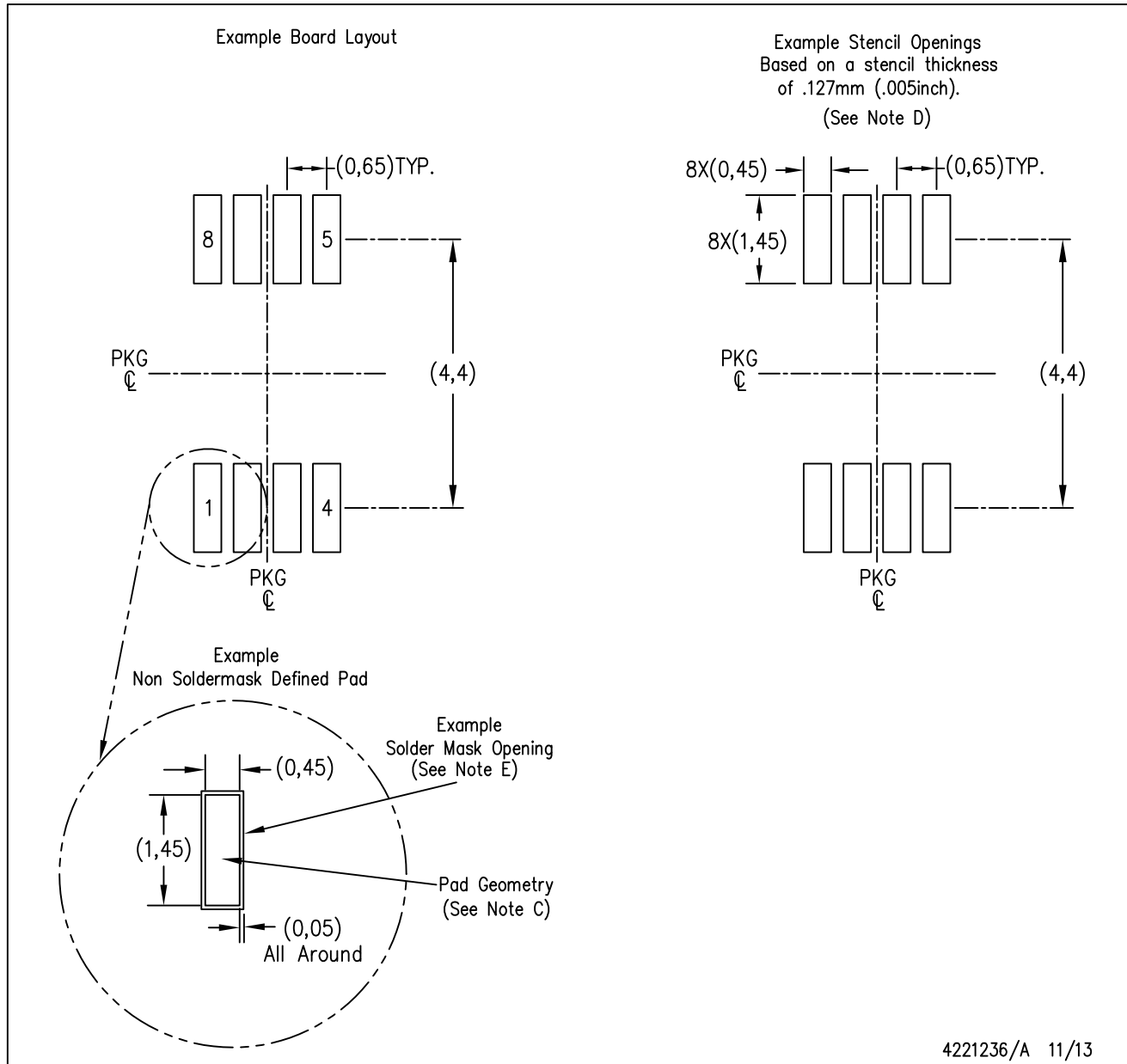
PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated