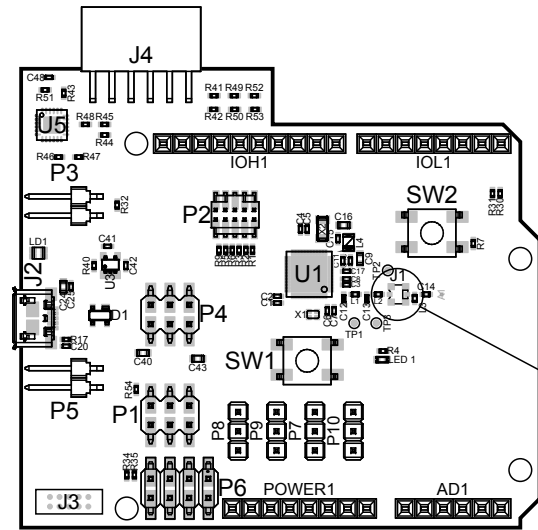
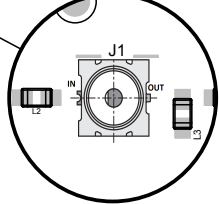


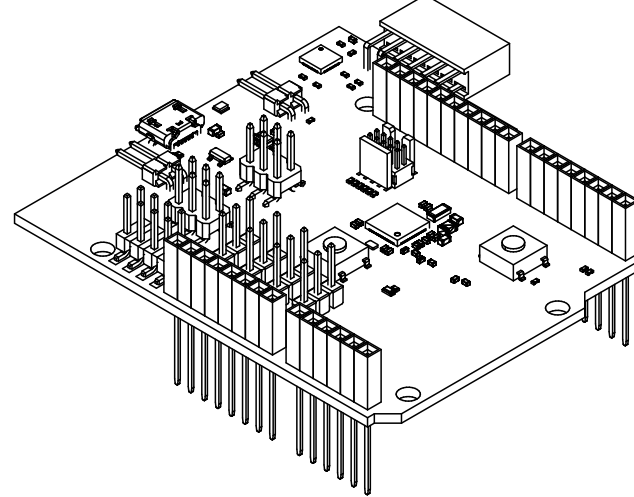
View from Top side (Scale 1:1)



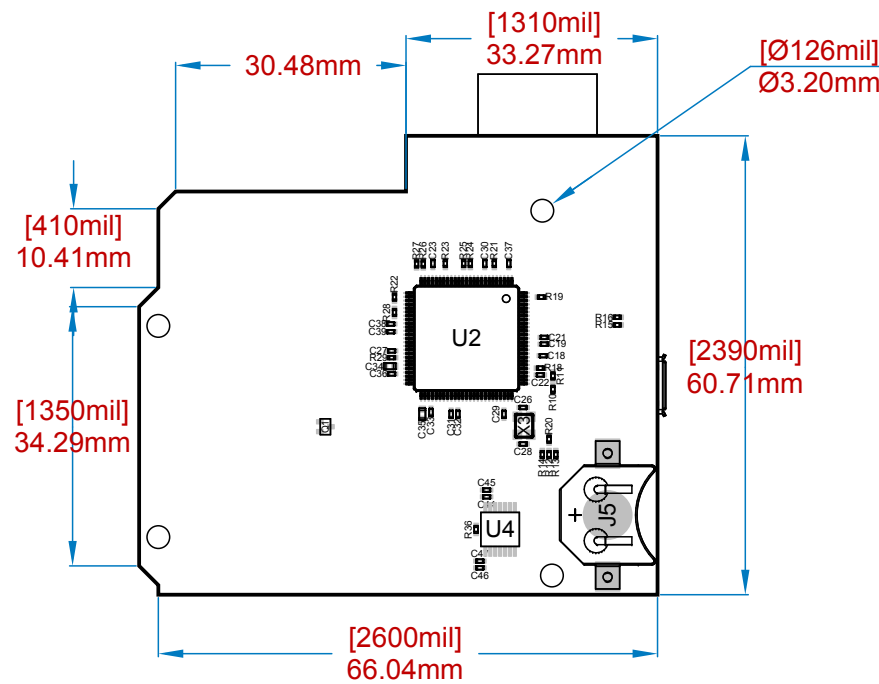
DETAIL A (Scale 4:1)



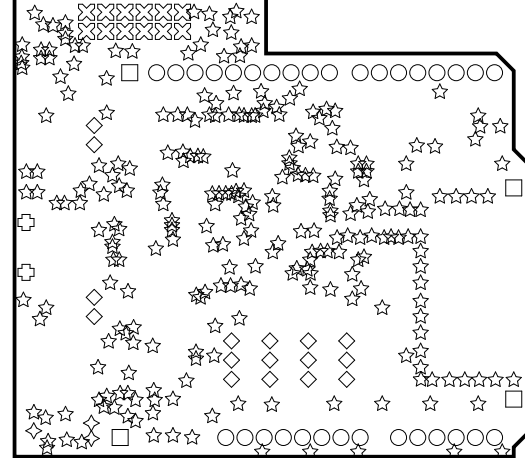
View from Front side (Scale 1:1)



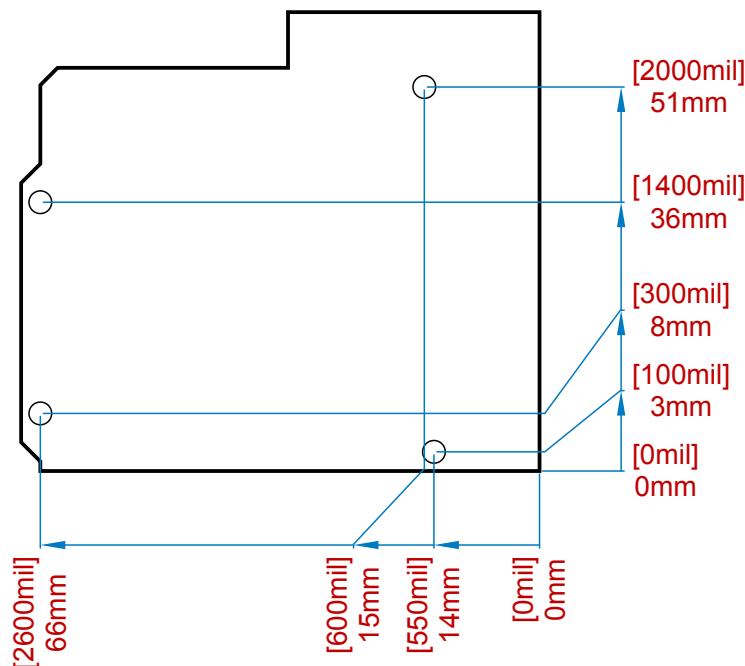
View from Bottom side (Scale 1:1)



Drill Drawing View (Scale 1:1)



View from Bottom side (Scale 1:1)



Drill Table

| Symbol    | Count | Hole Size | Plated     | Hole Type | Drill Layer Pair         |
|-----------|-------|-----------|------------|-----------|--------------------------|
| ☆         | 273   | 0.20mm    | Plated     | Round     | Top Layer - Bottom Layer |
| ⊗         | 2     | 0.50mm    | Plated     | Slot      | Top Layer - Bottom Layer |
| ◇         | 3     | 0.99mm    | Non-Plated | Round     | Top Layer - Bottom Layer |
| ○         | 32    | 1.02mm    | Plated     | Round     | Top Layer - Bottom Layer |
| ⊗         | 12    | 1.02mm    | Plated     | Round     | Top Layer - Bottom Layer |
| ◇         | 16    | 1.10mm    | Plated     | Round     | Top Layer - Bottom Layer |
| □         | 4     | 3.20mm    | Non-Plated | Round     | Top Layer - Bottom Layer |
| 342 Total |       |           |            |           |                          |

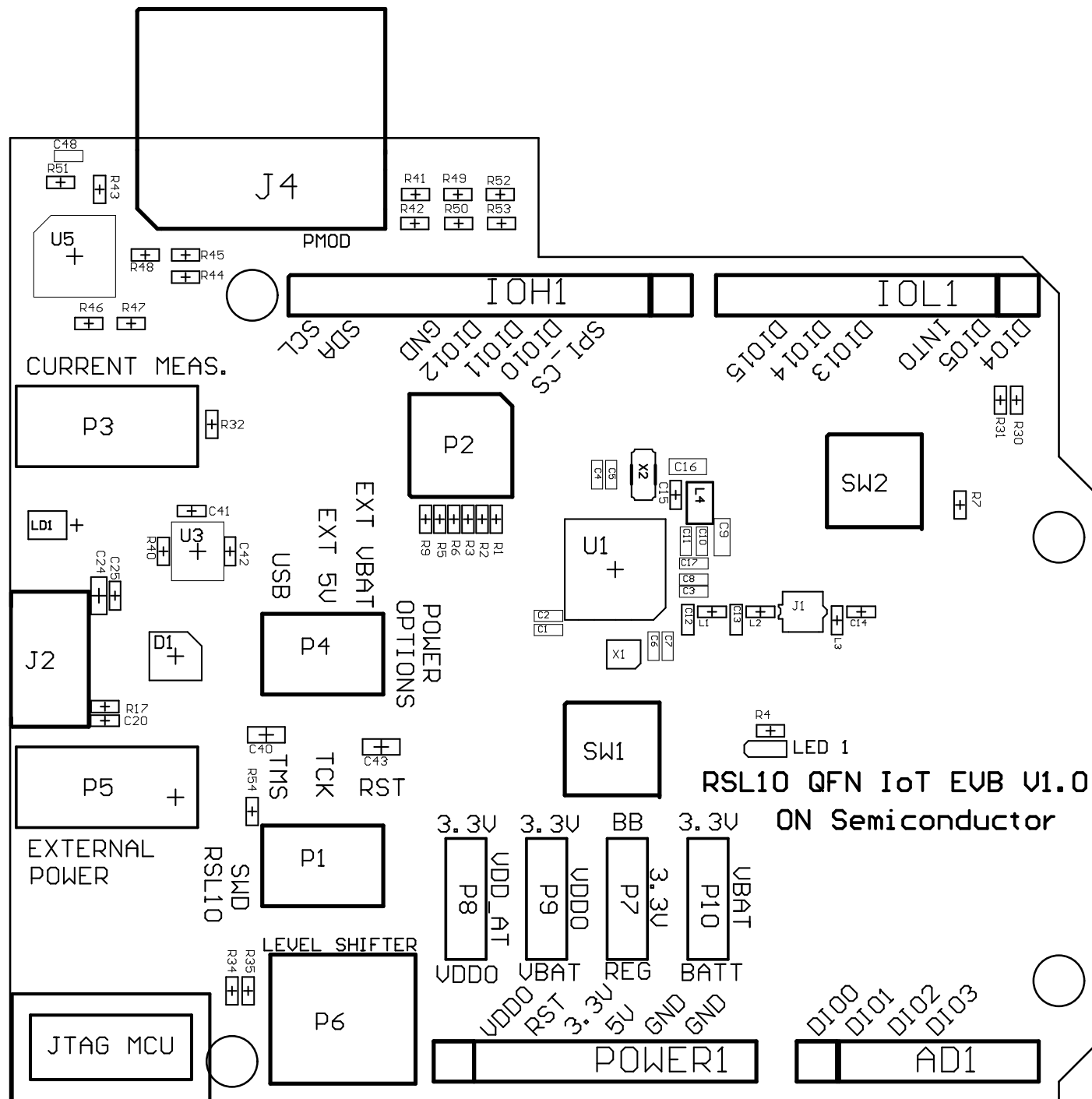
| Layer Stack Legend        | Material         | Layer          | Thickness | Dielectric Material | Type        | Gerber |
|---------------------------|------------------|----------------|-----------|---------------------|-------------|--------|
|                           |                  | Top Paste      |           |                     | Paste Mask  | GTP    |
|                           |                  | Top Overlay    |           |                     | Legend      | GTO    |
|                           | Surface Material | Top Solder     | 0.50mil   | Solder Resist       | Solder Mask | GTS    |
|                           | Copper           | Top Layer      | 2.00mil   |                     | Signal      | GTL    |
|                           | Core             |                | 15.30mil  | FR-4-370HR          | Dielectric  |        |
|                           | Copper           | Signal Layer 1 | 0.60mil   |                     | Signal      | G1     |
|                           | Prepreg          |                | 24.00mil  | FR4-370HR           | Dielectric  |        |
|                           | Copper           | Signal Layer 2 | 0.60mil   |                     | Signal      | G2     |
|                           | Core             |                | 15.30mil  | FR-4-370HR          | Dielectric  |        |
|                           | Copper           | Bottom Layer   | 2.00mil   |                     | Signal      | GBL    |
|                           | Surface Material | Bottom Solder  | 0.50mil   | Solder Resist       | Solder Mask | GBS    |
|                           |                  | Bottom Overlay |           |                     | Legend      | GBO    |
|                           |                  | Bottom Paste   |           |                     | Paste Mask  | GBP    |
| Total thickness: 60.80mil |                  |                |           |                     |             |        |

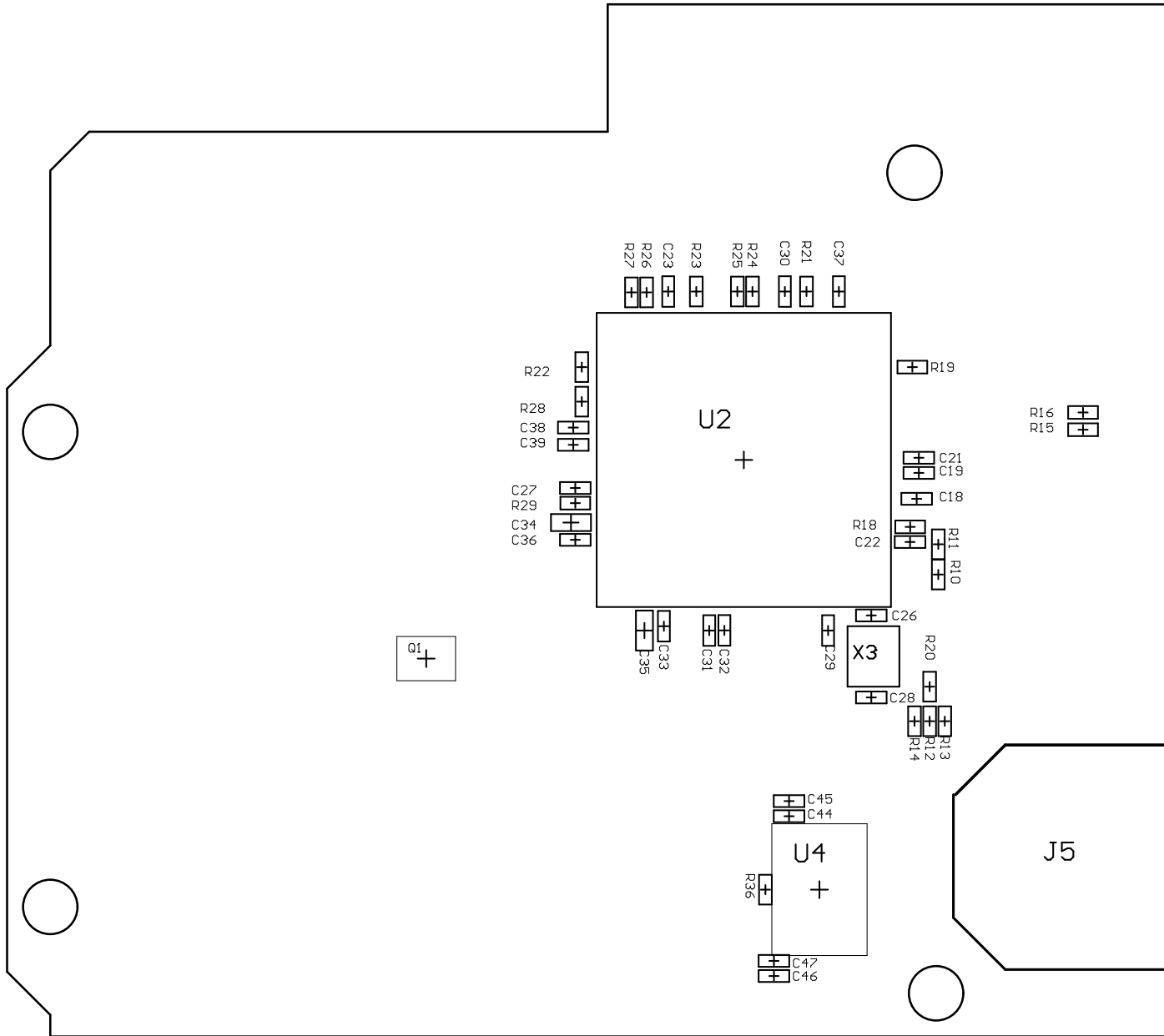
Notes

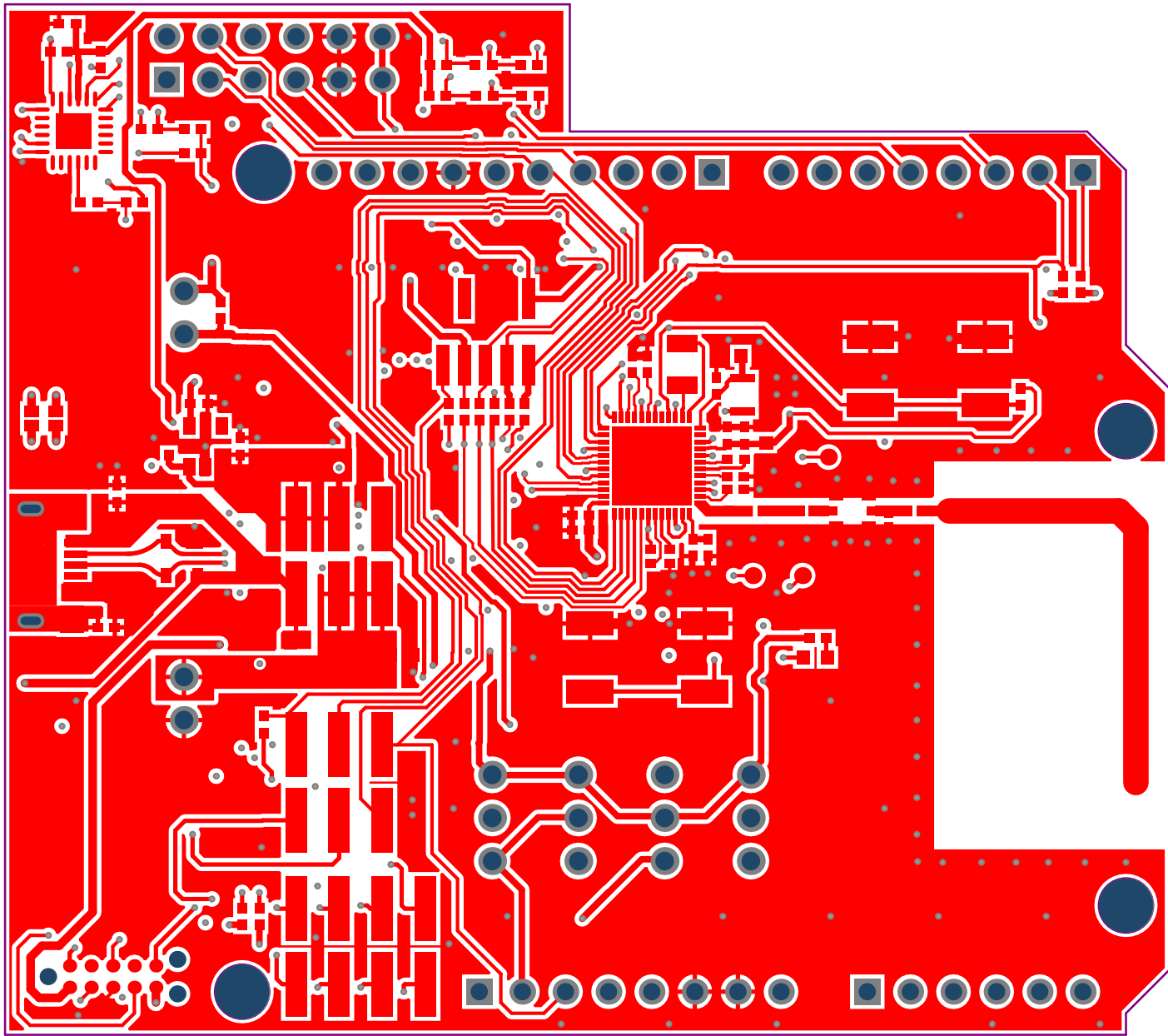
1. Fabricate to IPC6012 Class2.
2. Board material, Isola 370HR RoHS Compliant with nominal thickness of 0.062 INCH, 1/2 OZ copper on top and bottom layers, 1/2 OZ copper on inner layers.
3. Order of layers is Top\_Layer, Signal\_Layer1, Signal\_Layer2, Bottom\_Layer.
4. All dimensions +/- 5 MIL, unless otherwise specified.
5. LDI mask both sides, mask must be between lands. Minimum of 1.5 MIL per side around lands.
6. Silkscreen to be white ink, soldermask green. No ink to be on surface mount land pads. Vendor marking on bottom side.
7. Board to use ENIG (Electroless Nickel Immersion Gold) finish.
8. Board to be 100% tested to Gerber net list file.
9. Include a minimum of two fiducias per panel.
10. Controlled impedance board: Top\_Layer-microstrip,Signal\_Layer1-gnd.RF1 microstrip (25mil) traces on top layer shall be 50 ohms +/-10%.
11. USB Diff pair controlled impedance to be 90 ohm +/-10%, DHSD\_N and DHSD\_P traces.
12. Minimum copper hole wall plating 1 MIL.
13. Maximum warp/twist 0.005 INCH per INCH.
14. Finish all conductors +0.000/-0.002 from supplied artwork.

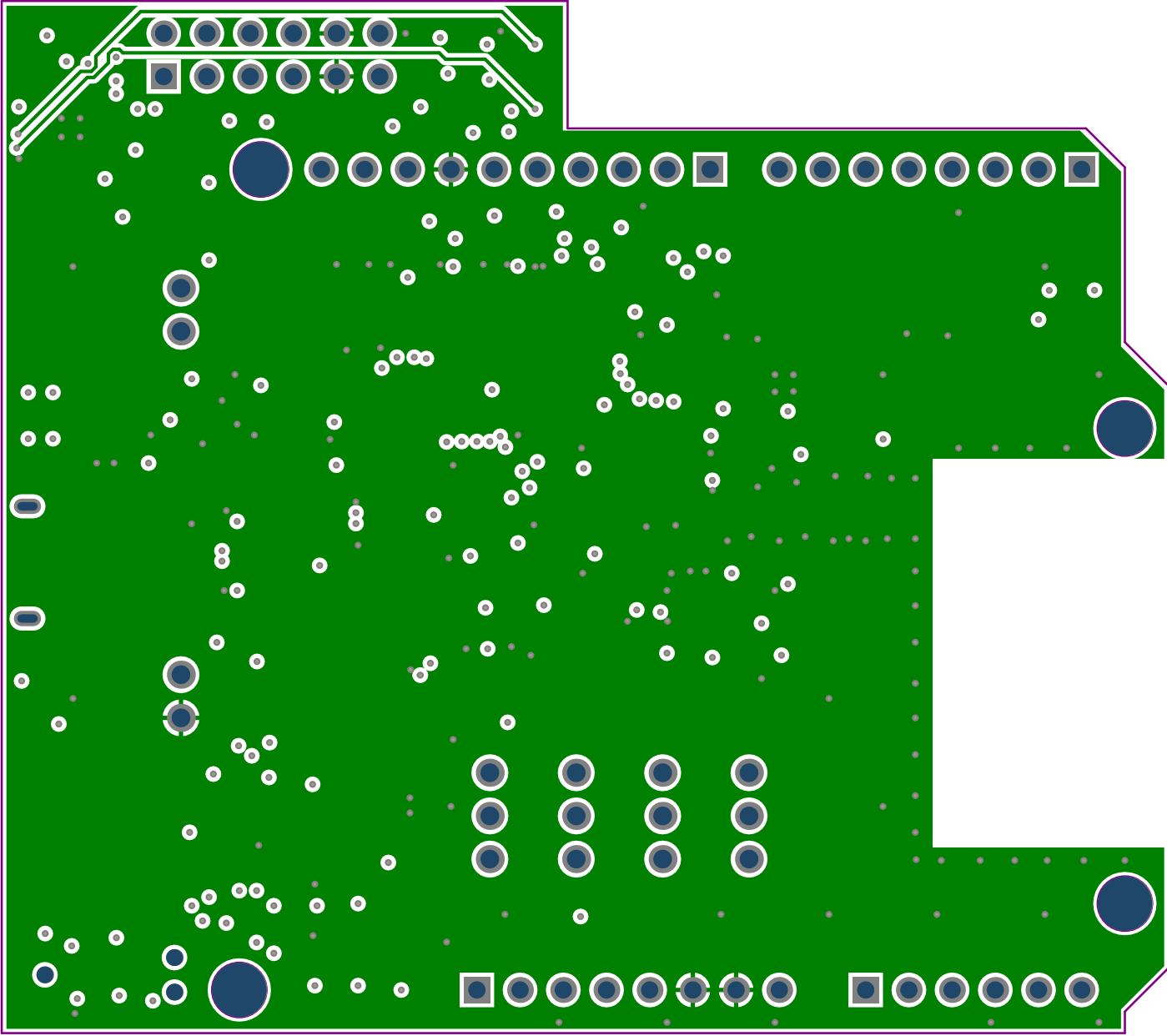
THE INFORMATION CONTAINED IN THIS DRAWING IS THE SOLE PROPERTY OF ON SEMICONDUCTOR. ANY REPRODUCTION IN PART OR AS A WHOLE WITHOUT THE WRITTEN PROPRIETARY AND CONFIDENTIAL

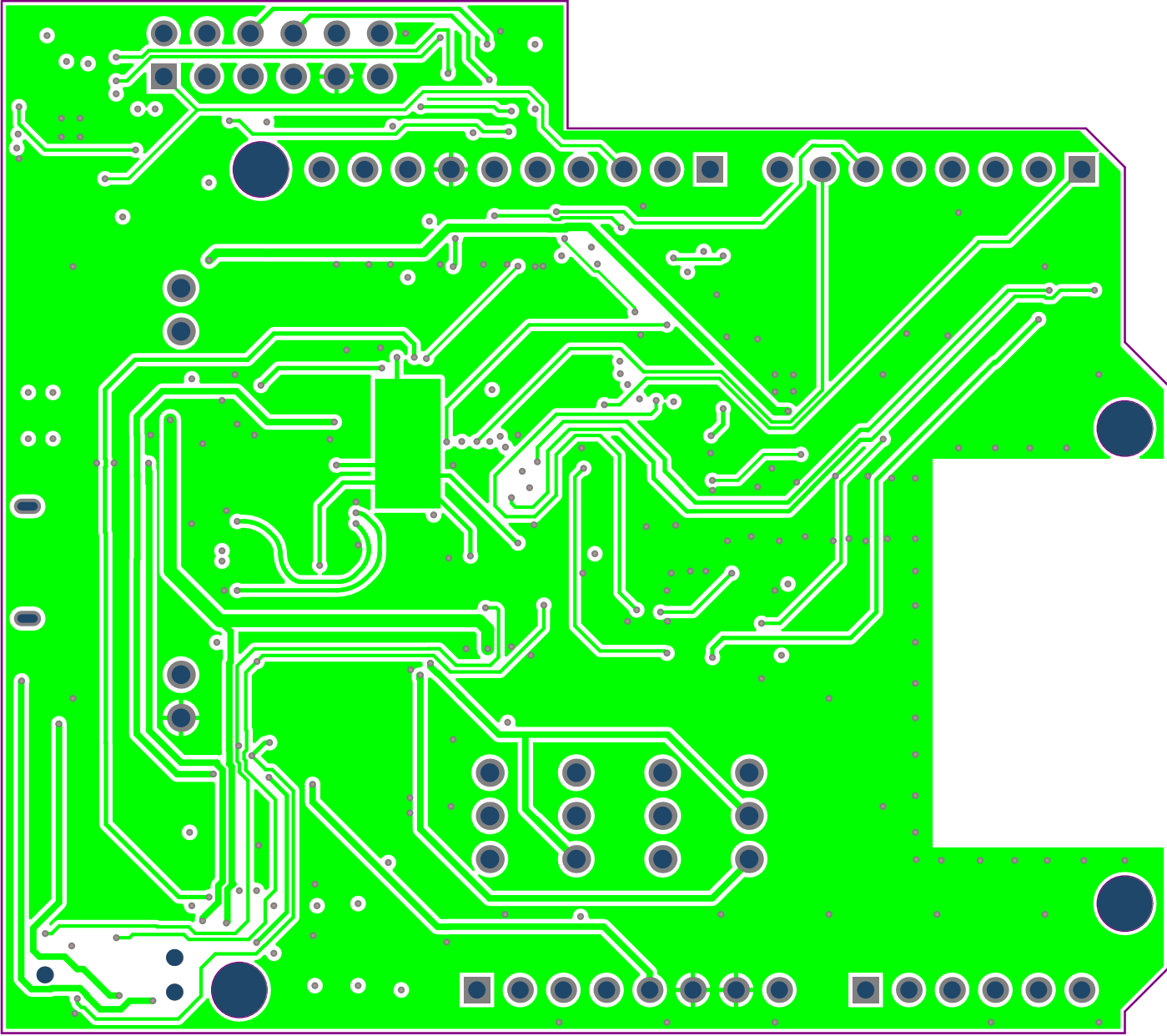
|             |  |                                      |  |           |           |           |                        |  |
|-------------|--|--------------------------------------|--|-----------|-----------|-----------|------------------------|--|
|             |  | UNLESS OTHERWISE SPECIFIED:          |  | NAME      | DATE      | ON        | ON SEMICONDUCTOR       |  |
|             |  | DIMENSIONS ARE IN INCHES             |  | DRAWN     | Marius C. | 6/28/2017 | TITLE                  |  |
|             |  | TOLERANCES:                          |  | CHECKED   |           |           | RSL10 QFN IoT EVB V1.0 |  |
|             |  | FRACTIONAL ±                         |  | ENG APPR. |           |           |                        |  |
|             |  | ANGULAR: MACH ± BEND ±               |  | MFG APPR. |           |           |                        |  |
|             |  | TWO PLACE DECIMAL ±                  |  |           |           |           | SIZE                   |  |
|             |  | THREE PLACE DECIMAL ±                |  |           |           |           | DWG. NO.               |  |
|             |  | INTERPRET GEOMETRIC TOLERANCING PER: |  |           |           |           | TBD                    |  |
|             |  | MATERIAL                             |  |           |           |           |                        |  |
|             |  | FINISH                               |  |           |           |           |                        |  |
|             |  | DO NOT SCALE DRAWING                 |  |           |           |           |                        |  |
| NEXT ASSY   |  | USED ON                              |  |           |           |           | SCALE: 1:1             |  |
| APPLICATION |  |                                      |  |           |           |           | WEIGHT:                |  |
|             |  |                                      |  |           |           |           | SHEET 1 OF 1           |  |

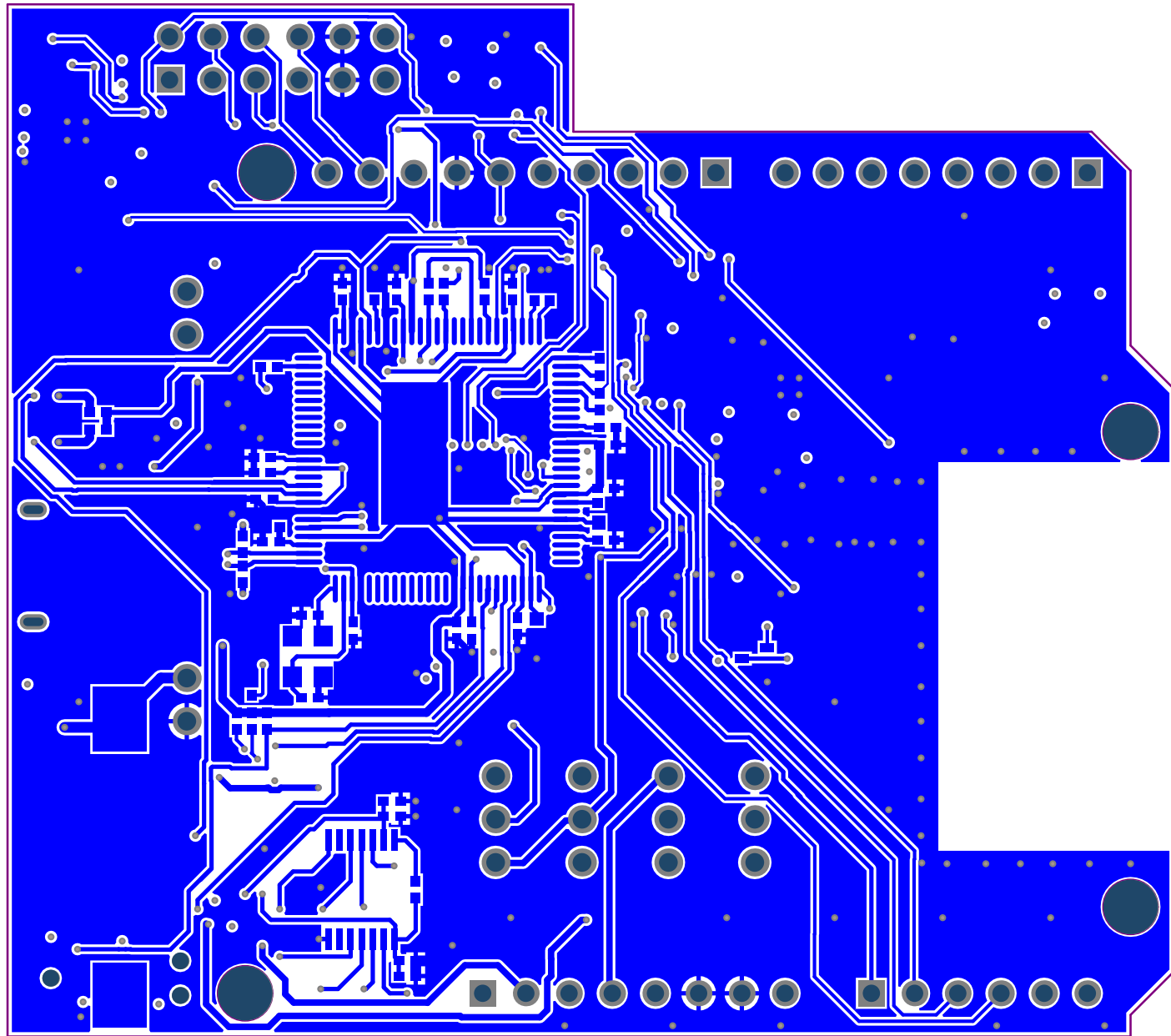














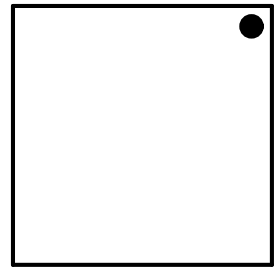


ON Semiconductor  
RSL10 QFN IoT EVB V1.0  
June 2017

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C37  
R21  
C30  
R25  
C23  
R23  
R29

C38  
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R22  
R28  
C27  
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C34  
C36



U2  
C19

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R11  
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R16  
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C26  
C29  
C28

R20  
R13  
R12  
R14

J5

C45  
C44



C47  
C46

Q1

