

SN54ALS241C, SN54AS241A, SN74ALS241C, SN74AS241A

OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SDAS153E – DECEMBER 1982 – REVISED AUGUST 1995

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- pnp Inputs Reduce dc Loading
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

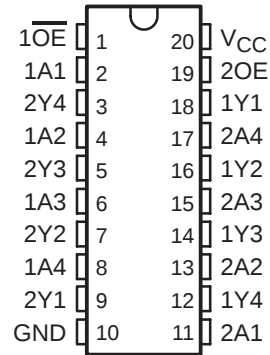
description

These octal buffers/drivers are designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable ($\overline{OE}$) inputs, and complementary OE and $\overline{OE}$ inputs. These devices feature high fan-out and improved fan-in.

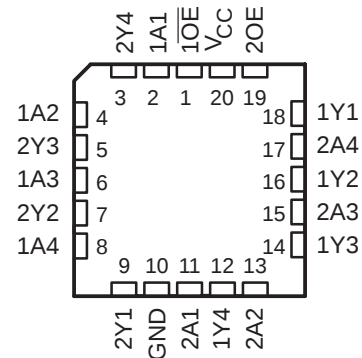
The -1 version of SN74ALS241C is identical to the standard version, except that the recommended maximum I_{OL} of the -1 version is 48 mA. There is no -1 version of the SN54ALS241C.

The SN54ALS241C and SN54AS241A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS241C and SN74AS241A are characterized for operation from 0°C to 70°C .

SN54ALS241C, SN54AS241A . . . J PACKAGE
SN74ALS241C, SN74AS241A . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS241C, SN54AS241A . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLES

INPUTS		OUTPUT
$\overline{1OE}$	1A	1Y
L	H	H
L	L	L
H	X	Z

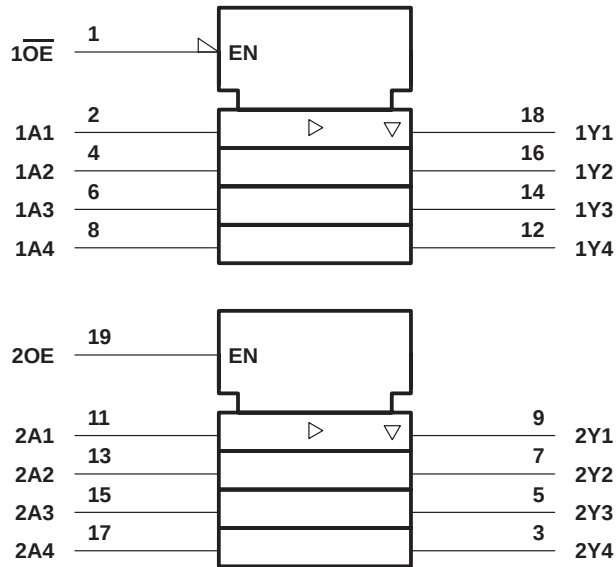
INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

SN54ALS241C, SN54AS241A, SN74ALS241C, SN74AS241A

OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

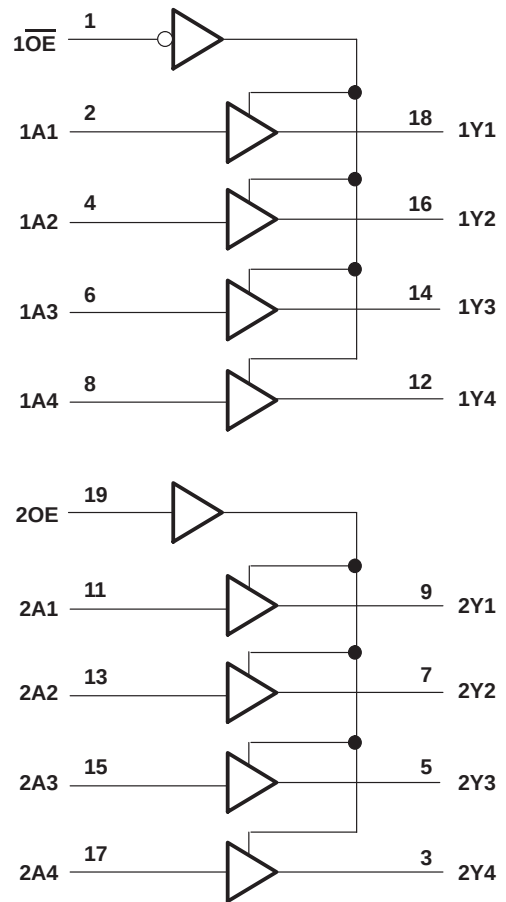
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A : SN54ALS241C	-55°C to 125°C
SN74ALS241C	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN54ALS241C, SN54AS241A, SN74ALS241C, SN74AS241A

OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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recommended operating conditions

		SN54ALS241C			SN74ALS241C			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-12			-15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	-55		125	0		70	°C

† Applies only to the -1 version and only if V_{CC} is between 4.75 V and 5.25 V

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS241C			SN74ALS241C			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V,	$I_{OH} = -0.4$ mA	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5$ V	$I_{OH} = -3$ mA	2.4	3.2		2.4	3.2		
		$I_{OH} = -12$ mA	2						
		$I_{OH} = -15$ mA				2			
V_{OL}	$V_{CC} = 4.5$ V	$I_{OL} = 12$ mA	0.25	0.4		0.25	0.4		V
		$I_{OL} = 24$ mA				0.35	0.5		
		$I_{OL} = 48$ mA (-1 version)				0.35	0.5		
I_{OZH}	$V_{CC} = 5.5$ V,	$V_O = 2.7$ V			20			20	μA
I_{OZL}	$V_{CC} = 5.5$ V,	$V_O = 0.4$ V			-20			-20	μA
I_I	$V_{CC} = 5.5$ V,	$V_I = 7$ V			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			20			20	μA
I_{IL}	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V			-0.1			-0.1	mA
I_O^S	$V_{CC} = 5.5$ V,	$V_O = 2.25$ V	-20		-112	-30		-112	mA
I_{CC}	$V_{CC} = 5.5$ V	Outputs high	9	17		9	18		mA
		Outputs low	15	28		15	26		
		Outputs disabled	17	32		17	30		

‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .



SN54ALS241C, SN54AS241A, SN74ALS241C, SN74AS241A

OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54ALS241C		SN74ALS241C		
			MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	3	31	2	11	ns
t _{PHL}			1	17	3	10	
t _{PZH}	1OE	Y	3	33	3	21	ns
t _{PZL}			3	27	4	21	
t _{PHZ}	1OE	Y	2	17	1	10	ns
t _{PLZ}			2	32	2	15	
t _{PZH}	2OE	Y	3	38	4	21	ns
t _{PZL}			3	30	5	21	
t _{PHZ}	2OE	Y	2	17	2	10	ns
t _{PLZ}			3	35	3	15	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V _{CC}	7 V
Input voltage, V _I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T _A : SN54AS241A	–55°C to 125°C
SN74AS241A	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS241A			SN74AS241A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			–12			–15	mA
I _{OL}	Low-level output current			48			64	mA
T _A	Operating free-air temperature	–55		125	0		70	°C



SN54ALS241C, SN54AS241A, SN74ALS241C, SN74AS241A

OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS241A			SN74AS241A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = −18 mA		−1.2			−1.2			V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = −2 mA		V _{CC} − 2			V _{CC} − 2			V
	V _{CC} = 4.5 V	I _{OH} = −3 mA	2.4	3.4	2.4	3.4			
		I _{OH} = −12 mA	2.4						
		I _{OH} = −15 mA		2.4					
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 48 mA	0.27	0.55					V
		I _{OL} = 64 mA	0.31 0.55						
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V		50			50			μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V		−50			−50			μA
I _I	V _{CC} = 5.5 V, V _I = 7 V		0.1			0.1			mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V		20			20			μA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V		−1			−1			mA
I _O ‡	V _{CC} = 5.5 V, V _O = 2.25 V		−50	−150	−50	−150			mA
I _{CC}	V _{CC} = 5.5 V	Outputs high	22	35	22	35			mA
		Outputs low	61	90	61	90			
		Outputs disabled	35	56	35	56			

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX§				UNIT
			SN54AS241A		SN74AS241A		
			MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	2	9	2	6.2	ns
t _{PHL}			1	7	1	6.2	
t _{PZH}	1OE	Y	1	10	1	9	ns
t _{PZL}			2	8	2	7.5	
t _{PHZ}	1OE	Y	1	6.5	1	6	ns
t _{PLZ}			1	10.5	1	9	
t _{PZH}	2OE	Y	2	11	2	10.5	ns
t _{PZL}			3	9.5	3	8.5	
t _{PHZ}	2OE	Y	1	7	1	7	ns
t _{PLZ}			2	12	2	12	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS241C, SN54AS241A, SN74ALS241C, SN74AS241A

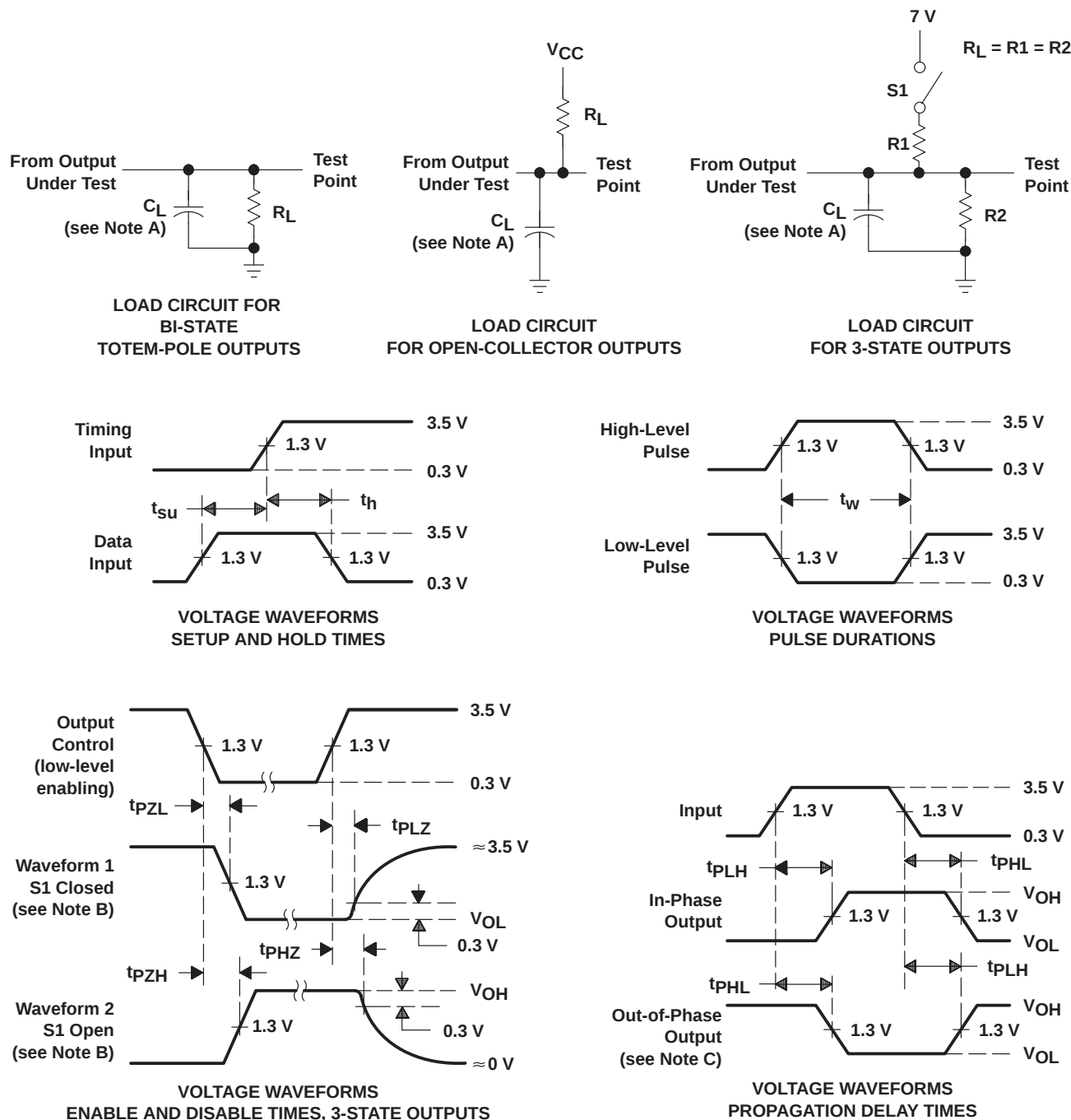
OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION

SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - When measuring propagation delay items of 3-state outputs, switch S1 is open.
 - All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/38302BRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type		JM38510/ 38302BRA	Samples
M38510/38302BRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 38302BRA	Samples
SN54ALS241CJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SN54ALS241CJ	Samples
SN54AS241AJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SN54AS241AJ	Samples
SN74ALS241CDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS241C	Samples
SN74ALS241CDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS241C	Samples
SN74ALS241CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS241CN	Samples
SN74AS241AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	0 to 70	SN74AS241AN	Samples
SNJ54ALS241CFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54 ALS241CFK	Samples
SNJ54ALS241CJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SNJ54ALS241CJ	Samples
SNJ54AS241AJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SNJ54AS241AJ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- ⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- ⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- ⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- ⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54ALS241C, SN54AS241A, SN74ALS241C, SN74AS241A :

- Catalog: [SN74ALS241C](#), [SN74AS241A](#)
- Military: [SN54ALS241C](#), [SN54AS241A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS241CDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS241CDWR	SOIC	DW	20	2000	367.0	367.0	45.0

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



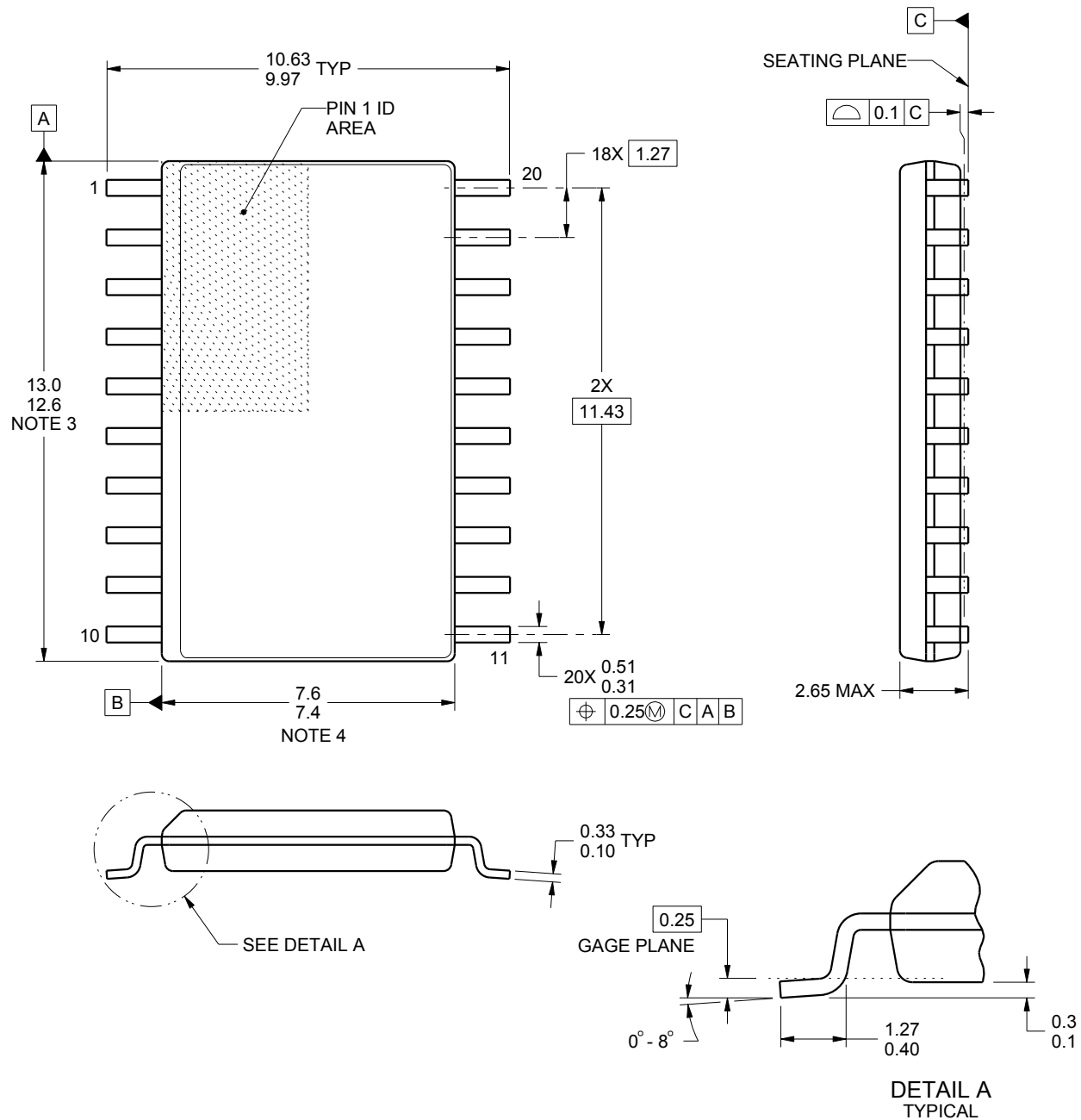
PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220724/A 05/2016

NOTES:

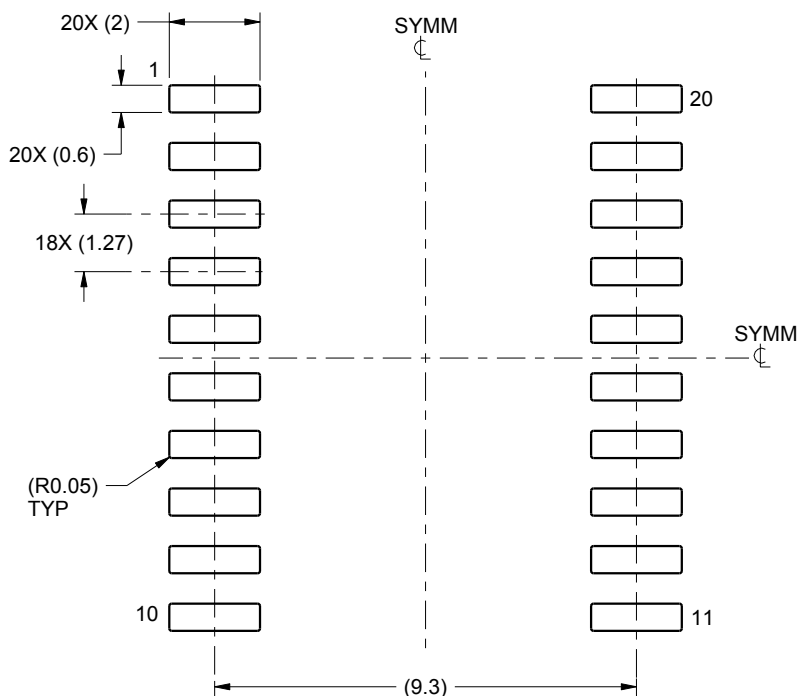
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

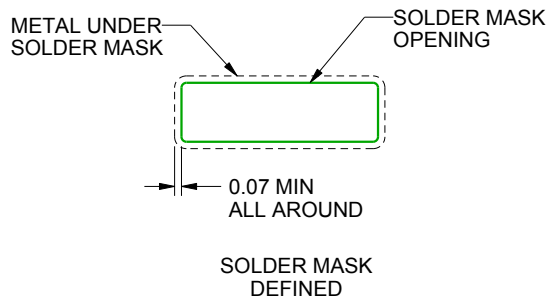
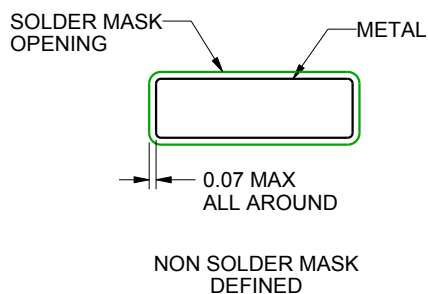
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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