TCA6424 Low-Voltage 24-Bit I^2C AND SMBus I/O Expander With Interrupt Output, Reset, and Configuration Registers

Not Recommended for New Designs

1 Features

- Operating Power-Supply Voltage Range of 1.65 V to 5.5 V
- Allows Bidirectional Voltage-Level Translation and GPIO Expansion Between:
  - 1.8-V SCL/SDA and 1.8-V, 2.5-V, 3.3-V, or 5-V P Port
  - 2.5-V SCL/SDA and 1.8-V, 2.5-V, 3.3-V, or 5-V P Port
  - 3.3-V SCL/SDA and 1.8-V, 2.5-V, 3.3-V, or 5-V P Port
  - 5-V SCL/SDA and 1.8-V, 2.5-V, 3.3-V, or 5-V P Port
- I^2C to Parallel Port Expander
- Low Standby Current Consumption of 1 µA
- Schmitt-Trigger Action Allows Slow Input Transition and Better Switching Noise Immunity at the SCL and SDA Inputs
  - V_{hys} = 0.18 V Typ at 1.8 V
  - V_{hys} = 0.25 V Typ at 2.5 V
  - V_{hys} = 0.33 V Typ at 3.3 V
  - V_{hys} = 0.5 V Typ at 5 V
- 5-V Tolerant I/O Ports
- Active-Low Reset ($\overline{RESET}$) Input
- Open-Drain Active-Low Interrupt ($\overline{INT}$) Output
- 400-kHz Fast I^2C Bus
- Input/Output Configuration Register
- Polarity Inversion Register
- Internal Power-On Reset
- Power Up With All Channels Configured as Inputs
- No Glitch On Power Up
- Noise Filter on SCL/SDA Inputs
- Latched Outputs With High-Current Drive Maximum Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Description

This 24-bit I/O expander for the two-line bidirectional bus (I^2C) is designed to provide general-purpose remote I/O expansion for most microcontroller families via the I^2C interface [serial clock (SCL) and serial data (SDA)].

The major benefit of this device is its wide V_{CC} range. It can operate from 1.65 V to 5.5 V on the P-port side and on the SDA/SCL side. This allows the TCA6424 to interface with next-generation microprocessors and microcontrollers on the SDA/SCL side, where supply levels are dropping down to conserve power. In contrast to the dropping power supplies of microprocessors and microcontrollers, some PCB components, such as LEDs, remain at a 5-V power supply.

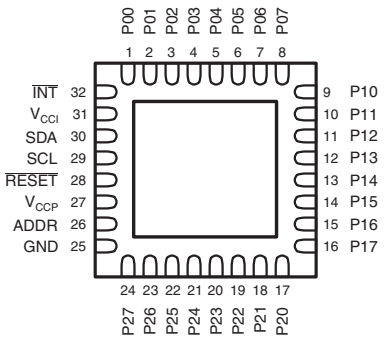
The bidirectional voltage level translation in the TCA6424 is provided through V_{CCI}. V_{CCI} should be connected to the V_{CC} of the external SCL/SDA lines. This indicates the V_{CC} level of the I^2C bus to the TCA6424. The voltage level on the P-port of the TCA6424 is determined by the V_{CCP}.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TCA6424	UQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

RGJ PACKAGE
(BOTTOM VIEW)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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3 Revision History

Changes from Revision A (November 2009) to Revision B **Page**

- Added $\overline{\text{RESET}}$ Errata section. ... 17
- Added Interrupt Errata section ... 18

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4 Description (Continued)

The TCA6424 consists of three 8-bit Configuration (input or output selection), Input, Output, and Polarity Inversion (active high) registers. At power on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The system master can reset the TCA6424 in the event of a timeout or other improper operation by asserting a low in the $\overline{\text{RESET}}$ input. The power-on reset puts the registers in their default state and initializes the I^2C/SMBus state machine. The $\overline{\text{RESET}}$ pin causes the same reset/initialization to occur without depowering the part.

The TCA6424 open-drain interrupt ($\overline{\text{INT}}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

$\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^2C bus. Thus, the TCA6424 can remain a simple slave device.

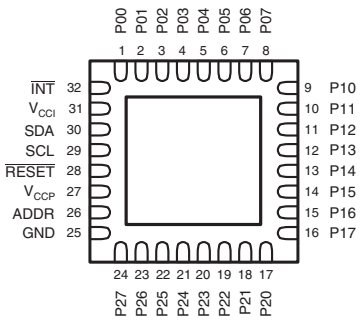
The device P-port outputs have high-current sink capabilities for directly driving LEDs while consuming low device current.

One hardware pin (ADDR) can be used to program and vary the fixed I^2C address and allow up to two devices to share the same I^2C bus or SMBus.

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5 Pin Configuration and Functions

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Pin Functions

TERMINAL		DESCRIPTION
PIN NO.	NAME	
1	P00	P-port input/output (push-pull design structure). At power on, P00 is configured as an input.
2	P01	P-port input/output (push-pull design structure). At power on, P01 is configured as an input.
3	P02	P-port input/output (push-pull design structure). At power on, P02 is configured as an input.
4	P03	P-port input/output (push-pull design structure). At power on, P03 is configured as an input.
5	P04	P-port input/output (push-pull design structure). At power on, P04 is configured as an input.
6	P05	P-port input/output (push-pull design structure). At power on, P05 is configured as an input.
7	P06	P-port input/output (push-pull design structure). At power on, P06 is configured as an input.
8	P07	P-port input/output (push-pull design structure). At power on, P07 is configured as an input.
9	P10	P-port input/output (push-pull design structure). At power on, P10 is configured as an input.
10	P11	P-port input/output (push-pull design structure). At power on, P11 is configured as an input.
11	P12	P-port input/output (push-pull design structure). At power on, P12 is configured as an input.
12	P13	P-port input/output (push-pull design structure). At power on, P13 is configured as an input.
13	P14	P-port input/output (push-pull design structure). At power on, P14 is configured as an input.
14	P15	P-port input/output (push-pull design structure). At power on, P15 is configured as an input.
15	P16	P-port input/output (push-pull design structure). At power on, P16 is configured as an input.
16	P17	P-port input/output (push-pull design structure). At power on, P17 is configured as an input.
17	P20	P-port input/output (push-pull design structure). At power on, P20 is configured as an input.
18	P21	P-port input/output (push-pull design structure). At power on, P21 is configured as an input.
19	P22	P-port input/output (push-pull design structure). At power on, P22 is configured as an input.
20	P23	P-port input/output (push-pull design structure). At power on, P23 is configured as an input.
21	P24	P-port input/output (push-pull design structure). At power on, P24 is configured as an input.
22	P25	P-port input/output (push-pull design structure). At power on, P25 is configured as an input.
23	P26	P-port input/output (push-pull design structure). At power on, P26 is configured as an input.
24	P27	P-port input/output (push-pull design structure). At power on, P27 is configured as an input.
25	GND	Ground
26	ADDR	Address input. Connect directly to V_{CCP} or ground.
27	V_{CCP}	Supply voltage of TCA6424 for P port
28	$\overline{RESET}$	Active-low reset input. Connect to V_{CCP} through a pullup resistor, if no active connection is used.
29	SCL	Serial clock bus. Connect to V_{CCI} through a pullup resistor.
30	SDA	Serial data bus. Connect to V_{CCI} through a pullup resistor.
31	V_{CCI}	Supply voltage of I^2C bus. Connect directly to the V_{CC} of the external I^2C master. Provides voltage-level translation.
32	$\overline{INT}$	Interrupt output. Connect to V_{CCI} through a pullup resistor.

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6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{CCI}	Supply voltage range			–0.5	6.5	V
V_{CCP}	Supply voltage range			–0.5	6.5	V
V_I	Input voltage range(2)			–0.5	6.5	V
V_O	Output voltage range(2)			–0.5	6.5	V
I_{IK}	Input clamp current	ADDR, $\overline{RESET}$, SCL	$V_I < 0$		±20	mA
I_{OK}	Output clamp current	$\overline{INT}$	$V_O < 0$		±20	mA
I_{IOK}	Input/output clamp current	P port	$V_O < 0$ or $V_O > V_{CCP}$		±20	mA
		SDA	$V_O < 0$ or $V_O > V_{CCI}$		±20	
I_{OL}	Continuous output low current	P port	V_O = 0 to V_{CCP}		25	mA
		SDA, $\overline{INT}$	V_O = 0 to V_{CCI}		15	
I_{OH}	Continuous output high current	P port	V_O = 0 to V_{CCP}		25	mA
I_{CC}	Continuous current through GND				200	mA
	Continuous current through V_{CCP}				160	
	Continuous current through V_{CCI}				10	
θ_{JA}	Package thermal impedance(3)		RGJ package		50.05	°C/W

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CCI}	Supply voltage		1.65	5.5	V
V_{CCP}	Supply voltage		1.65	5.5	
V_{IH}	High-level input voltage	SCL, SDA	0.7 × V_{CCI}	5.5	V
		ADDR, P27–P00, $\overline{RESET}$	0.7 × V_{CCP}	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	0.3 × V_{CCI}	V
		ADDR, P27–P00, $\overline{RESET}$	–0.5	0.3 × V_{CCP}	
I_{OH}	High-level output current	P27–P00		10	mA
I_{OL}	Low-level output current	P27–P00		25	mA
T_A	Operating free-air temperature		–40	85	°C

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6.4 Electrical Characteristics

over recommended operating free-air temperature range, V_{CCI} = 1.65 V to 5.5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CCP}	MIN	TYP(1)	MAX	UNIT
V_{IK}	Input diode clamp voltage		I_I = –18 mA	1.65 V to 5.5 V	–1.2			V
V_{POR}	Power-on reset voltage		$V_I = V_{CCP}$ or GND, I_O = 0	1.65 V to 5.5 V		1	1.4	V
V_{OH}	P-port high-level output voltage		I_{OH} = –8 mA	1.65 V	1.2			V
				2.3 V	1.8			
				3 V	2.6			
				4.5 V	4.1			
			I_{OH} = –10 mA	1.65 V	1			
				2.3 V	1.7			
				3 V	2.5			
				4.5 V	4.0			
V_{OL}	P-port low-level output voltage		I_{OL} = 8mA	1.65 V			0.45	V
				2.3 V			0.25	
				3 V			0.25	
				4.5 V			0.23	
			I_{OL} = 10 mA	1.65 V			0.6	
				2.3 V			0.3	
				3 V			0.25	
				4.5 V			0.24	
I_{OL}	SDA		V_{OL} = 0.4 V	1.65 V to 5.5 V	3			mA
	$\overline{INT}$		V_{OL} = 0.4 V	1.65 V to 5.5 V	3	15		
I_I	SCL, SDA		$V_I = V_{CCI}$ or GND	1.65 V to 5.5 V			±0.1	µA
	ADDR, $\overline{RESET}$		$V_I = V_{CCP}$ or GND				±0.1	
I_{IH}	P port		$V_I = V_{CCP}$	1.65 V to 5.5 V			1	µA
I_{IL}	P port		V_I = GND				1	µA
I_{CC} (I_{CCP} + I_{CCI})	Operating mode	SDA, P port, ADDR, $\overline{RESET}$	V_I on SDA = V_{CCI} or GND, V_I on P port, ADDR and $\overline{RESET}$ = V_{CCP}, I_O = 0, I/O = inputs, f_{SCL} = 400 kHz	1.65 V to 5.5 V		8	30	µA
		SDA, P port, ADDR, $\overline{RESET}$	V_I on SDA = V_{CCI} or GND, V_I on P port, ADDR and $\overline{RESET}$ = V_{CCP}, I_O = 0, I/O = inputs, f_{SCL} = 100 kHz	1.65 V to 5.5 V		1.7	10	
	Standby mode	SCL, SDA, P port, ADDR, $\overline{RESET}$	V_I on SCL and SDA = V_{CCI} or GND, V_I on P port, ADDR and $\overline{RESET}$ = V_{CCP}, I_O = 0, I/O = inputs, f_{SCL} = 0	1.65 V to 5.5 V		0.1	2	
ΔI_{CCI}	Additional current in Standby mode	SCL, SDA	One input at V_{CCI} – 0.6 V, Other inputs at V_{CCI} or GND	1.65 V to 5.5 V			25	µA
ΔI_{CCP}		P port, ADDR, $\overline{RESET}$	One input at V_{CCP} – 0.6 V, Other inputs at V_{CCP} or GND				60	
C_I	SCL		$V_I = V_{CCI}$ or GND	1.65 V to 5.5 V		6	7	pF
C_{io}	SDA		$V_{IO} = V_{CCI}$ or GND	1.65 V to 5.5 V		7	8	pF
	P port		$V_{IO} = V_{CCP}$ or GND			7.5	8.5	

(1) Except for I_{CC}, all typical values are at nominal supply voltage ($V_{CCP} = V_{CCI}$ =1.8-V, 2.5-V, 3.3-V, or 5-V V_{CC}) and T_A = 25°C. For I_{CC}, all typical values are at $V_{CCP} = V_{CCI}$ = 3.3 V and T_A = 25°C.

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6.5 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 14)

		STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
		MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency	0	100	0	400	kHz
t_{sch}	I²C clock high time	4		0.6		µs
t_{scl}	I²C clock low time	4.7		1.3		µs
t_{sp}	I²C spike time	0	50	0	50	ns
t_{sds}	I²C serial data setup time	250		100		ns
t_{sdh}	I²C serial data hold time	0		0		ns
t_{icr}	I²C input rise time		1000	$20 + 0.1C_b$ (1)	300	ns
t_{icf}	I²C input fall time		300	$20 + 0.1C_b$ (1)	300	ns
t_{ocf}	I²C output fall time; 10 pF to 400 pF bus		300	$20 + 0.1C_b$ (1)	300	µs
t_{buf}	I²C bus free time between Stop and Start	4.7		1.3		µs
t_{sts}	I²C Start or repeater Start condition setup time	4.7		0.6		µs
t_{sth}	I²C Start or repeater Start condition hold time	4		0.6		µs
t_{sps}	I²C Stop condition setup time	4		0.6		µs
$t_{vd(data)}$	Valid data time; SCL low to SDA output valid		1		1	µs
$t_{vd(ack)}$	Valid data time of ACK condition; ACK signal from SCL low to SDA (out) low		1		1	µs

(1) C_b = total capacitance of one bus line in pF

6.6 Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 17)

		STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
		MIN	MAX	MIN	MAX	
t_W	Reset pulse duration	4		4		ns
t_{REC}	Reset recovery time	0		0		ns
t_{RESET}	Time to reset (1)	600		600		ns

(1) Minimum time for SDA to become high or minimum time to wait before doing a START.

6.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (see Figure 14)

PARAMETER		FROM	TO	STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
				MIN	MAX	MIN	MAX	
t_{IV}	Interrupt valid time	P port	$\overline{INT}$		4		4	µs
t_{IR}	Interrupt reset delay time	SCL	$\overline{INT}$		4		4	µs
t_{PV}	Output data valid	SCL	P27–P00		400		400	ns
t_{PS}	Input data setup time	P port	SCL	0		0		ns
t_{PH}	Input data hold time	P port	SCL	300		300		ns

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6.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

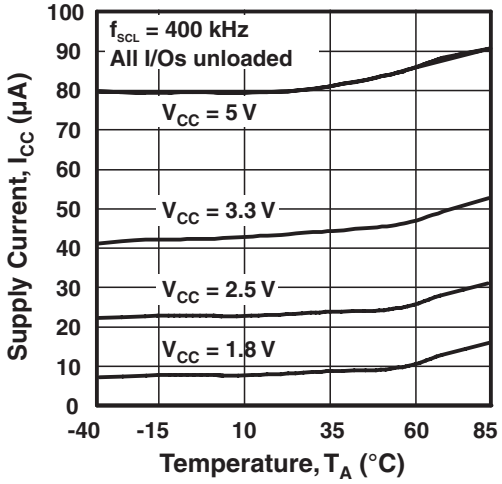


Figure 1. Supply Current vs Temperature

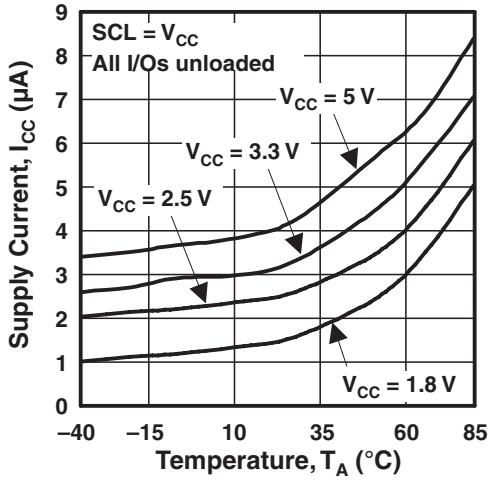


Figure 2. Standby Supply Current vs Temperature

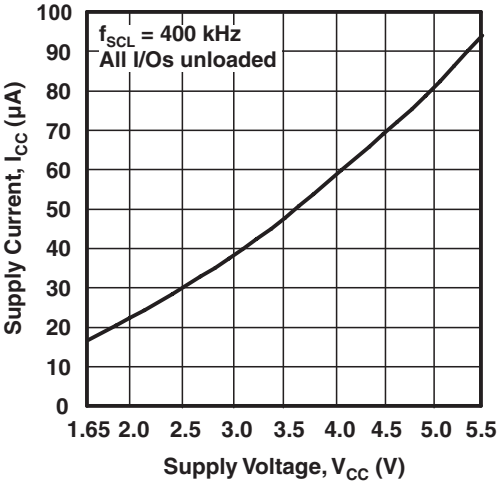


Figure 3. Supply Current vs Supply Voltage

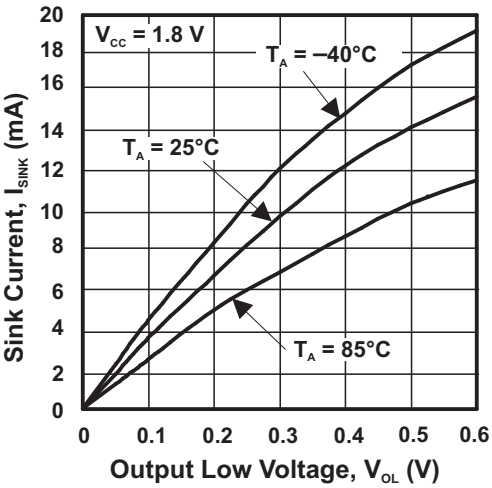


Figure 4. I/O Sink Current vs Output Low Voltage

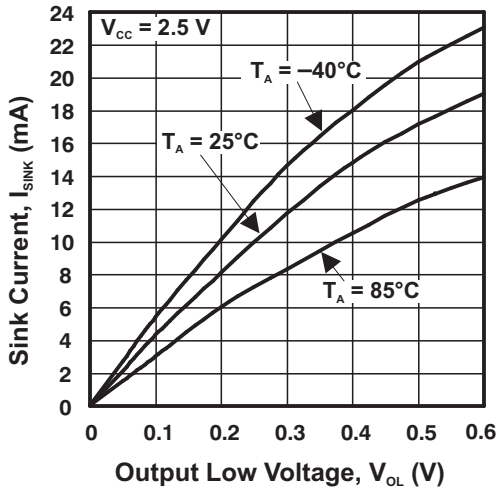


Figure 5. I/O Sink Current vs Output Low Voltage

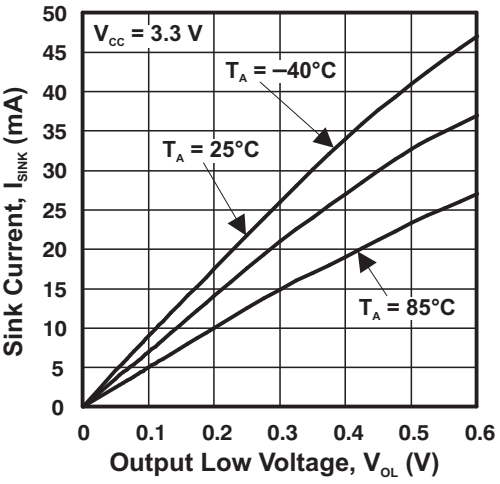


Figure 6. I/O Sink Current vs Output Low Voltage

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Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

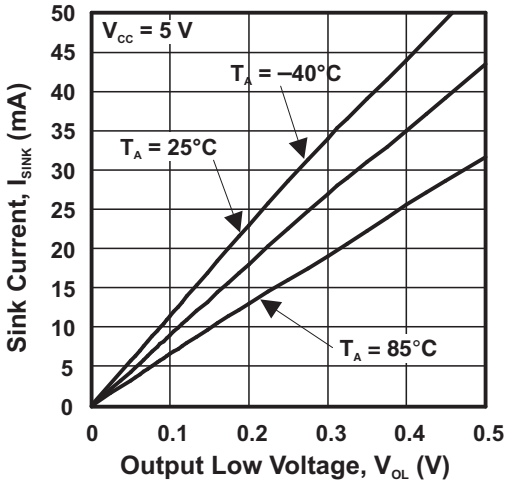


Figure 7. I/O Sink Current vs Output Low Voltage

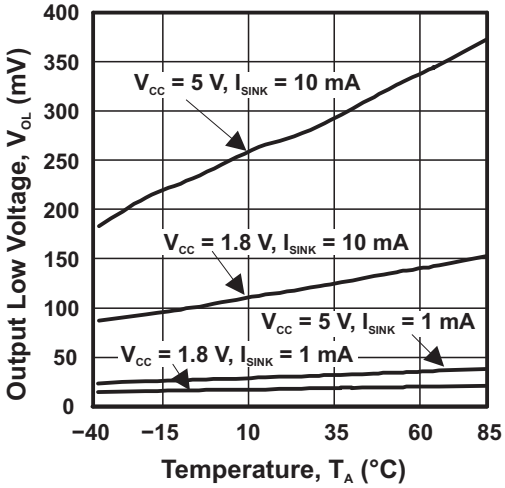


Figure 8. I/O Low Voltage vs Temperature

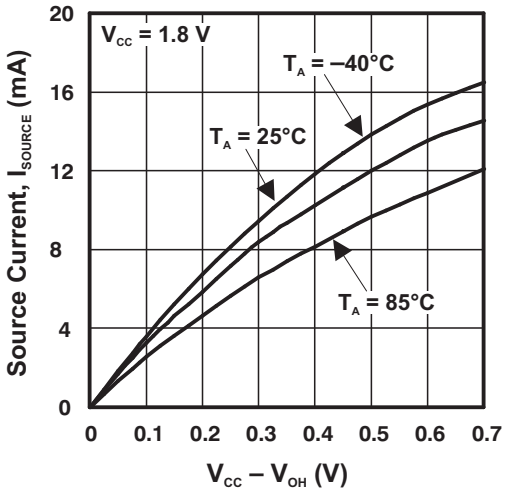


Figure 9. I/O Source Current vs Output High Voltage

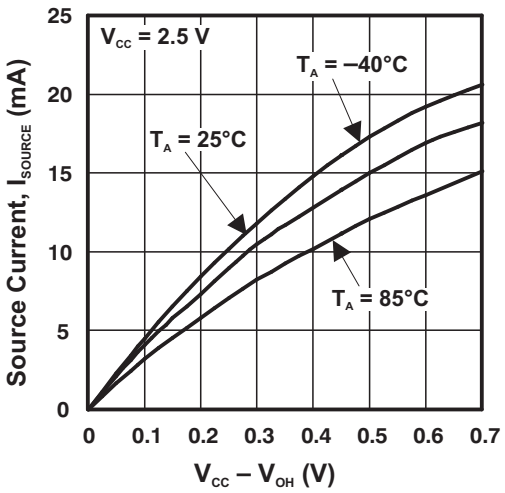


Figure 10. I/O Source Current vs Output High Voltage

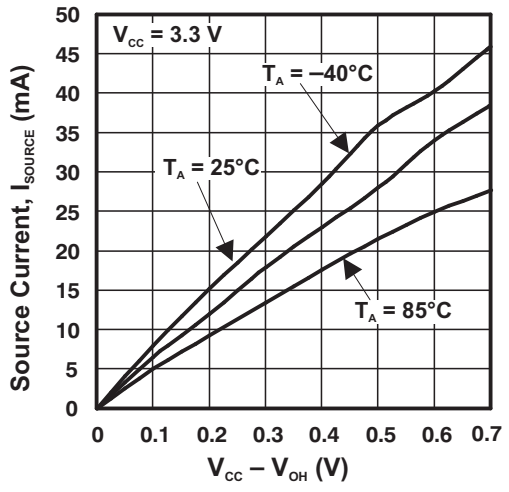


Figure 11. I/O Source Current vs Output High Voltage

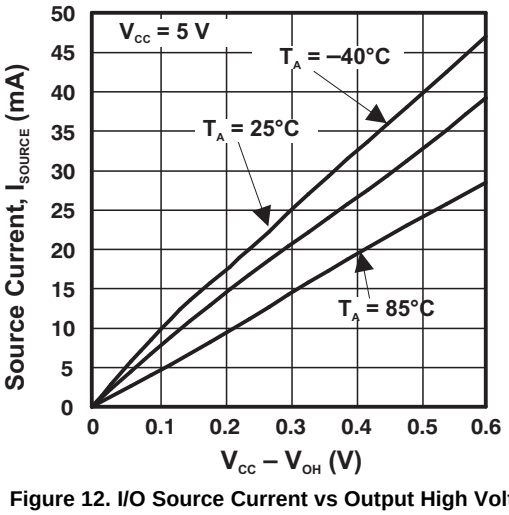


Figure 12. I/O Source Current vs Output High Voltage

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Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

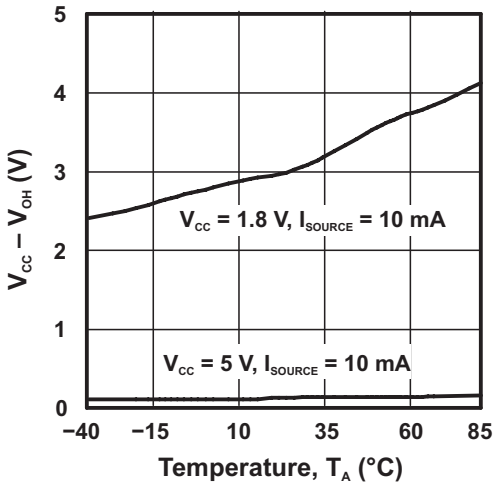
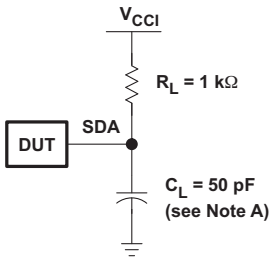


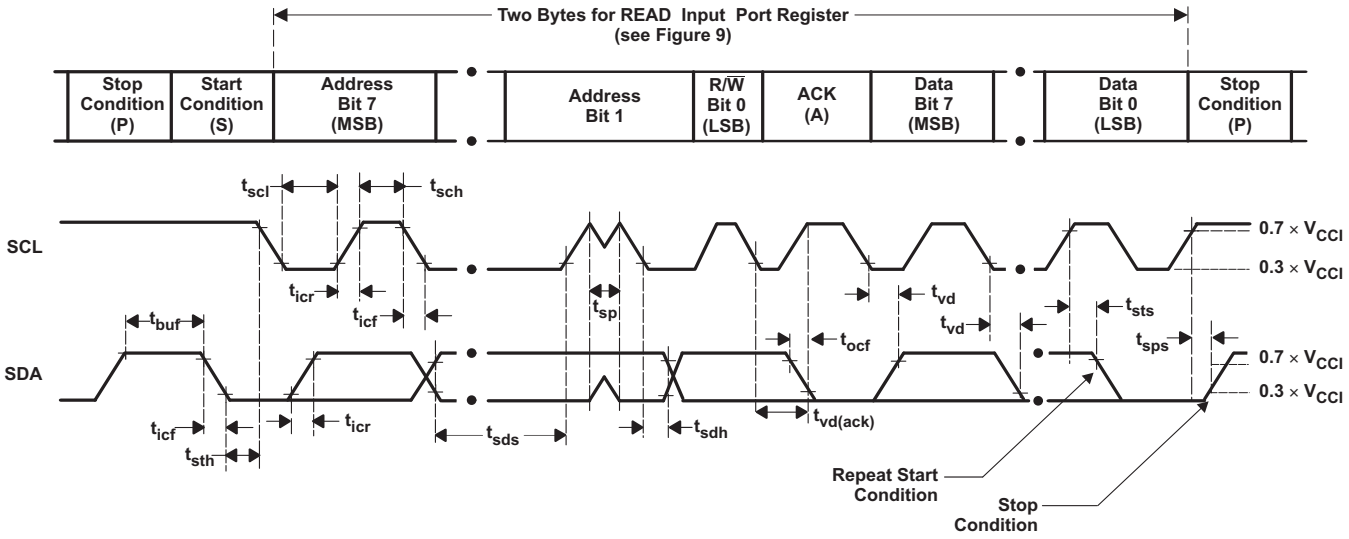
Figure 13. I/O High Voltage vs Temperature

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7 Parameter Measurement Information



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2	Input register port data

A. C_L includes probe and jig capacitance. tocf is measured with C_L of 10 pF or 400 pF.

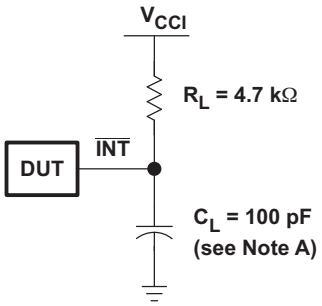
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. All parameters and waveforms are not applicable to all devices.

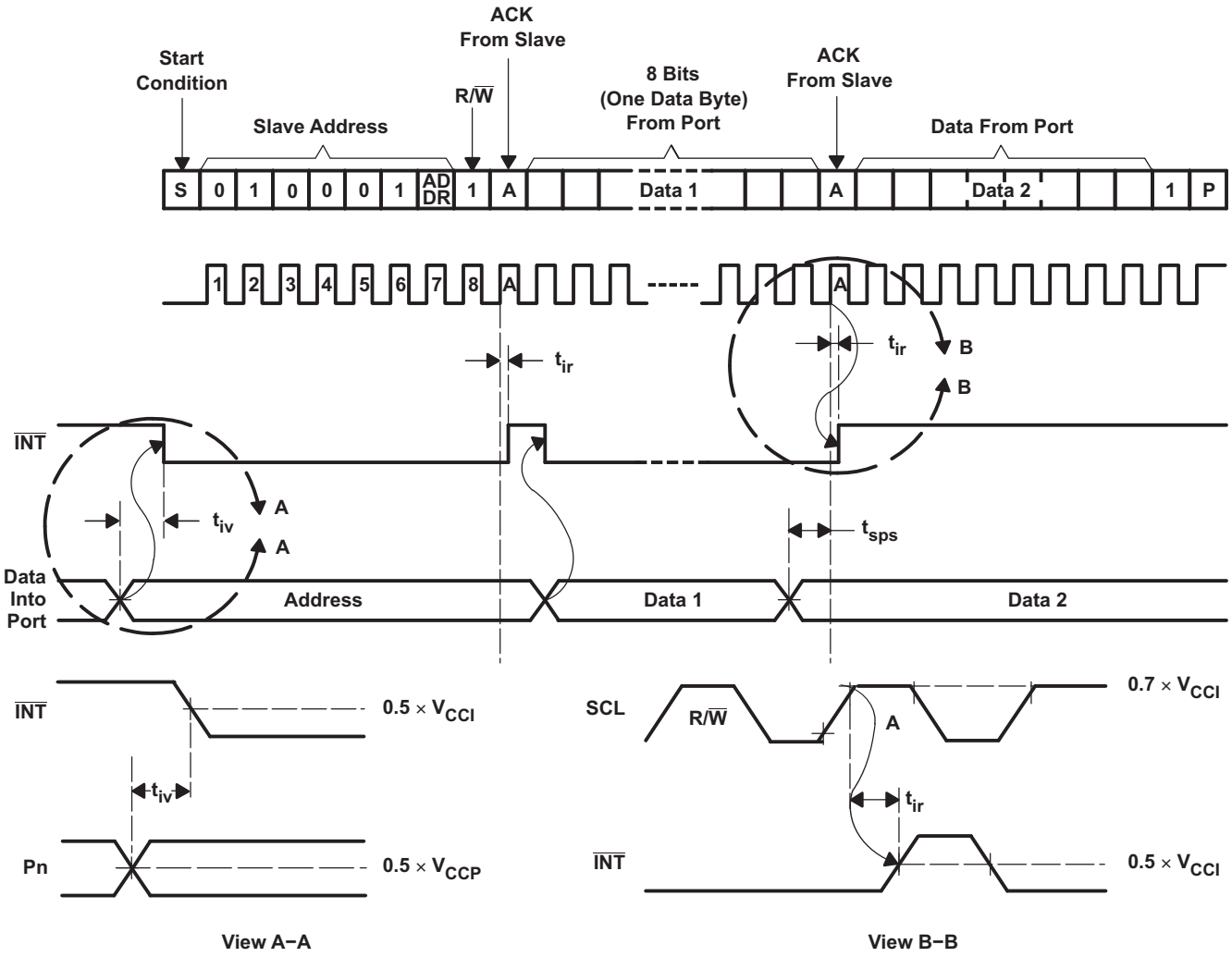
Figure 14. I^2C Interface Load Circuit And Voltage Waveforms

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Parameter Measurement Information (continued)



INTERRUPT LOAD CONFIGURATION



View A–A View B–B

A. C_L includes probe and jig capacitance.

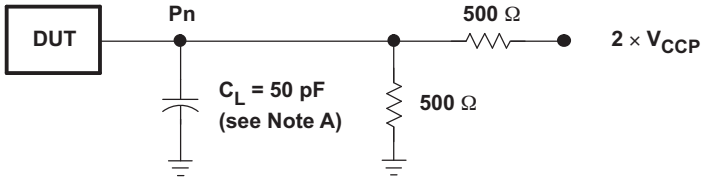
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. All parameters and waveforms are not applicable to all devices.

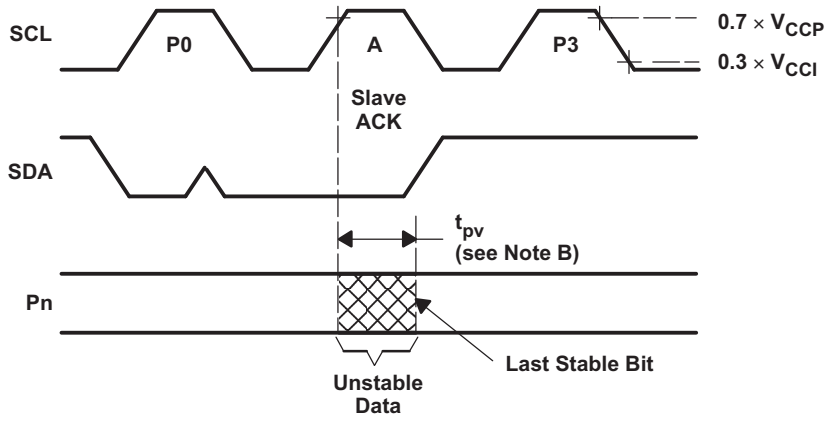
Figure 15. Interrupt Load Circuit And Voltage Waveforms

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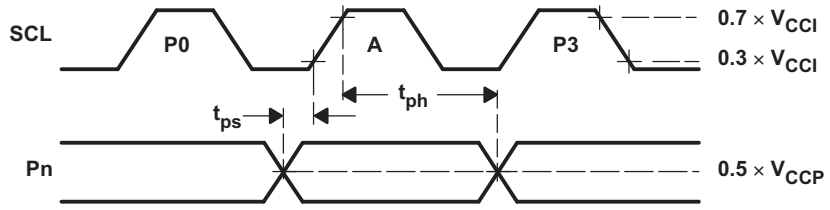
Parameter Measurement Information (continued)



P PORT LOAD CONFIGURATION



WRITE MODE (R/$\overline{W}$ = 0)



READ MODE (R/$\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.

B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output.

C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

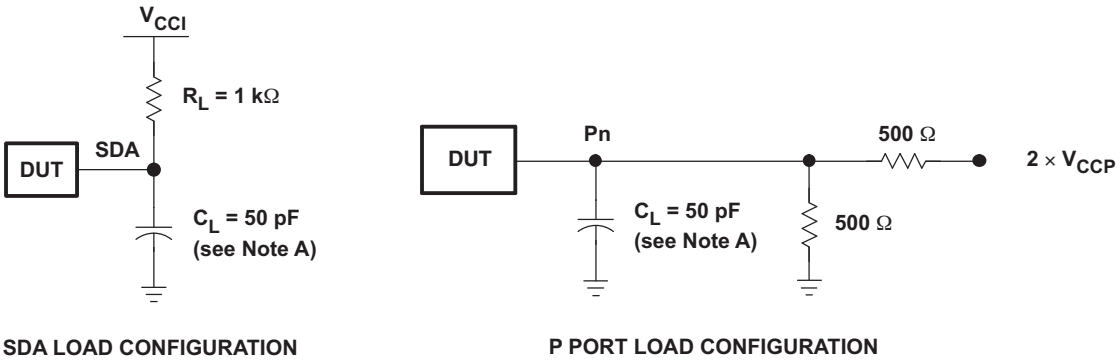
D. The outputs are measured one at a time, with one transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

Figure 16. P-Port Load Circuit And Timing Waveforms

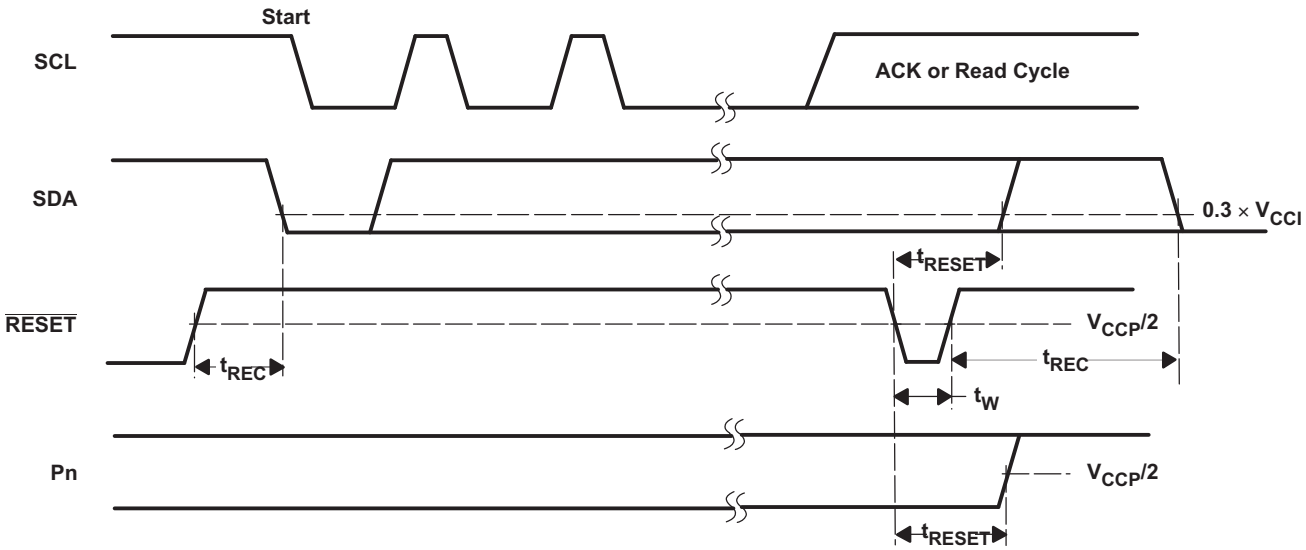
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Parameter Measurement Information (continued)



SDA LOAD CONFIGURATION

P PORT LOAD CONFIGURATION



A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. The outputs are measured one at a time, with one transition per measurement.

D. I/Os are configured as inputs.

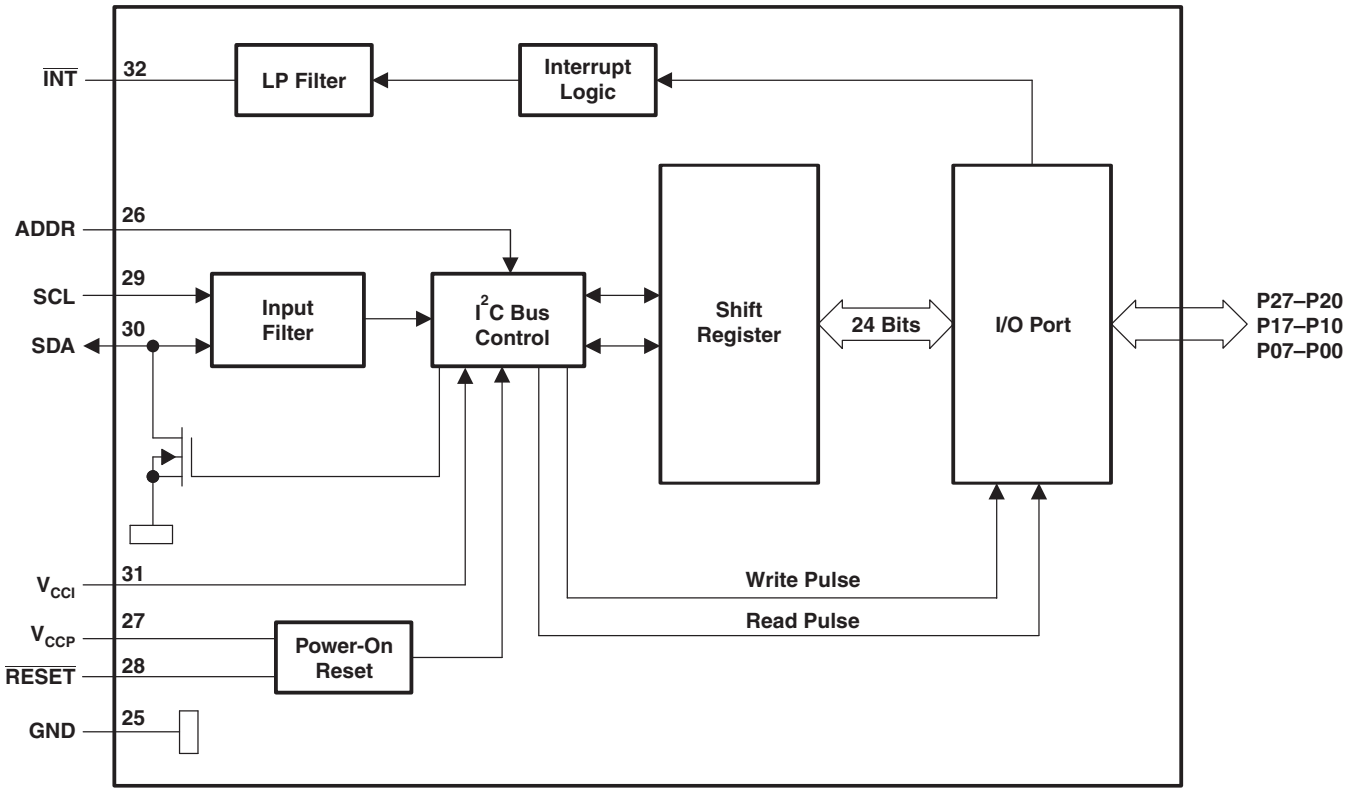
E. All parameters and waveforms are not applicable to all devices.

Figure 17. Reset Load Circuits And Voltage Waveforms

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8 Detailed Description

8.1 Functional Block Diagram

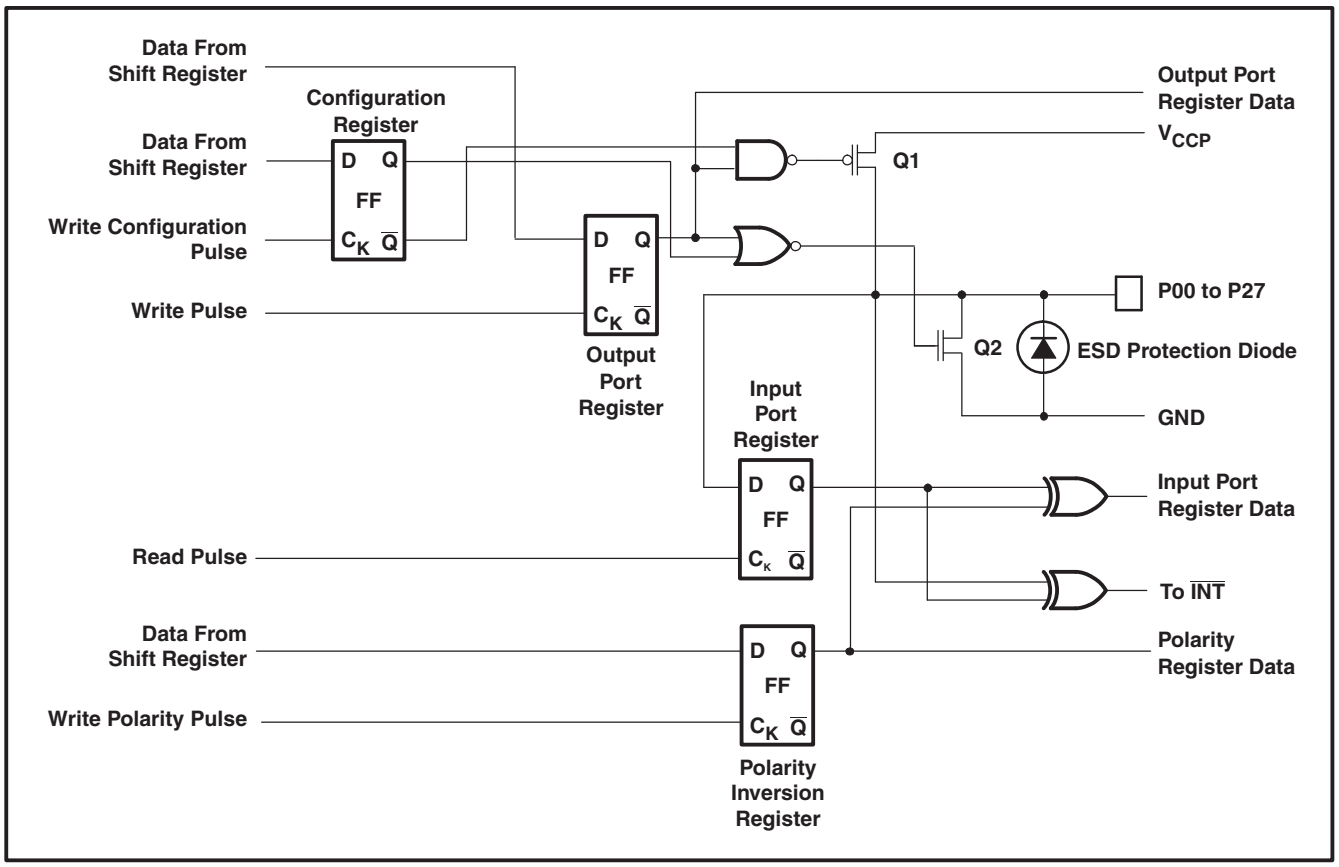


A. All I/Os are set to inputs at reset.

B. Pin numbers shown are for the RGJ package.

Figure 18. Logic Diagram (Positive Logic)

Functional Block Diagram (continued)



A. On power up or reset, all registers return to default values.

Figure 19. Simplified Schematic Of P00 To P27

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8.2 Device Functional Modes

8.2.1 Voltage Translation

Table 1 shows how to set up V_{CC} levels for the necessary voltage translation between the I^2C bus and the TCA6424.

Table 1. Voltage Translation

V_{CCI} (SDA AND SCL OF I^2C MASTER) (V)	V_{CCP} (P PORT) (V)
1.8	1.8
1.8	2.5
1.8	3.3
1.8	5
2.5	1.8
2.5	2.5
2.5	3.3
2.5	5
3.3	1.8
3.3	2.5
3.3	3.3
3.3	5
5	1.8
5	2.5
5	3.3
5	5

8.2.2 Reset Input ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ input can be asserted to initialize the system while keeping the V_{CCP} at its operating level. A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of t_W. The TCA6424 registers and I^2C/SMBus state machine are changed to their default state once $\overline{\text{RESET}}$ is low (0). When $\overline{\text{RESET}}$ is high (1), the I/O levels at the P port can be changed externally or through the master. This input requires a pullup resistor to V_{CCP}, if no active connection is used.

8.2.2.1 $\overline{\text{RESET}}$ Errata

If $\overline{\text{RESET}}$ voltage set higher than VCC, current will flow from $\overline{\text{RESET}}$ pin to VCC pin.

System Impact

VCC will be pulled above its regular voltage level

System Workaround

Design such that $\overline{\text{RESET}}$ voltage is same or lower than VCC

8.2.3 Power-On Reset

When power (from 0 V) is applied to V_{CCP}, an internal power-on reset holds the TCA6424 in a reset condition until V_{CCP} has reached V_{POR}. At that time, the reset condition is released, and the TCA6424 registers and I^2C/SMBus state machine initializes to their default states. After that, V_{CCP} must be lowered to below 0.2 V and back up to the operating voltage for a power-reset cycle.

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8.2.4 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 (in Figure 19) are off, which creates a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

8.2.5 Interrupt ($\overline{INT}$) Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting, data is read from the port that generated the interrupt or in a stop event. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register.

In the TCA6424, an interrupt is not immediately generated by any rising or falling edge of port inputs in input mode after issuing any I^2C commands (read or write). In order to capture the $\overline{INT}$ in the TCA6424, the user needs to add one more SCL clock pulse after a Stop signal.

The $\overline{INT}$ output has an open-drain structure and requires a pullup resistor to V_{CCP} or V_{CCI} depending on the application. If the $\overline{INT}$ signal is connected back to the processor that provides the SCL signal to the TCA6424, then the $\overline{INT}$ pin has to be connected to V_{CCI}. If not, the INT pin can be connected to V_{CCP}.

8.2.5.1 Interrupt Errata

The INT will be improperly de-asserted if the following two conditions occur:

1. The last I^2C command byte (register pointer) written to the device was 00h.

NOTE

This generally means the last operation with the device was a Read of the input register. However, the command byte may have been written with 00h without ever going on to read the input register. After reading from the device, if no other command byte written, it will remain 00h.

2. Any other slave device on the I^2C bus acknowledges an address byte with the R/W bit set high

System Impact

Can cause improper interrupt handling as the Master will see the interrupt as being cleared.

System Workaround

Minor software change: User must change command byte to something besides 00h after a Read operation to the TCA6424 device or before reading from another slave device.

NOTE

Software change will be compatible with other versions (competition and TI redesigns) of this device.

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8.3 Programming

8.3.1 I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output, while the SCL input is high (see Figure 20). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/$\overline{W}$).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address (ADDR) input of the slave device must not be changed between the Start and the Stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 21).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 20).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 22). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

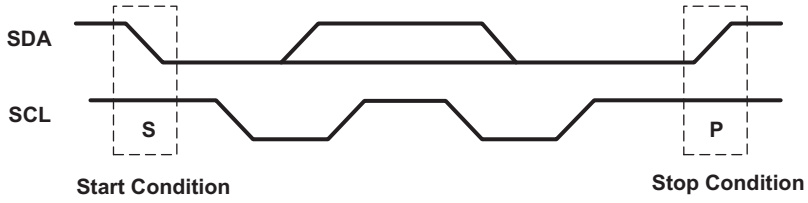


Figure 20. Definition Of Start And Stop Conditions

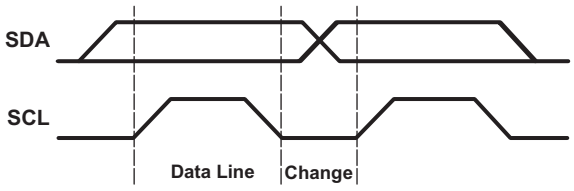


Figure 21. Bit Transfer

Programming (continued)

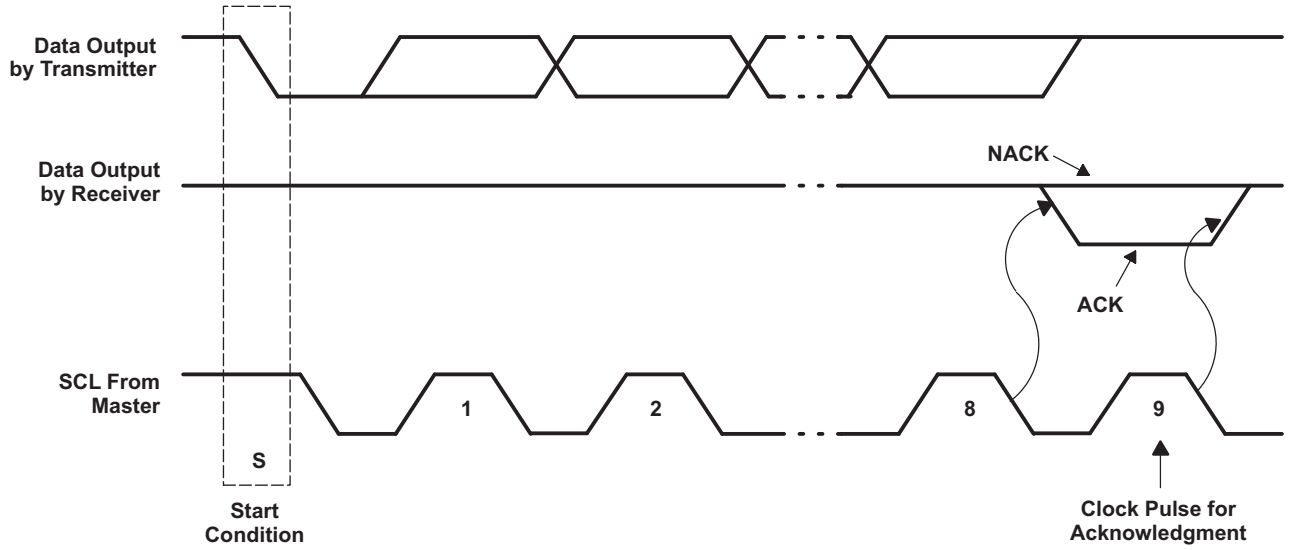


Figure 22. Acknowledgment On The I²C Bus

8.3.2 Register Map

Table 2. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C slave address	L	H	L	L	L	H	ADDR	R/$\overline{W}$
I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
	P17	P16	P15	P14	P13	P12	P11	P10
	P27	P26	P25	P24	P23	P22	P21	P20

8.3.2.1 Device Address

The address of the TCA6424 is shown in Figure 23.

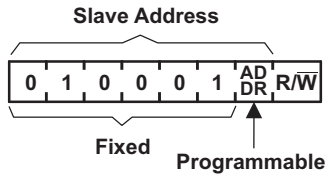


Figure 23. Tca6424 Address

Table 3. Address Reference

ADDR	I²C BUS SLAVE ADDRESS
L	34 (decimal), 22 (hexadecimal)
H	35 (decimal), 23 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

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8.3.2.2 Control Register And Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte, which is stored in the control register in the TCA6424. Four bits of this data byte state the operation (read or write) and the internal registers (input, output, polarity inversion, or configuration) that will be affected. The control register can be written or read through the I^2C bus. The command byte is sent only during a write transmission.

The control register includes an Auto-Increment (AI) bit which is the most significant bit (bit 7) of the command byte. At power-up, the control register defaults to 00 (hex), with the AI bit set to logic 1, and the lowest 7 bits set to logic 0.

If AI is 1, the 2 least significant bits are automatically incremented after a read or write. This allows the user to program and/or read the 3 register banks sequentially. If more than 3 bytes of data are written when AI is 1, previous data in the selected registers will be overwritten. Reserved registers are skipped and not accessed (refer to Table 5).

If AI is 0, the 2 least significant bits are not incremented after data is read or written. During a read operation, the same register bank is read each time. During a write operation, data is written to the same register bank each time.

Reserved command codes and command byte outside the range stated in the Command Byte table must not be accessed for proper device functionality.

AI	B6	B5	B4	B3	B2	B1	B0

Figure 24. Control Register Bits

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Table 4. Command Byte

CONTROL REGISTER BITS								AUTO-INCREMENT STATE	COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
AI	B6	B5	B4	B3	B2	B1	B0					
0	0	0	0	0	0	0	0	Disable	00	Input Port 0	Read byte	xxxx xxxx(1)
1	0	0	0	0	0	0	0	Enable	80			
0	0	0	0	0	0	0	1	Disable	01	Input Port 1	Read byte	xxxx xxxx(1)
1	0	0	0	0	0	0	1	Enable	81			
0	0	0	0	0	0	1	0	Disable	02	Input Port 2	Read byte	xxxx xxxx(1)
1	0	0	0	0	0	1	0	Enable	82			
0	0	0	0	0	0	1	1	Disable	03	Reserved	Reserved	Reserved
1	0	0	0	0	0	1	1	Enable	83			
0	0	0	0	0	1	0	0	Disable	04	Output Port 0	Read/write byte	1111 1111
1	0	0	0	0	1	0	0	Enable	84			
0	0	0	0	0	1	0	1	Disable	05	Output Port 1	Read/write byte	1111 1111
1	0	0	0	0	1	0	1	Enable	85			
0	0	0	0	0	1	1	0	Disable	06	Output Port 2	Read/write byte	1111 1111
1	0	0	0	0	1	1	0	Enable	86			
0	0	0	0	0	1	1	1	Disable	07	Reserved	Reserved	Reserved
1	0	0	0	0	1	1	1	Enable	87			
0	0	0	0	1	0	0	0	Disable	08	Polarity Inversion Port 0	Read/write byte	0000 0000
1	0	0	0	1	0	0	0	Enable	88			
0	0	0	0	1	0	0	1	Disable	09	Polarity Inversion Port 1	Read/write byte	0000 0000
1	0	0	0	1	0	0	1	Enable	89			
0	0	0	0	1	0	1	0	Disable	0A	Polarity Inversion Port 2	Read/write byte	0000 0000
1	0	0	0	1	0	1	0	Enable	8A			
0	0	0	0	1	0	1	1	Disable	0B	Reserved	Reserved	Reserved
1	0	0	0	1	0	1	1	Enable	8B			
0	0	0	0	1	1	0	0	Disable	0C	Configuration Port 0	Read/write byte	1111 1111
1	0	0	0	1	1	0	0	Enable	8C			
0	0	0	0	1	1	0	1	Disable	0D	Configuration Port 1	Read/write byte	1111 1111
1	0	0	0	1	1	0	1	Enable	8D			
0	0	0	0	1	1	1	0	Disable	0E	Configuration Port 2	Read/write byte	1111 1111
1	0	0	0	1	1	1	0	Enable	8E			
0	0	0	0	1	1	1	1	Disable	0F	Reserved	Reserved	Reserved
1	0	0	0	1	1	1	1	Enable	8F			

(1) Undefined

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8.3.2.3 Register Descriptions

The Input Port registers (registers 0, 1 and 2) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. They act only on read operation. Writes to these registers have no effect. The default value (X) is determined by the externally applied logic level. Before a read operation, a write transmission is sent with the command byte to indicate to the I^2C device that the Input Port register will be accessed next.

Table 5. Registers 0 And 1 (Input Port Registers)

BIT	I-07	I-06	I-05	I-04	I-03	I-02	I-01	I-00
DEFAULT	X	X	X	X	X	X	X	X
BIT	I-17	I-16	I-15	I-14	I-13	I-12	I-11	I-10
DEFAULT	X	X	X	X	X	X	X	X
BIT	I-27	I-26	I-25	I-24	I-23	I-22	I-21	I-20
DEFAULT	X	X	X	X	X	X	X	X

The Output Port registers (registers 4, 5 and 6) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that is in the flip-flop controlling the output selection, NOT the actual pin value.

Table 6. Registers 2 And 3 (Output Port Registers)

BIT	O-07	O-06	O-05	O-04	O-03	O-02	O-01	O-00
DEFAULT	1	1	1	1	1	1	1	1
BIT	O-17	O-16	O-15	O-14	O-13	O-12	O-11	O-10
DEFAULT	1	1	1	1	1	1	1	1
BIT	O-27	O-26	O-25	O-24	O-23	O-22	O-21	O-20
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion registers (registers 8, 9 and 10) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in these registers is cleared (written with a 0), the corresponding port pin's original polarity is retained.

Table 7. Registers 4 And 5 (Polarity Inversion Registers)

BIT	P-07	P-06	P-05	P-04	P-03	P-02	P-01	P-00
DEFAULT	0	0	0	0	0	0	0	0
BIT	P-17	P-16	P-15	P-14	P-13	P-12	P-11	P-10
DEFAULT	0	0	0	0	0	0	0	0
BIT	P-27	P-26	P-25	P-24	P-23	P-22	P-21	P-20
DEFAULT	0	0	0	0	0	0	0	0

The Configuration registers (registers 12, 13 and 14) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output.

Table 8. Registers 6 And 7 (Configuration Registers)

BIT	C-07	C-06	C-05	C-04	C-03	C-02	C-01	C-00
DEFAULT	1	1	1	1	1	1	1	1
BIT	C-17	C-16	C-15	C-14	C-13	C-12	C-11	C-10
DEFAULT	1	1	1	1	1	1	1	1
BIT	C-27	C-26	C-25	C-24	C-23	C-22	C-21	C-20
DEFAULT	1	1	1	1	1	1	1	1

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8.3.2.4 Bus Transactions

Data is exchanged between the master and TCA6424 through write and read commands.

8.3.2.4.1 Writes

Data is transmitted to the TCA6424 by sending the device address and setting the least-significant bit (LSB) to a logic 0 (see Figure 23 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission.

The twelve registers within the TCA6424 are grouped into four different sets. The four sets of registers are input ports, output ports, polarity inversion ports and configuration ports. After sending data to one register, the next data byte is sent to the next register in the group of 3 registers (see Figure 25 and Figure 26). For example, if the first byte is send to Output Port 2 (register 6), the next byte is stored in Output Port 0 (register 4).

There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

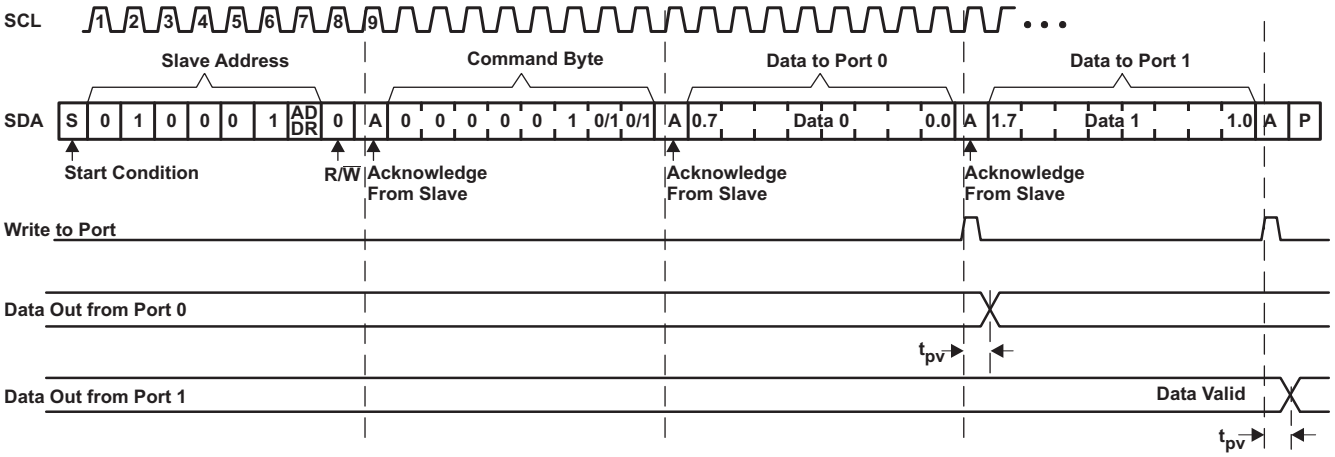


Figure 25. Write To Output Port Register

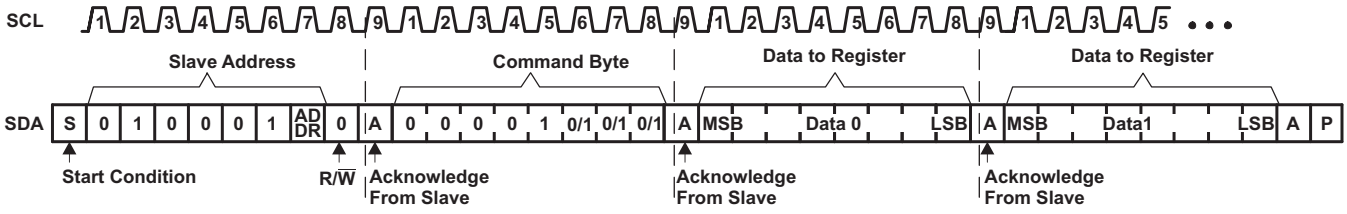


Figure 26. Write To Configuration Or Polarity Inversion Registers

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8.3.2.4.2 Reads

The bus master first must send the TCA6424 address with the LSB set to a logic 0 (see Figure 23 for device address). The command byte is sent after the address and determines which register is accessed.

After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the TCA6424 (see Figure 27 and Figure 28).

After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. For example, if the command byte references Input Port 1 before the restart, and the restart occurs when Input Port 0 is being read, the stored command byte changes to reference Input Port 0. The original command byte is forgotten. If a subsequent restart occurs, Input Port 0 is read first. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflects the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0.

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

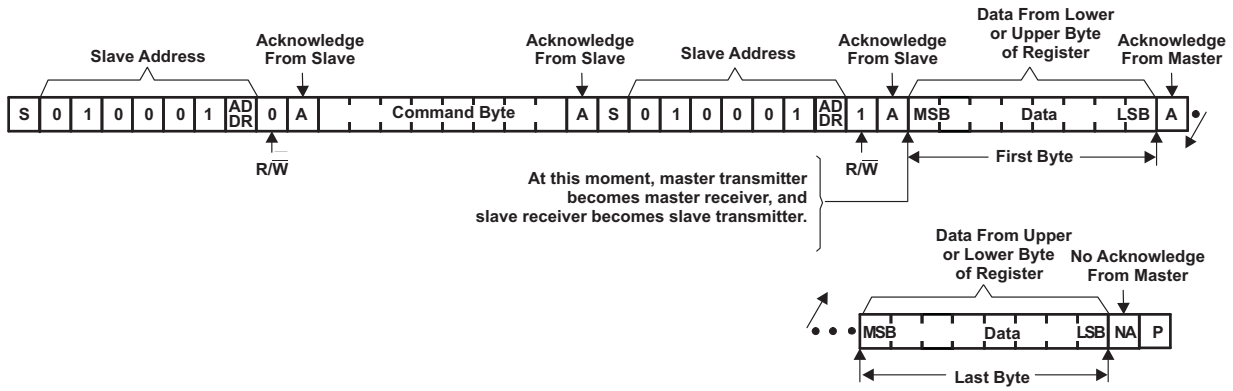
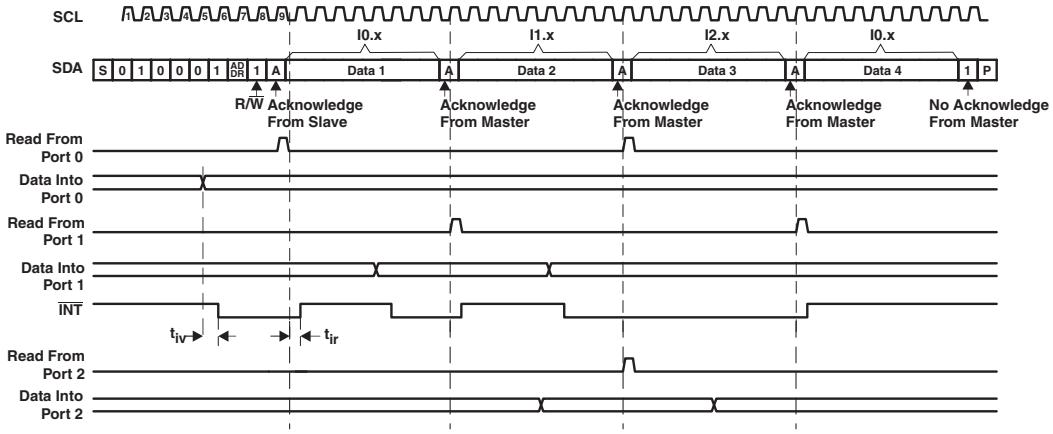


Figure 27. Read From Register



A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).

B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from P port (see Figure 27).

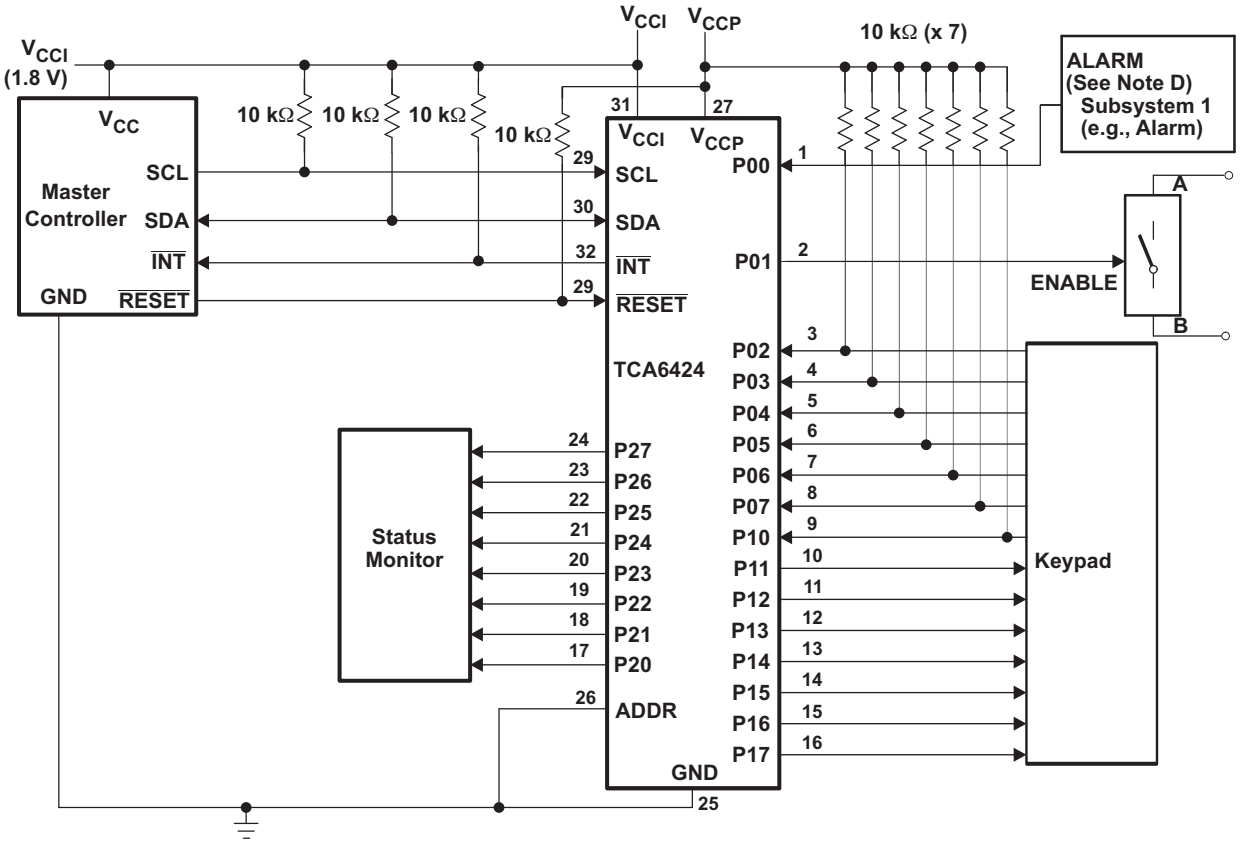
C. Auto-increment mode is enabled.

Figure 28. Read Input Port Register

9 Application And Implementation

9.1 Typical Application

Figure 29 shows an application in which the TCA6424 can be used.



A. Device address configured as 0100000 for this example.

B. P00 and P02–P10 are configured as inputs.

C. P01, P11-P17, and P20-P27 are configured as outputs.

D. Resistors are required for inputs (on P port) that may float. If a driver to an input will not let the input float, a resistor is not needed. Outputs (in the P port) do not need pullup resistors.

Figure 29. Typical Application

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Typical Application (continued)

9.1.1 Detailed Design Procedure

9.1.1.1 Minimizing I_{CC} When I/Os Control Leds

When the I/Os are used to control LEDs, normally they are connected to V_{CC} through a resistor as shown in Figure 29. The LED acts as a diode so, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The ΔI_{CC} parameter in Electrical Characteristics shows how I_{CC} increases as V_{IN} becomes lower than V_{CC}. Designs that must minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{CC} when the LED is off.

Figure 30 shows a high-value resistor in parallel with the LED. Figure 31 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevent additional supply current consumption when the LED is off.

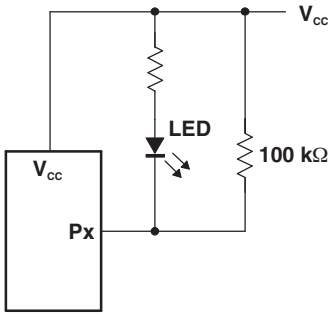


Figure 30. High-Value Resistor In Parallel With The Led

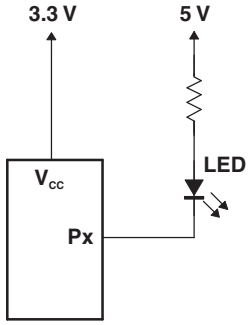


Figure 31. Device Supplied By A Low Voltage

10 Power Supply Recommendations

10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, TCA6424 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 32 and Figure 33.

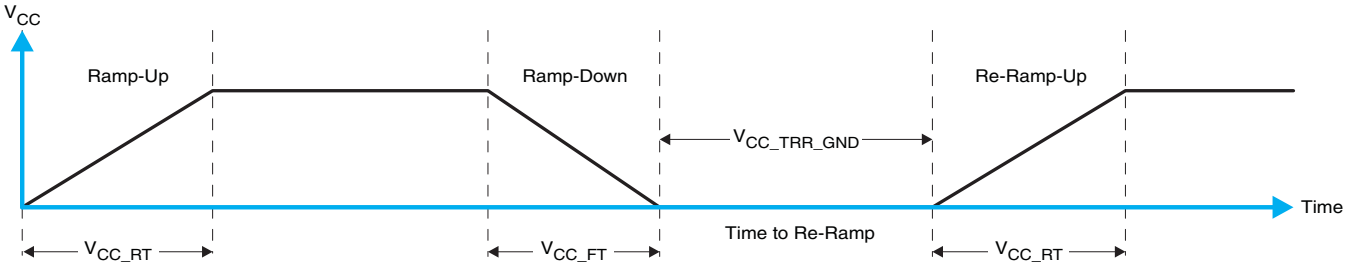


Figure 32. V_{CC} Is Lowered Below 0.2 V Or 0 V And Then Ramped Up To V_{CC}

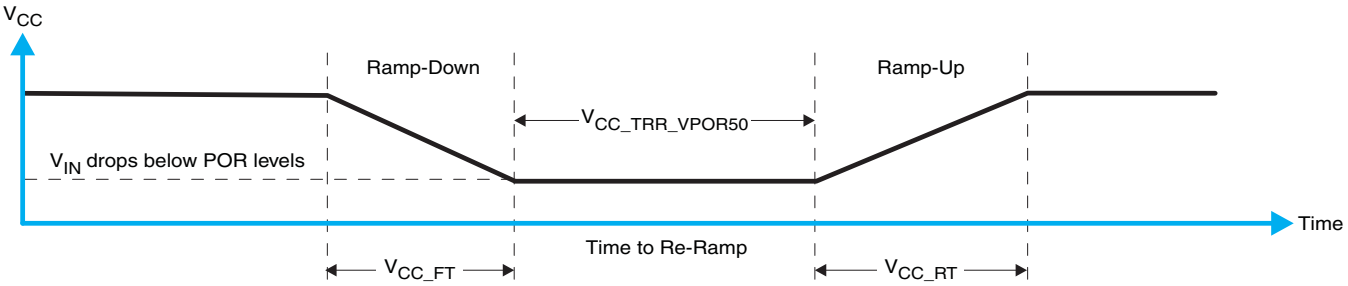


Figure 33. V_{CC} Is Lowered Below The Por Threshold, Then Ramped Back Up To V_{CC}

Table 9 specifies the performance of the power-on reset feature for TCA6424 for both types of power-on reset.

Table 9. Recommended Supply Sequencing And Ramp Rates(1)

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See Figure 32	1		100	ms
V_{CC_RT}	Rise rate	See Figure 32	0.01		100	ms
$V_{CC_TRR_GND}$	Time to re-ramp (when V_{CC} drops to GND)	See Figure 32	0.001			ms
$V_{CC_TRR_POR50}$	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV)	See Figure 33	0.001			ms
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCX_GW} = 1 µs	See Figure 34			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when V_{CCX_GH} = 0.5 × V_{CCx}	See Figure 34				µs
V_{PORF}	Voltage trip point of POR on falling V_{CC}		0.767		1.144	V
V_{PORR}	Voltage trip point of POR on fising V_{CC}		1.033		1.428	V

(1) T_A = –40°C to 85°C (unless otherwise noted)

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Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 34 and Table 9 provide more information on how to measure these specifications.

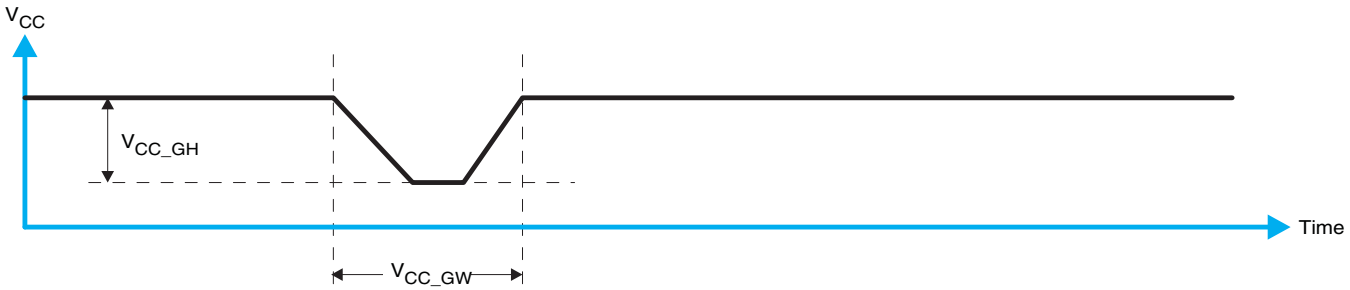


Figure 34. Glitch Width And Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 35 and Table 9 provide more details on this specification.

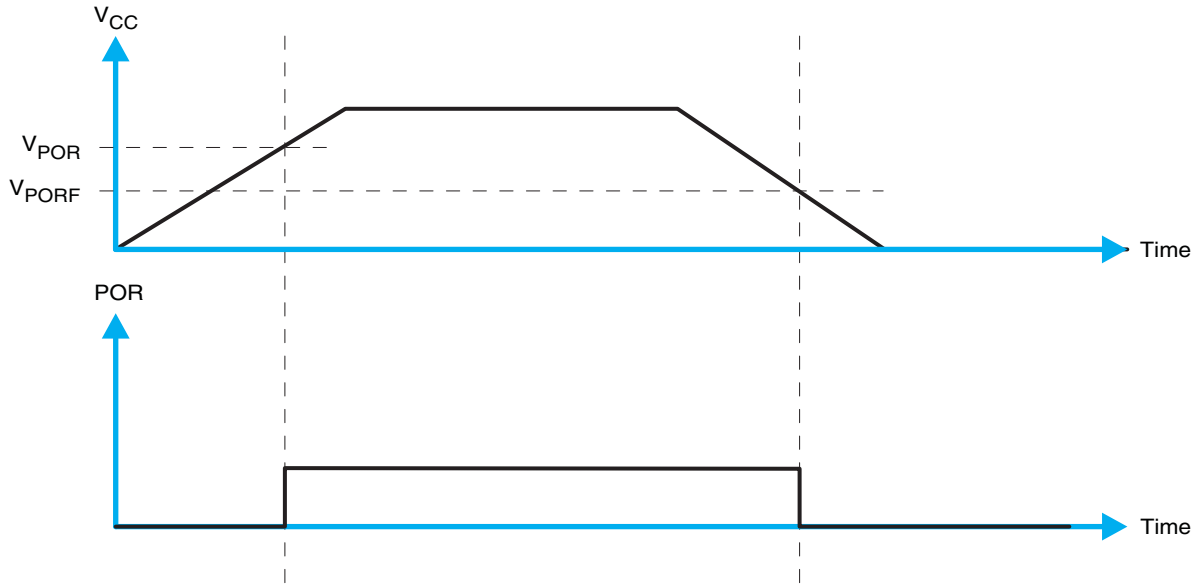


Figure 35. V_{POR}

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA6424RGJR	NRND	UQFN	RGJ	32	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PH424	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

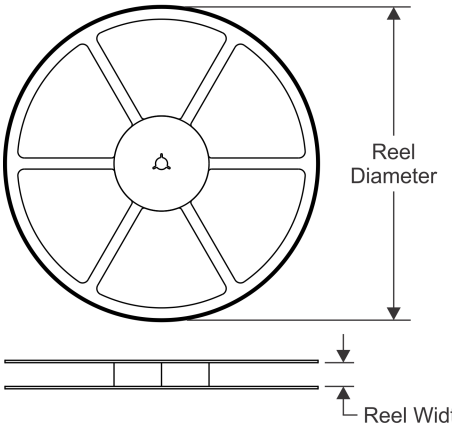
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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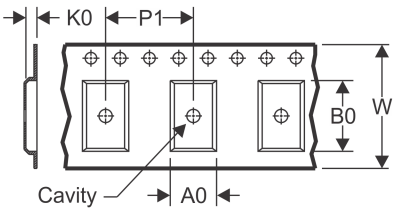
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

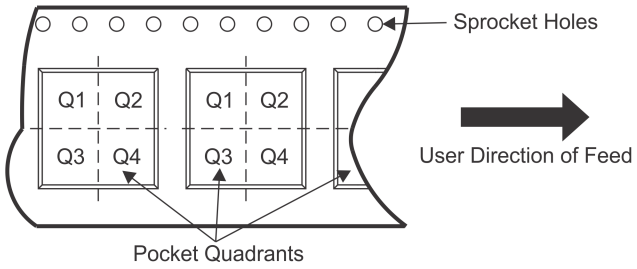


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

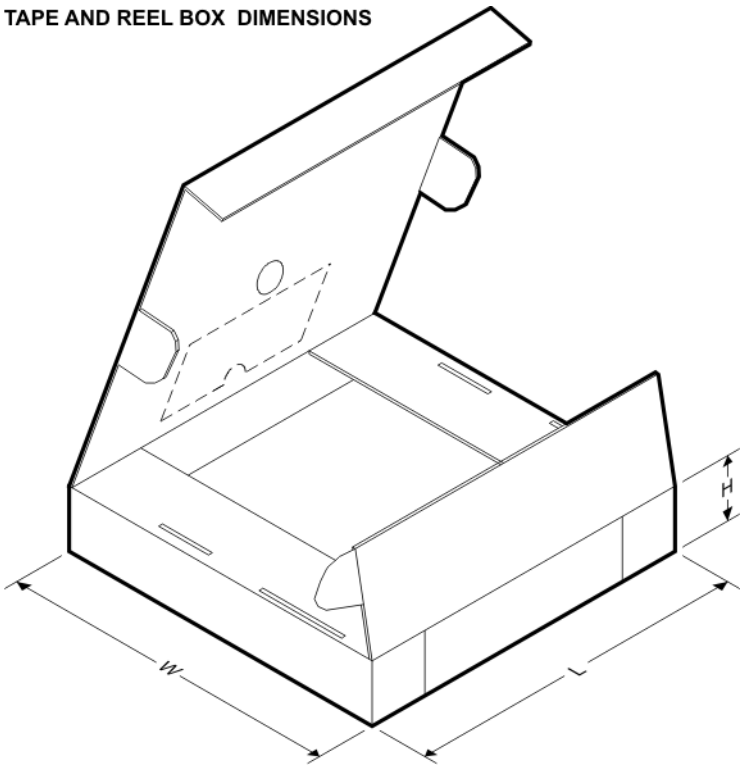
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA6424RGJR	UQFN	RGJ	32	3000	330.0	12.4	5.3	5.3	0.75	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

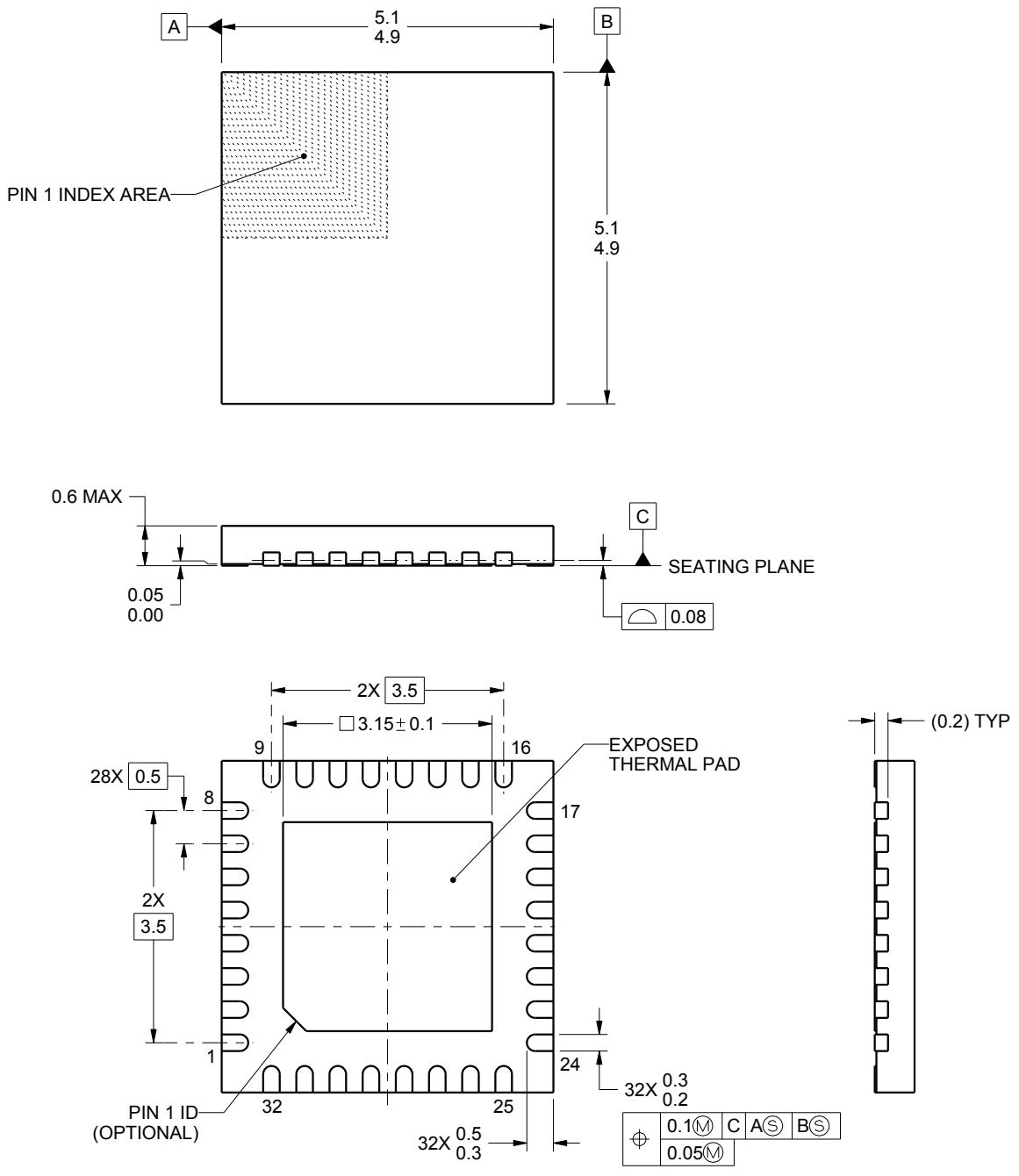
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA6424RGJR	UQFN	RGJ	32	3000	346.0	346.0	35.0

PACKAGE OUTLINE

RGJ0032A

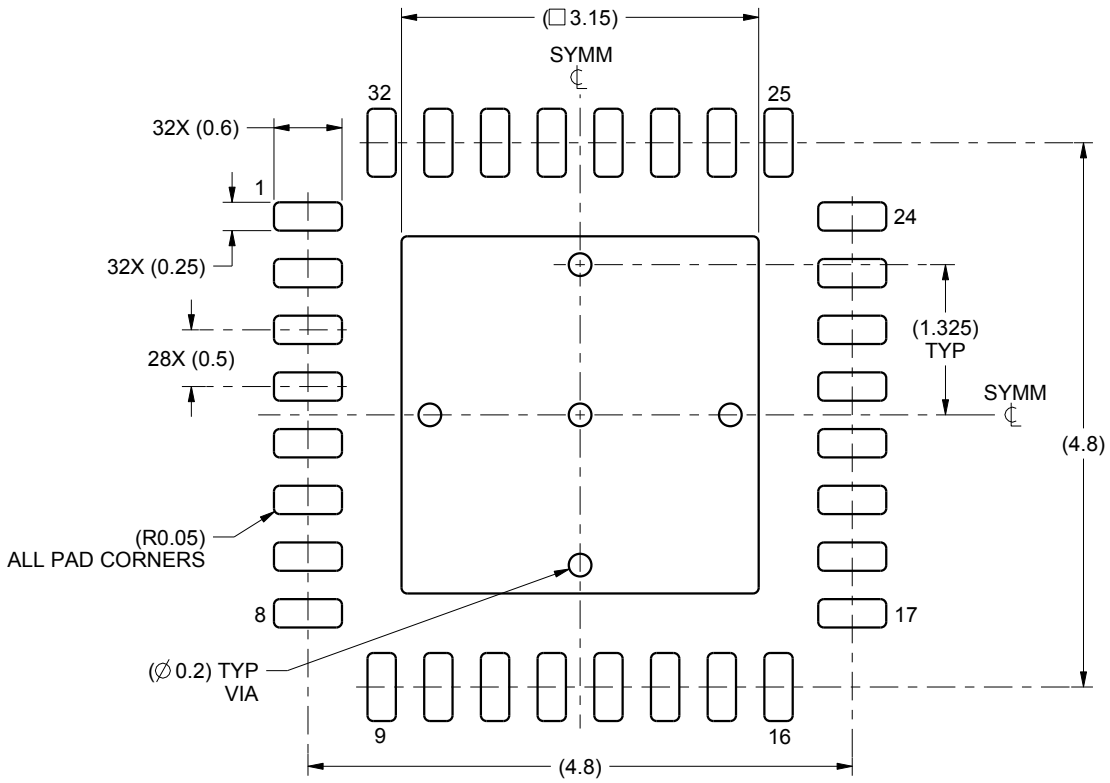
UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

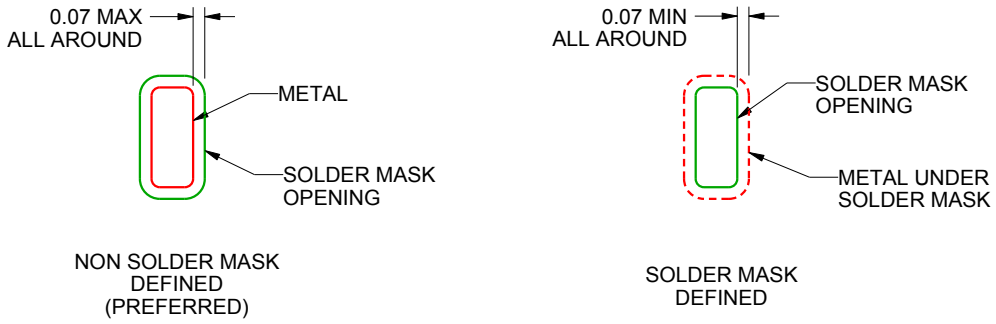


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

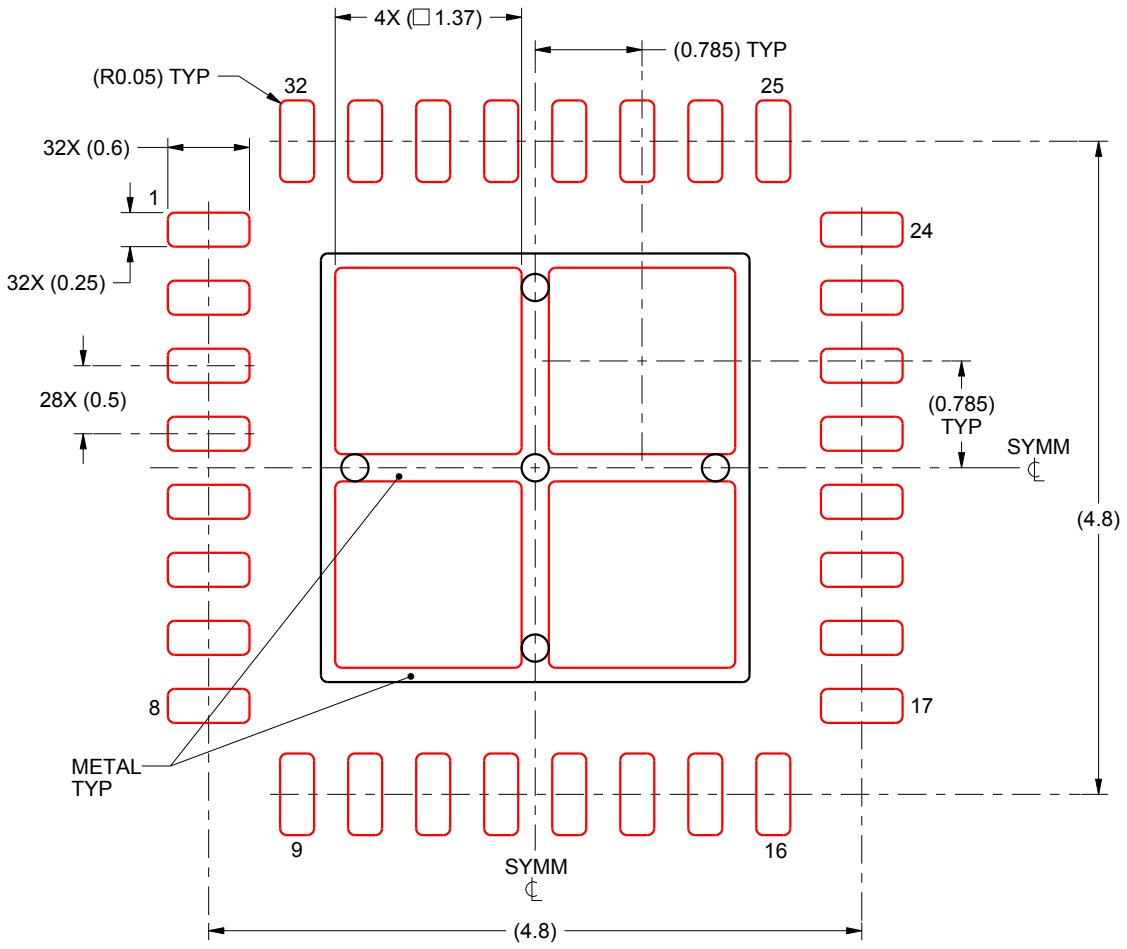


SOLDER MASK DETAILS

4222103/A 08/2015

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED SOLDER COVERAGE BY AREA
SCALE:18X

4222103/A 08/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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