NB6L14M

2.5 V/3.3 V 3.0 GHz Differential 1:4 CML Fanout Buffer

Multi−Level Inputs with Internal Termination

Description

The NB6L14M is a 3.0 GHz differential 1:4 CML clock or data fanout buffer. The differential inputs incorporate internal 50 Ω termination resistors that are accessed through the VT pin. This feature allows the NB6L14M to accept various logic standards, such as LVPECL, CML, or LVDS logic levels. The 16 mA differential CML outputs provide matching internal 50 Ω terminations and produce 400 mV output swings when externally terminated with a 50 Ω resistor to V_{CC}. The V_{REFAC} reference output can be used to rebias capacitor−coupled differential or single−ended input signals. The 1:4 fanout design was optimized for low output skew applications.

The NB6L14M is a member of the ECLinPS MAX™ family of high performance clock and data products.

Features

- Input Clock Frequency > 3.0 GHz
- Input Data Rate > 2.5 Gb/s
- < 20 ps Within Device Output Skew
- 350 ps Typical Propagation Delay
- 90 ps Typical Rise and Fall Times
- Differential CML Outputs, 340 mV Amplitude, Typical
- CML Mode Operating Range: V_{CC} = 2.375 V to 3.63 V with GND = 0 V
- Internal Input and Output Termination Resistors, 50 Ω
- V_{REFAC} Reference Output Voltage
- −40°C to +85°C Ambient Operating Temperature
- Available in 3 mm x 3 mm 16 Pin QFN
- These are Pb−Free Devices

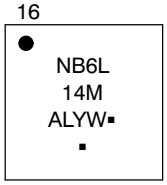
ON Semiconductor®

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QFN−16
MN SUFFIX
CASE 485G

MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

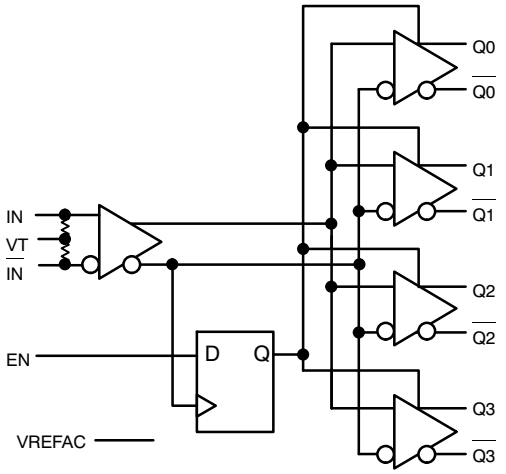


Figure 1. Simplified Logic Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

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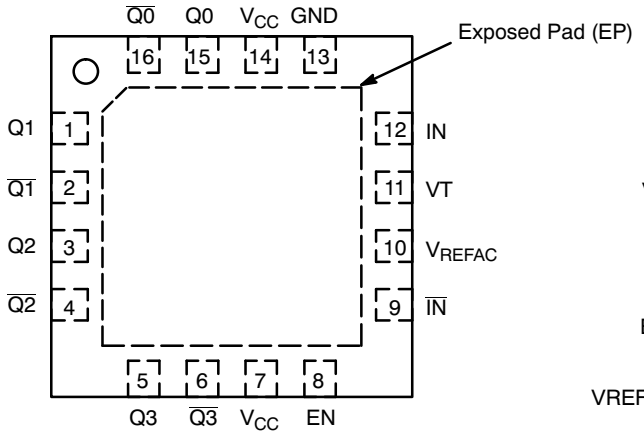


Figure 2. QFN−16 Pinout
(Top View)

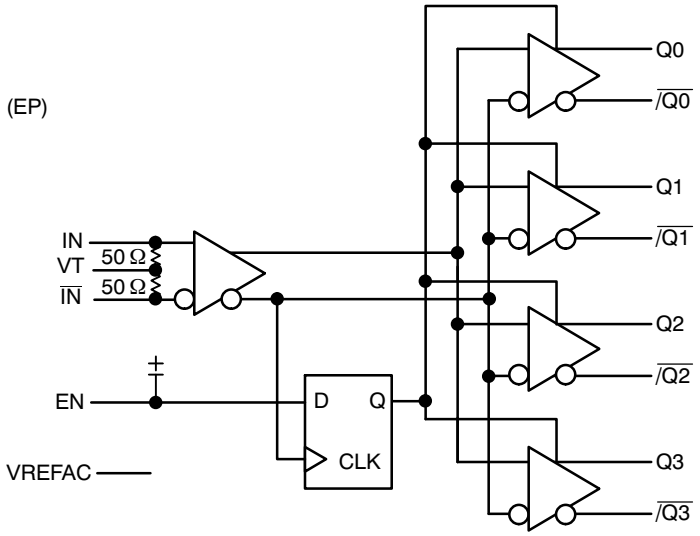


Figure 3. Logic Diagram

Table 1. EN TRUTH TABLE

IN	$\overline{IN}$	EN	Q0:Q3	$\overline{Q0}$:$\overline{Q3}$
0	1	1	0	1
1	0	1	1	0
x	x	0	0+	1+

+ = On next negative transition of the input signal (IN).
x = Don't care.

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
1	Q1	CML Output	Non−inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
2	$\overline{Q1}$	CML Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC} .
3	Q2	CML Output	Non−inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
4	$\overline{Q2}$	CML Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
5	Q3	CML Output	Non−inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
6	$\overline{Q3}$	CML Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
7	V_{CC}	−	Positive Supply Voltage
8	EN	LVTTL/LVCMOS	Synchronous Output Enable. When LOW, Q outputs will go LOW and $\overline{Q}$ outputs will go HIGH on the next negative transition of IN input. The internal D_{FF} register is clocked on the falling edge of IN input (see Figure 16). The EN pin has an internal pullup resistor and defaults HIGH when left open.
9	$\overline{IN}$	LVPECL, CML, LVDS	Inverted Differential Clock Input. Internal 50 Ω Resistor to Termination Pin, VT.
10	V_{REFAC}		Output Voltage Reference for capacitor−coupled inputs, only.
11	VT		Internal 100 Ω center−tapped Termination Pin for IN and $\overline{IN}$.
12	IN	LVPECL, CML, LVDS	Non−inverted Differential Clock Input. Internal 50 Ω Resistor to Termination Pin, VT.
13	GND	−	Negative Supply Voltage
14	V_{CC}	−	Positive Supply Voltage
15	Q0	CML Output	Noninverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
16	$\overline{Q0}$	CML Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}.
−	EP	−	The Exposed Pad (EP) on the QFN−16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat−sinking conduit. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to GND on the PC board.

1. In the differential configuration when the input termination pin VT, is connected to a common termination voltage or left open, and if no signal is applied on IN/$\overline{IN}$ inputs, then the device will be susceptible to self−oscillation.

Table 3. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Mode	> 2 kV > 200 V
Moisture Sensitivity (Note 2)	QFN−16	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		167
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

2. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		4.0	V
V_{Io}	Positive Input/Output	GND = 0 V	$-0.5\ V \le V_{Io} \le V_{CC} + 0.5\ V$	4.5	V
I_{IN}	Input Current Source or Sink Current (IN/$\overline{IN}$)			±50	mA
I_{VREFAC}	Sink/Source Current			±2.0	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 3)	0 lfpm 500 lfpm	QFN−16 QFN−16	42 35	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P (Note 3)	QFN−16	4	°C/W
T_{sol}	Wave Solder Pb−Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 5. DC CHARACTERISTICS, Multi−Level Inputs, CML Outputs

V_{CC} = 2.375 V to 3.63 V, GND = 0 V, T_A = −40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CC}	Power Supply Current (Inputs and Outputs Open)	80	100	130	mA
CML OUTPUT (Notes 4 and 5)					
V_{OH}	Output HIGH Voltage V_{CC} = 3.3 V V_{CC} = 2.5 V	V_{CC} − 40 3260 2460	V_{CC} − 10 3290 2490	V_{CC} 3300 2500	mV
V_{OL}	Output LOW Voltage V_{CC} = 3.3 V V_{CC} = 2.5 V	V_{CC} − 500 2800 2000	V_{CC} − 400 2900 2100	V_{CC} − 300 3000 2200	mV
DIFFERENTIAL INPUT DRIVEN SINGLE−ENDED (See Figures 5 and 6)					
V_{th}	Input Threshold Reference Voltage Range (Note 6)	1100		V_{CC} − 100	mV
V_{IH}	Single−Ended Input High Voltage	V_{th} + 100		V_{CC}	mV
V_{IL}	Single−Ended Input LOW Voltage	GND		V_{th} − 100	mV
V_{ISE}	Single−Ended Input Voltage Amplitude (V_{IH} − V_{IL})	200		V_{CC} − GND	mV
V_{REFAC}					
V_{REFAC}	Output Reference Voltage (V_{CC} ≥ 2.5 V)	V_{CC} − 1525	V_{CC} − 1425	V_{CC} − 1325	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (See Figures 7 and 8) (Note 7)					
V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	GND		V_{IHD} − 100	mV
V_{ID}	Differential Input Voltage (IN−$\overline{IN}$) (V_{IHD}−V_{ILD})	100		V_{CC} − GND	mV
V_{CMR}	Input Common Mode Range (Differential Configuration) (Note 8)	950		V_{CC} − 50	mV
I_{IH}	Input HIGH Current IN/$\overline{IN}$ (VT Open)	−150		+150	μA
I_{IL}	Input LOW Current IN/$\overline{IN}$ (VT Open)	−150		+150	μA
LVTTL/LVCMOS INPUT DC ELECTRICAL CHARACTERISTICS					
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V
V_{IL}	Input LOW Voltage	GND		0.8	V
I_{IH}	Input HIGH Current, V_{CC} = V_{IN} = 3.63 V	−150		+150	μA
I_{IL}	Input LOW Current, V_{CC} = 3.63 V, V_{IN} = 0 V	−150		+150	μA
TERMINATION RESISTORS					
R_{TIN}	Internal Input Termination Resistor (IN to VT)	40	50	60	Ω
R_{DIFF_IN}	Differential Input Resistance (IN to $\overline{IN}$)	80	100	120	Ω
R_{TOUT}	Internal Output Termination Resistor	40	50	60	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. CML outputs loaded with 50 Ω to V_{CC} for proper operation.
5. Input and output parameters vary 1:1 with V_{CC}.
6. V_{th} is applied to the complementary input when operating in single−ended mode.
7. V_{IHD}, V_{ILD}, V_{ID} and V_{CMR} parameters must be complied with simultaneously.
8. V_{CMR} minimum varies 1:1 with GND, V_{CMR} max varies 1:1 with V_{CC}. The V_{CMR} range is referenced to the most positive side of the differential input signal.

Table 6. AC CHARACTERISTICS V_{CC} = 2.375 V to 3.63 V, GND = 0 V, T_A = −40°C to +85°C (Note 9)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) (Note 10) $f_{in} \le 2.5$ GHz 2.5 GHz ≤ $f_{in} \le 3.0$ GHz	 180 100	 340 250		mV
f_{DATA}	Maximum Operating Data Rate		2.5		Gb/s
t_{PD}	Propagation Delay IN to Q	230	350	480	ps
t_S	Set−Up Time (Note 11) EN to IN, $\overline{IN}$	300			ps
t_H	Hold Time (Note 11) EN to IN, $\overline{IN}$	300			ps
t_{SKEW}	Within−Device Skew (Note 12) Device−to−Device Skew (Note 13)		5.0	20 80	ps
t_{DC}	Output Clock Duty Cycle $f_{in} \le 3.0$ GHz (Referenced Duty Cycle = 50%)	40	50	60	%
t_{JITTER}	RMS Random Jitter (Note 14) $f_{IN} \le 3.0$ GHz Peak−to−Peak Data Dependent Jitter (Note 15) $f_{DATA} \le 3.0$ Gb/s		 0.2 20	0.5	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 10)	100		V_{CC} − GND	mV
t_r,t_f	Output Rise/Fall Times (20%−80%)		90	150	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. Measured by forcing V_{INPP} (minimum) from a 50% duty cycle clock source. All loading with an external R_L = 50 Ω to V_{CC}. Input edge rates 40 ps (20%−80%).
10. Input and output voltage swing is a single−ended measurement operating in differential mode.
11. Set−up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set−up and hold times do not apply.
12. Within device skew is measured between two different outputs under identical power supply, temperature and input conditions.
13. Device to device skew is measured between outputs under identical transition @ 0.5 GHz.
14. Additive RMS jitter with 50% duty cycle clock signal.
15. Additive peak−to−peak data dependent jitter with input NRZ data at PRBS 23−1 and K28.5 at 2.5 Gb/s.

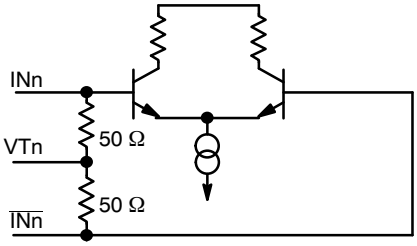


Figure 4. Input Structure

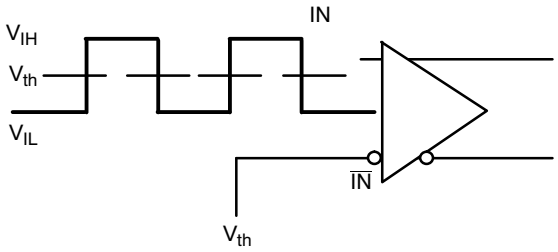


Figure 5. Differential Input Driven Single−Ended

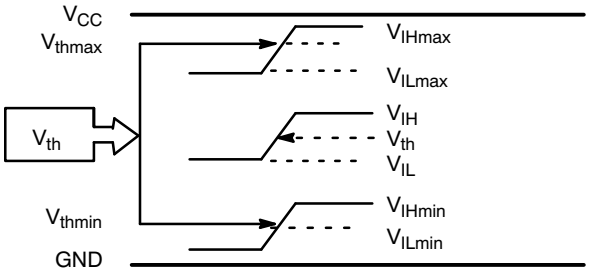


Figure 6. V_{th} Diagram

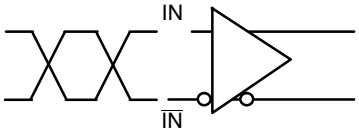


Figure 7. Differential Inputs Driven Differentially

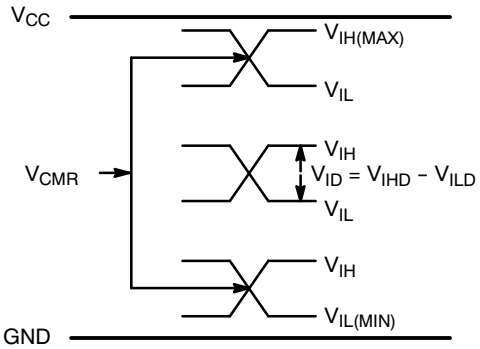


Figure 8. V_{CMR} Diagram

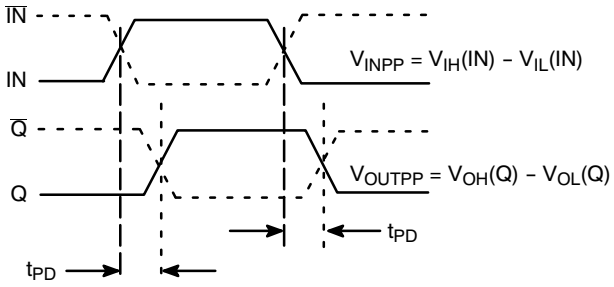


Figure 9. AC Reference Measurement

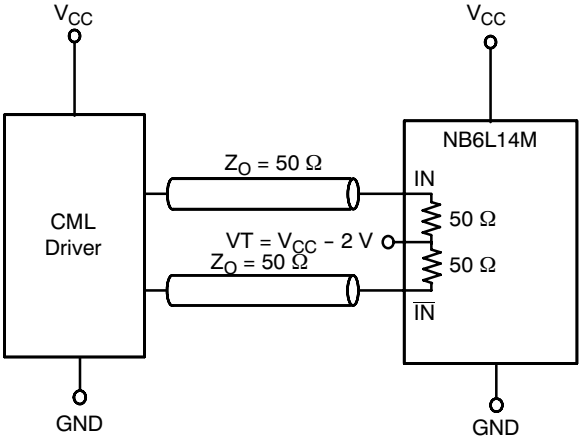


Figure 10. CML Interface

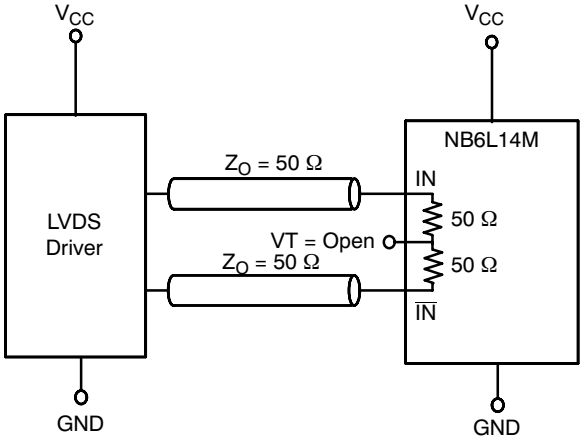


Figure 11. LVDS Interface

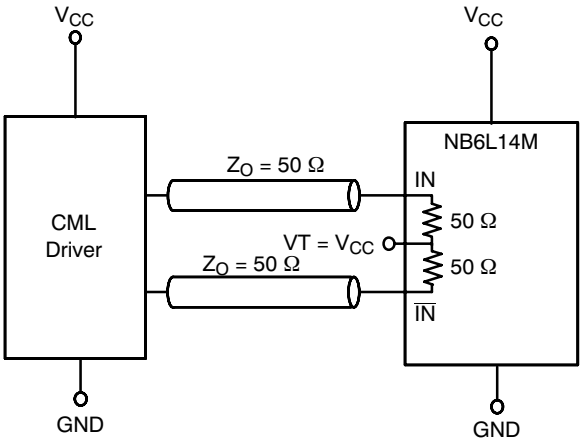


Figure 12. Standard 50 Ω Load CML Interface

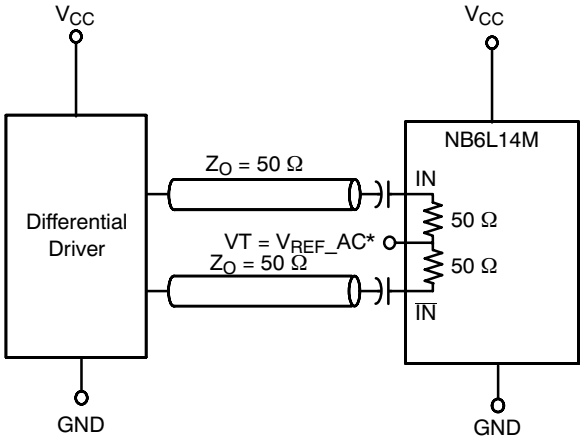


Figure 13. Capacitor−Coupled Differential Interface (VT Connected to V_{REFAC})

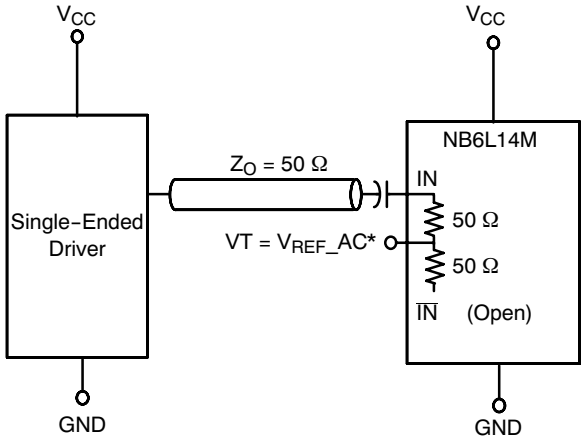


Figure 14. Capacitor−Coupled Single−Ended Interface (VT Connected to V_{REFAC})

*V_{REFAC} bypassed to ground with a 0.01 μF capacitor

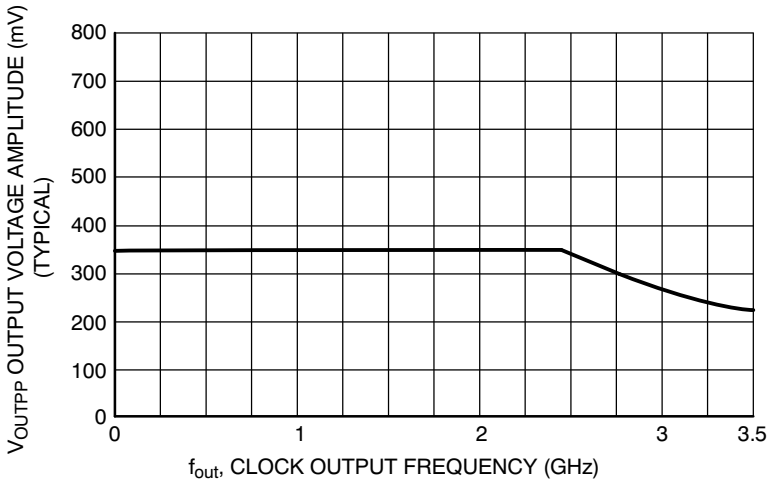


Figure 15. Output Voltage Amplitude (V_{OUTPP}) versus Output Frequency at Ambient Temperature (Typical)

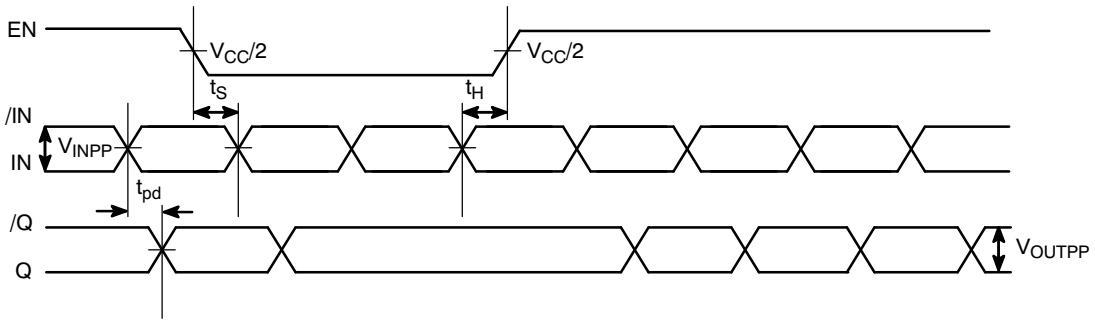


Figure 16. EN Timing Diagram

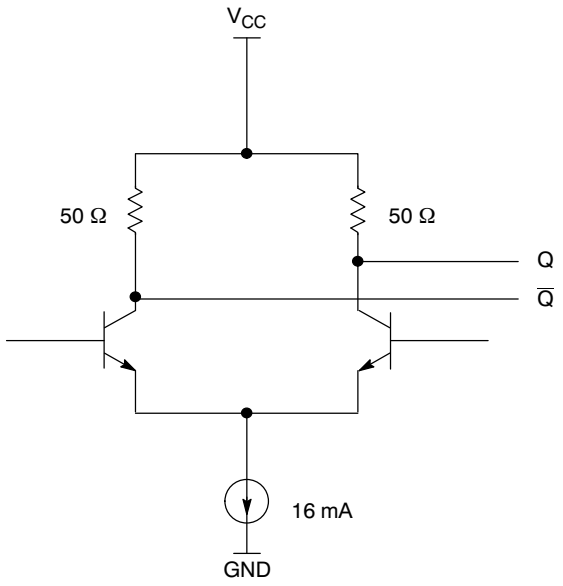


Figure 17. CML Output Structure

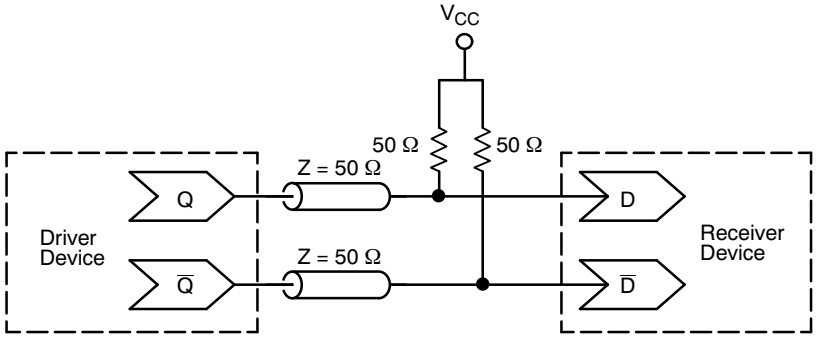


Figure 18. Typical CML Termination for Output Driver and Device Evaluation

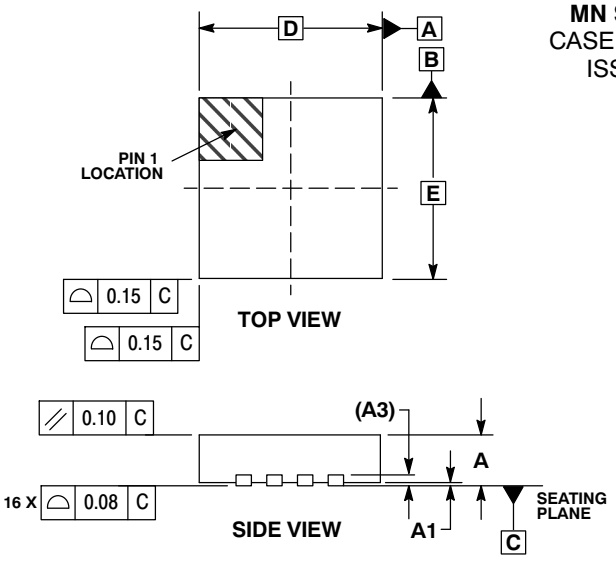
ORDERING INFORMATION

Device	Package	Shipping†
NB6L14MMNG	QFN−16, 3x3 mm (Pb−Free)	123 Units / Rail
NB6L14MMNR2G	QFN−16, 3x3 mm (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

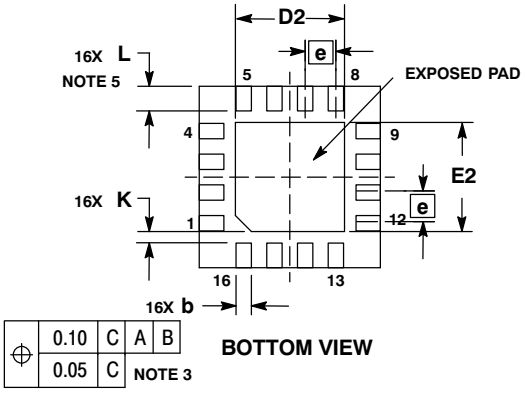
PACKAGE DIMENSIONS

16 PIN QFN
MN SUFFIX
CASE 485G−01
ISSUE C

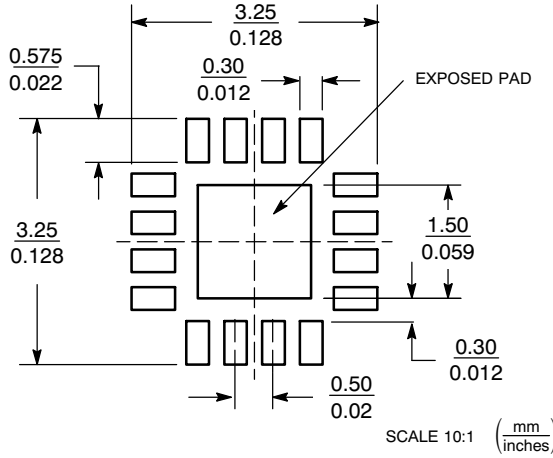


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.18 TYP	
L	0.30	0.50



SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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