ISOLATED FEEDBACK GENERATOR

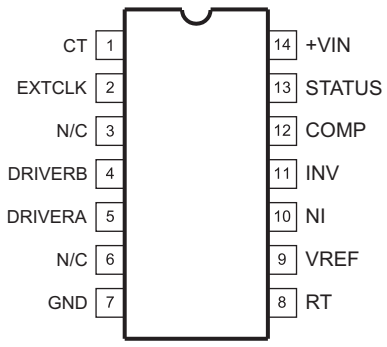
Check for Samples: UC2901-EP

FEATURES

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **Amplitude-Modulation System for Transformer Coupling an Isolated Feedback Error Signal**
- **Low-Cost Alternative to Optical Couplers**
- **Internal 1% Reference and Error Amplifier**
- **Internal Carrier Oscillator Usable to 5 MHz**
- **Modulator Synchronizable to an External Clock**
- **Loop Status Monitor**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

D PACKAGE
(TOP VIEW)



N/C = No internal connection

DESCRIPTION

The UC2901 is designed to solve many of the problems associated with closing a feedback control loop across a voltage isolation boundary. As a stable and reliable alternative to an optical coupler, UC2901 features an amplitude modulation system that allows a loop error signal to be coupled with a small RF transformer or capacitor.

The programmable, high-frequency oscillator within the UC2901 permits the use of smaller, less-expensive transformers, which can readily be built to meet the isolation requirements of today's line-operated power systems. As an alternative to RF operation, the external clock input to these devices allows synchronization to a system clock or to the switching frequency of an SMPS.

An additional feature is a status monitoring circuit that provides an active low output when the sensed error voltage is within ±10% of the reference. The DRIVERA output, DRIVERB output, and STATUS output are disabled until the input supply has reached a sufficient level to allow proper operation of the device.

Because these devices also can be used as a DC driver for optical couplers, the benefits of 4.5 V to 40 V supply operation, a 1% accurate reference, and a high-gain general-purpose amplifier offer advantages, even though an AC system may not be desired.

ORDERING INFORMATION

T_A	PACKAGE(1)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	D (SOIC)	UC2901MDREP	UC2901MEP

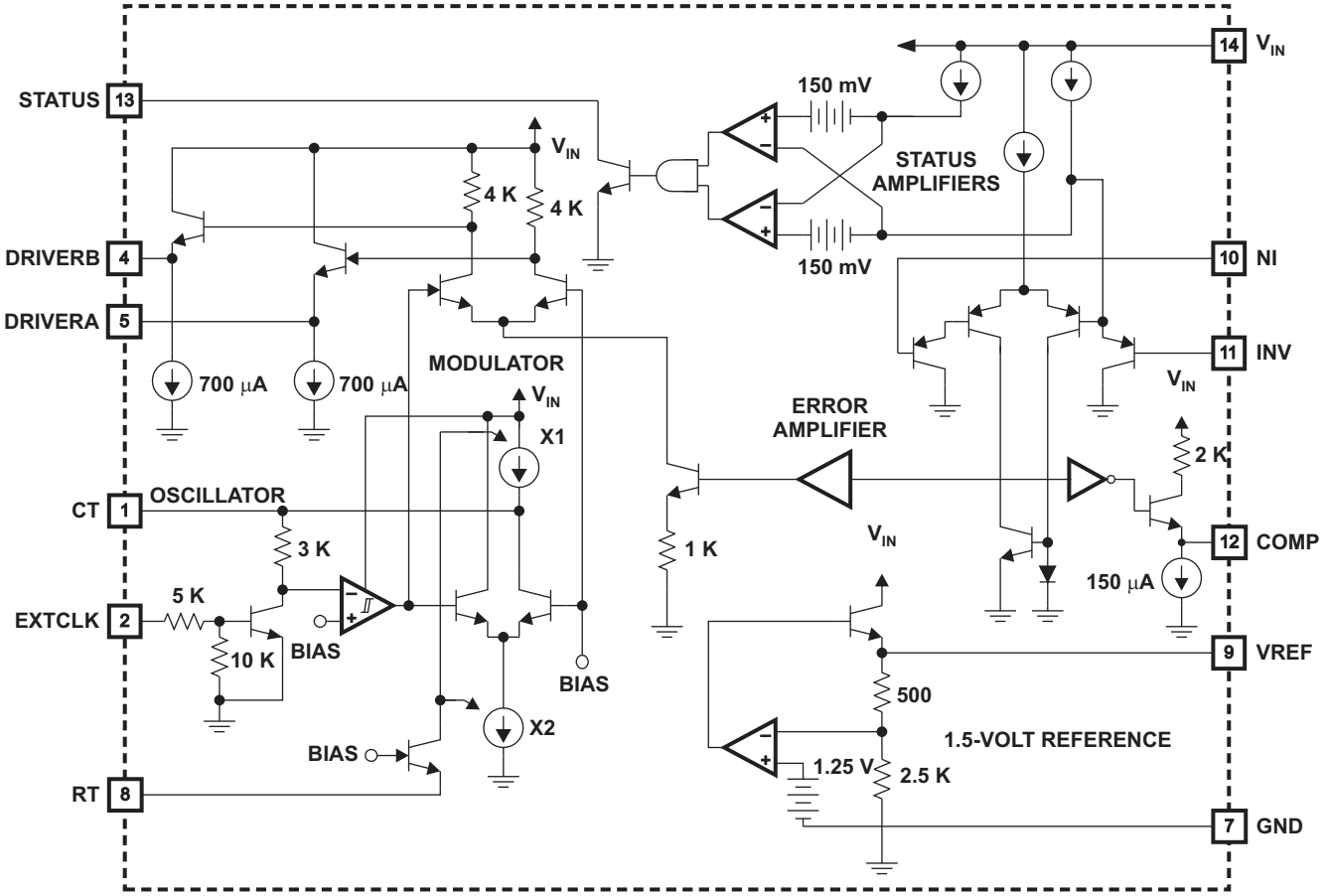
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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UC2901 SIMPLIFIED SCHEMATIC



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input supply voltage		40	V
	Reference output current		–10	mA
	Driver output current		–35	mA
	Status indicator voltage		40	V
	Status indicator current		20	mA
	External clock input		40	V
	Error amplifier inputs	–0.5	35	V
	Power dissipation at T_A = 25°C		1000	mW
	Operating junction temperature range	–55	150	°C
	Storage temperature range(2)	–65	150	°C
	Lead temperature (soldering, 10 seconds)		300	°C

(1) Voltages are referenced to ground, pin 7. Currents are positive into, and negative out of the specified terminal.
(2) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

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DISSIPATION RATING TABLE - FREE-AIR TEMPERATURE

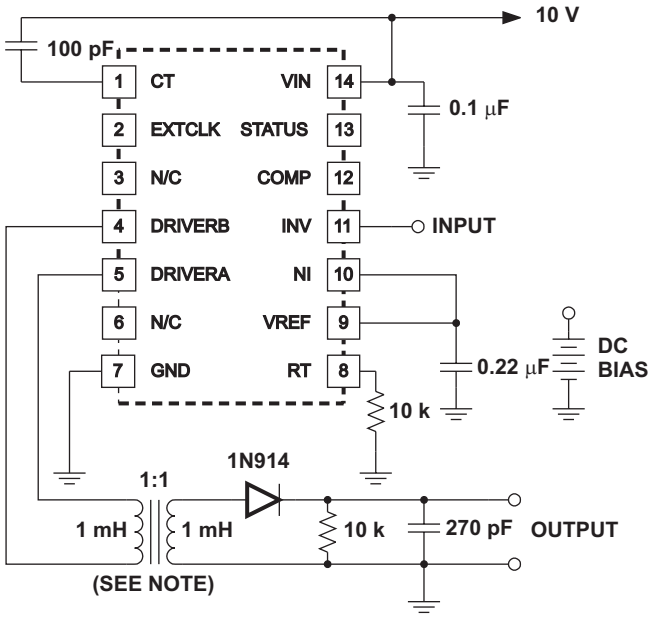
PACKAGE	AIR FLOW (CFM)	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	0	1000 mW	8 mW/°C	630 mW	510 mW	180 mW

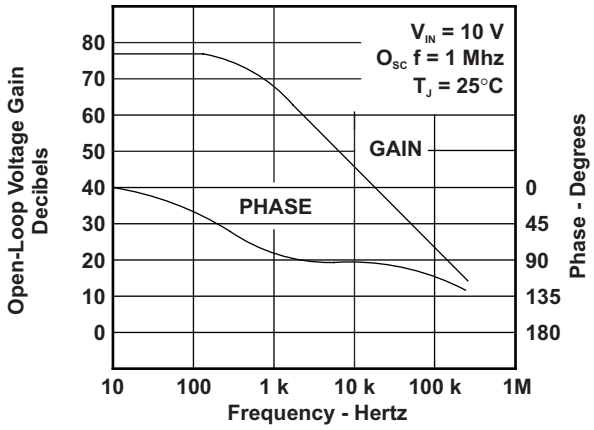
Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference Section					
Output voltage	T_A = 25°C	1.485	1.5	1.515	V
	$T_{MIN} \leq T_A \leq T_{MAX}$	1.470	1.5	1.530	
Line regulation	V_{IN} = 4.5 to 35 V		2	10	mV
Load regulation	I_{OUT} = 0 to 5 mA		4	10	mV
Short-circuit current	T_A = 25°C		–35	–55	mA
Error Amplifier Section (To Compensation Terminal)					
Input offset voltage	V_{CM} = 1.5 V		1	4	mV
Input bias current	V_{CM} = 1.5 V		–1	–3	µA
Input offset current	V_{CM} = 1.5 V		0.1	1	µA
Small-signal open-loop gain		40	60		dB
CMRR	V_{CM} = 0.5 V to 7.5 V	60	80		dB
PSRR	V_{IN} = 5 V to 25 V	80	100		dB
Output swing, ΔV_O		0.4	0.7		V
Maximum sink current		90	150		µA
Maximum source current		–2	–3		mA
Gain bandwidth product			1		MHz
Slew rate			0.3		V/µs
Modulators/Drivers Section (From Compensation Terminal)					
Voltage gain		11	12	13	dB
Output swing		±1.6	±2.8		V
Driver sink current		500	700		µA
Driver source current		–15	–35		mA
Gain bandwidth product			25		MHz
Oscillator Section					
Initial accuracy	T_A = 25°C	140	150	160	kHz
	$T_{MIN} \leq T_A \leq T_{MAX}$	130		170	kHz
Line sensitivity	V_{IN} = 5 V to 35 V		0.15	0.35	%/V
Maximum frequency	R_T = 10 K, C_T = 10 pF		5		MHz
External clock low threshold	Pin 1 (C_T) = V_{IN}	0.5			V
External clock high threshold	Pin 1 (C_T) = V_{IN}			1.6	V
Status Indicator Section					
Input voltage window	At E/A inputs, V_{CM} = 1.5 V	±135	±150	±165	mV
Saturation voltage	E/A Δinput = 0 V, I_{SINK} = 1.6 mA			0.45	V
Maximum output current	Pin 13 = 3 V, E/A Δ input = 0 V	8	15		mA
Leakage current	Pin 13 = 40 V, E/A Δ input = 0.2 V		0.05	1	µA
Supply current	V_{IN} = 35 V		5	8	mA
UVLO Section					
Drivers-enabled threshold	At input supply V_{IN}		3.9	4.5	V
Status output-enabled threshold	At input supply V_{IN}		3.9	4.5	V
Change in reference output	When VIN reaches UVLO threshold		–2	–30	mV

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Note: Transformer Data: N1 = N2 = 20 TAWG 26
Core = Ferroxcube 3E2A Ferrite, 0.5" O.D. Toroid
Carrier Frequency = 1 Mhz

Figure 1. Transformer-Coupled Open-Loop Transfer Function

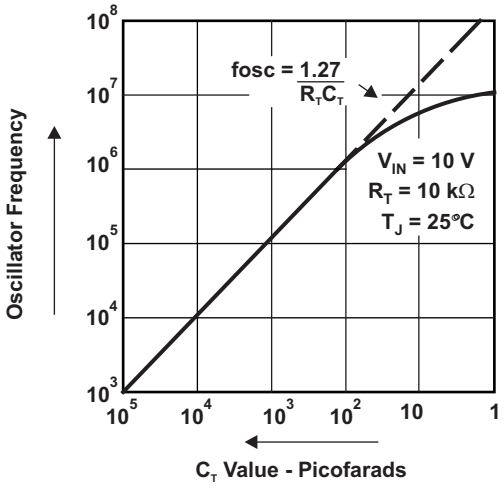


Figure 2. Oscillator Frequency

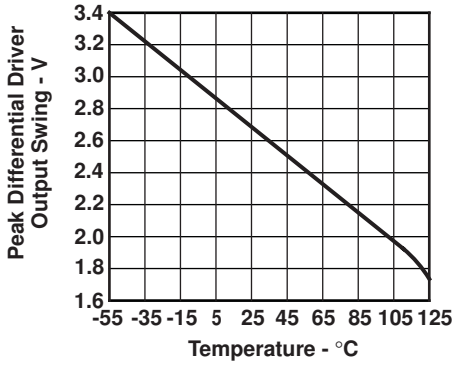


Figure 3. Typical Driver Output Swing vs Temperature

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APPLICATION INFORMATION

The error amplifier compensation terminal, pin 12, is intended as a source of feedback to the amplifier's inverting input at pin 11. For most applications, a series DC blocking capacitor should be part of the feedback network. The amplifier is compensated internally for unity feedback.

The waveform at the driver outputs is a squarewave, with an amplitude that is proportional to the error amplifier input signal. There is a fixed 12 dB of gain from the error amplifier compensation pin to the modulator driver outputs. The frequency of the output waveform is controlled by either the internal oscillator or an external clock signal.

With the internal oscillator, the squarewave has a fixed 50% duty cycle. If the internal oscillator is disabled by connecting pin 1, C_R, to V_{IN}, then the frequency and duty cycle of the output is determined by the input clock waveform at pin 2. If the oscillator remains disabled, and there is not clock input at pin 2, there will be a linear 12-dB signal gain to one or the other of the driver outputs, depending on the DC state of pin 2.

The driver outputs are emitter followers that source a minimum of 15 mA of current. The sink current, internally limited at 700 mA, can be increased by adding resistors to ground at the driver outputs.

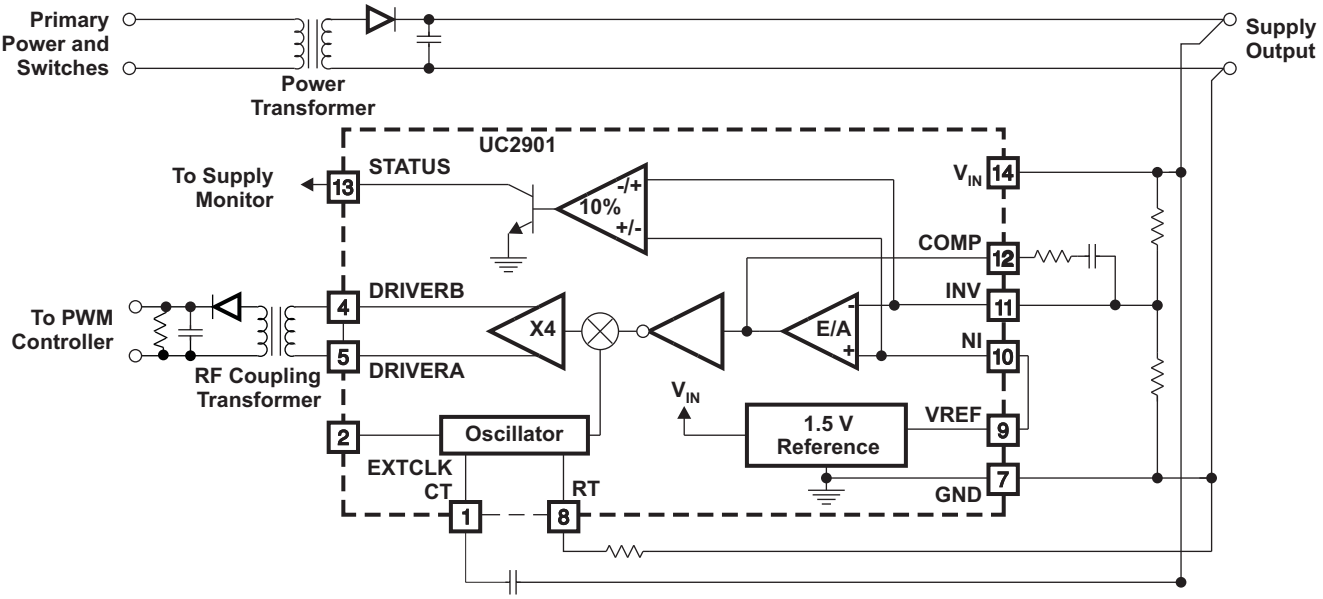


Figure 4. Transformer-Coupled Feedback

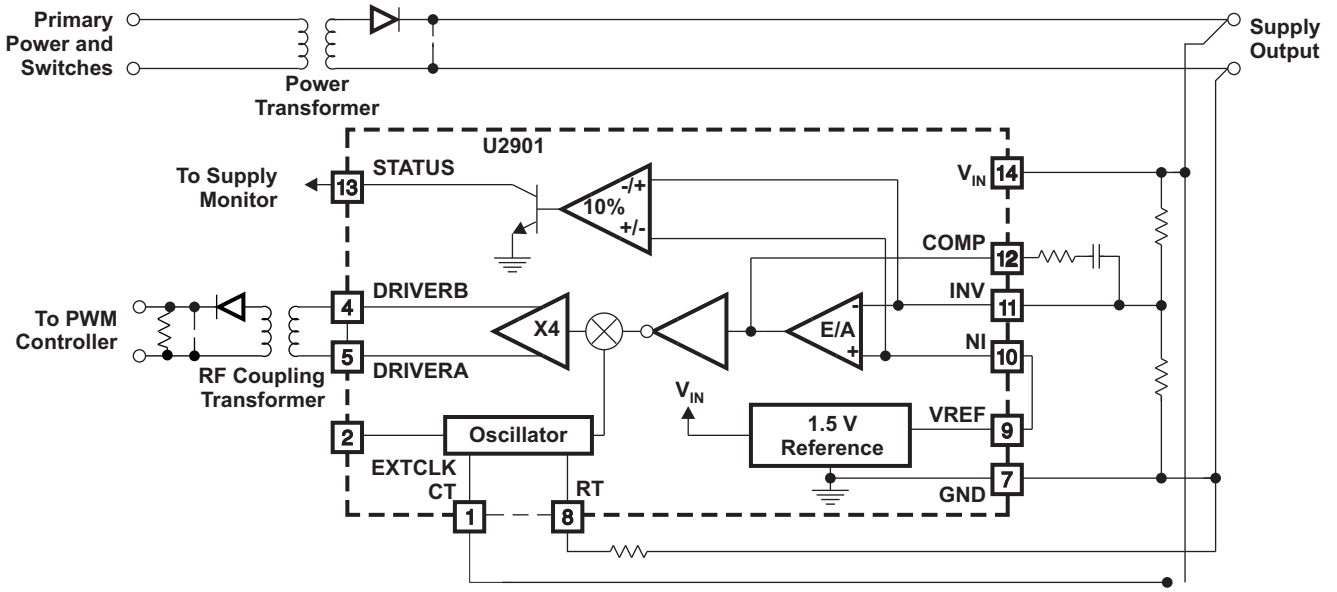


Figure 5. Feedback-Coupled at Switching Frequency

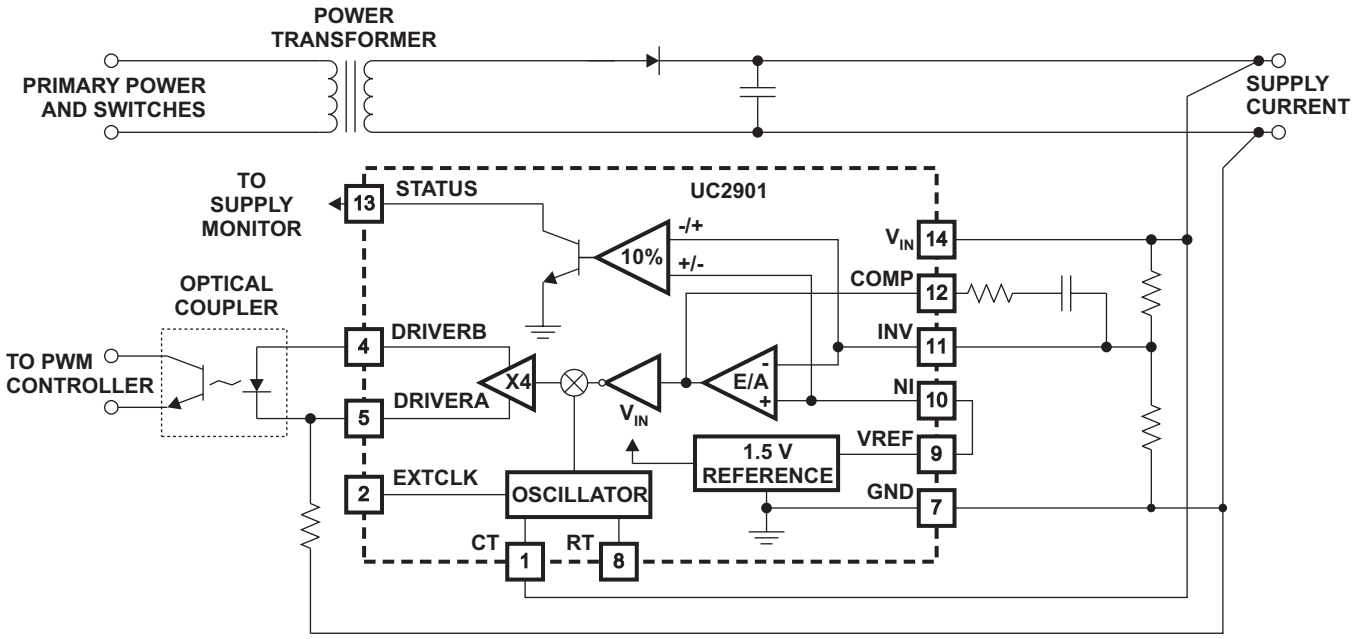


Figure 6. Optically-Coupled DC Feedback

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2901MDREP	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	UC2901MEP	Samples
UC2901MDREPG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	UC2901MEP	Samples
V62/07609-01XE	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	UC2901MEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF UC2901-EP :

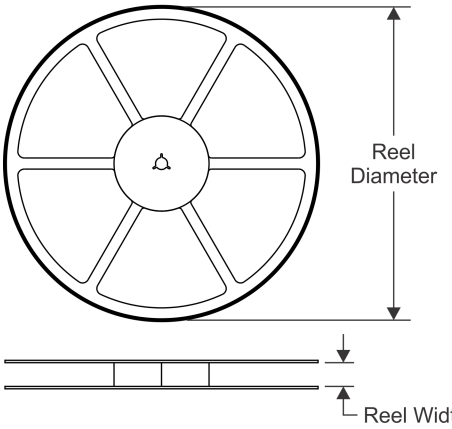
- Catalog: UC2901

NOTE: Qualified Version Definitions:

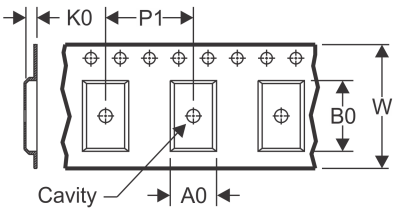
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

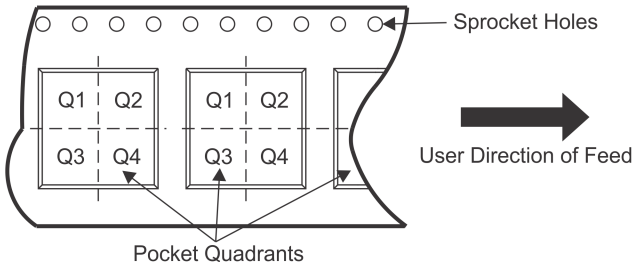


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

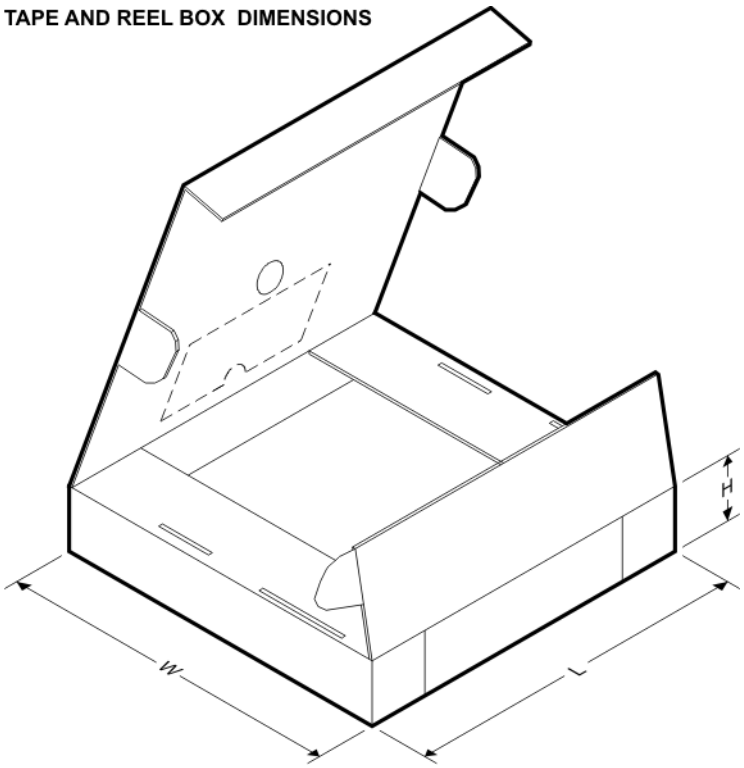
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2901MDREP	SOIC	D	14	2500	330.0	16.4	6.55	9.05	2.1	8.0	16.0	Q1

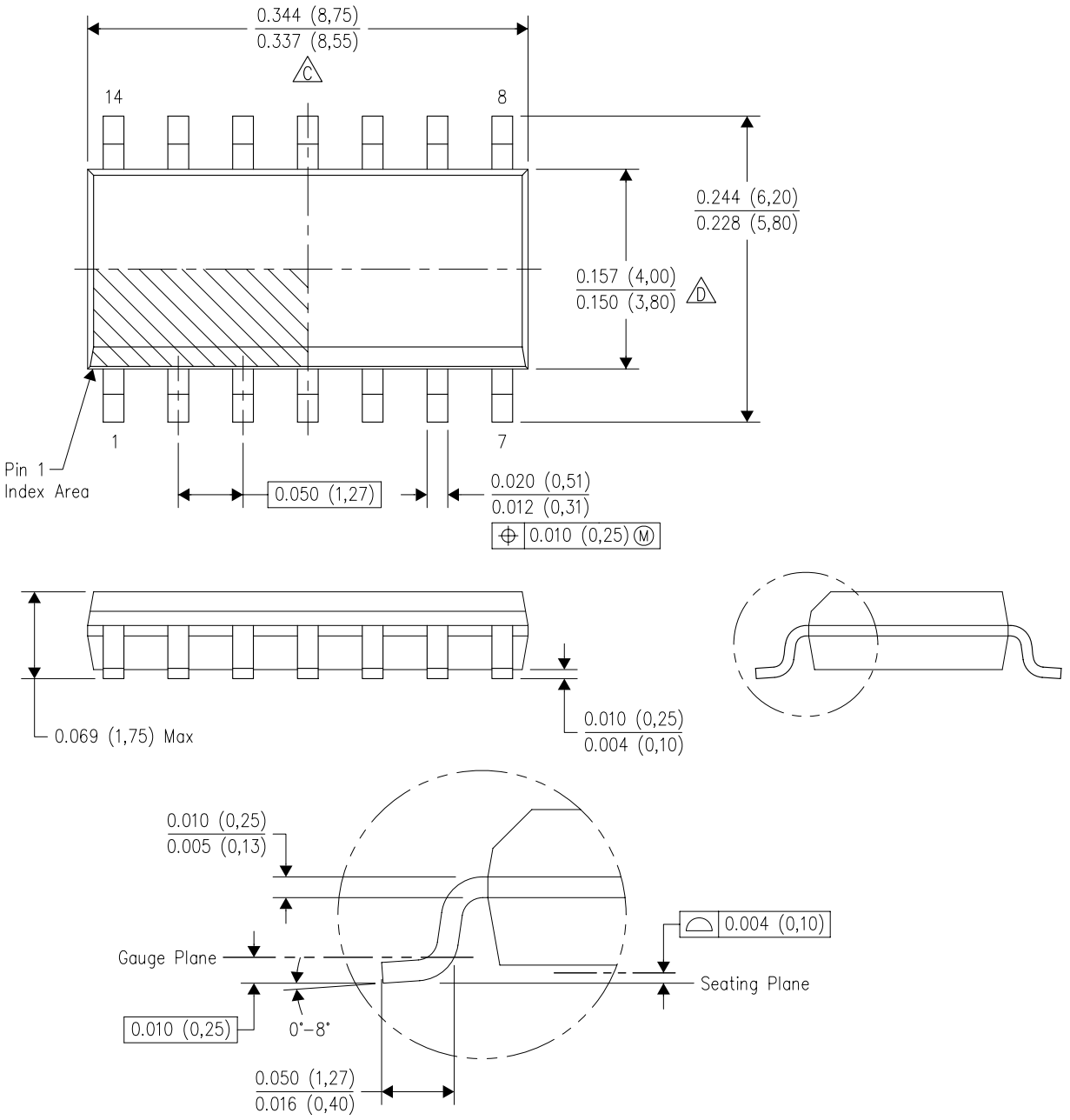
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2901MDREP	SOIC	D	14	2500	346.0	346.0	33.0

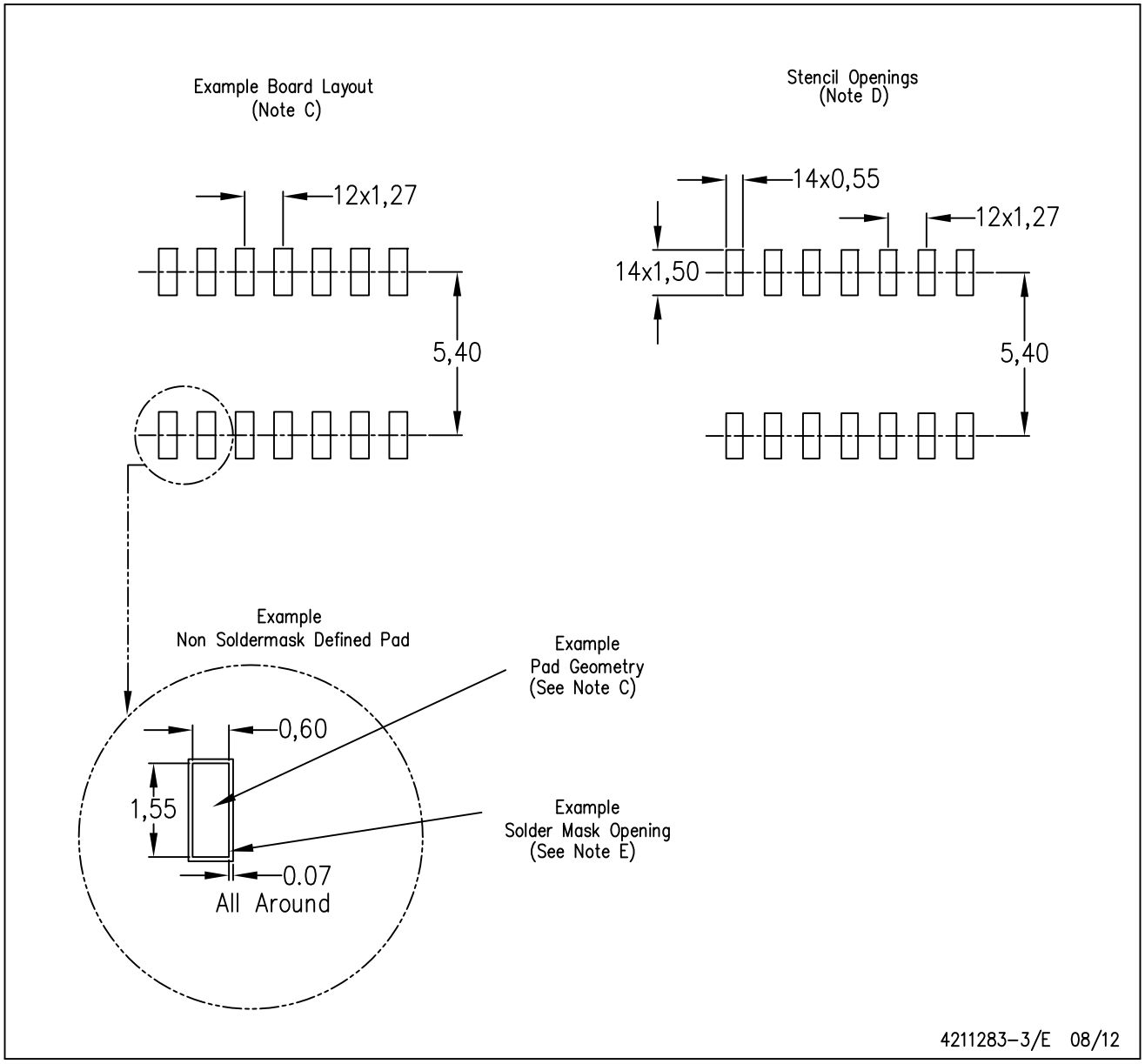
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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