19-2483; Rev 0; 12/07

High-Performance, Dual-Output, Network Clock Synthesizer

General Description

The MAX3674 is a high-performance network clock synthesizer IC for networking, computing, and telecom applications. It integrates a crystal oscillator, a low-noise phase-locked loop (PLL), programmable dividers, and high-frequency LVPECL output buffers. The PLL generates a high-frequency clock based on a low-frequency reference clock provided by the on-chip crystal oscillator or an external LVCMOS clock. The MAX3674 has excellent period jitter, cycle-to-cycle jitter, and supply noise rejection performance. With output frequencies programmable from 21.25MHz to 1360MHz and support of two differential PECL output signals, the device provides a versatile solution for the most demanding clock applications.

Programming is accomplished through a 2-wire I²C bus or parallel interface that can change the output frequency on demand for frequency margining. Both LVPECL outputs have synchronous stop functionality, and the PLL has a LOCK indicator output. The MAX3674 operates from a +3.3V supply and typically consumes 396mW. The device is packaged in a 48-pin LQFP, and the operating temperature range is from -40°C to +85°C.

Applications

Ethernet Network ASIC Clock Generation

Storage Area Network ASIC Clocking

Optical Network ASIC Clocking

Programmable Clock Source for Server, Computing, or Communication Systems

Frequency Margining

Features

- **21.25MHz to 1360MHz Programmable PLL Synthesized Output Clocks**
- **Two Differential LVPECL-Compatible Outputs**
- **Cycle-to-Cycle Jitter 1.6ps RMS and Period Jitter 0.9ps RMS at 500MHz**
- **On-Chip Crystal Oscillator or Selectable LVCMOS-Compatible Reference Clock Input**
- **Excellent Power-Supply Noise Rejection**
- **Parallel or 2-Wire I²C Programming Interface**
- **Lock Indicator Output**
- **+3.3V Power Supply**
- **Power Consumption: 396mW at 3.3V**
- **48-Pin LQFP Pb-Free Package**
- **-40°C to +85°C Temperature Range**

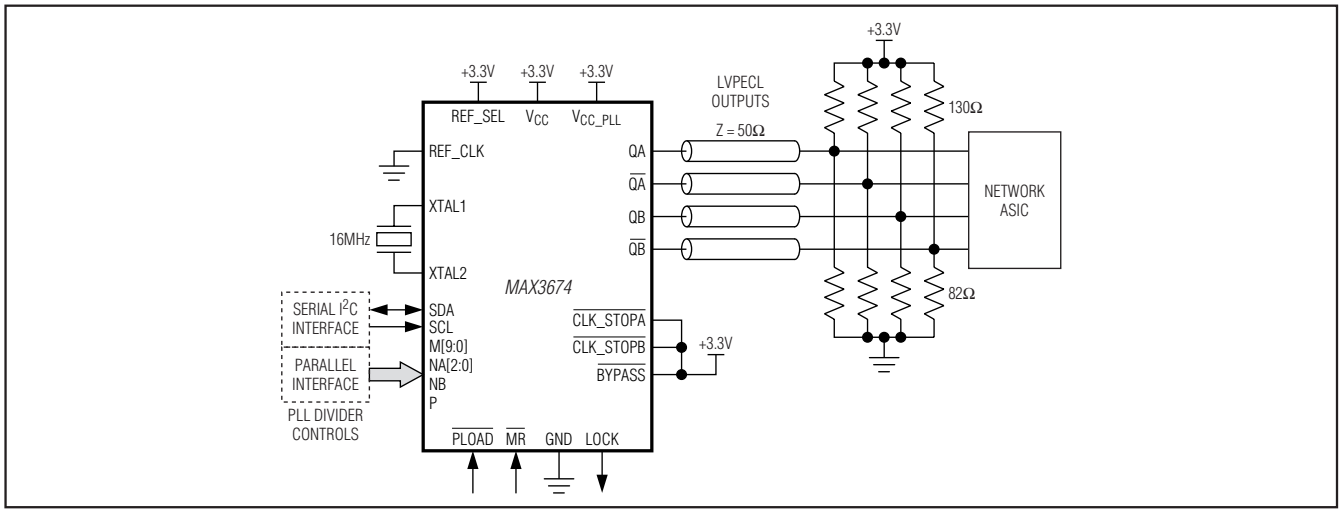
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3674ECM+	-40°C to +85°C	48 LQFP

+Denotes a lead-free/RoHS-compliant package.

Pin Configuration appears at end of data sheet.

Typical Application Circuit



High-Performance, Dual-Output, Network Clock Synthesizer

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range (V_{CC} and V_{CC_PLL}).....-0.3V to +3.9V
DC Input Voltage Range ($\overline{BYPASS}$, REF_SEL, REF_CLK, $\overline{CLK_STOPx}$, XTAL1, XTAL2, M[9:0], TEST_EN, NB, NA[2:0], $\overline{PLOAD}$, $\overline{MR}$, SDA, SCL, ADR[1:0], P) to GND.....-0.3V to (V_{CC} + 0.3V)
DC Output Voltage Range (LOCK, SDA, Qx, $\overline{Qx}$).....-0.3V to (V_{CC} + 0.3V)
DC Input Current.....±20mA
DC Output Current.....±50mA
Continuous Power Dissipation (T_A = +70°C)
48-Pin LQFP (derate 21.7mW/°C above 70°C).....1739mW
Operating Ambient Temperature Range (T_A).....-40°C to +85°C
Operating Junction Temperature (T_J).....+150°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{CC_PLL} = +3.3V ±5%, T_A = -40°C to +85°C, $\overline{BYPASS}$ = high, TEST_EN = low. Typical values are at V_{CC} = V_{CC_PLL} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVCMOS INPUTS ($\overline{BYPASS}$, REF_SEL, REF_CLK, $\overline{CLK_STOPx}$, M[9:0], TEST_EN, NB, NA[2:0], $\overline{PLOAD}$, $\overline{MR}$, ADR[1:0], P)						
Input High Voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		-0.3		+0.8	V
Input Current	I_{IH}, I_{IL}	V_{IN} = V_{CC} or GND (Note 2)			±200	µA
Input Capacitance	C_{IN}			4.0		pF
I²C INPUTS (SDA, SCL)						
Input High Voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		-0.3		+0.8	V
Input Current	I_{IH}, I_{IL}	V_{IN} = V_{CC} or GND			±10	µA
I²C OPEN-DRAIN OUTPUT (SDA)						
Output Low Voltage	V_{OL}	I_{OL} = +4mA			0.4	V
LVCMOS/TTL OUTPUT (LOCK)						
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = +4mA			0.4	V
LVPECL DIFFERENTIAL CLOCK OUTPUTS (Qx, $\overline{Qx}$)						
Output High Voltage	V_{OH}	(Note 3)	V_{CC} - 1.25		V_{CC} - 0.74	V
Output Low Voltage	V_{OL}	(Note 3)	V_{CC} - 1.95		V_{CC} - 1.45	V
POWER SUPPLY						
Supply Voltage	V_{CC}		3.135	3.3	3.465	V
PLL Supply Voltage	V_{CC_PLL}	(Note 4)	3.035	3.3	3.465	V
Supply Current	I_{CC}	Includes PECL output currents (Note 3)		120	136	mA
		PECL outputs open		81		
PLL Supply Current	I_{CC_PLL}				10	mA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{CC_PLL} = +3.3V ±5%, T_A = -40°C to +85°C, NB = 1 (low), P = 4 (high), $\overline{BYPASS}$ = high, TEST_EN = low. Typical values are at V_{CC} = V_{CC_PLL} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTERNAL REFERENCE CLOCK INPUT (REF_CLK)						
Input Frequency	f_{REF_CLK}		15	16	20	MHz
Input Rise/Fall Time		20% to 80%		5		ns
Input Duty Cycle			30		70	%
CRYSTAL OSCILLATOR (XTAL1, XTAL2)						
Crystal Input Frequency	f_{XTAL}		15	16	20	MHz
CLOCK OUTPUT PERFORMANCE (Qx, $\overline{Qx}$) (Note 3)						
VCO Frequency	f_{VCO}	(Note 5)	1360		2720	MHz
Output Frequency (Note 6)	f_{OUT}	NA = 2	680		1360	MHz
		NA = 4	340		680	
		NA = 8	170		340	
		NA = 16	85.0		170	
		NA = 32	42.5		85.0	
		NA = 64	21.25		42.50	
Output Clock Duty Cycle	DC	f_{QA} = f_{QB} ≤ 500MHz	46.0	50	54.0	%
		f_{QA} = f_{QB} ≤ 680MHz	44.8	50	55.2	
		f_{QA} = f_{QB} ≤ 1360MHz	42.0	50	56.8	
Output-to-Output Skew		NB = 1 (f_{QA} = f_{QB}) (Note 7)			38	ps
		NB = 2 (f_{QA} = 2 × f_{QB}), f_{QA} ≤ 500MHz		10		
Output Rise/Fall Time	t_R, t_F	20% to 80%	45		340	ps
Output Peak-to-Peak Voltage (Single-Ended) (Note 7)		f_{OUT} ≤ 1000MHz	0.49		1.0	V_{P-P}
		1000MHz < f_{OUT} ≤ 1360MHz	0.32		1.0	
Output Enable Time	t_{EN}	Figures 3 and 4, t_{Qx} = output period		2 × t_{Qx}		
Output Disable Time	t_{DIS}	Figures 3 and 4, t_{Qx} = output period		2 × t_{Qx}		
Cycle-to-Cycle Jitter (Notes 7, 8)	J_{CC}	NA = 2			3.7	ps_{RMS} (1σ)
		NA = 4			6.4	
		NA = 8, 16, 32, 64			8.5	
		NA = 4, NB = 1		13		ps_{P-P}
		NA = 4, NB = 2 (Note 9)		35		
Period Jitter (Notes 7, 8)	J_{PER}	NA = 2			2.5	ps_{RMS} (1σ)
		NA = 4			3.7	
		NA = 8, 16, 32, 64			4.9	
		NA = 4, NB = 1		7		ps_{P-P}
		NA = 4, NB = 2 (Note 9)		18		
Relative Sideband Spur Power Due to Power-Supply Noise		(Note 10)		-38		dBc

High-Performance, Dual-Output, Network Clock Synthesizer

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{CC_PLL} = +3.3V ±5%, T_A = -40°C to +85°C, NB = 1 (low), P = 4 (high), $\overline{BYPASS}$ = high, TEST_EN = low. Typical values are at V_{CC} = V_{CC_PLL} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PLL Closed-Loop Bandwidth (Note 11)		P = 2		150 to 450		kHz
		P = 4		75 to 225		
PLL Lock Time	t_{LOCK}	(Note 12)		3	6	ms
PLL Acquisition Time When Incrementing or Decrementing M		(Note 13)		50		µs
CONTROL TIMING ($\overline{PLOAD}$, $\overline{MR}$)						
$\overline{PLOAD}$ Pulse Width			50			ns
$\overline{MR}$ Pulse Width			50			ns
SERIAL INTERFACE I^2C (SDA, SCL)						
I^2C Clock Frequency	f_{SCL}				400	kHz
SDA Output Fall Time	t_F	(Note 14)			300	ns

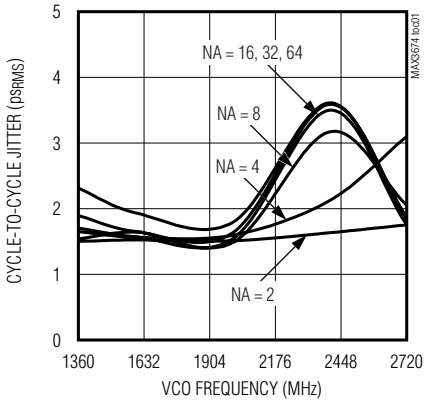
Note 1: Specifications ≥ +25°C guaranteed by production test, < +25°C guaranteed by design and characterization.
Note 2: Inputs have pullup and pulldown resistors affecting the input current.
Note 3: Outputs terminated 50Ω to V_{TT} = V_{CC} - 2V. See the *AC Electrical Characteristics* section for Peak-to-Peak Voltage.
Note 4: PLL supply voltage must also satisfy $V_{CC_PLL} \le V_{CC}$ + 0.3V.
Note 5: The reference clock input frequency f_{XTAL} (and f_{REF_CLK}) and the PLL divider M and P must match the VCO frequency range: $f_{VCO} = f_{XTAL} \times M / P$ for stable PLL operation.
Note 6: The output frequency for QA and QB if NB = 1 (low) and f_{REF} = 16MHz. With NB = 2 (high) the QB output frequency is half the QA output frequency.
Note 7: Guaranteed by design and characterization over full temperature range (-40°C to +85°C).
Note 8: Selecting crystal oscillator as reference with f_{XTAL}= 16MHz.
Note 9: When NB = 2 (high), the QA output has a bimodal jitter distribution. Sample size = 20,000 cycles.
Note 10: Measured as spur in frequency domain with 50mV_{P-P} sinusoidal noise (10kHz to 10MHz) on the supply. See the *Typical Operating Characteristics*.
Note 11: -3dB point of PLL transfer characteristics.
Note 12: Time period from master reset release ($\overline{MR}$ rising edge) to when PLL indicates lock (LOCK rising edge). Valid for both crystal (after crystal oscillator stabilized) and reference clock inputs.
Note 13: Time period after incrementing or decrementing (ΔM < 5) within valid M range to when PLL indicates lock (LOCK rising edge).
Note 14: An appropriate bus pullup resistance must be selected depending on board capacitance.

High-Performance, Dual-Output, Network Clock Synthesizer

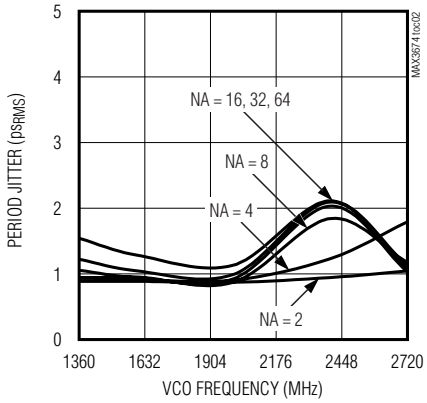
Typical Operating Characteristics

(V_{CC} = V_{CC_PLL} = +3.3V, T_A = +25°C, f_{QA} = f_{QB} = 500MHz (P = 4, NA = 4, NB = 1, M = 500), REF_SEL= high (crystal oscillator), f_{XTAL} = 16MHz, unless otherwise noted.)

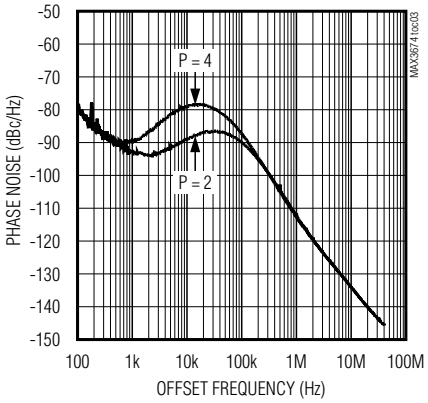
CYCLE-TO-CYCLE JITTER vs. VCO FREQUENCY



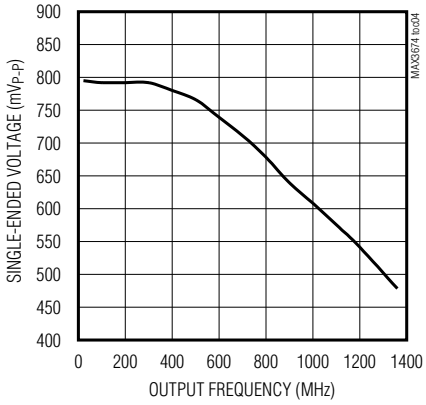
PERIOD JITTER vs. VCO FREQUENCY



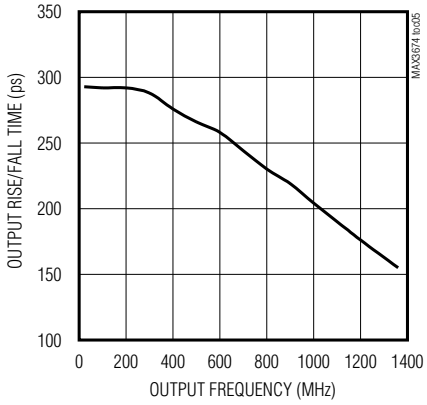
PHASE NOISE



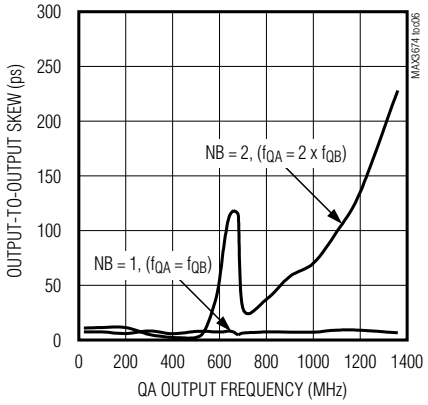
OUTPUT PEAK-TO PEAK VOLTAGE vs. OUTPUT FREQUENCY



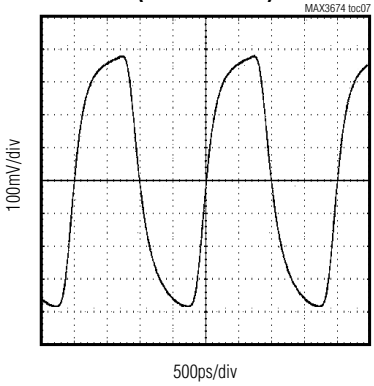
OUTPUT RISE/FALL TIME vs. OUTPUT FREQUENCY



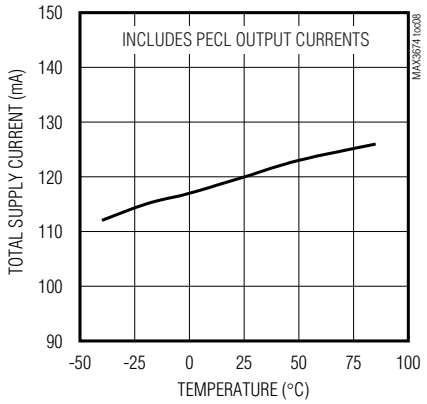
OUTPUT-TO-OUTPUT SKEW vs. OUTPUT FREQUENCY



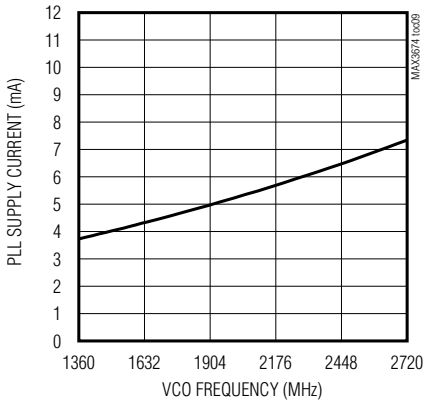
Qx CLOCK OUTPUT (SINGLE-ENDED)



TOTAL SUPPLY CURRENT vs. TEMPERATURE



PLL SUPPLY CURRENT vs. VCO FREQUENCY

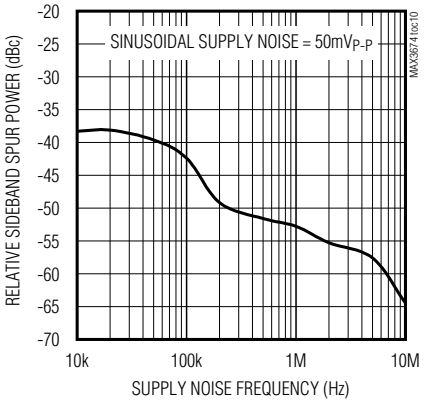


High-Performance, Dual-Output, Network Clock Synthesizer

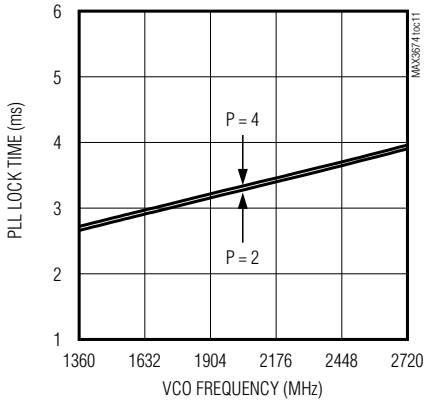
Typical Operating Characteristics (continued)

(V_{CC} = V_{CC_PLL} = +3.3V, T_A = +25°C, f_{QA} = f_{QB} = 500MHz (P = 4, NA = 4, NB = 1, M = 500), REF_SEL= high (crystal oscillator), f_{XTAL} = 16MHz, unless otherwise noted.)

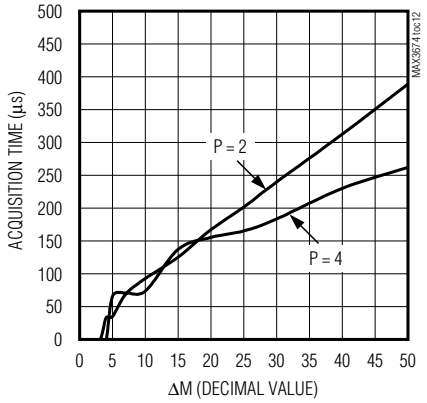
RELATIVE SIDEBAND SPUR POWER DUE TO POWER-SUPPLY NOISE



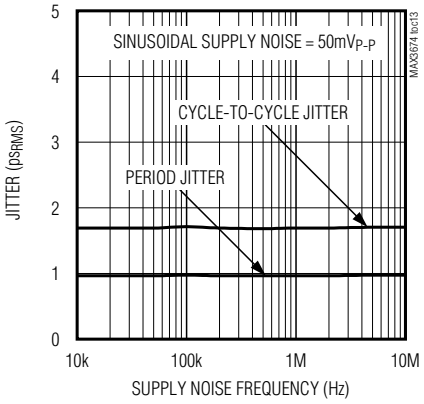
PLL LOCK TIME vs. VCO FREQUENCY ($\overline{MR}$ DEASSERT TO LOCK ASSERT)



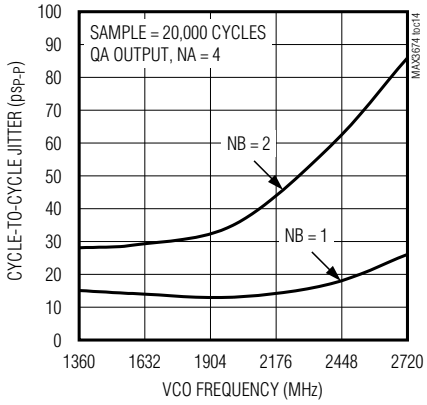
PLL ACQUISITION TIME WHEN INCREMENTING/DECREMENTING M



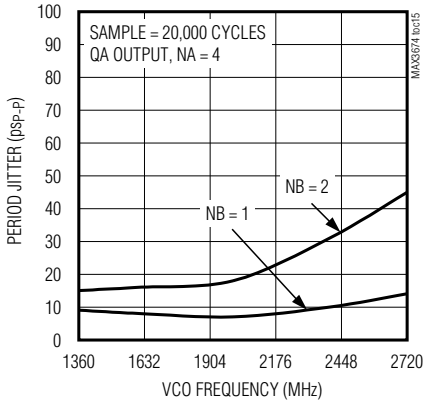
JITTER vs. SUPPLY NOISE FREQUENCY



CYCLE-TO-CYCLE JITTER (PEAK-TO-PEAK) vs. VCO FREQUENCY



PERIOD JITTER (PEAK-TO-PEAK) vs. VCO FREQUENCY



Pin Description

PIN	NAME	I/O	TYPE	FUNCTION
1, 4, 13, 30, 34, 36, 42	V_{CC}	Supply	V_{CC}	Positive Power Supply
2	$\overline{BYPASS}$	Input	LVCMOS	Selects the Static Circuit Bypass Mode
3, 8, 19, 27, 31, 37	GND	Supply	Ground	Ground
5	V_{CC_PLL}	Supply	V_{CC}	Positive Power Supply for the PLL (Analog Power Supply). It is recommended to use an external passive filter for the supply pin V_{CC_PLL}. See Figure 5.
6	REF_SEL	Input	LVCMOS	Selects Reference Clock Input
7	REF_CLK	Input	LVCMOS	PLL External Reference Clock Input
9, 10	$\overline{CLK_STOPA}$, $\overline{CLK_STOPB}$	Input	LVCMOS	Output Qx Disable in Logic-Low State
11, 12	XTAL1, XTAL2	Input	Analog	Crystal Oscillator Interface
14–18, 20–24	M[9:0]	Input	LVCMOS	PLL Feedback-Divider Configuration
25	TEST_EN	Input	LVCMOS	Factory Test Mode Enable. This pin must be connected to GND in all applications of the device.
26	LOCK	Output	LVCMOS	PLL Lock Indicator
28	$\overline{QB}$	Output	LVPECL	Channel B Differential Clock Output
29	QB			
32	$\overline{QA}$	Output	LVPECL	Channel A Differential Clock Output
33	QA			
35	NB	Input	LVCMOS	PLL Postdivider Configuration for Output QB
38, 39, 40	NA[2:0]	Input	LVCMOS	PLL Postdivider Configuration for Output QA and QB
41	$\overline{PLOAD}$	Input	LVCMOS	Selects the Programming Interface for Parallel or I^2C
43	$\overline{MR}$	Input	LVCMOS	Device Master Reset
44	SDA	Input/ Output	LVCMOS/ Open Drain	I^2C Data
45	SCL	Input	LVCMOS	I^2C Clock
46, 47	ADR[1:0]	Input	LVCMOS	Selectable Two Bits of the I^2C Slave Address
48	P	Input	LVCMOS	PLL Predivider Configuration

High-Performance, Dual-Output, Network Clock Synthesizer

Function Table

PIN	DEFAULT (Note 1)	FUNCTION WHEN SET LOW 0	FUNCTION WHEN SET HIGH 1
INPUT PINS			
REF_SEL	1	Selects REF_CLK input as PLL reference clock.	Selects XTAL interface as PLL reference clock.
P	1	PLL predivider parallel programming interface. See Table 4.	
M[9:0]	01 1111 0100 b (Note 2)	PLL feedback-divider (10-bit) parallel programming interface. See Table 5.	
NA[2:0]	010	PLL postdivider parallel programming interface. See Table 6.	
NB	0	PLL postdivider parallel programming interface. See Table 7.	
$\overline{PLOAD}$	0	Selects the parallel programming interface. The internal PLL divider settings (M, NA, NB, and P) are equal to the setting of the hardware pins. Leaving the M, NA, NB, and P pins open (floating) results in a default PLL configuration with f_{OUT} = 250MHz. PLL settings can be read through the I^2C interface.	Selects the serial (I^2C) programming interface. The internal PLL divider settings (M, NA, NB, and P) are set and read through the serial interface.
ADR[1:0]	00	Address bit = 0	Address bit = 1
SDA, SCL	—	See the *Programming Through Serial I^2C Interface* section.	
$\overline{BYPASS}$	1	PLL function bypassed. $f_{QA} = f_{REF} / NA$ and $f_{QB} = f_{REF} / (NA \times NB)$ LOCK = test output	PLL function enabled. $f_{QA} = (f_{REF} / P) \times M / NA$ and $f_{QB} = (f_{REF} / P) \times M / (NA \times NB)$
TEST_EN	0	Normal operation mode. Factory test mode disabled.	Factory test mode enabled.
$\overline{CLK_STOPx}$	1	Output Qx is synchronously disabled in logic-low state.	Output Qx is synchronously enabled.
$\overline{MR}$	—	The device is reset. The output frequency is zero and the outputs are asynchronously forced to a logic-low state. After releasing reset (upon the rising edge of $\overline{MR}$ and independent on the state of $\overline{PLOAD}$), the MAX3674 reads the parallel interface (M, NA, NB, and P) to acquire a valid startup frequency configuration.	The PLL attempts to lock to the reference signal. The t_{LOCK} specification applies.
OUTPUT PIN			
LOCK	—	PLL is not locked.	PLL is frequency locked.

Note 1: Default states are set by internal input 75kΩ pullup or pulldown resistors.
Note 2: If f_{REF} = 16MHz, the default configuration results in a 250MHz output frequency.

Detailed Description

The MAX3674 is a high-performance wide-frequency range clock synthesizer. It integrates a crystal oscillator, PLL, programmable dividers, configuration registers, two differential PECL outputs buffers (QA, QB), and an LVCMOS lock indicator output (Figure 1). Using a low-frequency clock as a reference, the internal PLL generates a high-frequency output clock with excellent jitter performance. The programmable dividers make it possible to generate a wide range of output frequencies (21.25MHz to 1360MHz) and perform frequency margining using the increment and decrement functions.

Reference Clock

An integrated oscillator provides the low-frequency reference clock for the PLL. This oscillator requires an external quartz crystal connected between XTAL1 and XTAL2 (Table 12). Alternatively, an LVCMOS-compatible clock source can be connected to the REF_CLK input to serve as the reference clock.

Phase-Locked Loop (PLL)

The reference clock passes through a predivider (P) before entering the PLL. The PLL contains a phase-frequency detector (PFD), lowpass filter, and voltage-controlled oscillator (VCO) with a 1360MHz to 2720MHz operating range. The VCO output is connected to the PFD input through a feedback divider (M). The PFD compares the divided reference clock (f_{REF} / P) to the divided-down VCO output (f_{VCO} / M) and generates a control signal that keeps the VCO locked to the reference clock. After scaling the VCO output with postdividers ($N_{A,B}$), the high-frequency clock is sent to the PECL output buffers. To minimize noise-induced jitter, the PLL supply (V_{CC_PLL}) is isolated from the supply for the core logic and output buffers.

Configuration Registers and Dividers

Output frequency depends on the reference clock frequency f_{REF}, the predivider P, the feedback divider M, and the postdividers $N_{A,B}$. Dividers are programmable through configuration logic that uses either a serial or parallel interface as selected by the $\overline{PLOAD}$ input. The parallel interface uses the values at the P, M[9:0], NA[2:0], and NB parallel inputs to configure the internal dividers. The serial interface is I^2C compatible and provides read and write access to configuration registers.

LVPECL Outputs

The high-frequency outputs, QA and QB, use differential PECL buffers designed to drive a pair of transmission lines terminated 50Ω to $V_{TT} = V_{CC}$ - 2.0V. Both differential outputs can be enabled/disabled independently using the $\overline{CLK_STOPx}$ inputs. The $\overline{CLK_STOPx}$ inputs are synchronized to the output clock signal to eliminate the possibility of producing runt pulses. Using the postdivider NB, the secondary output QB can be configured to run at 1x or 1/2x the frequency of the primary output QA.

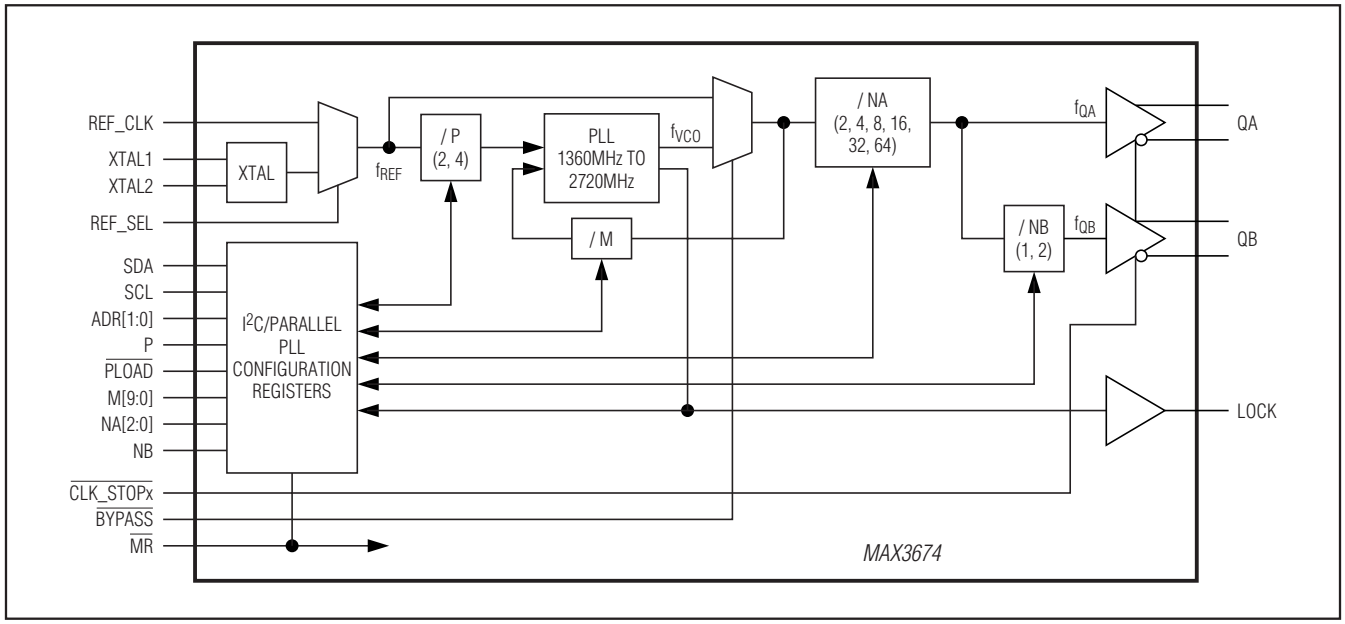


Figure 1. Functional Diagram

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Lock Indicator

The PFD within the PLL generates the lock indicator and operates by comparing the divided down VCO output (f_{VCO} / M) to a divided down reference clock (f_{REF} / P). The LOCK output pin indicates that the PLL is locked (LOCK = 1) when the VCO has obtained phase and frequency lock with the reference clock. See the *LOCK Detect* section in the *Applications Information* section for further details.

Internal Register Definitions

The MAX3674 has four 8-bit-wide internal registers for accessing through the I^2C interface. The registers include two configuration registers (PLL_L and PLL_H), a command register (CMD), and an ID register (ID). Tables 1 and 2 show the register map, definitions, and default values.

Table 1. Register Map

ADDRESS	NAME	CONTENT	ACCESS
0x00h	PLL_L	Least significant 8 bits of PLL feedback divider M, M[7:0]	R/W
0x01h	PLL_H	Most significant 2 bits of M, M[9:8] and NA[2:0], NB, P, LOCK	R/W
0xF0h	CMD	Command register	W
0x08h	ID	Unique bit pattern for identification (8'b01010100)	R

Table 2. Register Definition and Default Values

REGISTER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
PLL_L	M7	M6	M5	M4	M3	M2	M1	M0
	1	1	1	1	0	1	0	0
PLL_H	M9	M8	NA2	NA1	NA0	NB	P	LOCK
	0	1	0	1	0	0	1	x
CMD	Command INC (0x01), increase internal PLL frequency M := M + 1							
	x	x	x	x	0	0	0	1
	Command DEC (0x02), decrease internal PLL frequency M := M - 1							
	x	x	x	x	0	0	1	0
	Command LOAD (0x04), update PLL divider configuration, PLL divider M, NA, NB, P := PLL_L, PLL_H							
	x	x	x	x	0	1	0	0
	Command GET (0x08), update the configuration registers, PLL_L, PLL_H := PLL divider M, NA, NB, P							
	x	x	x	x	1	0	0	0
ID	MAX3674 unique device ID							
	0	1	0	1	0	1	0	0

I²C Characteristics

The MAX3674 acts as a slave device on the I²C bus supporting fast-mode data transfer (up to 400kbps). Its clock pin, SCL, is an input only. It does not support clock stretching. Table 3 shows the I²C slave address.

Table 3. I²C Slave Address

BIT	7 (MSB)	6	5	4	3	2	1	0 (LSB)
VALUE	1	0	1	1	0	ADR1	ADR0	R/$\overline{W}$

The slave address is composed of a 5-bit fixed address and 2-bit variable address that is set by the input pins ADR[1:0]. The variable address pins are used to avoid address conflicts of multiple MAX3674 devices on the same I²C bus.

The host controller uses bit 0 (LSB) of the MAX3674 slave address to select either read or write mode. "0" indicates I²C "write" to the MAX3674 registers; "1" indicates I²C "read" from the MAX3674 registers.

Applications Information

Programming the MAX3674

The MAX3674 PLL configurations can be controlled either through the parallel interface or the serial I²C interface. The parallel interface allows the user to directly configure the PLL dividers through hardwired pins without the overhead of a serial interface. At device startup, the device always obtains an initial PLL frequency configuration through the parallel interface. The PLL configuration can be read through I²C in parallel interface mode.

The serial interface is I²C compatible. It allows reading and writing device settings through built-in registers. It also allows a host controller to program the output frequency of the synthesizer on the fly using the increment and decrement functions for frequency margining applications.

An LVCMOS-compatible input ($\overline{PLOAD}$) is used to select the parallel interface or serial interface, as described in the *Function Table*.

Output Frequency Configuration

The MAX3674 output frequency (f_{OUT}) is a function of the reference frequency (f_{REF}) and the programmable dividers (P, M, and $N_{A,B}$) and is expressed as:

$$f_{OUT} = \frac{f_{REF}}{P} \times \frac{M}{N_{A,B}}$$

The numbers P, M, NA, and NB are divider ratios requiring configuration through parallel programming or I²C serial interfaces using registers PLL_L and PLL_H. P is the predivider to the input of the phase-locked loop (PLL) and has a valid division ratio of 2 or 4 (Table 4). P can be set by the parallel interface pin P or through the serial I²C interface. M is determined by the inputs at the 10-pin M[9:0] through parallel interface or by programming through the serial I²C interface (Table 5). NA determines the postdivider for differential output QA and QB, and has a valid division value of 2, 4, 8, 16, 32, or 64 based on the 3-pin inputs NA[2:0] (Table 6). NA can also be set through the serial I²C interface. NB is the postdivider for output QB and has a valid value of 1 or 2 (Table 7). NB can be set by the parallel interface pin NB or through the serial I²C interface.

Table 4. Pre-PLL Divider P

P	VALUE	DEFAULT VALUE
0	f_{REF} / 2	—
1	f_{REF} / 4	1

Table 5. PLL Feedback Divider M

M[9:0]	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	DEFAULT VALUE
136	0	0	1	0	0	0	1	0	0	0	—
137	0	0	1	0	0	0	1	0	0	1	—
. . .											—
500	0	1	1	1	1	1	0	1	0	0	01 1111 0100
. . .											—
512	1	0	0	0	0	0	0	0	0	0	—
. . .											—
724	1	0	1	1	0	1	0	1	0	0	—
725	1	0	1	1	0	1	0	1	0	1	—

High-Performance, Dual-Output, Network Clock Synthesizer

Table 6. Post-PLL Divider NA

NA2	NA1	NA0	f_{OUT} (QA)	DEFAULT VALUE
0	0	0	f_{VCO} / 2	—
1	0	0	f_{VCO} / 4	—
0	1	0	f_{VCO} / 8	0 1 0
1	1	0	f_{VCO} / 16	—
0	0	1	f_{VCO} / 32	—
1	0	1	f_{VCO} / 64	—

Table 7. Output NB Divider Setting

NB INPUT	QB DIVIDER RATIO	OUTPUT FREQUENCY f_{QB} (MHz)	DEFAULT VALUE
0	1	$f_{QB} = f_{QA}$	0
1	2	$f_{QB} = f_{QA} / 2$	—

For a given reference frequency f_{REF} (f_{XTAL}), the PLL feedback divider M must be configured to match the specified VCO frequency range (1360MHz to 2720MHz) to achieve a valid PLL configuration. For example, with f_{REF} = 16MHz and P = 4, M has a valid value between 340 and 680.

$$f_{VCO} = \frac{f_{REF}}{P} \times M$$

$$1360 \le f_{VCO} \le 2720$$

Invalid PLL configuration leads to VCO frequencies beyond the specified lock range and can result in loss of lock. M is chosen to be between 136 and 725 for the whole reference frequency range, 15MHz to 20MHz.

The smallest possible change in the output frequency is the synthesizer granularity G (difference in f_{OUT} when incrementing or decrementing M). G is a function of f_{REF} and dividers P, NA, and NB. The MAX3674 typically provides a resolution of less than 1% for granularity G. See Table 8.

$$G = \frac{f_{REF}}{P \times N_{A,B}}$$

The purpose of the PLL predivider P is to scale the reference frequency for operations within the PLL. The setting for P affects the generator output frequency granularity and PLL loop bandwidth. For a given output frequency, P = 4 results in a finer (smaller) output frequency granularity, G, and a smaller PLL bandwidth compared to the P = 2 setting.

Table 8 shows an example of the output frequency resolution at different output frequencies, assuming a 16MHz reference clock is used.

Table 8. Frequency Ranges (f_{REF} = 16MHz)

f_{OUT} (QA) (MHz)		NA	M	P	G (MHz)
MIN	MAX				
680	1360	2	170–340	2	4
			340–680	4	2
340	680	4	170–340	2	2
			340–680	4	1
170	340	8	170–340	2	1
			340–680	4	0.5
85	170	16	170–340	2	0.5
			340–680	4	0.25
42.5	85	32	170–340	2	0.25
			340–680	4	0.125
21.25	42.5	64	170–340	2	0.125
			340–680	4	0.0625

Example of Output Frequency Configuration

The following steps provide an example of how to determine the appropriate settings for P, M, NA, and NB given that a 16MHz reference (f_{REF}) is available and the desired output frequency (f_{OUT}) is 500MHz with fine granularity (P = 4).

1) Determine the output divider setting for NA that provides an output frequency range that encompasses the desired output frequency. According to Table 8, the desired frequency of 500MHz falls into the f_{OUT} range of 340MHz–680MHz, requiring NA = 4.

2) Calculate the VCO frequency:

$$f_{VCO} = f_{OUT} \times NA$$

In this case, f_{OUT} = 500MHz, NA = 4, giving f_{VCO} = 500MHz × 4 = 2000MHz.

3) Determine the setting for the feedback divider M:

$$M = \frac{f_{VCO}}{f_{REF}} \times P$$

The finest granularity is obtained with P = 4, and in this case corresponds to 1MHz (see Table 8). The value for M is then calculated as M = (2000MHz / 16MHz) × 4 = 500.

4) Configure the MAX3674 with the obtained settings:

   P = 1b (/ 4 divider, see Table 4)
   M[9:0] = 0111110100b (binary number for M = 500)
   NA[2:0] = 100b (/ 4 divider, see Table 6)
   NB = 0b (/ 1 divider, $f_{QA} = f_{QB}$)

5) Apply the settings with the parallel or serial interface. The I²C configuration bytes for this example are PLL_L = 11110100b and PLL_H = 01100010b. See Tables 1 and 2 for the registers maps.

Programming Through Parallel Interface

The parallel interface comprises 15 pins (P, M[9:0], NA[2:0], and NB) for configuring the PLL frequency setting. The parallel interface is enabled with the $\overline{PLOAD}$ input set to logic-low. While $\overline{PLOAD}$ remains low, any logical state change on the 15 parallel pins immediately affects the internal divider settings, resulting in a change of the internal VCO frequency and the output frequency.

Upon startup, when the device master reset signal is released (rising edge of the $\overline{MR}$ signal), the device reads its startup configuration through the parallel interface and is independent of the $\overline{PLOAD}$ state. For startup, it is recommended to provide a valid PLL configuration (satisfying the VCO frequency range constraint). If all the parallel interface pins are left open, a default PLL configuration is loaded (Table 9).

While in parallel mode operation ($\overline{PLOAD}$ = 0), the I²C write access is disabled. Therefore, all data written into the MAX3674 registers through I²C is ignored. However, the MAX3674 is still present on the I²C interface and is read accessible, allowing the host controller to read the internal registers through the I²C interface for monitoring purpose.

In parallel mode ($\overline{PLOAD}$ = 0), I²C register access is limited to read only, implying that CMD register access is invalid. The MAX3674 allows read access to registers PLL_L, PLL_H, and ID through I²C and can verify the divider setting since the current PLL configuration in parallel mode is always stored in PLL_L and PLL_H.

After the low-to-high transition of $\overline{PLOAD}$, the configuration pins have no more effect, and the programming interface is now accessible through the serial I²C interface.

Programming Through Serial I²C Interface

While $\overline{PLOAD}$ = 1 the MAX3674 internal registers are read and write accessible through the 2-wire I²C interface using the SDA (configuration data) and SCL (configuration clock) signals. The MAX3674 acts as a slave device on the I²C bus, supporting fast-mode data transfer rates up to 400kbps.

The internal registers include two configuration registers (PLL_L and PLL_H), a command register (CMD), and an ID register (ID). See Tables 1 and 2 for the register maps. Registers PLL_L and PLL_H store a PLL configuration and provide full read/write access through the serial I²C interface. Register CMD is write only and accepts commands (LOAD, GET, INC, DEC) to update registers and for direct PLL frequency changes.

The CMD register provides a fast way to increase or decrease the synthesizer frequency and to update the PLL_L and PLL_H registers. LOAD and GET are inverse commands to each other. LOAD copies the data stored in the configuration registers into the PLL divider latches. GET copies the PLL dividers settings into the configuration registers (PLL_L, PLL_H). INC (DEC) directly increments (decrements) the PLL feedback divider M (M := M + 1, M := M - 1) and immediately changes the PLL frequency by the granularity step G (see Table 8 for available G) in a single I²C transfer without using the LOAD command. The INC and DEC commands are useful for frequency margining applications that require multiple and rapid PLL frequency changes. Note that the INC and DEC commands do not update the PLL_L and PLL_H registers. It is, therefore, recommended to use LOAD to set a valid PLL divider setting before using INC or DEC. In addition, the synthesizer does not check the validity of divider settings for proper operation bounded by the VCO range. So, applying the DEC and INC commands can result in invalid VCO frequencies and lead to loss of lock.

Programming the synthesizer output frequency through the serial I²C interface requires two steps: writing a valid PLL configuration to the configuration registers and loading the register data into the PLL divider latches with an I²C command. The PLL frequency is affected as a result of the second step. The two-step operations can be performed by a single I²C transaction or by multiple

Table 9. Parallel Interface Default

PARALLEL INTERFACE	M[9:0]	NA[2:0]	NB	P	f_{OUT}, QA (f_{REF} = 16MHz)
DEFAULT VALUE	01 1111 0100	010	0	1	250MHz

High-Performance, Dual-Output, Network Clock Synthesizer

independent I²C transactions. Alternatively, small frequency changes can be made in one step using the increment and decrement commands.

The following are three examples using the serial I²C interface.

Example 1: Set the synthesizer frequency.

1) Write the PLL_L and PLL_H registers with a valid configuration.
2) Write the LOAD command to update the PLL dividers with the current PLL_L, PLL_H content.

Example 2: Read the synthesizer frequency.

1) Write the GET command to update the PLL_L, PLL_H registers with the PLL divider settings.
2) Read the PLL_L, PLL_H registers through I²C protocol.

Example 3: Change the synthesizer frequency in small steps.

1) Write the INC or DEC command to change the synthesizer frequency by granularity step G.

The ID register is read only, used for the purpose of identification. When a read command is sent to the MAX3674, the content in ID is sent back to the controller together with the data in PLL_L and PLL_H, so a system can use this information accordingly. See Table 11.

When changing parallel mode into serial mode, at the rising edge of $\overline{PLOAD}$ input, the MAX3674 internal register contents and frequency divider configurations are not changed until rewritten by the user through the serial I²C interface. However, when changing serial mode into parallel mode, at the falling edge of $\overline{PLOAD}$ input, the internal register contents and frequency divider configurations immediately reflect the logic state of the hardwired pins (M[9:0], NA[2:0], NB, and P).

Register Read/Write Transfer

Write Mode (R/$\overline{W}$ = 0)

The host controller writes the configuration registers by initiating a write transfer with the MAX3674 slave address (first byte), followed by the address of the configuration register (second byte: 0x00, 0x01, or 0xF0), and the configuration data byte (third byte). This transfer can be followed by writing more registers by sending the configuration register address followed by one data byte. The MAX3674 acknowledges each byte sent by the host controller. The transfer ends by a stop bit sent by the host controller. The number of configuration data bytes and the write sequence are not restricted. Table 10 shows an example of the complete configuration register write transfer.

Read Mode (R/$\overline{W}$ = 1)

The host controller reads the configuration registers by initiating a read transfer. The MAX3674 supports read transfer immediately after the first byte without a change in the transfer direction. Immediately after the host controller sends the slave address, the MAX3674 acknowledges and then sends the configuration registers and identification (PLL_L , PLL_H, and ID) back-to-back to the host controller. The CMD register cannot be read. To read the two configuration registers and the current PLL settings, the user can read PLL_L and PLL_H, write the GET command (loads the current configuration into PLL_L and PLL_H), and read PLL_L and PLL_H again. Table 11 shows the complete register read transfer.

Note that the PLL_L and PLL_H registers and divider settings may not be equivalent after the following example cases:

- Writing the INC command.
- Writing the DEC command.
- Writing the PLL_L, PLL_H registers with a new configuration and not writing the LOAD command.

Table 10. Configuration Register Write Transfer

1 BIT	7 BITS	1 BIT	1 BIT	8 BITS	1 BIT	8 BITS	1 BIT	8 BITS	1 BIT	8 BITS	1 BIT	1 BIT
Start	Slave Address	R/$\overline{W}$	ACK	&PLL_H	ACK	Config-Byte 1	ACK	&PLL_L	ACK	Config-Byte 2	ACK	Stop
—	10110xx	0	—	0x01	—	Data	—	0x00	—	Data	—	—
M	M	M	S	M	S	M	S	M	S	M	S	M

M = master, S = slave.

Table 11. Configuration Register Read Transfer

1 BIT	7 BITS	1 BIT	1 BIT	8 BITS	1 BIT	8 BITS	1 BIT	8 BITS	1 BIT	1 BIT
Start	Slave Address	R/$\overline{W}$	ACK	PLL_L Content	ACK	PLL_H Content	ACK	ID Content	Non-ACK	Stop
—	10110xx	1	—	Data	—	Data	—	Data	—	—
M	M	M	S	S	M	S	M	S	M	M

M = master, S = slave.

Device Startup and Reset

General Device Configuration

It is recommended to apply a master reset signal ($\overline{MR}$ = 0) during or immediately after the system power-up. Upon the release of this master reset signal at the low-to-high transition of the $\overline{MR}$, the MAX3674 automatically acquires a startup configuration from the parallel interface pins (M[9:0], NA[2:0], NB, and P) independent of the $\overline{PLOAD}$ input status. If all parallel interface pins are left open, the MAX3674 loads its internal default values for each divider setting as the startup condition.

The MAX3674 acquires frequency lock within the specified lock time, t_{LOCK}, and is indicated by an assertion of the LOCK signal, which completes the startup procedure. It is recommended to disable the outputs ($\overline{CLK_STOPx}$ = 0) until PLL lock is achieved to suppress output frequency transitions. The output frequency can be reconfigured at any time through either the parallel or the serial interface.

Upon applying a master reset ($\overline{MR}$ = 0), the I²C logic is also reset and restored to a valid state, and all the register contents are set to the default values. Read and write access is not permitted while master reset is asserted ($\overline{MR}$ = 0).

Starting Up Using the Parallel Interface

In this mode, the serial interface pins (SDA, SCL, and ADR[1:0]) can be left open and $\overline{PLOAD}$ is set to logic-low. After release of $\overline{MR}$ and at any other time, the synthesizer configuration is directly set according to the inputs through the M[9:0], NA[2:0], NB, and P pins.

Starting Up Using the Serial (I²C) Interface

In this mode, set $\overline{PLOAD}$ = 1, $\overline{CLK_STOPx}$ = 0 (suppressing output frequency transitions). Upon the rising edge of $\overline{MR}$, the MAX3674 dividers are configured by the default setting of the parallel interface pins independent of the $\overline{PLOAD}$ input status. This initial PLL configuration can be reprogrammed to the final setting at any time through the serial interface. After the PLL achieves lock at the desired VCO frequency, enable the outputs by setting $\overline{CLK_STOPx}$ = 1. PLL lock or relock (after any configuration change through M or P) is indicated by assertion of LOCK output. See Figure 2 for the timing diagram.

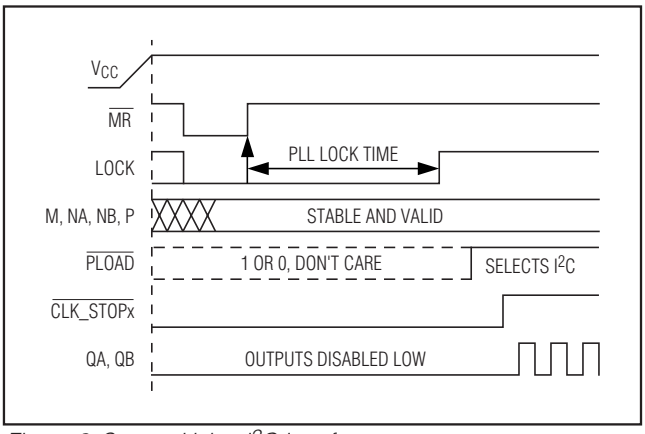


Figure 2. Startup Using I²C Interface

LOCK Detect

The LOCK detect circuitry indicates the frequency lock status of the PLL by setting and resetting the pin LOCK and register bit LOCK simultaneously. Attempts to write the LOCK bit through the serial I²C interface are ignored. The LOCK status is asserted after the PLL acquires frequency lock during any configuration change to the MAX3674, such as the startup, the update of the PLL output frequency, etc. The LOCK status is immediately deasserted when the PLL loses lock; for instance, when the PLL feedback divider M or predivider P is changed, or master reset is asserted. The PLL may not lose lock as a result of slow or small reference frequency changes. LOCK assertion and deassertion is indicated by the LOCK signal after a delay to prevent transient PLL status change during frequency transitions. A valid reference clock is required to update the LOCK register. An interrupted reference clock makes the LOCK output indeterminate. In bypass mode ($\overline{BYPASS}$ = 0), LOCK becomes a production test output.

High-Performance, Dual-Output, Network Clock Synthesizer

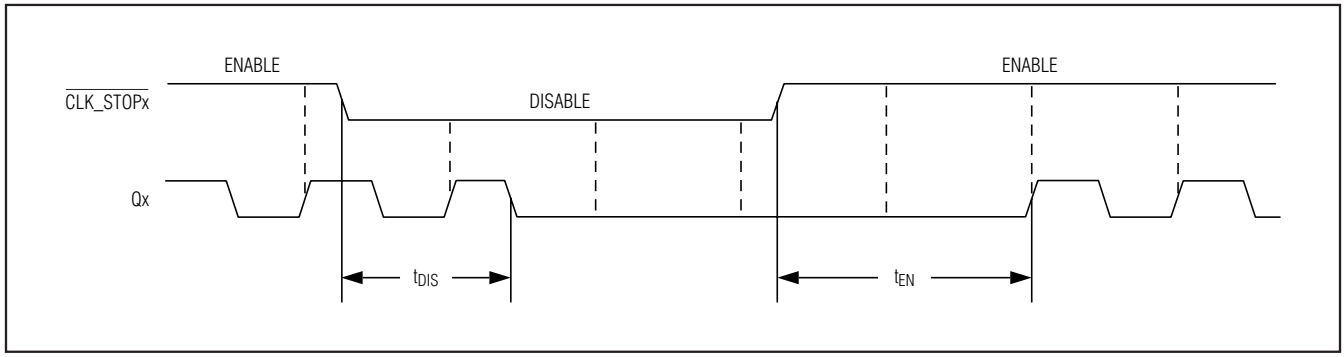


Figure 3. Clock Stop Timing for NB = 1 ($f_{QA} = f_{QB}$)

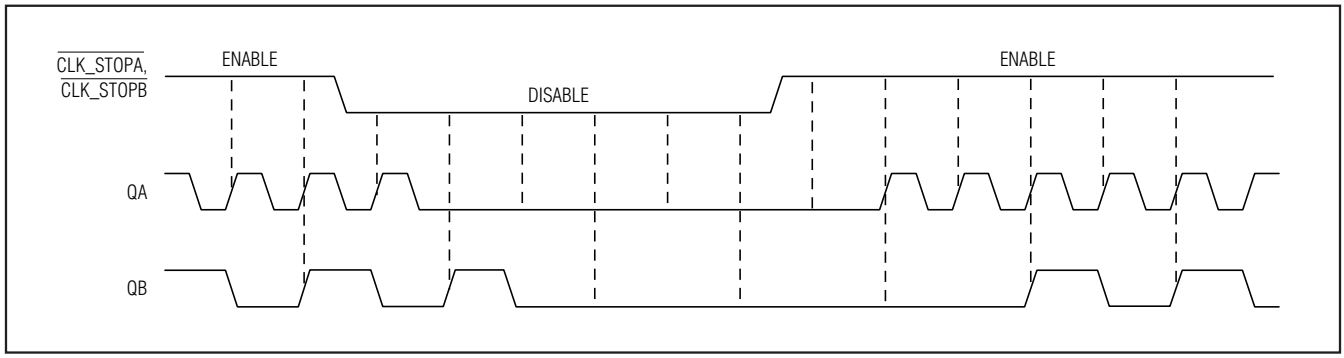


Figure 4. Clock Stop Timing for NB = 2 ($f_{QA} = 2 \times f_{QB}$)

Output Clock Stop

Assertion of $\overline{\text{CLK_STOPx}}$ stops the respective output clock in a logic-low state (Qx = low, $\overline{\text{Qx}}$ = high). The $\overline{\text{CLK_STOPx}}$ control is internally synchronized to the output clock signal, and enabling and disabling outputs does not produce runt pulses. See Figure 3. The clock-stop controls of the QA and QB outputs are independent of each other. If the QB runs at half the QA output frequency and both outputs are enabled at the same time, the first clock pulse of QA may not appear at the same time as the first QB output (Figure 4). Coincident rising edges of QA and QB stay synchronous after the assertion and deassertion of the $\overline{\text{CLK_STOPx}}$ controls. Asserting $\overline{\text{MR}}$ asynchronously forces the output buffer to a logic-low state, with the risk of producing an output runt pulse.

V_{CC_PLL} Filter

The MAX3674 is a mixed-analog/digital IC. The PLL contains analog circuitry susceptible to random noise. To take full advantage of on-board filtering and noise attenuation in addition to excellent on-chip power-supply noise rejection, the MAX3674 provides a separate power-supply pin, V_{CC_PLL}, for the PLL circuitry. The purpose of this design technique is to ensure clean input power supply to the sensitive PLL circuitry and to improve the overall immunity to power-supply noise. Figure 5 illustrates the recommended power-supply filter network.

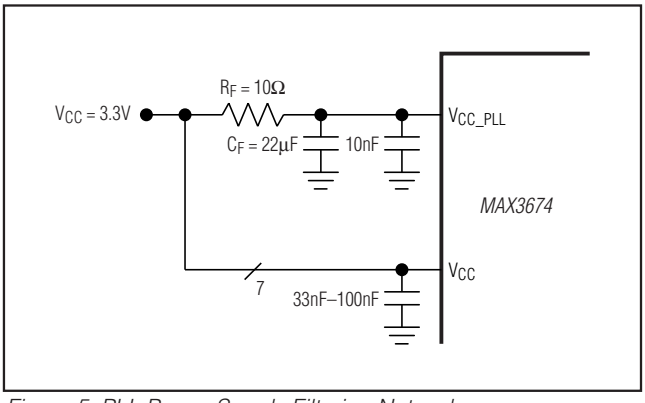


Figure 5. PLL Power-Supply Filtering Network

The minimum values for R_F and C_F should be chosen to achieve greater than 40dB attenuation for noise whose spectral content is above 100kHz, as is the case for the recommended filter. Another important aspect to the filter design is the DC voltage drop between the V_{CC} supply and the V_{CC_PLL} pin. The *DC Electrical Characteristics* table specifies a maximum 10mA PLL supply current (the current sourced into the V_{CC_PLL} pin) with a minimum 3.035V supply voltage at the V_{CC_PLL} pin. The minimum voltage at the V_{CC_PLL} pin is met over the full V_{CC} range (+3.3V ±5%) with $R_F \le 10\Omega$.

The parallel capacitor combination shown in Figure 5 ensures that a low-impedance path to ground exists for a wide band of frequencies, including frequencies well above the PLL bandwidth. For optimal performance, filter capacitors should be placed as close to the supply pins as possible.

Jitter Analysis When NB = 2 ($f_{QA} = 2 \times f_{QB}$)

The high-frequency outputs, QA and QB, are synchronized on the rising edges. Using the postdivider NB, the outputs can be configured such that $f_{QA} = f_{QB}$ with NB = 1, or $f_{QA} = 2 \times f_{QB}$ with NB = 2. See Figure 4 for a timing diagram. In the case where NB = 1, both outputs have corresponding rising and falling edges, and generate cycle-to-cycle and period jitter with normal Gaussian distributions. In the case where NB = 2, rising edges of the two outputs correspond every other QA cycle, causing the cycle-to-cycle and period jitter distributions to be bimodal on the QA output. The QB jitter distribution remains normal Gaussian in both cases (NB = 1 or 2). See the peak-to-peak jitter graphs in the *Typical Operating Characteristics* for comparisons of the two cases.

Interfacing with LVPECL Outputs

Figure 6 shows the equivalent LVPECL output circuit. These outputs are designed to drive a pair of 50Ω transmission lines DC terminated 50Ω to $V_{TT} = V_{CC}$ - 2V. If a separate termination voltage (V_{TT}) is not available, other terminations methods can be used such as shown in Figures 7 and 8. Unused outputs should be disabled and left open. For more information on LVPECL terminations and how to interface with other logic families, refer to Maxim Application Note *HFAN-01.0: Introduction to LVDS, PECL, and CML*.

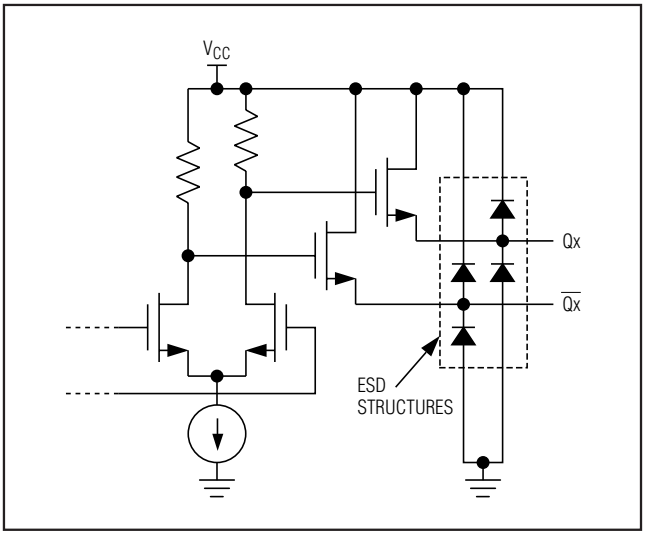


Figure 6. Equivalent PECL Output Circuit

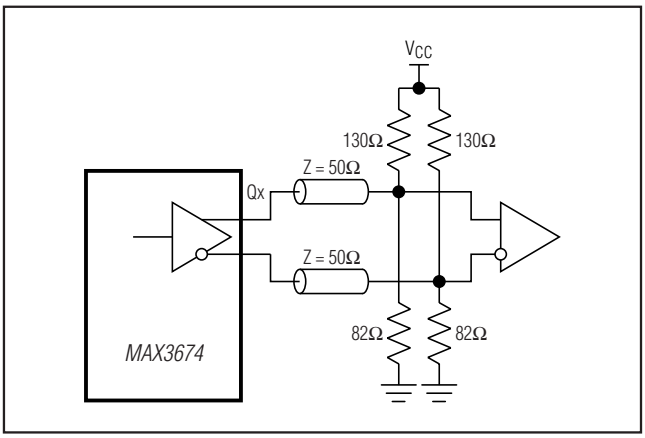


Figure 7. Thevenin Equivalent Termination

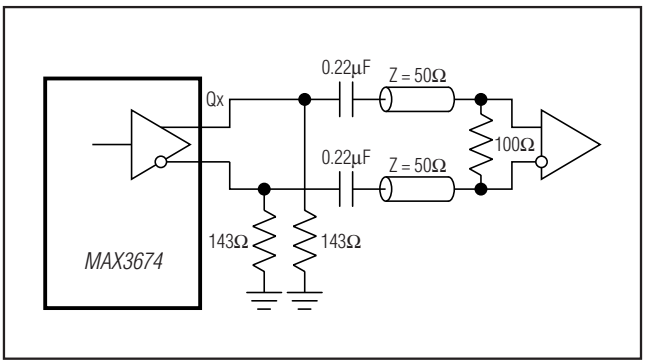


Figure 8. AC-Coupled Termination

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Crystal Oscillator

The MAX3674 features an integrated crystal oscillator to minimize system implementation cost. The integrated oscillator is a Pierce-type that uses the crystal in its parallel resonance mode. It is recommended to use a 15MHz to 20 MHz crystal with a load specification of C_L = 10pF. See Table 12 for the recommended crystal specifications. Crystals with a load specification of C_L = 20pF can be used at the expense of a resulting slightly higher frequency than specified for the crystal. Externally connected capacitors on both the XTAL1 and XTAL2 pins are not required but can be used to fine-tune the crystal frequency as desired.

The crystal, trace, and optional capacitors should be placed on the board as close as possible to the MAX3674 XTAL1 and XTAL2 pins to reduce crosstalk of active signals into the oscillator. Short and wide traces further reduce parasitic inductance and resistance.

Table 12. Recommended Crystal Specifications

PARAMETER	VALUE
Crystal Cut	Fundamental AT cut
Resonance Mode	Parallel
Crystal Frequency	15MHz to 20MHz
Shunt Capacitance, C_0	5pF to 7pF
Load Capacitance, C_L	10pF
Equivalent Series Resistance (ESR), R_S	20Ω to 60Ω
Maximum Crystal Drive Level	≥ 200µW

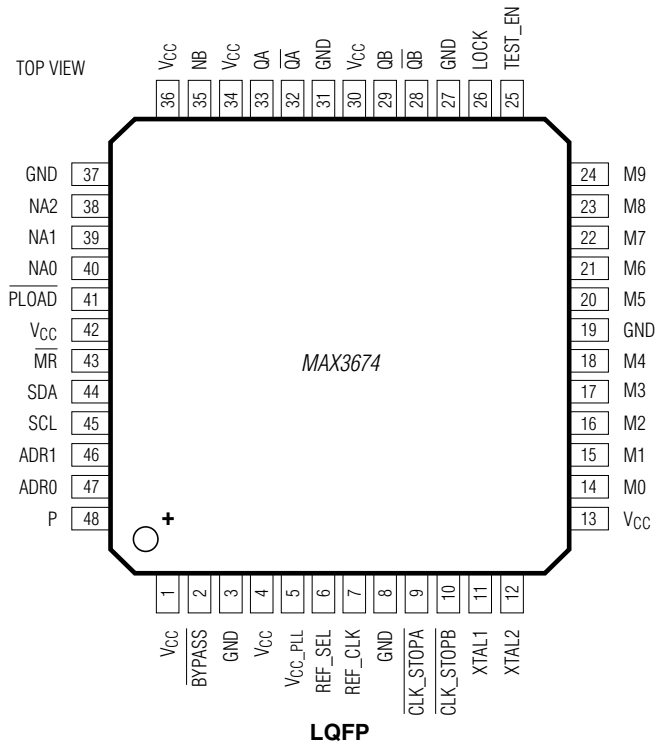
Board Layout

Circuit-board trace layout is very important to maintain the signal integrity of high-frequency differential signals. Maintaining integrity is accomplished in part by reducing signal reflections and skew and increasing common-mode noise immunity.

Signal reflections are caused by discontinuities in the 50Ω characteristic impedance of the traces. Avoid discontinuities by maintaining the distance between differential traces, and not using sharp corners or vias. Ensure the two traces are parallel and close to each other to increase common-mode noise immunity and reduce EMI. Matching the electrical length of the differential traces further reduces signal skew.

High-Performance, Dual-Output, Network Clock Synthesizer

Pin Configuration



LQFP

Chip Information

TRANSISTOR COUNT: 96,136

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **http://www.microsemi.com**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
48 LQFP	—	21-0054



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