CC3120 SimpleLink™ Wi-Fi® Wireless Network Processor, Internet-of-Things Solution for MCU Applications

1 Device Overview

1.1 Features

- CC3120R SimpleLink™ Wi-Fi® Consists of a Wireless Network Processor (NWP) and Power-Management Subsystems
- Featuring Wi-Fi Internet-on-a chip™ Dedicated ARM® Cortex®-M3 Microcontroller Unit (MCU) Completely Offloads Wi-Fi and Internet Protocols from the Application MCU
- Wi-Fi Modes:
  - 802.11b/g/n Station
  - 802.11b/g Access Point (AP) Supports up to Four Stations
  - Wi-Fi Direct® Client/Group Owner
- WPA2 Personal and Enterprise Security: WEP, WPA/WPA2 PSK, WPA2 Enterprise (802.1x)
- IPv4 and IPv6 TCP/IP Stack
  - Industry-Standard BSD Socket Application Programming Interfaces (APIs)
    - 16 Simultaneous TCP or UDP Sockets
    - 6 Simultaneous TLS and SSL Sockets
- IP Addressing: Static IP, LLA, DHCPv4, and DHCPv6 With Duplicate Address Detection (DAD)
- SimpleLink Connection Manager for Autonomous and Fast Wi-Fi Connections
- Flexible Wi-Fi Provisioning With SmartConfig™ Technology, AP Mode, and WPS2 Options
- RESTful API Support Using Internal HTTP Server
- Wide Set of Security Features
  - Hardware Features
    - Separate Execution Environments
    - Device Identity
  - Networking security
    - Personal and Enterprise Wi-Fi Security
    - Secure Sockets (SSLv3, TLS1.0/1.1/TLS1.2)
    - HTTPS Server
    - Trusted Root-Certificate Catalog
    - TI Root-of-Trust Public key
  - Software IP protection
    - Secure Key Storage
    - File System Security
    - Software Tamper Detection
    - Cloning Protection
- Embedded Network Applications Running on the Dedicated NWP
  - HTTP/HTTPS Web Server With Dynamic User Callbacks
  - mDNS, DNS-SD, DHCP Server
  - Ping
- Recovery Mechanism—Can Recover to Factory Defaults or to a Complete Factory Image
- Wi-Fi TX Power
  - 18.0 dBm @ 1 DSSS
  - 14.5 dBm @ 54 OFDM
- Wi-Fi RX Sensitivity
  - –96.0 dBm @ 1 DSSS
  - –74.5 dBm @ 54 OFDM
- Application Throughput
  - UDP: 16 Mbps
  - TCP: 13 Mbps
- Power-Management Subsystem
  - Integrated DC-DC Converters Support a Wide Range of Supply Voltage:
    - VBAT Wide-Voltage Mode: 2.1 V to 3.6 V
    - VIO is Always Tied With VBAT
    - Preregulated 1.85-V Mode
  - Advanced Low-Power Modes
    - Shutdown: 1 µA
    - Hibernate: 4.5 µA
    - Low-Power Deep Sleep (LPDS): 115 µA
    - RX Traffic: 59 mA @ 54 OFDM
    - TX Traffic: 229 mA @ 54 OFDM, Maximum Power
    - Idle Connected (MCU in LPDS): 690 µA @ DTIM = 1
- Clock Source
  - 40.0-MHz Crystal With Internal Oscillator
  - 32.768-kHz Crystal or External RTC
- RGK Package
  - 64-Pin, 9-mm × 9-mm Very Thin Quad Flat Nonleaded (VQFN) Package, 0.5-mm Pitch
- Operating Temperature
  - Ambient Temperature Range: –40°C to +85°C
- Device Supports SimpleLink Developers Ecosystem

1.2 Applications

- For Internet-of-Things (IoT) applications, such as:
  - Cloud Connectivity
  - Internet Gateway
  - Home and Building Automation
  - Appliances
  - Access Control
  - Security Systems
  - Smart Energy
  - Industrial Control
  - Smart Plug and Metering
  - Wireless Audio
  - IP Network Sensor Nodes
  - Asset Tracking
  - Medical Devices

1.3 Description

The CC3120R device is part of the SimpleLink™ microcontroller (MCU) platform which consists of Wi-Fi, *Bluetooth*® low energy, Sub-1 GHz and host MCUs, which all share a common, easy-to-use development environment with a single core software development kit (SDK) and rich tool set. A one-time integration of the SimpleLink platform enables you to add any combination of the portfolio's devices into your design, allowing 100 percent code reuse when your design requirements change. For more information, visit *Overview for SimpleLink™ solutions*.

Connect any microcontroller (MCU) to the Internet of Things (IoT) cloud with the CC3120R device from Texas Instruments™. The Wi-Fi® Alliance CERTIFIED® CC3120R device is part of the second generation of the SimpleLink™ Wi-Fi family that dramatically simplifies the implementation of low-power Internet connectivity.

The CC3120R has all of the Wi-Fi and Internet protocols implemented in the ROM, which runs from the dedicated on-chip ARM® network processor and significantly offloads the host MCU and simplifies the system integration.

The CC3120R Wi-Fi Internet-on-a chip™ device contains a dedicated ARM MCU that offloads many of the networking activities from the host MCU. This subsystem includes an 802.11b/g/n radio, baseband, and MAC with a powerful crypto engine for fast, secure Internet connections with 256-bit encryption. The CC3120R device supports station, AP, and Wi-Fi direct modes. The device also supports WPA2 personal and enterprise security. The device includes embedded TCP/IP and TLS/SSL stacks, an HTTP server, and multiple Internet protocols. The CC3120R device supports a variety of Wi-Fi provisioning methods, including HTTP based on AP mode, SmartConfig™ technology, and WPS2.0.

As part of TI's SimpleLink Wi-Fi family second generation, the CC3120R device introduces the new features and enhanced capabilities, such as the following:

IPv6
Enhanced Wi-Fi provisioning
Enhanced power consumption
Wi-Fi AP connection with up to four stations
More concurrently opened BSD sockets; up to 16 BSD sockets, of which 6 are secure
HTTPS support
RESTful API support
Asymmetric keys crypto library

The CC3120R device is delivered with a slim and user-friendly host driver to simplify the integration and development of networking applications. The host driver can easily be ported to most platforms and operating systems (OS). The driver is written in strict ANSI-C (C89) and requires minimal platform adaptation layer (porting layer). The driver has a small memory footprint and can run on 8-, 16-, or 32-bit microcontrollers with any clock speed (no performance or real-time dependency).

The CC3120R device comes in an easy-to-layout VQFN package and is delivered as a complete platform solution, including various tools and software, sample applications, user and programming guides, reference designs, and the TI E2E™ support community. The CC3120R device is part of the SimpleLink MCU Ecosystem.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
CC3120RNMARGKT/R	VQFN (64)	9.00 mm × 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

1.4 Functional Block Diagrams

Figure 1-1 shows the CC3120R hardware overview.

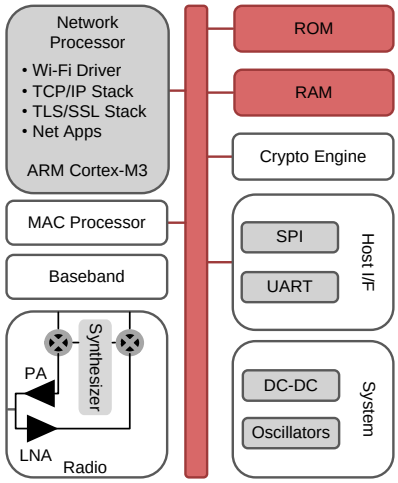

Figure 1-1. CC3120R Hardware Overview

Figure 1-2 shows an overview of the CC3120R embedded software.

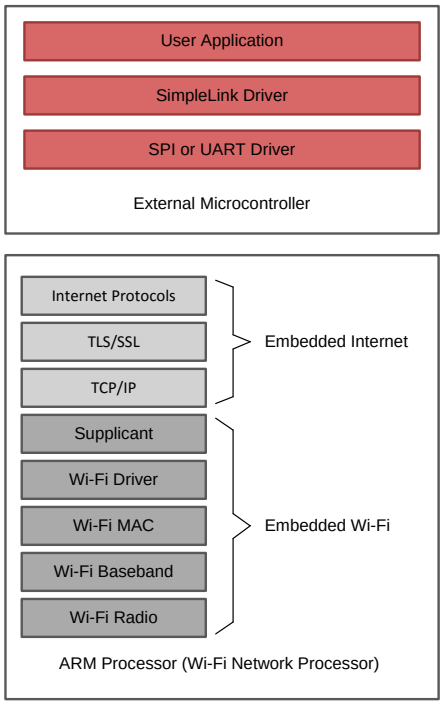

Figure 1-2. CC3120R Software Overview

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2 Revision History

DATE	REVISION	NOTES
February 2017	SWAS034*	Initial Release

3 Terminal Configuration and Functions

3.1 Pin Diagram

Figure 3-1 shows pin assignments for the 64-pin VQFN package.

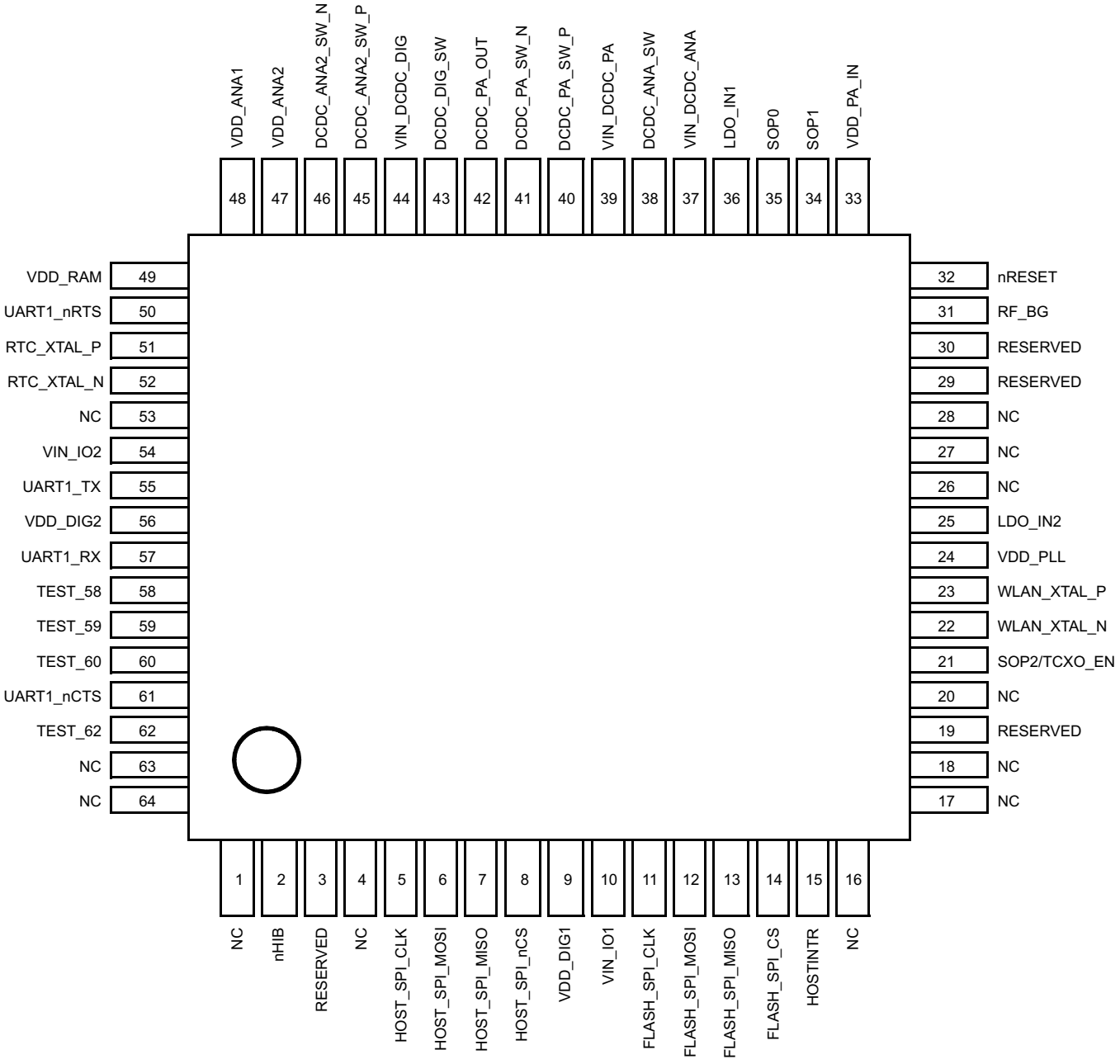


Figure 3-1. VQFN 64-Pin Assignments
Top View

3.2 Pin Attributes

Table 3-1 describes the CC3120R pins.

NOTE

If an external device drives a positive voltage to signal pads when the CC3120R device is not powered, DC current is drawn from the other device. If the drive strength of the external device is adequate, an unintentional wakeup and boot of the CC3120R device can occur. To prevent current draw, TI recommends one of the following:

- All devices interfaced to the CC3120R device must be powered from the same power rail as the CC3120R device.
- Use level shifters between the CC3120R device and any external devices fed from other independent rails.
- The nRESET pin of the CC3120R device must be held low until the VBAT supply to the device is driven and stable.

Table 3-1. Pin Attributes

PIN	DEFAULT FUNCTION	STATE AT RESET AND HIBERNATE	I/O TYPE(1)	DESCRIPTION
2	nHIB	Hi-Z	I	Hibernate signal input to the NWP subsystem (active low). This is connected to the MCU GPIO. If the GPIO from the MCU can float while the MCU enters low power, consider adding a pullup resistor on the board to avoid floating.
3	Reserved	Hi-Z	–	Reserved for future use
5	HOST_SPI_CLK	Hi-Z	I	Host interface SPI clock
6	HOST_SPI_MOSI	Hi-Z	I	Host interface SPI data input
7	HOST_SPI_MISO	Hi-Z	O	Host interface SPI data output
8	HOST_SPI_nCS	Hi-Z	I	Host interface SPI chip select (active low)
9	VDD_DIG1	Hi-Z	Power	Digital core supply (1.2 V)
10	VIN_IO1	Hi-Z	Power	I/O supply
11	FLASH_SPI_CLK	Hi-Z	O	Serial flash interface: SPI clock
12	FLASH_SPI_MOSI	Hi-Z	O	Serial flash interface: SPI data out
13	FLASH _SPI_MISO	Hi-Z	I	Serial flash interface: SPI data in (active high)
14	FLASH _SPI_CS	Hi-Z	O	Serial flash interface: SPI chip select (active low)
15	HOST_INTR	Hi-Z	O	Interrupt output (active high)
19	Reserved	Hi-Z	–	Connect a 100-kΩ pulldown resistor to ground.
21	SOP2/TCXO_EN	Hi-Z	O	Controls restore to default mode. Enable signal for external TCXO. Add a 10-kΩ pulldown resistor to ground.
22	WLAN_XTAL_N	Hi-Z	Analog	Connect the WLAN 40-MHz XTAL here.
23	WLAN_XTAL_P	Hi-Z	Analog	Connect the WLAN 40-MHz XTAL here.
24	VDD_PLL	Hi-Z	Power	Internal PLL power supply (1.4 V nominal)
25	LDO_IN2	Hi-Z	Power	Input to internal LDO
29	Reserved	Hi-Z	O	Reserved for future use
30				
31	RF_BG	Hi-Z	RF	2.4-GHz RF TX, RX
32	nRESET	Hi-Z	I	RESET input for the device. Active low input. Use RC circuit (100 k || 0.1 µF) for power on reset (POR).

(1) I = Input
O = Output RF = radio frequency
I/O = bidirectional

Table 3-1. Pin Attributes (continued)

PIN	DEFAULT FUNCTION	STATE AT RESET AND HIBERNATE	I/O TYPE[1]	DESCRIPTION
33	VDD_PA_IN	Hi-Z	Power	Power supply for the RF power amplifier (PA)
34	SOP1	Hi-Z	–	Controls restore to default mode. Add 100-kΩ pulldown to ground. Factory default function.
35	SOP0	Hi-Z	–	Controls restore to default mode. Add 100-kΩ pulldown to ground. Factory default function.
36	LDO_IN1	Hi-Z	Power	Input to internal LDO
37	VIN_DCDC_ANA	Hi-Z	Power	Power supply for the DC-DC converter for analog section
38	DCDC_ANA_SW	Hi-Z	Power	Analog DC-DC converter switch output
39	VIN_DCDC_PA	Hi-Z	Power	PA DC-DC converter input supply
40	DCDC_PA_SW_P	Hi-Z	Power	PA DC-DC converter switch output +ve
41	DCDC_PA_SW_N	Hi-Z	Power	PA DC-DC converter switch output –ve
42	DCDC_PA_OUT	Hi-Z	Power	PA DC-DC converter output. Connect the output capacitor for DC-DC here.
43	DCDC_DIG_SW	Hi-Z	Power	Digital DC-DC converter switch output
44	VIN_DCDC_DIG	Hi-Z	Power	Power supply input for the digital DC-DC converter
45	DCDC_ANA2_SW_P	Hi-Z	Power	Analog2 DC-DC converter switch output +ve
46	DCDC_ANA2_SW_N	Hi-Z	Power	Analog2 DC-DC converter switch output –ve
47	VDD_ANA2	Hi-Z	Power	Analog2 power supply input
48	VDD_ANA1	Hi-Z	Power	Analog1 power supply input
49	VDD_RAM	Hi-Z	Power	Power supply for the internal RAM
50	UART1_nRTS	Hi-Z	O	UART host interface (active low)
51	RTC_XTAL_P	Hi-Z	Analog	32.768-kHz XTAL_P or external CMOS level clock input
52	RTC_XTAL_N	Hi-Z	Analog	32.768-kHz XTAL_N or 100-kΩ external pullup for external clock
54	VIN_IO2	Hi-Z	Power	I/O power supply. Same as battery voltage.
55	UART1_TX	Hi-Z	O	UART host interface. Connect to test point on prototype for flash programming.
56	VDD_DIG2	Hi-Z	Power	Digital power supply (1.2 V)
57	UART1_RX	Hi-Z	I	UART host interface; connect to test point on prototype for flash programming.
58	TEST_58		–	Test signal; connect to an external test point.
59	TEST_59		–	Test signal; connect to an external test point.
60	TEST_60	Hi-Z	O	Test signal; connect to an external test point.
61	UART1_nCTS	Hi-Z	I	UART host interface (active low)
62	TEST_62	Hi-Z	O	Test signal; connect to an external test point.
65	GND		Power	Ground tab used as thermal and electrical ground

3.3 Connections for Unused Pins

All unused pins must be left as no connect (NC) pins. Table 3-2 provides a list of NC pins.

Table 3-2. Connections for Unused Pins

PIN	DEFAULT FUNCTION	STATE AT RESET AND HIBERNATE	I/O TYPE(1)	DESCRIPTION
1	NC	WLAN analog	–	Unused; leave unconnected.
4	NC	WLAN analog	–	Unused; leave unconnected.
16	NC	WLAN analog	–	Unused; leave unconnected.
17	NC	WLAN analog	–	Unused; leave unconnected.
18	NC	WLAN analog	–	Unused; leave unconnected.
20	NC	WLAN analog	–	Unused; leave unconnected.
26	NC	WLAN analog	–	Unused; leave unconnected.
27	NC	WLAN analog	–	Unused; leave unconnected.
28	NC	WLAN analog	–	Unused; leave unconnected.
26	NC	WLAN analog	–	Unused; leave unconnected.
27	NC	WLAN analog	–	Unused; leave unconnected.
28	NC	WLAN analog	–	Unused; leave unconnected.
53	NC	WLAN analog	–	Unused; leave unconnected.
63	NC	WLAN analog	–	Unused; leave unconnected.
64	NC	WLAN analog	–	Unused; leave unconnected.

(1) I = Input
O = Output RF = radio frequency
I/O = bidirectional

4 Specifications

All measurements are referenced at the device pins, unless otherwise indicated. All specifications are over process and voltage, unless otherwise indicated.

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VBAT and VIO	Pins: 37, 39, 44	–0.5	3.8	V
VIO – VBAT (differential)	Pins: 10, 54		0.0	V
Digital inputs		–0.5	V_{IO} + 0.5	V
RF pins		–0.5	2.1	V
Analog pins, XTAL	Pins: 22, 23, 51, 52	–0.5	2.1	V
Operating temperature, T_A		–40	85	°C
Storage temperature, T_{stg}		–55	125	°C

4.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Power-On Hours

NOTE

This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

CONDITIONS	POH
T_A up to 85°C(1)	87,600

(1) The TX duty cycle (power amplifier ON time) is assumed to be 10% of the device POH. Of the remaining 90% of the time, the device can be in any other state.

4.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	TYP	MAX	UNIT
VBAT, VIO (shorted to VBAT)	Pins: 10, 37, 39, 44, 54	Direct battery connection(3)	2.1(4)	3.3	3.6	V
		Preregulated 1.85 V(5)(6)				
Ambient thermal slew			–20		20	°C/minute

(1) Operating temperature is limited by crystal frequency variation.
(2) When operating at an ambient temperature of over 75°C, the transmit duty cycle must remain below 50% to avoid the auto-protect feature of the power amplifier. If the auto-protect feature triggers, the device takes a maximum of 60 seconds to restart the transmission.
(3) To ensure WLAN performance, ripple on the 2.1- to 3.3-V supply must be less than ±300 mV.
(4) The minimum voltage specified includes the ripple on the supply voltage and all other transient dips. The brownout condition is also 2.1 V, and care must be taken when operating at the minimum specified voltage.
(5) To ensure WLAN performance, ripple on the 1.85-V supply must be less than 2% (±40 mV).
(6) TI recommends keeping VBAT above 1.85 V. For lower voltages, use a boost converter.

4.5 Current Consumption Summary

T_A = 25°C, V_{BAT} = 3.6 V

PARAMETER	TEST CONDITIONS (1) (2)		MIN	TYP	MAX	UNIT
TX	1 DSSS	TX power level = 0		272		mA
		TX power level = 4		188		
	6 OFDM	TX power level = 0		248		
		TX power level = 4		179		
	54 OFDM	TX power level = 0		223		
		TX power level = 4		160		
RX (3)	1 DSSS			53		mA
	54 OFDM			53		
Idle connected (4)				690		µA
LPDS				115		
Hibernate (5)				4		
Peak calibration current (6) (3)	VBAT = 3.3 V			450		mA
	VBAT = 2.1 V			670		
	VBAT = 1.85 V			700		

(1) TX power level = 0 implies maximum power (see Figure 4-1, Figure 4-2, and Figure 4-3). TX power level = 4 implies output power backed off approximately 4 dB.
(2) The CC3120R system is a constant power-source system. The active current numbers scale based on the VBAT voltage supplied.
(3) The RX current is measured with a 1-Mbps throughput rate.
(4) DTIM = 1
(5) For the 1.85-V mode, the hibernate current is higher by 50 µA across all operating modes because of leakage into the PA and analog power inputs.
(6) The complete calibration can take up to 17 mJ of energy from the battery over a time of 24 ms. In default mode, calibration is performed sparingly, and typically occurs when re-enabling the NWP and when the temperature has changed by more than 20°C. There are two additional calibration modes that may be used to reduced or completely eliminate the calibration event. For further details, see *CC3120, CC3220 SimpleLink™ Wi-Fi® and IoT Network Processor Programmer's Guide*.

4.6 TX Power and IBAT versus TX Power Level Settings

Figure 4-1, Figure 4-2, and Figure 4-3 show TX Power and IBAT versus TX power level settings for modulations of 1 DSSS, 6 OFDM, and 54 OFDM, respectively.

In Figure 4-1, the area enclosed in the circle represents a significant reduction in current during transition from TX power level 3 to level 4. In the case of lower range requirements (14-dBm output power), TI recommends using TX power level 4 to reduce the current.

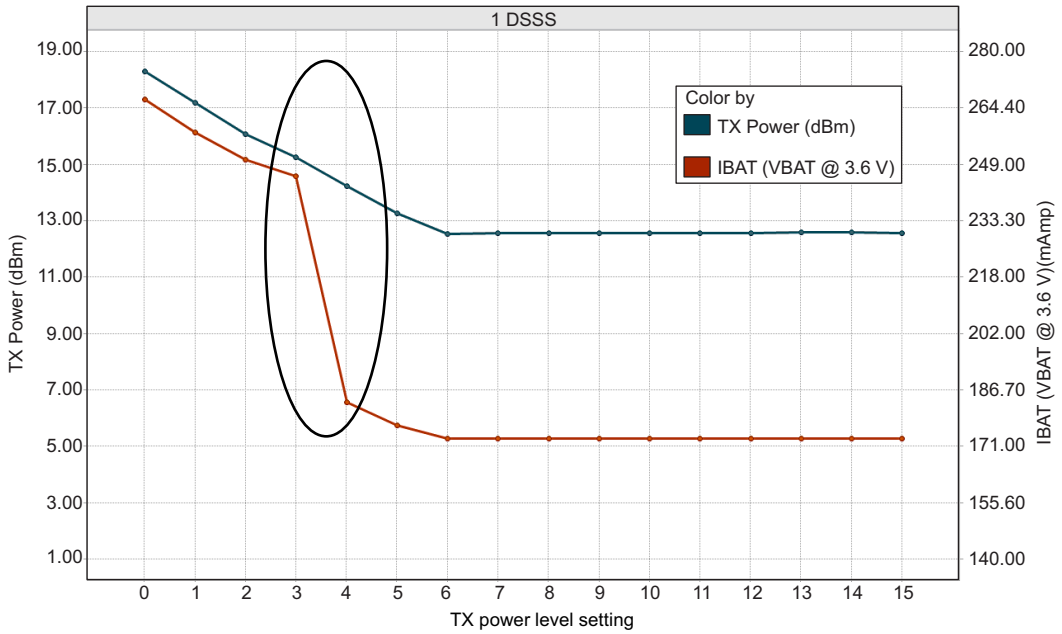


Figure 4-1. TX Power and IBAT vs TX Power Level Settings (1 DSSS)

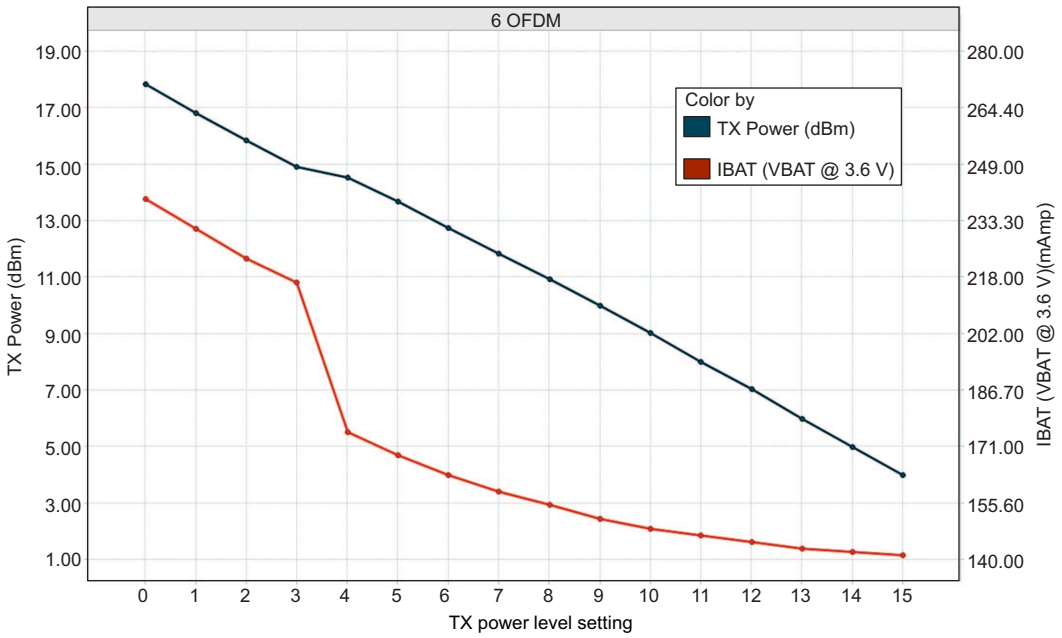


Figure 4-2. TX Power and IBAT vs TX Power Level Settings (6 OFDM)

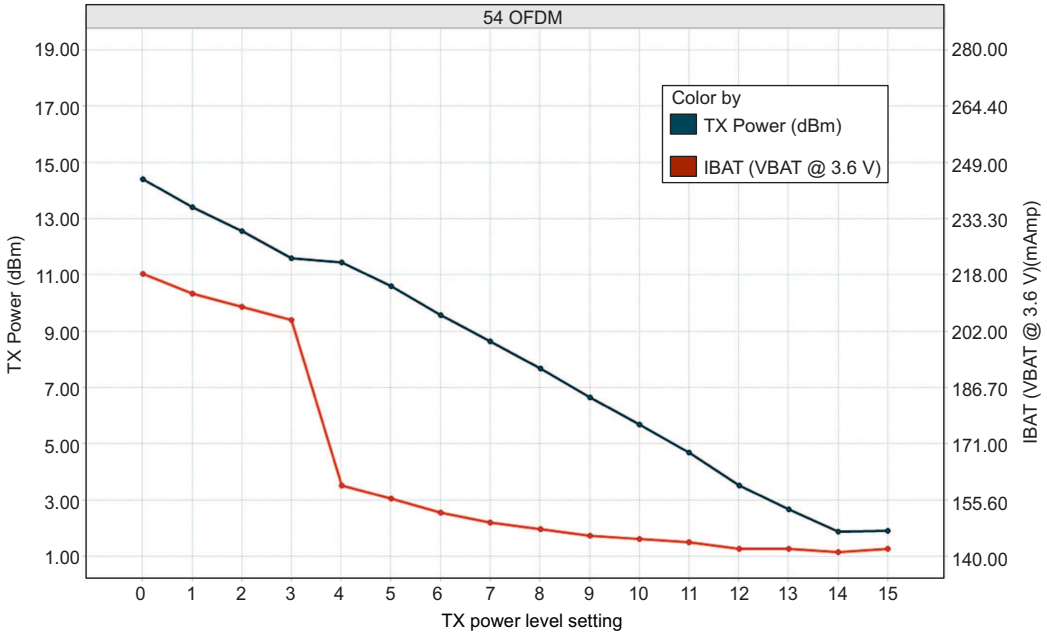


Figure 4-3. TX Power and IBAT vs TX Power Level Settings (54 OFDM)

4.7 Brownout and Blackout Conditions

The device enters a brownout condition when the input voltage drops below $V_{brownout}$ (see Figure 4-4 and Figure 4-5). This condition must be considered during design of the power supply routing, especially when operating from a battery. High-current operations, such as a TX packet or any external activity (not necessarily related directly to networking) can cause a drop in the supply voltage, potentially triggering a brownout condition. The resistance includes the internal resistance of the battery, the contact resistance of the battery holder (four contacts for 2× AA batteries), and the wiring and PCB routing resistance.

NOTE

When the device is in HIBERNATE state, brownout is not detected. Only blackout is in effect during HIBERNATE state.

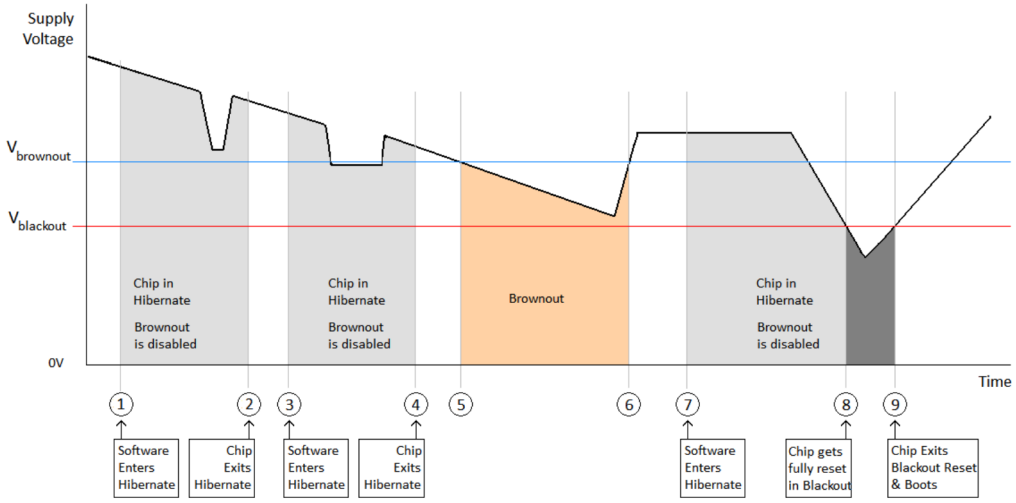


Figure 4-4. Brownout and Blackout Levels (1 of 2)

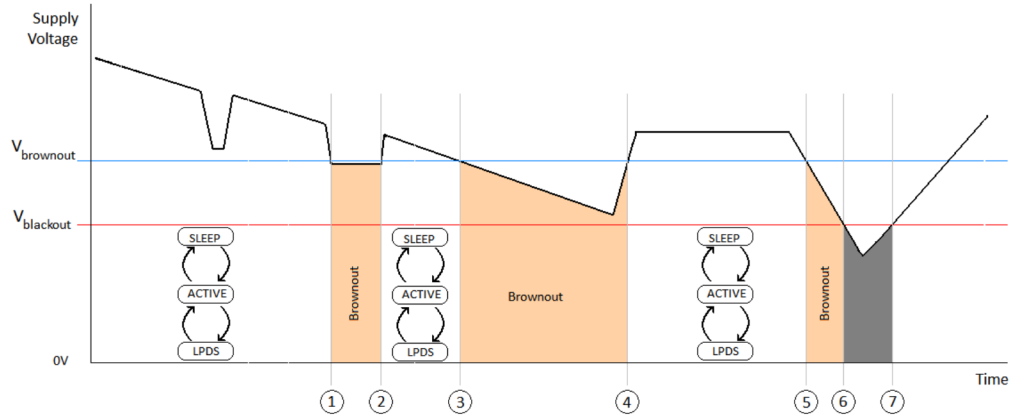


Figure 4-5. Brownout and Blackout Levels (2 of 2)

In the brownout condition, all sections of the device (including the 32-kHz RTC) shut down except for the Hibernate module, which remains on. The current in this state can reach approximately 400 µA. The blackout condition is equivalent to a hardware reset event in which all states within the device are lost.

Table 4-1 lists the brownout and blackout voltage levels.

Table 4-1. Brownout and Blackout Voltage Levels

CONDITION	VOLTAGE LEVEL	UNIT
$V_{brownout}$	2.1	V
$V_{blackout}$	1.67	V

4.8 Electrical Characteristics (3.3 V, 25°C)

GPIO Pins Except 29, 30, 50, 52, and 53 (25°C)							
PARAMETER			TEST CONDITIONS	MIN	NOM	MAX	UNIT
C_{IN}	Pin capacitance				4		pF
V_{IH}	High-level input voltage			0.65 × V_{DD}		V_{DD} + 0.5 V	V
V_{IL}	Low-level input voltage			–0.5		0.35 × V_{DD}	V
I_{IH}	High-level input current				5		nA
I_{IL}	Low-level input current				5		nA
V_{OH}	High-level output voltage		IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ≤ V_{DD} < 3.6 V			V_{DD} × 0.8	V
			IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ≤ V_{DD} < 3.6 V			V_{DD} × 0.7	
			IL = 8 mA; configured I/O drive strength = 8 mA; 2.4 V ≤ V_{DD} < 3.6 V			V_{DD} × 0.7	
			IL = 2 mA; configured I/O drive strength = 2 mA; 2.1 V ≤ V_{DD} < 2.4 V			V_{DD} × 0.75	
			IL = 2 mA; configured I/O drive strength = 2 mA; V_{DD} = 1.85 V			V_{DD} × 0.7	
V_{OL}	Low-level output voltage		IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ≤ V_{DD} < 3.6 V	V_{DD} × 0.2			V
			IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ≤ V_{DD} < 3.6 V	V_{DD} × 0.2			
			IL = 8 mA; configured I/O drive strength = 8 mA; 2.4 V ≤ V_{DD} < 3.6 V	V_{DD} × 0.2			
			IL = 2 mA; configured I/O drive strength = 2 mA; 2.1 V ≤ V_{DD} < 2.4 V	V_{DD} × 0.25			
			IL = 2 mA; configured I/O drive strength = 2 mA; V_{DD} = 1.85 V	V_{DD} × 0.35			
I_{OH}	High-level source current,	2-mA drive		2			mA
		4-mA drive		4			
		6-mA drive		6			
I_{OL}	Low-level sink current,	2-mA drive		2			mA
		4-mA drive		4			
		6-mA drive		6			
V_{IL}	nRESET(1)				0.6		V

(1) The nRESET pin must be held below 0.6 V for the device to register a reset.

4.9 WLAN Receiver Characteristics

T_A = 25°C, VBAT = 2.1 V to 3.6 V. Parameters are measured at the SoC pin on channel 6 (2437 MHz).

PARAMETER	TEST CONDITIONS (Mbps)	MIN	TYP(1)	MAX	UNIT
Sensitivity (8% PER for 11b rates, 10% PER for 11g/11n rates) (10% PER)(2)	1 DSSS		–96.0		dBm
	2 DSSS		–94.0		
	11 CCK		–88.0		
	6 OFDM		–90.5		
	9 OFDM		–90.0		
	18 OFDM		–86.5		
	36 OFDM		–80.5		
	54 OFDM		–74.5		
	MCS7 (GF)(3)		–71.5		
	MCS7 (MM)(3)		–70.5		
Maximum input level (10% PER)	802.11b		–4.0		dBm
	802.11g		–10.0		

(1) In preregulated 1.85-V mode, RX sensitivity is 0.25- to 1-dB lower.
(2) Sensitivity is 1-dB worse on channel 13 (2472 MHz).
(3) Sensitivity for mixed mode is 1-dB worse.

4.10 WLAN Transmitter Characteristics

T_A = 25°C, V_{BAT} = 2.1 V to 3.6 V. Parameters measured at SoC pin on channel 7 (2442 MHz).(1)

PARAMETER	TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT
Maximum RMS output power measured at 1 dB from IEEE spectral mask or EVM	1 DSSS		+18.0		dBm
	2 DSSS		+18.0		
	11 CCK		+18.3		
	6 OFDM		+17.3		
	9 OFDM		+17.3		
	18 OFDM		+17.0		
	36 OFDM		+16.0		
	54 OFDM		+14.5		
	MCS7 (MM)		+13.0		
Transmit center frequency accuracy		–25		25	ppm

(1) Channel-to-channel variation is up to 2 dB. The edge channels (2412 and 2472 MHz) have reduced TX power to meet FCC emission limits.
(2) In preregulated 1.85-V mode, maximum TX power is 0.25- to 0.75-dB lower for modulations higher than 18 OFDM.

4.11 WLAN Filter Requirements

The device requires an external band-pass filter to meet the various emission standards, including FCC. Table 4-2 presents the attenuation requirements for the band-pass filter. TI recommends using the same filter used in the reference design to ease the process of certification.

Table 4-2. WLAN Filter Requirements

PARAMETER	FREQUENCY (MHz)	MIN	TYP	MAX	UNIT
Return loss	2412 to 2484	10			dB
Insertion loss(1)	2412 to 2484		1	1.5	dB
Attenuation	800 to 830	30	45		dB
	1600 to 1670	20	25		
	3200 to 3300	30	48		
	4000 to 4150	45	50		
	4800 to 5000	20	25		
	5600 to 5800	20	25		
	6400 to 6600	20	35		
	7200 to 7500	35	45		
	7500 to 10000	20	25		
Reference impendence	2412 to 2484		50		Ω
Filter type	Bandpass				

(1) Insertion loss directly impacts output power and sensitivity. At customer discretion, insertion loss can be relaxed to meet attenuation requirements.

4.12 Thermal Resistance Characteristics for RGK Package

AIR FLOW				
PARAMETER	0 lfm (C/W)	150 lfm (C/W)	250 lfm (C/W)	500 lfm (C/W)
θ_{ja}	23	14.6	12.4	10.8
Ψ_{jt}	0.2	0.2	0.3	0.1
Ψ_{jb}	2.3	2.3	2.2	2.4
θ_{jc}	6.3			
θ_{jb}	2.4			

4.13 Timing and Switching Characteristics

4.13.1 Power Supply Sequencing

For proper operation of the CC3120R device, perform the recommended power-up sequencing as follows:

1. Tie VBAT (pins 37, 39, 44) and VIO (pins 54 and 10) together on the board.
2. Hold the RESET pin low while the supplies are ramping up. TI recommends using a simple RC circuit (100 K ||, 1 µF, RC = 100 ms).
3. For an external RTC, ensure that the clock is stable before RESET is deasserted (high).

For timing diagrams, see Section 4.13.3.

4.13.2 Device Reset

When a device restart is required, the user may either issue a negative pulse on the nHIB pin (pin 2) or on the nRESET pin (pin 32), keeping the other pulled high, depending on the configuration of the platform. In case the nRESET pin is used, the user must follow one of the two alternatives to ensure the reset is properly applied:

- A high-to-low reset pulse (on pin 32) of at least 200-mS duration
- If the above cannot be ensured, a pulldown resistor of 2M Ω should be connected to pin 32 (RTC_XTAL_N). If implemented, a shorter pulse of at least 100 uSec can be used.

To ensure a proper reset sequence, the user has to call the sl_stop function prior to toggling the reset.

4.13.3 Reset Timing

4.13.3.1 nRESET (32k XTAL)

Figure 4-6 shows the reset timing diagram for the 32k XTAL first-time power-up and reset removal.

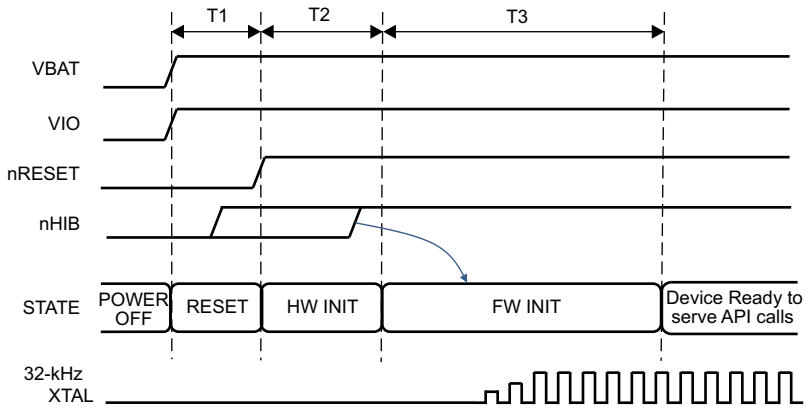


Figure 4-6. First-Time Power-Up and Reset Removal Timing Diagram (32k XTAL)

Table 4-3 describes the timing requirements for the XTAL first-time power-up and reset removal.

Table 4-3. First-Time Power-Up and Reset Removal Timing Requirements (32k XTAL)

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
T1	Supply settling time	Depends on application board power supply, decoupling capacitor, and so on		3		ms
T2	Hardware wake-up time			25		ms
T3	Initialization time	32-kHz XTAL settling plus firmware initialization time plus radio calibration		1.35		s

4.13.3.2 nRESET (External 32K)

Figure 4-7 shows the reset timing diagram for the external 32K first-time power-up and reset removal.

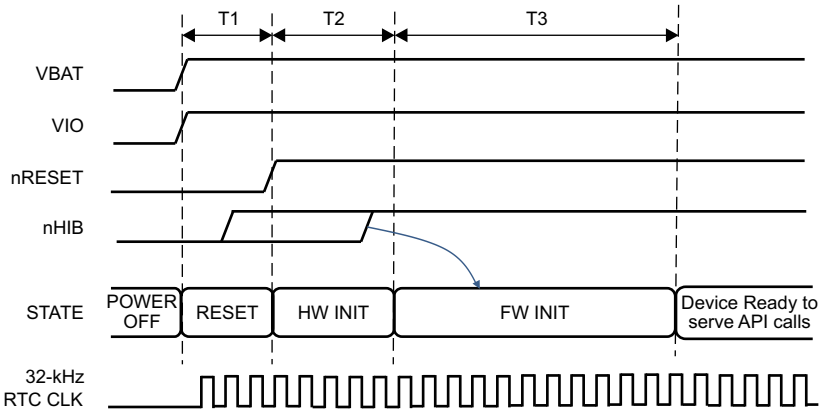


Figure 4-7. First-Time Power-Up and Reset Removal Timing Diagram (External 32K)

describes the timing requirements for the external first-time power-up and reset removal.

Table 4-4. First-Time Power-Up and Reset Removal Timing Requirements (External 32K)

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
T1	Supply settling time	Depends on application board power supply, decoupling capacitor, and so on		3		ms
T2	Hardware wake-up time			25		ms
T3	Initialization time	Firmware initialization time plus radio calibration		250		ms

4.13.3.3 Wakeup From HIBERNATE Mode

Figure 4-8 shows the timing diagram for wakeup from HIBERNATE mode.

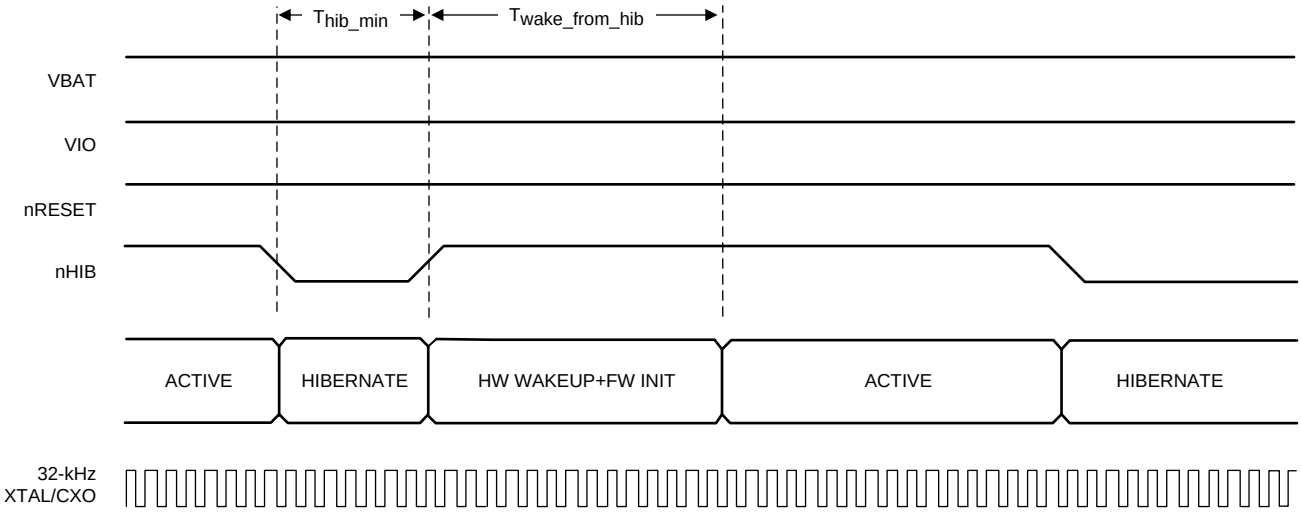


Figure 4-8. nHIB Timing Diagram

NOTE

The 32.768-kHz XTAL is kept enabled by default when the chip goes into HIBERNATE mode in response to nHIB being pulled low.

Table 4-5 describes the timing requirements for nHIB.

Table 4-5. nHIB Timing Requirements

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{hib_min}	Minimum hibernate time	Minimum pulse width of nHIB being low(1)	10			ms
$T_{wake\_from\_hib}$	Hardware wakeup time plus firmware initialization time	See(2)		50		ms

(1) Ensure that the nHIB pulse width is kept above the minimum requirement under all conditions (such as power up, MCU reset, and so on).
(2) If temperature changes by more than 20°C, initialization time from HIB can increase by 200 ms due to radio calibration.

4.13.4 Clock Specifications

The CC3120R device requires two separate clocks for its operation:

- A slow clock running at 32.768 kHz is used for the RTC.
- A fast clock running at 40 MHz is used by the device for the internal processor and the WLAN subsystem.

The device features internal oscillators that enable the use of less-expensive crystals rather than dedicated TCXOs for these clocks. The RTC can also be fed externally to provide reuse of an existing clock on the system and to reduce overall cost.

4.13.4.1 Slow Clock Using Internal Oscillator

The RTC crystal connected on the device supplies the free-running slow clock. The accuracy of the slow clock frequency must be 32.768 kHz ±150 ppm. In this mode of operation, the crystal is tied between RTC_XTAL_P (pin 51) and RTC_XTAL_N (pin 52) with a suitable load capacitance to meet the ppm requirement.

Figure 4-9 shows the crystal connections for the slow clock.

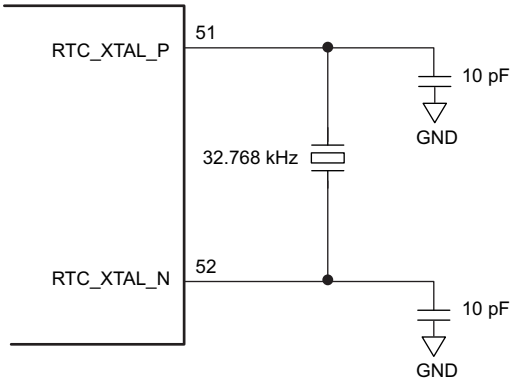


Figure 4-9. RTC Crystal Connections

Table 4-6 lists the RTC crystal requirements.

Table 4-6. RTC Crystal Requirements

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			32.768		kHz
Frequency accuracy	Initial plus temperature plus aging			±150	ppm
Crystal ESR	32.768 kHz			70	kΩ

4.13.4.2 Slow Clock Using an External Clock

When an RTC oscillator is present in the system, the CC3120R device can accept this clock directly as an input. The clock is fed on the RTC_XTAL_P line, and the RTC_XTAL_N line is held to VIO. The clock must be a CMOS-level clock compatible with VIO fed to the device.

Figure 4-10 shows the external RTC input connection.

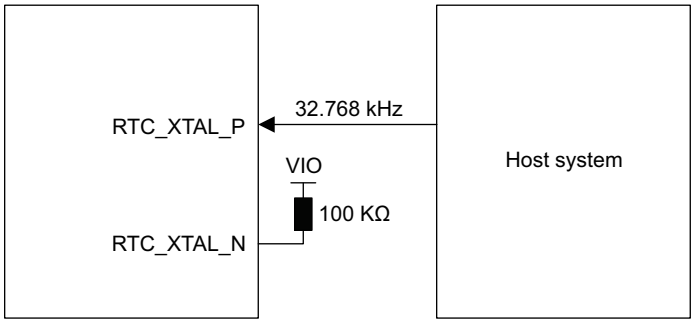


Figure 4-10. External RTC Input

Table 4-7 lists the external RTC digital clock requirements.

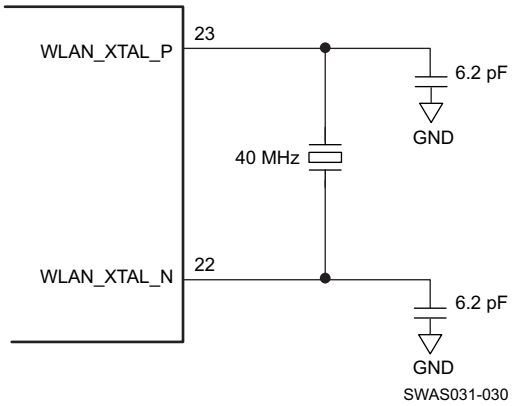
Table 4-7. External RTC Digital Clock Requirements

CHARACTERISTICS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Frequency			32768		Hz
	Frequency accuracy (Initial plus temperature plus aging)			±150		ppm
t_r, t_f	Input transition time t_r, t_f (10% to 90%)				100	ns
	Frequency input duty cycle		20%	50%	80%	
V_{ih}	Slow clock input voltage limits	Square wave, DC coupled	0.65 × VIO		VIO	V
V_{il}			0		0.35 × VIO	V_{peak}
	Input impedance		1			MΩ
					5	pF

4.13.4.3 Fast Clock (F_{ref}) Using an External Crystal

The CC3120R device also incorporates an internal crystal oscillator to support a crystal-based fast clock. The XTAL is fed directly between WLAN_XTAL_P (pin 23) and WLAN_XTAL_N (pin 22) with suitable loading capacitors.

Figure 4-11 shows the crystal connections for the fast clock.



NOTE: The XTAL capacitance must be tuned to ensure that the PPM requirement is met. See *CC31xx & CC32xx Frequency Tuning* for information on frequency tuning.

Figure 4-11. Fast Clock Crystal Connections

Table 4-8 lists the WLAN fast-clock crystal requirements.

Table 4-8. WLAN Fast-Clock Crystal Requirements

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			40		MHz
Frequency accuracy	Initial plus temperature plus aging			±25	ppm
Crystal ESR	40 MHz			60	Ω

4.13.4.4 Fast Clock (F_{ref}) Using an External Oscillator

The CC3120R device can accept an external TCXO/XO for the 40-MHz clock. In this mode of operation, the clock is connected to WLAN_XTAL_P (pin 23). WLAN_XTAL_N (pin 22) is connected to GND. The external TCXO/XO can be enabled by TCXO_EN (pin 21) from the device to optimize the power consumption of the system.

If the TCXO does not have an enable input, an external LDO with an enable function can be used. Using the LDO improves noise on the TCXO power supply.

Figure 4-12 shows the connection.

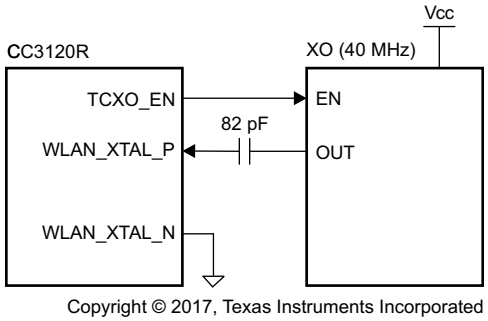


Figure 4-12. External TCXO Input

Table 4-9 lists the external F_{ref} clock requirements.

Table 4-9. External F_{ref} Clock Requirements (–40°C to +85°C)

CHARACTERISTICS			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Frequency				40.00		MHz
	Frequency accuracy (Initial plus temperature plus aging)					±25	ppm
	Frequency input duty cycle			45%	50%	55%	
V_{pp}	Clock voltage limits		Sine or clipped sine wave, AC coupled	0.7		1.2	V_{pp}
	Phase noise @ 40 MHz		@ 1 kHz			–125	dBc/Hz
			@ 10 kHz			–138.5	
			@ 100 kHz			–143	
	Input impedance	Resistance		12			kΩ
		Capacitance				7	pF

4.13.5 Interfaces

This section describes the interfaces that are supported by the CC3120R device:

- Host SPI
- Flash SPI

4.13.5.1 Host SPI Interface Timing

Figure 4-13 shows the Host SPI interface timing diagram.

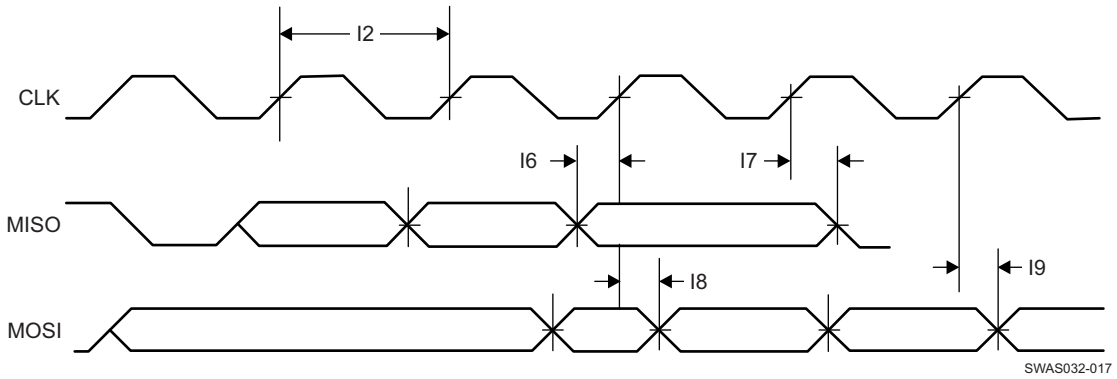


Figure 4-13. Host SPI Interface Timing

Table 4-10 lists the Host SPI interface timing parameters.

Table 4-10. Host SPI Interface Timing Parameters

PARAMETER NUMBER			MIN	MAX	UNIT
I1	F(1)	Clock frequency @ V_{BAT} = 3.3 V		20	MHz
		Clock frequency @ V_{BAT} ≤ 2.1 V		12	
I2	t_{clk}(2)(1)	Clock period	50		ns
I3	t_{LP}(1)	Clock low period		25	ns
I4	t_{HT}(1)	Clock high period		25	ns
I5	D(1)	Duty cycle	45%	55%	
I6	t_{IS}(1)	RX data setup time	4		ns
I7	t_{IH}(1)	RX data hold time	4		ns
I8	t_{OD}(1)	TX data output delay		20	ns
I9	t_{OH}(1)	TX data hold time		24	ns

(1) The timing parameter has a maximum load of 20 pF at 3.3 V.
(2) Ensure that nCS (active-low signal) is asserted 10 ns before the clock is toggled. nCS can be deasserted 10 ns after the clock edge.

4.13.5.2 Flash SPI Interface Timing

Figure 4-14 shows the Flash SPI interface timing diagram.

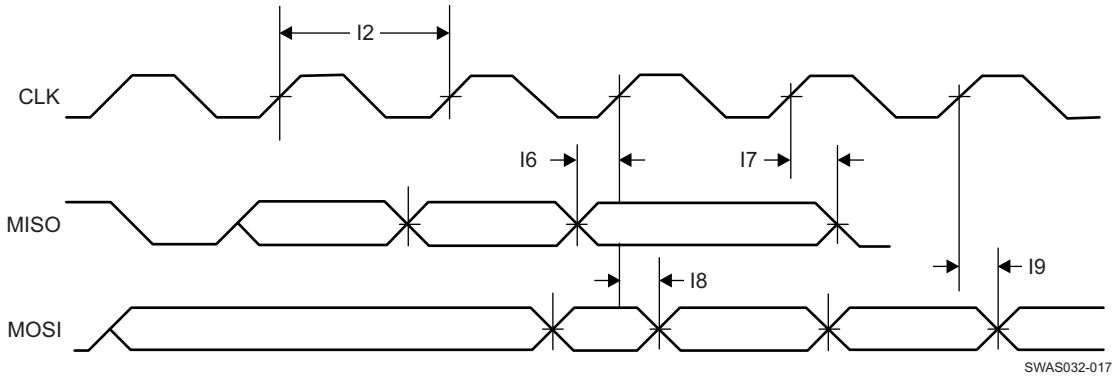


Figure 4-14. Flash SPI Interface Timing

Table 4-11 lists the Flash SPI interface timing parameters.

Table 4-11. Flash SPI Interface Timing Parameters

PARAMETER NUMBER			MIN	MAX	UNIT
I1	F	Clock frequency		20	MHz
I2	t_{clk}	Clock period	50		ns
I3	t_{LP}	Clock low period		25	ns
I4	t_{HT}	Clock high period		25	ns
I5	D	Duty cycle	45%	55%	
I6	t_{IS}	RX data setup time	1		ns
I7	t_{IH}	RX data hold time	2		ns
I8	t_{OD}	TX data output delay		8.5	ns
I9	t_{OH}	TX data hold time		8	ns

4.14 External Interfaces

4.14.1 SPI Flash Interface

The external serial flash stores the user profiles and firmware patch updates. The CC3120R device acts as a master in this case; the SPI serial flash acts as the slave device. This interface can work up to a speed of 20 MHz.

Figure 4-15 shows the SPI flash interface.

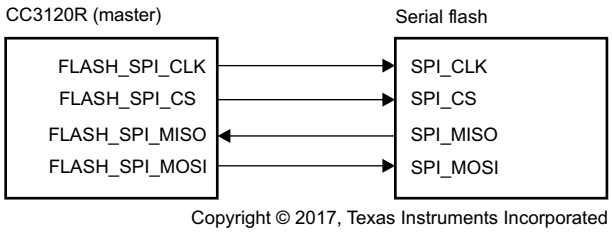


Figure 4-15. SPI Flash Interface

Table 4-12 lists the SPI flash interface pins.

Table 4-12. SPI Flash Interface

PIN NAME	DESCRIPTION
FLASH_SPI_CLK	Clock (up to 20 MHz) CC3120R device to serial flash
FLASH_SPI_CS	CS signal from CC3120R device to serial flash
FLASH_SPI_MISO	Data from serial flash to CC3120R device
FLASH_SPI_MOSI	Data from CC3120R device to serial flash

4.14.2 SPI Host Interface

The device interfaces to an external host using the SPI interface. The CC3120R device can interrupt the host using the HOST_INTR line to initiate the data transfer over the interface. The SPI host interface can work up to a speed of 20 MHz.

Figure 4-16 shows the SPI host interface.

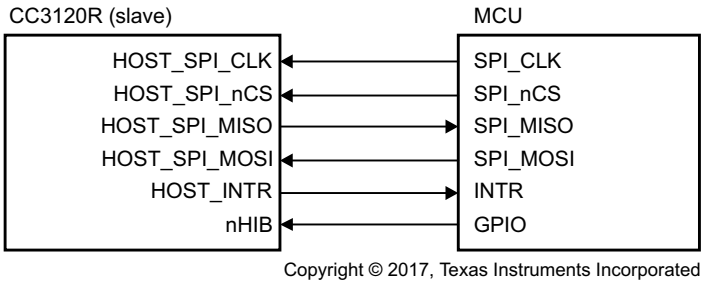


Figure 4-16. SPI Host Interface

Table 4-13 lists the SPI host interface pins.

Table 4-13. SPI Host Interface

PIN NAME	DESCRIPTION
HOST_SPI_CLK	Clock (up to 20 MHz) from MCU host to CC3120R device
HOST_SPI_nCS	CS (active low) signal from MCU host to CC3120R device
HOST_SPI_MOSI	Data from MCU host to CC3120R device
HOST_INTR	Interrupt from CC3120R device to MCU host
HOST_SPI_MISO	Data from CC3120R device to MCU host
nHIB	Active-low signal that commands the CC3120R device to enter hibernate mode (lowest power state)

4.15 Host UART

The SimpleLink device requires the UART configuration described in Table 4-14.

Table 4-14. SimpleLink UART Configuration

PROPERTY	SUPPORTED CC3120R CONFIGURATION
Baud rate	115200 bps, no auto-baud rate detection, can be changed by the host up to 3 Mbps using a special command
Data bits	8 bits
Flow control	CTS/RTS
Parity	None
Stop bits	1
Bit order	LSBit first
Host interrupt polarity	Active high
Host interrupt mode	Rising edge or level 1
Endianness	Little-endian only(1)

(1) The SimpleLink device does not support automatic detection of the host length while using the UART interface.

4.15.1 5-Wire UART Topology

Figure 4-17 shows the typical 5-wire UART topology comprised of four standard UART lines plus one IRQ line from the device to the host controller to allow efficient low-power mode.

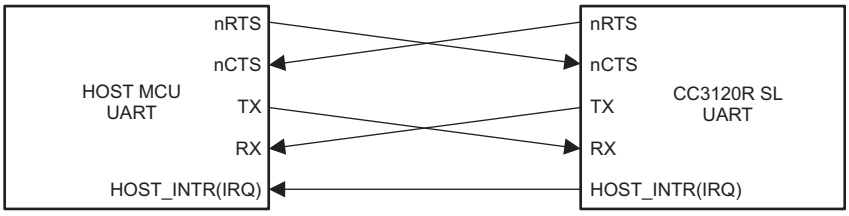


Figure 4-17. Typical 5-Wire UART Topology

This topology is recommended because the configuration offers the maximum communication reliability and flexibility between the host and the SimpleLink device.

4.15.2 4-Wire UART Topology

The 4-wire UART topology eliminates the host IRQ line (see Figure 4-18). Using this topology requires meeting one of the following conditions:

- The host is always awake or active.
- The host goes to sleep, but the UART module has receiver start-edge detection for auto wakeup and does not lose data.

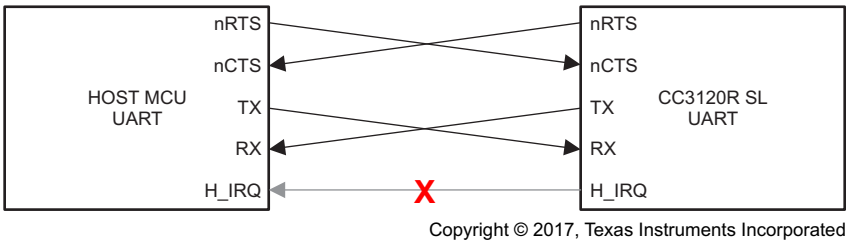


Figure 4-18. 4-Wire UART Configuration

4.15.3 3-Wire UART Topology

The 3-wire UART topology requires only the following lines (see Figure 4-19):

- RX
- TX
- CTS

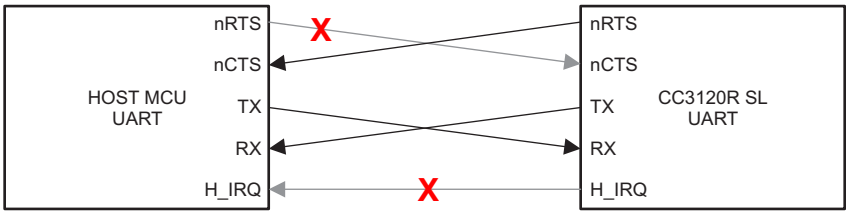


Figure 4-19. 3-Wire UART Topology

Using this topology requires meeting one of the following conditions:

- The host always stays awake or active.
- The host goes to sleep but the UART module has receiver start-edge detection for auto-wake-up and does not lose data.
- The host can always receive any amount of data transmitted by the SimpleLink device because there is no flow control in this direction.

Because there is no full flow control, the host cannot stop the SimpleLink device to send its data; thus, the following parameters must be carefully considered:

- Maximum baud rate
- RX character interrupt latency and low-level driver jitter buffer
- Time consumed by the user's application

5 Detailed Description

5.1 Overview

The CC3120R Wi-Fi Internet-on-a-chip contains a dedicated ARM MCU that offloads many of the networking activities from the host MCU. The device includes an 802.11b/g/n radio, baseband, and MAC with a powerful crypto engine for a fast, secure WLAN and Internet connections with 256-bit encryption. The CC3120R device supports station, AP, and Wi-Fi Direct modes. The device also supports WPA2 personal and enterprise security and WPS 2.0. The Wi-Fi network processor includes an embedded IPv6 and IPv4 TCP/IP stack.

5.2 Functional Block Diagram

Figure 5-1 shows the functional block diagram of the CC3120R SimpleLink Wi-Fi solution.

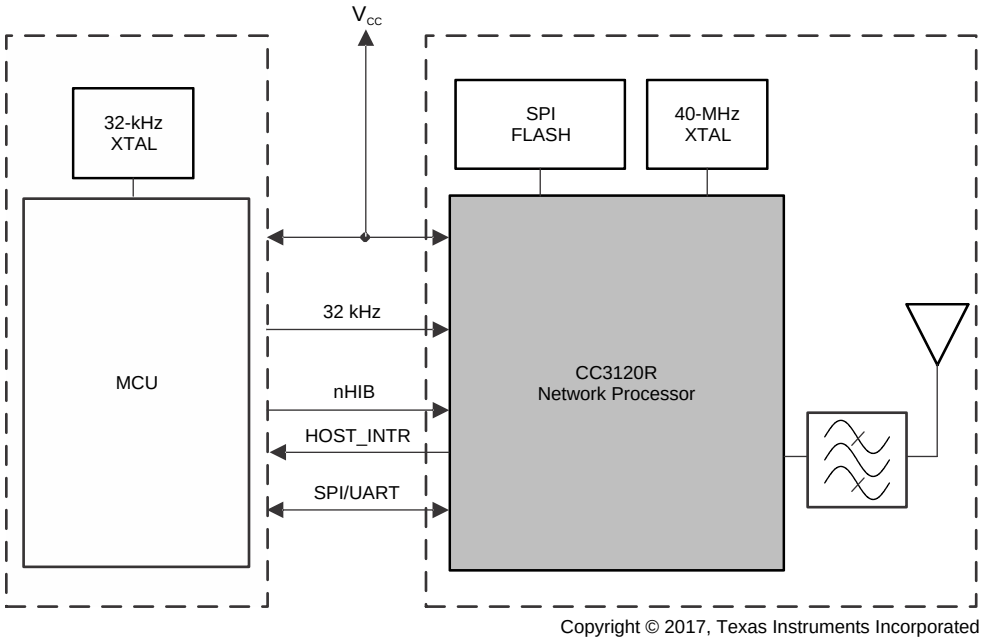


Figure 5-1. Functional Block Diagram

5.3 Device Features

5.3.1 WLAN

The WLAN features are as follows:

- 802.11b/g/n integrated radio, modem, and MAC supporting WLAN communication as a BSS station, AP, Wi-Fi Direct client and group owner with CCK and OFDM rates in the 2.4-GHz ISM band, channels 1 to 13.

NOTE

802.11n is supported only in Wi-Fi station, Wi-Fi direct, and P2P client mode

- Autocalibrated radio with a single-ended 50-Ω interface enables easy connection to the antenna without requiring expertise in radio circuit design.
- Advanced connection manager with multiple user-configurable profiles stored in serial-flash allows automatic fast connection to an access point without user or host intervention.
- Supports all common Wi-Fi security modes for personal and enterprise networks with on-chip security accelerators, including: WEP, WPA/WPA2 PSK, WPA2 Enterprise (802.1x).
- Smart provisioning options deeply integrated within the device providing a comprehensive end-to-end solution. With elaborate events notification to the host, enabling the application to control the provisioning decision flow. The wide variety of Wi-Fi provisioning methods include:
  - Access Point using HTTPS
  - SmartConfig Technology: a 1-step, 1-time process to connect a CC3120R-enabled device to the home wireless network, removing dependency on the I/O capabilities of the host MCU; thus, it is usable by deeply embedded applications
- 802.11 transceiver mode allows transmitting and receiving of proprietary data through a socket without adding MAC or PHY headers. The 802.11 transceiver mode provides the option to select the working channel, rate, and transmitted power. The receiver mode works with the filtering options.

5.3.2 Network Stack

The Network Stack features are as follows:

- Integrated IPv4, IPv6 TCP/IP stack with BSD (BSD adjacent) socket APIs for simple Internet connectivity with any MCU, microprocessor, or ASIC

NOTE

Not all APIs are 100% BSD compliant. Not all BSD APIs are supported.

- Support of 16 simultaneous TCP, UDP, or RAW sockets
- Support of 6 simultaneous SSL\TLS sockets
- Built-in network protocols:
  - Static IP, LLA, DHCPv4, DHCPv6 with DAD and stateless autoconfiguration
  - ARP, ICMPv4, IGMP, ICMPv6, MLD, ND
  - DNS client for easy connection to the local network and the Internet

- Built-in network application and utilities:
  - HTTP/HTTPS
    - Web page content stored on serial flash
    - RESTful APIs for setting and configuring application content
    - Dynamic user callbacks
  - Service discovery: Multicast DNS service discovery lets a client advertise its service without a centralized server. After connecting to the access point, the CC3120R device provides critical information, such as device name, IP, vendor, and port number.
  - DHCP server
  - Ping

Table 5-1 summarizes the NWP features.

Table 5-1. NWP Features

Feature	Description
Wi-Fi standards	802.11b/g/n station 802.11b/g AP supporting up to four stations Wi-Fi Direct client and group owner
Wi-Fi	Channels 1 to 13
Wi-Fi security	WEP, WPA/WPA2 PSK, WPA2 enterprise (802.1x)
Wi-Fi provisioning	SmartConfig technology, Wi-Fi protected setup (WPS2), AP mode with internal HTTP/HTTPS web server
IP protocols	IPv4/IPv6
IP addressing	Static IP, LLA, DHCPv4, DHCPv6 (Stateful) with DAD and stateless auto configuration
Cross layer	ARP, ICMPv4, IGMP, ICMPv6, MLD, NDP
Transport	UDP, TCP SSLv3.0/TLSv1.0/TLSv1.1/TLSv1.2 RAW IP
Network applications and utilities	Ping HTTP/HTTPS web server mDNS DNS-SD DHCP server
Host interface	UART/SPI
Security	Device identity Trusted root-certificate catalog TI root-of-trust public key
Power management	Enhanced power policy management uses 802.11 power save and deep sleep power modes
Other	RF Transceiver Programmable RX Filters with Events trigger mechanism including WoWLAN Recovery mechanism – Restore to factory default

5.3.3 Security

The SimpleLink Wi-Fi CC3120R Internet-on-a-chip device enhances the security capabilities available for development of IoT devices, while completely offloading these activities from the MCU to the networking subsystem. The security capabilities include the following key features:

Wi-Fi and Internet Security:

- Personal and enterprise Wi-Fi security
  - Personal standards
    - AES (WPA2-PSK)
    - TKIP (WPA-PSK
    - WEP
  - Enterprise standards
    - EAP Fast
    - EAP PEAPv0 MSCHAPv2
    - EAP PEAPv0 TLS
    - EAP PEAPv1 TLS EAP LS
    - EAP TTLS TLS
    - EAP TTLS MSCHAPv2

- Secure sockets
  - Protocol versions: SSL v3/TLS 1.0/TLS 1.1/TLS 1.2
  - On-chip powerful crypto engine for fast, secure Wi-Fi and internet connections with 256-bit AES encryption for TLS and SSL connections
  - Ciphers suites
    - SL_SEC_MASK_SSL_RSA_WITH_RC4_128_SHA
    - SL_SEC_MASK_SSL_RSA_WITH_RC4_128_MD5
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_RC4_128_SHA
    - SL_SEC_MASK_TLS_RSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_RSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_CHACHA20_POLY1305_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_CHACHA20_POLY1305_SHA256
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_CHACHA20_POLY1305_SHA256
  - Server authentication
  - Client authentication
  - Domain name verification
  - Socket upgrade to secure socket – STARTTLS
- Secure HTTP server (HTTPS)
- The Trusted root-certificate catalog verifies that the CA used by the application is trusted and known secure content delivery
- The TI root-of-trust public key is a hardware-based mechanism that allows authenticating TI as the genuine origin of a given content using asymmetric keys
- Secure content delivery allows file transfer to the system in a secure way on any unsecured tunnel

Code and Data Security:

- Secured network information: Network passwords and certificates are encrypted
- Secured and authenticated service pack: SP is signed based on TI certificate

5.3.4 Host Interface and Driver

- Interfaces over a 4-wire serial peripheral interface (SPI) with any MCU or a processor at a clock speed of 20 MHz.
- Interfaces over UART with any MCU with a baud rate up to 3 Mbps. A low footprint driver is provided for TI MCUs and is easily ported to any processor or ASIC.
- Simple APIs enable easy integration with any single-threaded or multithreaded application.

5.3.5 System

- Works from a single preregulated power supply or connects directly to a battery
- Ultra-low leakage when disabled (hibernate mode) with a current of less than 4 µA with the RTC running
- Integrated clock sources

5.4 Power-Management Subsystem

The CC3120R power-management subsystem contains DC-DC converters to accommodate the different voltage or current requirements of the system.

- Digital DC-DC (Pin 44)
  - Input: VBAT wide voltage (2.1 to 3.6 V) or preregulated 1.85 V
- ANA1 DC-DC (Pin 38)
  - Input: VBAT wide voltage (2.1 to 3.6 V)
  - In preregulated 1.85-V mode, the ANA1 DC-DC converter is bypassed.
- PA DC-DC (Pin 39)
  - Input: VBAT wide voltage (2.1 to 3.6 V)
  - In preregulated 1.85-V mode, the PA DC-DC converter is bypassed.

The CC3120R device is a single-chip WLAN radio solution used on an embedded system with a wide-voltage supply range. The internal power management, including DC-DC converters and LDOs, generates all of the voltages required for the device to operate from a wide variety of input sources. For maximum flexibility, the device can operate in the modes described in Section 5.4.1 and Section 5.4.2.

5.4.1 VBAT Wide-Voltage Connection

In the wide-voltage battery connection, the device is powered directly by the battery or preregulated 3.3-V supply. All other voltages required to operate the device are generated internally by the DC-DC converters. This scheme supports wide-voltage operation from 2.1 to 3.6 V and is thus the most common mode for the device.

5.4.2 Preregulated 1.85V

The preregulated 1.85-V mode of operation applies an external regulated 1.85 V directly at pins 10, 25, 33, 36, 37, 39, 44, 48, and 54 of the device. The VBAT and the VIO are also connected to the 1.85-V supply. This mode provides the lowest BOM count version in which inductors used for PA DC-DC and ANA1 DC-DC (2.2 and 1 µH) and a capacitor (22 µF) can be avoided.

In the preregulated 1.85-V mode, the regulator providing the 1.85 V must have the following characteristics:

- Load current capacity ≥900 mA
- Line and load regulation with <2% ripple with 500-mA step current and settling time of < 4 µs with the load step

NOTE

The regulator must be placed as close as possible to the device so that the IR drop to the device is very low.

5.5 Low-Power Operating Modes

This section describes the low-power modes supported by the device to optimize battery life.

5.5.1 Low-Power Deep Sleep

The low-power deep-sleep (LPDS) mode is an energy-efficient and transparent sleep mode that is entered automatically during periods of inactivity based on internal power optimization algorithms. The device can wake up in less than 3 ms from the internal timer or from any incoming host command. Typical battery drain in this mode is 115 µA. During LPDS mode, the device retains the software state and certain configuration information. The operation is transparent to the external host; thus, no additional handshake is required to enter or exit LPDS mode.

5.5.2 Hibernate

The hibernate mode is the lowest power mode in which all of the digital logic is power-gated. Only a small section of the logic powered directly by the main input supply is retained. The RTC is kept running and the device wakes up once the nHIB line is asserted by the host driver. The wake-up time is longer than LPDS mode at approximately 50 ms.

NOTE

Wake-up time can be extended depending on the service-pack size.

5.5.3 Shutdown

The shutdown mode is the lowest power-mode system-wise. All device logics are off, including the real-time clock (RTC). The wake-up time in this mode is longer than hibernate at approximately 1.1 s.

5.6 Memory

5.6.1 External Memory Requirements

The CC3120R device maintains a proprietary file system on the sFLASH. The CC3120R file system stores the service pack file, system files, configuration files, certificate files, web page files, and user files. By using a format command through the API, users can provide the total size allocated for the file system. The starting address of the file system cannot be set and is always at the beginning of the sFLASH. The applications microcontroller must access the sFLASH memory area allocated to the file system directly through the CC3120R file system. The applications microcontroller must not access the sFLASH memory area directly.

The file system manages the allocation of sFLASH blocks for stored files according to download order, which means that the location of a specific file is not fixed in all systems. Files are stored on sFLASH using human-readable filenames rather than file IDs. The file system API works using plain text, and file encryption and decryption is invisible to the user. Encrypted files can be accessed only through the file system.

All file types can have a maximum of 100 supported files in the file system. All files are stored in 4-KB blocks and thus use a minimum of 4KB of flash space. Fail-safe files require twice the original size and use a minimum of 8KB. Encrypted files are counted as fail-safe in terms of space. The maximum file size is 1MB.

Table 5-2 lists the minimum required memory consumption under the following assumptions:

- System files in use consume 64 blocks (256KB).
- Vendor files are not taken into account.
- Gang image:
  - Storage for the gang image is rounded up to 32 blocks (meaning 128-KB resolution).
  - Gang image size depends on the actual content size of all components. Additionally, the image should be 128-KB aligned so unaligned memory is considered lost. Service pack, system files, and the 128-KB aligned memory are assumed to occupy 256KB.
- All calculations consider that the restore-to-default is enabled.

Table 5-2. Title

ITEM	CC3120 [KB]
File system allocation table	20
System and configuration files	256
Service Pack	264
Gang image size	256
Total	796
Minimal flash size	8MBit
Recommended flash size	16MBit

NOTE

The maximum supported sFLASH size is 32MB (256Mb). Please refer to *Using Serial Flash on CC3120/CC3220 SimpleLink™ Wi-Fi® and Internet-of-Things Devices*.

5.7 Restoring Factory Default Configuration

The device has an internal recovery mechanism that allows rolling back the file system to its predefined factory image or restoring the factory default parameters of the device. The factory image is kept in a separate sector on the sFLASH in a secure manner and cannot be accessed from the host processor. The following restore modes are supported:

- None—no factory restore settings
- Enable restore of factory default parameters
- Enable restore of factory image and factory default parameters

The restore process is performed by pulling or forcing SOP[2:0] = 110 pins and toggling the nRESET pin from low to high.

The process is fail-safe and resumes operation if a power failure occurs before the restore is finished. The restore process typically takes about 8 seconds, depending on the attributes of the serial flash vendor.

6 Applications, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

6.1.1 Typical Application—CC3120R Wide-Voltage Mode

Figure 6-1 shows the typical application schematic using the CC3120R device in the wide-voltage mode of operation. For a full operation reference design, refer to the BoosterPack that uses the CC3120R device (see *CC3120 SimpleLink™ and Internet of Things Hardware Design Files*).

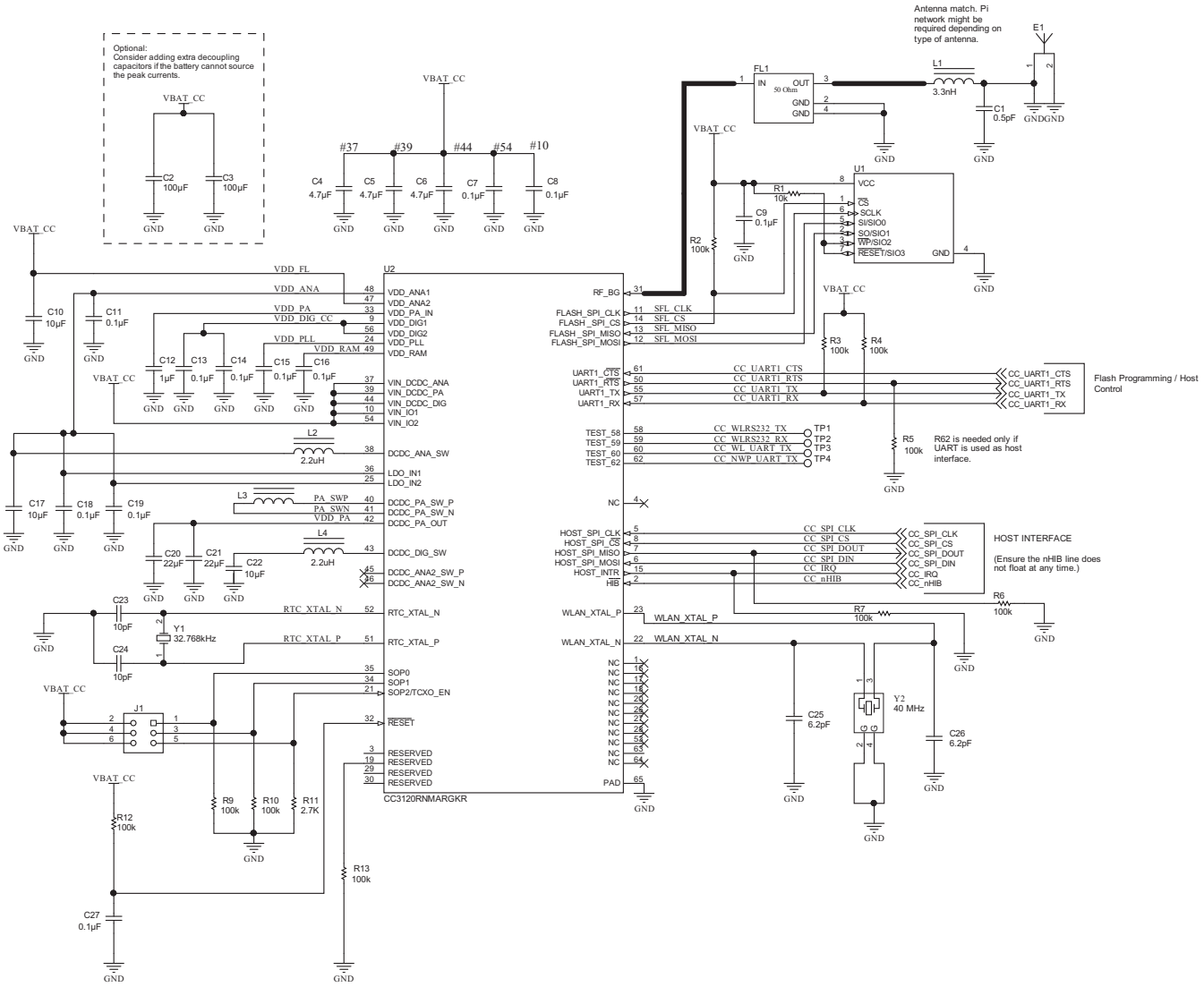


Figure 6-1. CC3120R Wide-Voltage Mode Application

Table 6-1 lists the bill of materials for an application using the CC3120R device in wide-voltage mode.

Table 6-1. Bill of Materials for CC3120R in Wide-Voltage Mode

QUANTITY	PART REFERENCE	VALUE	MANUFACTURER	PART NUMBER	DESCRIPTION
1	C1	0.5 pF	Murata	GRM1555C1HR50BA01D	CAP, CERM, 0.5 pF, 50 V, ±20%, C0G/NP0, 0402
2	C2, C3	100 µF	Taiyo Yuden	LMK325ABJ107MMHT	CAP, CERM, 100 µF, 10 V, ±20%, X5R, AEC-Q200 Grade 3, 1210
3	C4, C5, C6	4.7 µF	TDK	C1005X5R0J475M050BC	CAP, CERM, 4.7 µF, 6.3 V, ±20%, X5R, 0402
11	C7, C8, C9, C11, C13, C14, C15, C16, C18, C19, C27	0.1 µF	TDK	C1005X5R1A104K050BA	CAP, CERM, 0.1 µF, 10 V, ±10%, X5R, 0402
3	C10, C17, C22	10 µF	Murata	GRM188R60J106ME47D	CAP, CERM, 10 µF, 6.3 V, ±20%, X5R, 0603
1	C12	1 µF	TDK	C1005X5R1A105K050BB	CAP, CERM, 1 µF, 10 V, ±10%, X5R, 0402
2	C20, C21	22 µF	TDK	C1608X5R0G226M080AA	CAP, CERM, 22 µF, 4 V, ±20%, X5R, 0603
2	C23, C24	10 pF	Johanson Technology	500R07S100JV4T	CAP, CERM, 10 pF, 50 V, ±5%, C0G/NP0, 0402
2	C25, C26	6.2 pF	Murata	GRM1555C1H6R2CA01D	CAP, CERM, 6.2 pF, 50 V, ±5%, C0G/NP0, 0402
1	E1	2.45-GHz Ant	Taiyo Yuden	AH316M245001-T	ANT Bluetooth W-LAN ZIGBEE WIMAX, SMD
1	FL1	1.02 dB	TDK	DEA202450BT-1294C1-H	Multilayer Chip Band Pass Filter For 2.4GHz W-LAN/Bluetooth, SMD
1	L1	3.3 nH	Murata	LQG15HS3N3S02D	Inductor, Multilayer, Air Core, 3.3 nH, 0.3 A, 0.17 ohm, SMD
2	L2, L4	2.2 uH	Murata	LQM2HPN2R2MG0L	Inductor, Multilayer, Ferrite, 2.2 µH, 1.3 A, 0.08 ohm, SMD
1	L3	1 uH	Murata	LQM2HPN1R0MG0L	Inductor, Multilayer, Ferrite, 1 µH, 1.6 A, 0.055 ohm, SMD
1	R1	10 k	Vishay-Dale	CRCW040210K0JNED	RES, 10 k, 5%, 0.063 W, 0402
1	R11	2.7 k	Vishay-Dale	CRCW04022K70JNED	RES, 2.7 k, 5%, 0.063 W, 0402
10	R2, R3, R4, R5, R6, R7, R9, R10, R12, R13	100 k	Vishay-Dale	CRCW0402100KJNED	RES, 100 k, 5%, 0.063 W, 0402
1	U1	MX25R	Macronix International	MX25R1635FM1IL0	ULTRA LOW POWER, 16M-BIT [x 1/x 2/x 4] CMOS MXSMIO(SERIAL MULTI I/O) FLASH MEMORY, SOP-8
1	U2	CC3120	Texas Instruments	CC3120RNMRGK	SimpleLink Wi-Fi Network Processor, Internet-of-Things Solution for MCU Applications, RGK0064B
1	Y1	Crystal	Abracon Corporation	ABS07-32.768KHZ-9-T	CRYSTAL, 32.768KHZ, 9PF, SMD
1	Y2	Crystal	Epson	Q24FA20H0039600	Crystal, 40MHz, 8pF, SMD

6.1.2 Typical Application Schematic—CC3120R Preregulated, 1.85-V Mode

Figure 6-2 shows the typical application schematic using the CC3120R in preregulated, 1.85-V mode of operation. For addition information on this mode of operation please contact your TI representative.

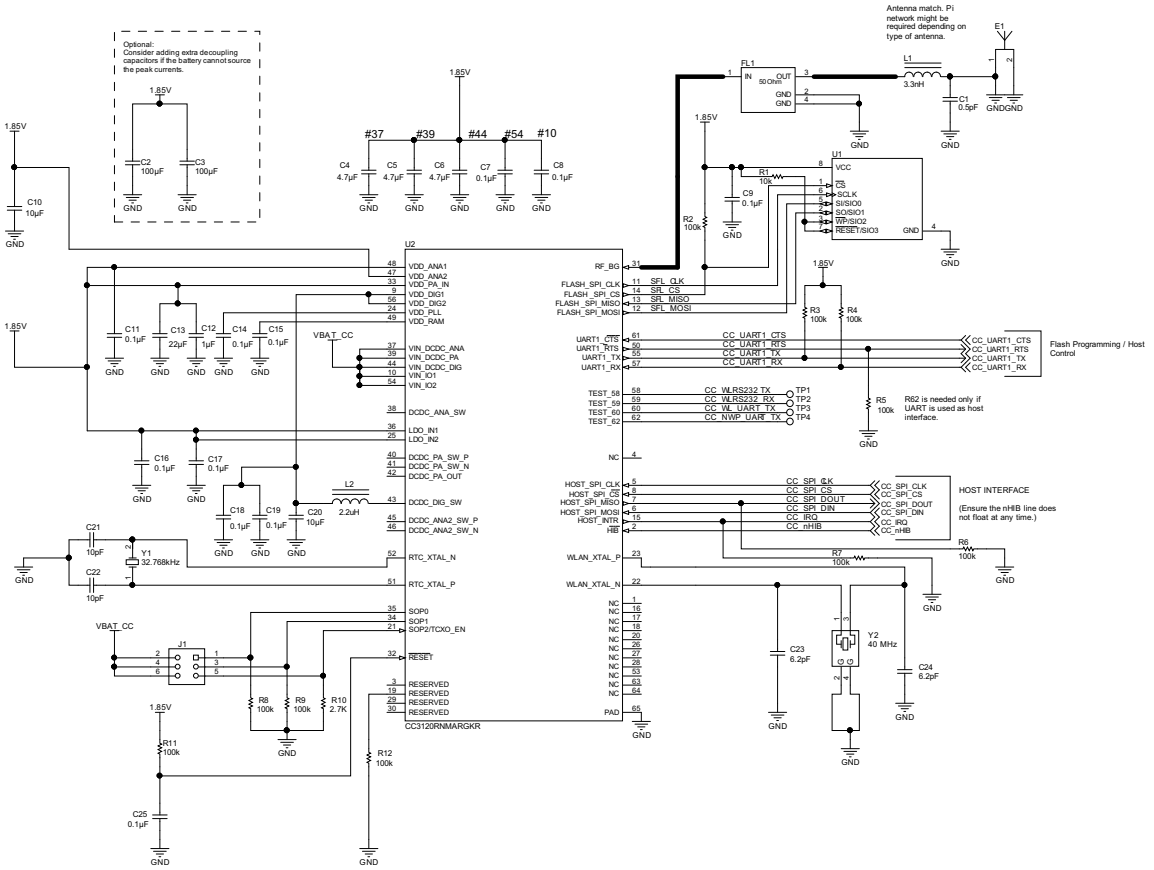


Figure 6-2. CC3120R Preregulated 1.85-V Mode Application Circuit

Table 6-2 lists the bill of materials for an application using the CC3120R device in preregulated 1.85-V mode.

Table 6-2. Bill of Materials for CC3120R in Preregulated, 1.85-V Mode

QUANTITY	DESIGNATOR	VALUE	MANUFACTURER	PART NUMBER	DESCRIPTION
1	U1	MX25R	Macronix International Co., LTD	MX25R1635FM1IL0	ULTRA LOW POWER, 16M-BIT [x 1/x 2/x 4] CMOS MXSMIO(SERIAL MULTI I/O) FLASH MEMORY, SOP-8
1	U2	CC3120	Texas Instruments	CC3120RNMRGK	SimpleLink Wi-Fi Network Processor, Internet-of-Things Solution for MCU Applications, RGK0064B
1	R10	2.7 k	Vishay-Dale	CRCW04022K70JNED	RES, 2.7 k, 5%, 0.063 W, 0402
10	R2, R3, R4, R5, R6, R7, R8, R9, R11, R12	100 k	Vishay-Dale	CRCW0402100KJNED	RES, 100 k, 5%, 0.063 W, 0402
1	R1	10 k	Vishay-Dale	CRCW040210K0JNED	RES, 10 k, 5%, 0.063 W, 0402
1	FL1	1.02 dB	TDK	DEA202450BT-1294C1-H	Multilayer Chip Band Pass Filter For 2.4-GHz W-LAN/Bluetooth, SMD
1	L2	2.2 µH	MuRata	LQM2HPN2R2MG0L	Inductor, Multilayer, Ferrite, 2.2 µH, 1.3 A, 0.08 ohm, SMD
1	L1	3.3 nH	MuRata	LQG15HS3N3S02D	Inductor, Multilayer, Air Core, 3.3 nH, 0.3 A, 0.17 Ω, SMD
1	Y1	Crystal	Abracon Corportation	ABS07-32.768KHZ-9-T	CRYSTAL, 32.768 kHz, 9 pF, SMD
1	Y2	Crystal	Epson	Q24FA20H0039600	Crystal, 40 MHz, 8 pF, SMD
2	C2, C3	100 µF	Taiyo Yuden	LMK325ABJ107MMHT	CAP, CERM, 100 µF, 10 V, ±20%, X5R, AEC-Q200 Grade 3, 1210
1	C13	22 µF	TDK	C1608X5R0G226M080AA	CAP, CERM, 22 µF, 4 V, ±20%, X5R, 0603
2	C10, C20	10 µF	MuRata	GRM188R60J106ME47D	CAP, CERM, 10 µF, 6.3 V, ±20%, X5R, 0603
2	C21, C22	10 pF	Johanson Technology	500R07S100JV4T	CAP, CERM, 10 pF, 50 V, ±5%, C0G/NP0, 0402
2	C23, C24	6.2 pF	MuRata	GRM1555C1H6R2CA01D	CAP, CERM, 6.2 pF, 50 V, ±5%, C0G/NP0, 0402
3	C4, C5, C6	4.7 µF	TDK	C1005X5R0J475M050BC	CAP, CERM, 4.7 µF, 6.3 V, ±20%, X5R, 0402
1	C12	1 µF	TDK	C1005X5R1A105K050BB	CAP, CERM, 1 µF, 10 V, ±10%, X5R, 0402
1	C1	0.5 pF	MuRata	GRM1555C1HR50BA01D	CAP, CERM, 0.5 pF, 50 V, ±20%, C0G/NP0, 0402
11	C7, C8, C9, C11, C14, C15, C16, C17, C18, C19, C25	0.1 µF	TDK	C1005X5R1A104K050BA	CAP, CERM, 0.1 µF, 10 V, ±10%, X5R, 0402
1	E1	2.45-Ghz Ant	Taiyo Yuden	AH316M245001-T	ANT BLUETOOTH W-LAN ZIGBEE WIMAX, SMD

6.2 PCB Layout Guidelines

This section details the PCB guidelines to speed up the PCB design using the CC3120R VQFN device. Follow these guidelines ensures that the design will minimize the risk with regulatory certifications including FCC, ETSI, and CE. For more information, see *CC3120 and CC3220 SimpleLink™ Wi-Fi® and IoT Solution Layout Guidelines*.

6.2.1 General PCB Guidelines

Use the following PCB guidelines:

- Verify the recommended PCB stackup in the PCB design guidelines, as well as the recommended layers for signals and ground.
- Ensure that the QFN PCB footprint follows the information in Section 8.
- Ensure that the QFN PCB GND and solder paste follow the recommendations provided in *CC3120 and CC3220 SimpleLink™ Wi-Fi® and IoT Solution Layout Guidelines*.
- Decoupling capacitors must be as close as possible to the QFN device.

6.2.2 Power Layout and Routing

Three critical DC-DC converters must be considered for the CC3120R device.

- Analog DC-DC converter
- PA DC-DC converter
- Digital DC-DC converter

Each converter requires an external inductor and capacitor that must be laid out with care. DC current loops are formed when laying out the power components.

6.2.2.1 Design Considerations

The following design guidelines must be followed when laying out the CC3120R device:

- Route all of the input decoupling capacitors (C11, C13, and C18) on L2 using thick traces, to isolate the RF ground from the noisy supply ground. This step is also required to meet the IEEE spectral mask specifications.
- Maintain the thickness of power traces to be greater than 12 mils. Take special consideration for power amplifier supply lines (pin 33, 40, 41, and 42), and all input supply pins (pin 37, 39, and 44).
- Ensure the shortest grounding loop for the PLL supply decoupling capacitor (pin 24).
- Place all decoupling capacitors as close to the respective pins as possible.
- Power budget: The CC3120R device can consume up to 450 mA for 3.3 V, 670 mA for 2.1 V, and 700 mA for 1.85 V, for 24 ms during the calibration cycle.
- Ensure the power supply is designed to source this current without any issues. The complete calibration (TX and RX) can take up to 17 mJ of energy from the battery over a time of 24 ms.
- The CC3120R device contains many high-current input pins. Ensure the trace feeding these pins is capable of handling the following currents:
  - PA DCDC input (pin 39) maximum 1 A
  - ANA DCDC input (pin 37) maximum 600 mA
  - DIG DCDC input (pin 44) maximum 500 mA
  - PA DCDC switching nodes (pin 40 and pin 41) maximum 1 A
  - PA DCDC output node (pin 42) maximum 1 A
  - ANA DCDC switching node (pin 38) maximum 600 mA
  - DIG DCDC switching node (pin 43) maximum 500 mA
  - PA supply (pin 33) maximum 500 mA

Figure 6-3 shows the ground routing for the input decoupling capacitors.

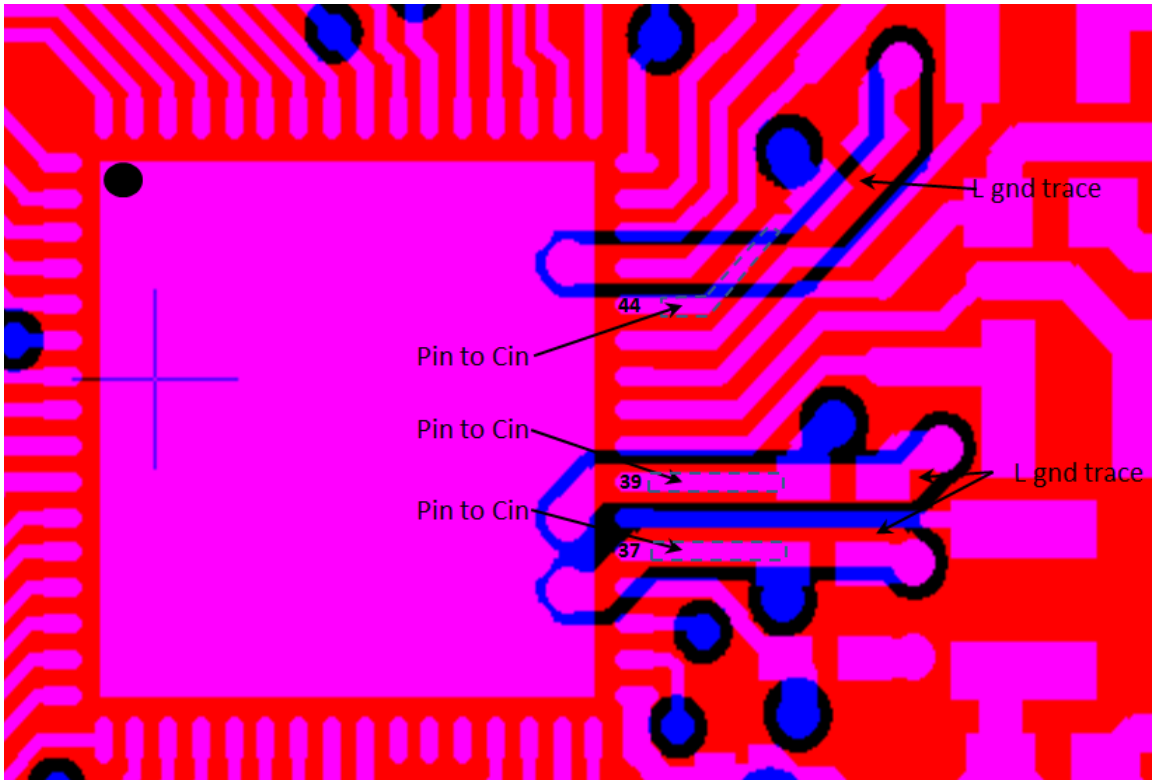


Figure 6-3. Ground Routing for the Input Decoupling Capacitors

The ground return for the input capacitors are routed on L2 to reduce the EMI and improve the spectral mask. This routing must be strictly followed because it is critical for the overall performance of the device.

6.2.3 Clock Interfaces

The following guidelines are for the slow clock.

- The 32.768-kHz crystal must be placed close to the QFN package.
- Ensure that the load capacitance is tuned according to the board parasitics to the frequency tolerance is within ±150 ppm.
- The ground plane on layer two is solid below the trace lanes and there is ground around these traces on the top layer.

The following guidelines are for the fast clock.

- The 40-MHz crystal must be placed close to the QFN package.
- Ensure that he load capacitance is tuned according to the board parasitics to the frequency tolerance is within ±100 ppm at room temperature. The total frequency across parts, temperature, and with aging, must be ±25 ppm to meet the WLAN specification.
- Ensure that no high-frequency lines are routed close to the XTAL routing to avoid noise degradation.
- Ensure that crystal tuning capacitors are close to the crystal pads.
- Make both traces (XTALM and XTALP) as close to parallel as possible and approximately the same length.
- The ground plane on layer two is solid below the trace lines and that there is ground around these traces on the top layer.
- See *CC31xx & CC32xx Frequency Tuning* for frequency tuning.

6.2.4 Digital Input and Output

The following guidelines are for the digital I/O.

- Route SPI and UART lines away from any RF traces.
- Keep the length of the high-speed lines as short as possible to avoid transmission line effects.
- Keep the line lower than 1/10 of the rise time of the signal to ignore transmission line effects. This is required if the traces cannot be kept short. Place the resistor at the source end, closer to the device that is driving the signal.
- Add series-terminating resistor for each high-speed line (such as SPI_CLK or SPI_DATA) to match the driver impedance to the line. Typical terminating-resistor values range from 27 to 36 Ω for a 50-Ω line impedance.
- Route high-speed lines with a ground reference plane continuously below it to offer good impedance throughout. This routing also helps shield the trace against EMI.
- Avoid stubs on high-speed lines to minimize the reflections. If the line must be routed to multiple locations, use a separate line driver for each line.
- If the lines are longer compared to the rise time, add series-terminating resistors near the driver for each high-speed line to match the driver impedance to the line. Typical terminating-resistor values range from 27 to 36 Ω for a 50-Ω line impedance.

6.2.5 RF Interface

The following guidelines are for the RF interface. Follow guidelines specified in the vendor-specific antenna design guides (including placement of the antenna). Also see *CC3120 and CC3220 SimpleLink™ Wi-Fi® and IoT Solution Layout Guidelines* for general antenna guidelines.

- Ensure that the antenna is matched for 50-Ω. A Pi-matching network is recommended.
- Ensure that the area underneath the BPF pads are grounded on layer one and layer two, and that the minimum fulter requirements are met.
- Verify that the Wi-Fi RF trace is a 50-Ω, impedance-controlled trace with a reference to solid ground.
- The RF trace bends must be made with gradual curves, and 90-degree bends must be avoided.
- The RF traces must not have sharp corners.
- There must be no traces or ground under the antenna section.
- The RF traces must have via stitching on the ground plane beside the RF trace on both sides.

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed in this section.

7.1 Tools and Software

Development Tools

SimpleLink Studio for CC3120R The CC3120R device is supported.

SimpleLink Studio for CC3120R is a Windows®-based software tool used to aid in the development of embedded networking applications and software for microcontrollers. Using SimpleLink Studio for CC3120R, embedded software developers can develop and test applications using any desktop IDE, such as Visual Studio or Eclipse, and connect their applications to the cloud using the CC3120R BoosterPack™ Plug-in Module. The application can then be easily ported to any microcontroller. With the SimpleLink Wi-Fi CC3120R solution, customers now have the flexibility to add Wi-Fi to any microcontroller (MCU). This Internet-on-a-chip solution contains all you need to easily create IoT solutions: security, quick connection, cloud support, and more. For more information on CC3120R, visit SimpleLink Wi-Fi Solutions.

CC3120R Software Development Kit (SDK) The CC3120R device is supported.

The SimpleLink Wi-Fi CC3220 SDK contains drivers for the CC3220 programmable MCU, 30+ sample applications, and documentation needed to use the solution. The SDK also contains the flash programmer, a command line tool for flashing software, configuring network and software parameters (SSID, access point channel, network profile, and so on), system files, and user files (certificates, web pages, and so on). This SDK can be used with TI's SimpleLInk Wi-Fi CC3220 LaunchPad™ development kit.

The SDK has a variety of support offerings. All sample applications in the SDK are supported on the integrated Cortex-M4 processor with CCS IDE and no RTOS. In addition, a few of the applications support IAR, Free RTOS, and TI-RTOS.

TI Designs and Reference Designs

The TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor, and connectivity. Created by TI experts to help you jumpstart your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market.

7.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of the CC3120R device and support tools (see Figure 7-1).

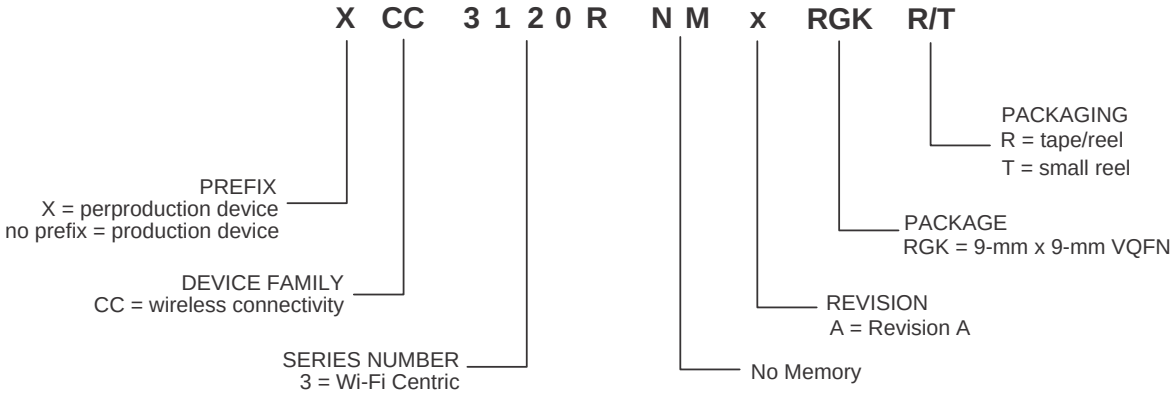


Figure 7-1. CC3120R Device Nomenclature

7.3 Documentation Support

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (CC3120). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document. The current documentation that describes the processor, related peripherals, and other technical collateral follows.

The following documents provide support for the CC3120 device.

Application Reports

SimpleLink™ CC3120, CC3220 Wi-Fi® Internet-on-a chip™ Networking Sub-System Power Management
This application report describes the best practices for power management and extended battery life for embedded low-power Wi-Fi devices such as the SimpleLink Wi-Fi Internet-on-a chip™ solution from Texas Instruments™.

SimpleLink™ CC3120, CC3220 Wi-Fi® Internet-on-a chip™ Solution Built-In Security Features The SimpleLink Wi-Fi CC3120 and CC3220 Internet-on-a chip™ family of devices from Texas Instruments™ offer a wide range of built-in security features to help developers address a variety of security needs, which is achieved without any processing burden on the main microcontroller (MCU). This document describes these security-related features and provides recommendations for leveraging each in the context of practical system implementation.

SimpleLink™ CC3120, CC3220 Wi-Fi® and Internet of Things Over-the-Air Update This document describes the OTA library for the SimpleLink™ Wi-Fi® CC3x20 family of devices from Texas Instruments™ and explains how to prepare a new cloud-ready update to be downloaded by the OTA library.

SimpleLink™ CC3120, CC3220 Wi-Fi® Internet-on-a chip™ Solution Device Provisioning This guide describes the provisioning process, which provides the SimpleLink Wi-Fi device with the information (network name, password, and so forth) needed to connect to a wireless network.

Using Serial Flash on SimpleLink™ CC3120 and CC3220 Wi-Fi® and Internet-of-Things Devices
This application note is divided into two parts. The first part provides important guidelines and best- practice design techniques to consider when choosing and embedding a serial flash paired with the CC3120 and CC3220 (CC3x20) devices. The second part describes the file system, along with guidelines and considerations for system designers working with the CC3x20 devices.

User's Guides

SimpleLink™ Wi-Fi® and Internet of Things CC3120 and CC3220 Network Processor This document provides software (SW) programmers with all of the required knowledge for working with the networking subsystem of the SimpleLink Wi-Fi devices. This guide provides basic guidelines for writing robust, optimized networking host applications, and describes the capabilities of the networking subsystem. The guide contains some example code snapshots, to give users an idea of how to work with the host driver. More comprehensive code examples can be found in the formal software development kit (SDK). This guide does not provide a detailed description of the host driver APIs.

SimpleLink™ Wi-Fi® CC3120 BoosterPack™ Plug-In Module and IoT Solution The SimpleLink Wi-Fi CC3120 wireless network processor from Texas Instruments™ provides users the flexibility to add Wi-Fi to any MCU. This user's guide explains the various configurations of the CC3120 BoosterPack™ Plug-In Module.

SimpleLink™ Wi-Fi® CC3120 and CC3220 and IoT Solution Layout Guidelines This document provides the design guidelines of the 4-layer PCB used for the CC3120 and CC3220 SimpleLink Wi-Fi family of devices from Texas Instruments™. The CC3120 and CC3220 devices are easy to lay out and are available in quad flat no-leads (QFNS) packages. When designing the board, follow the suggestions in this document to optimize performance of the board.

SimpleLink™ Wi-Fi® CC3120 Internet-on-a-chip™ Solution SDK This guide is intended to help users in the initial setup and demonstration of the different demos in the CC3120 SDK. The guide lists the software and hardware components required to get started, and explains how to install the supported integrated development environment (IDE), SimpleLink CC3120 SDK, and the various other tools required.

SimpleLink™ Wi-Fi® and Internet-on-a-chip™ CC3120 and CC3220 Solution Radio Tool The Radio Tool serves as a control panel for direct access to the radio, and can be used for both the radio frequency (RF) evaluation and for certification purposes. This guide describes how to have the tool work seamlessly on Texas Instruments ™ evaluation platforms such as the BoosterPack™ plus FTDI emulation board for CC3120 devices, and the LaunchPad™ for CC3220 devices.

SimpleLink™ Wi-Fi® CC3120 and CC3220 Provisioning for Mobile Applications This guide describes TI's SimpleLink™ Wi-Fi® provisioning solution for mobile applications, specifically on the usage of the Android™ and iOS® building blocks for UI requirements, networking, and provisioning APIs required for building the mobile application.

More Literature

RemoTI Manifest

CC3120 SimpleLink™ WI-Fi® and Internet of Things CC3120 hardware design files.

7.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.5 Trademarks

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ARM is a registered trademark of ARM Physical IP, Inc.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
Windows is a registered trademark of Microsoft Inc.
Wi-Fi, Wi-Fi Direct are registered trademarks of Wi-Fi Alliance.
All other trademarks are the property of their respective owners.

7.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.7 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

7.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC3120RNMARGKR	ACTIVE	VQFN	RGK	64	2500	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC3120R NMA	Samples
CC3120RNMARGKT	ACTIVE	VQFN	RGK	64	250	Green (RoHS & no Sb/Br)	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC3120R NMA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

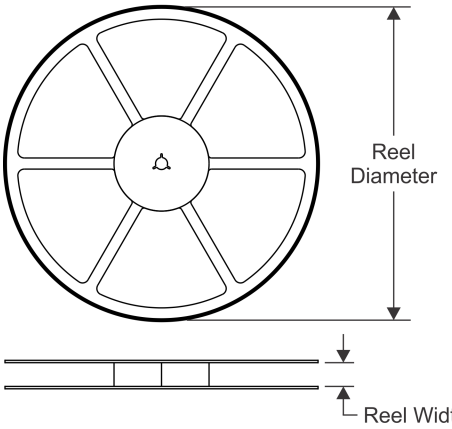
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

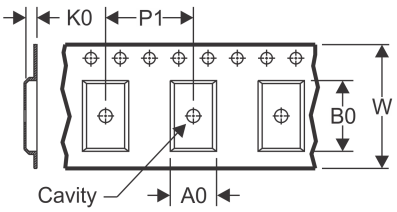
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

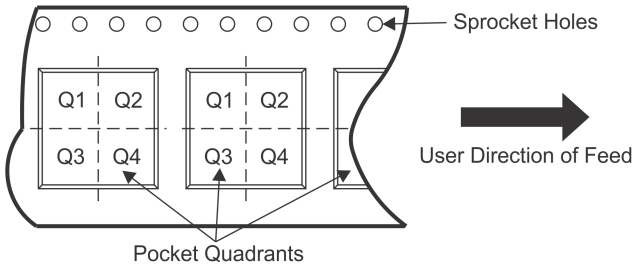


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

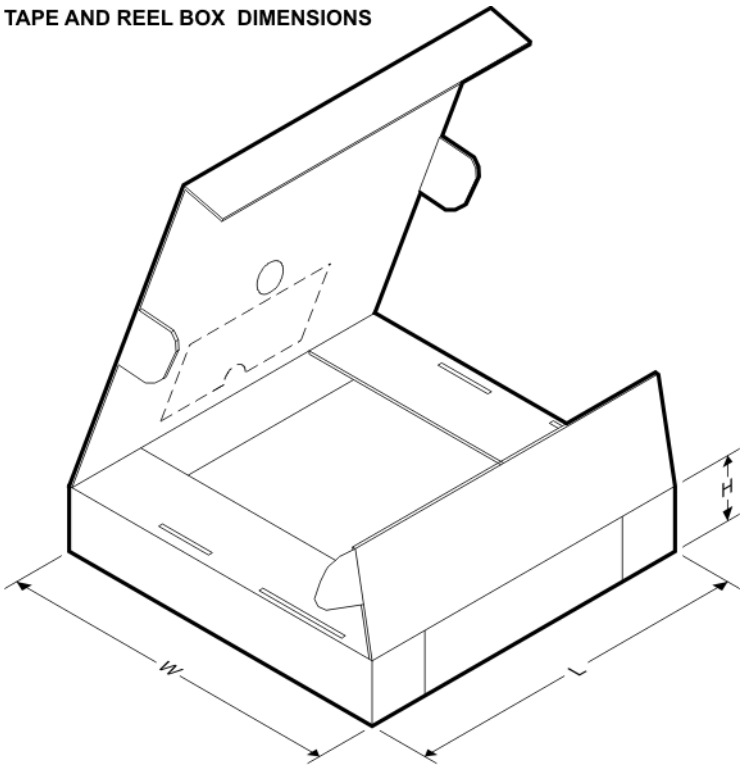
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC3120RNMARGKR	VQFN	RGK	64	2500	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
CC3120RNMARGKR	VQFN	RGK	64	2500	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
CC3120RNMARGKT	VQFN	RGK	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
CC3120RNMARGKT	VQFN	RGK	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



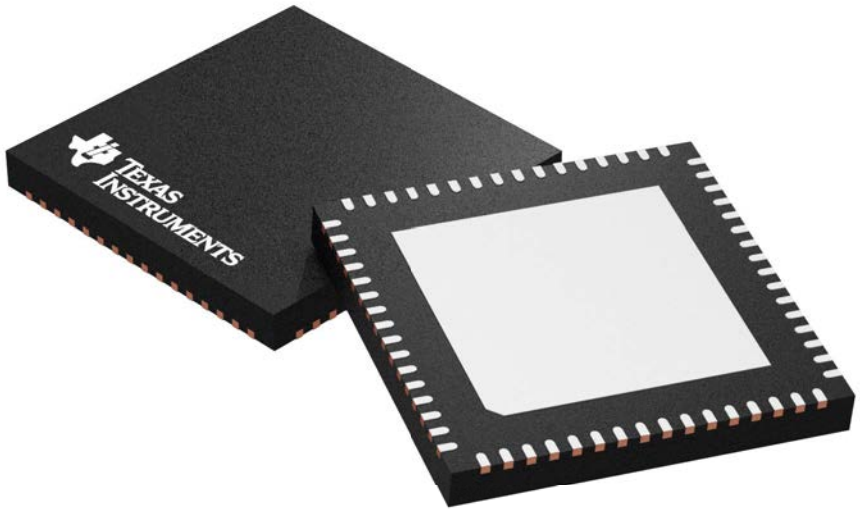
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC3120RNMARGKR	VQFN	RGK	64	2500	336.6	336.6	31.8
CC3120RNMARGKR	VQFN	RGK	64	2500	367.0	367.0	38.0
CC3120RNMARGKT	VQFN	RGK	64	250	210.0	185.0	35.0
CC3120RNMARGKT	VQFN	RGK	64	250	210.0	185.0	35.0

RGK 64

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



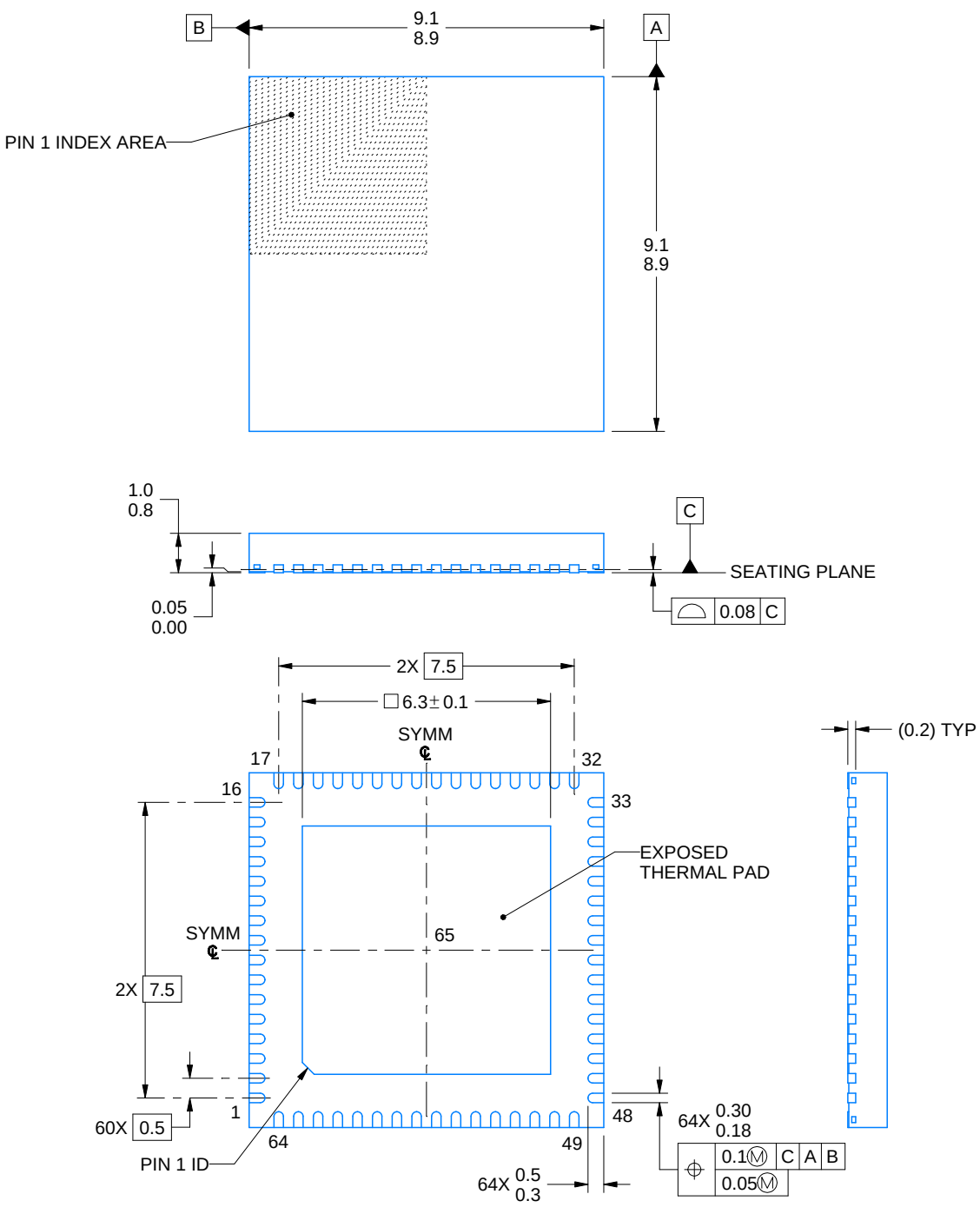
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGK0064B

PACKAGE OUTLINE

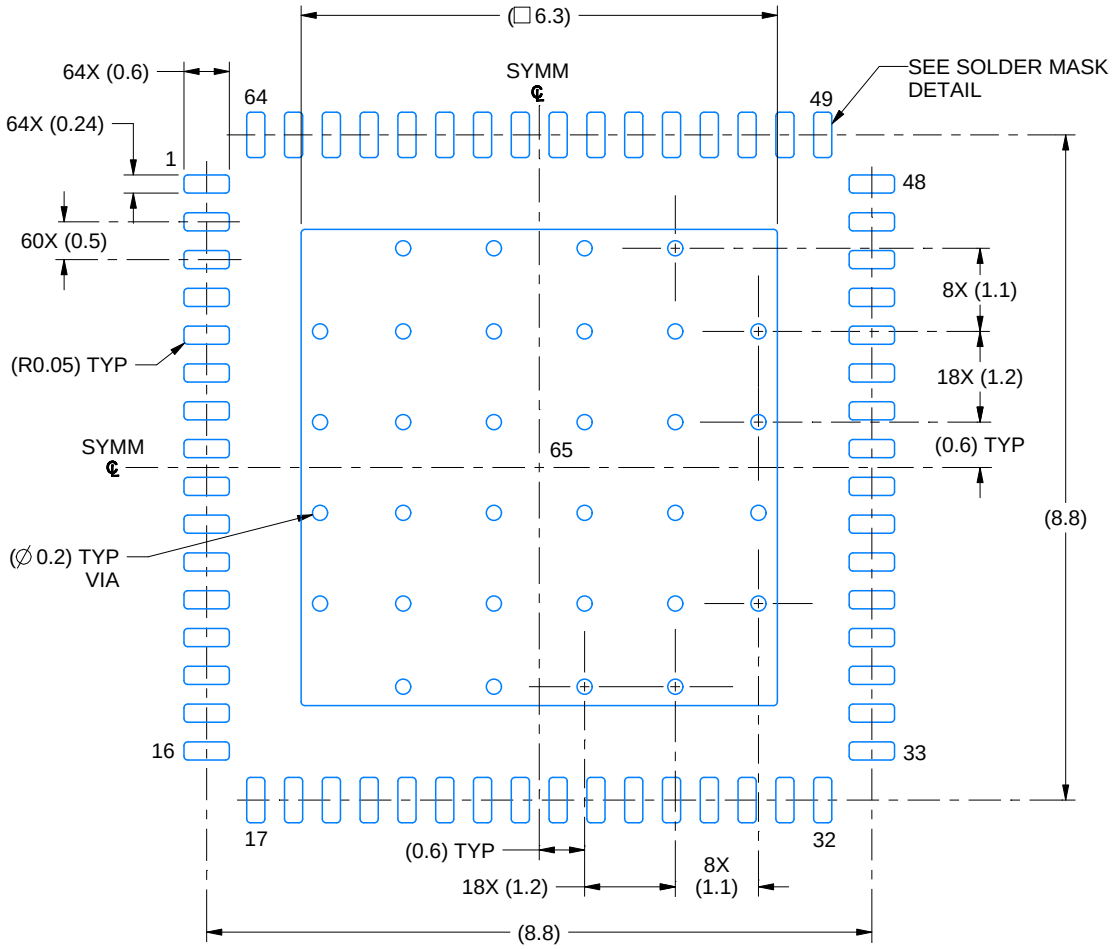
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

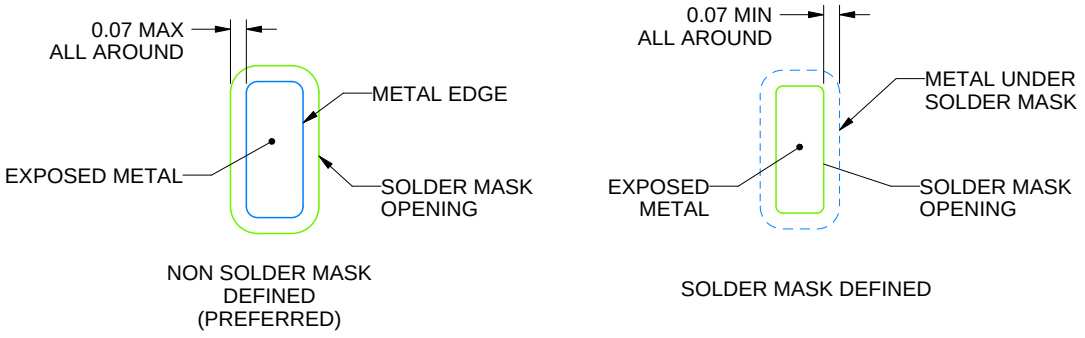


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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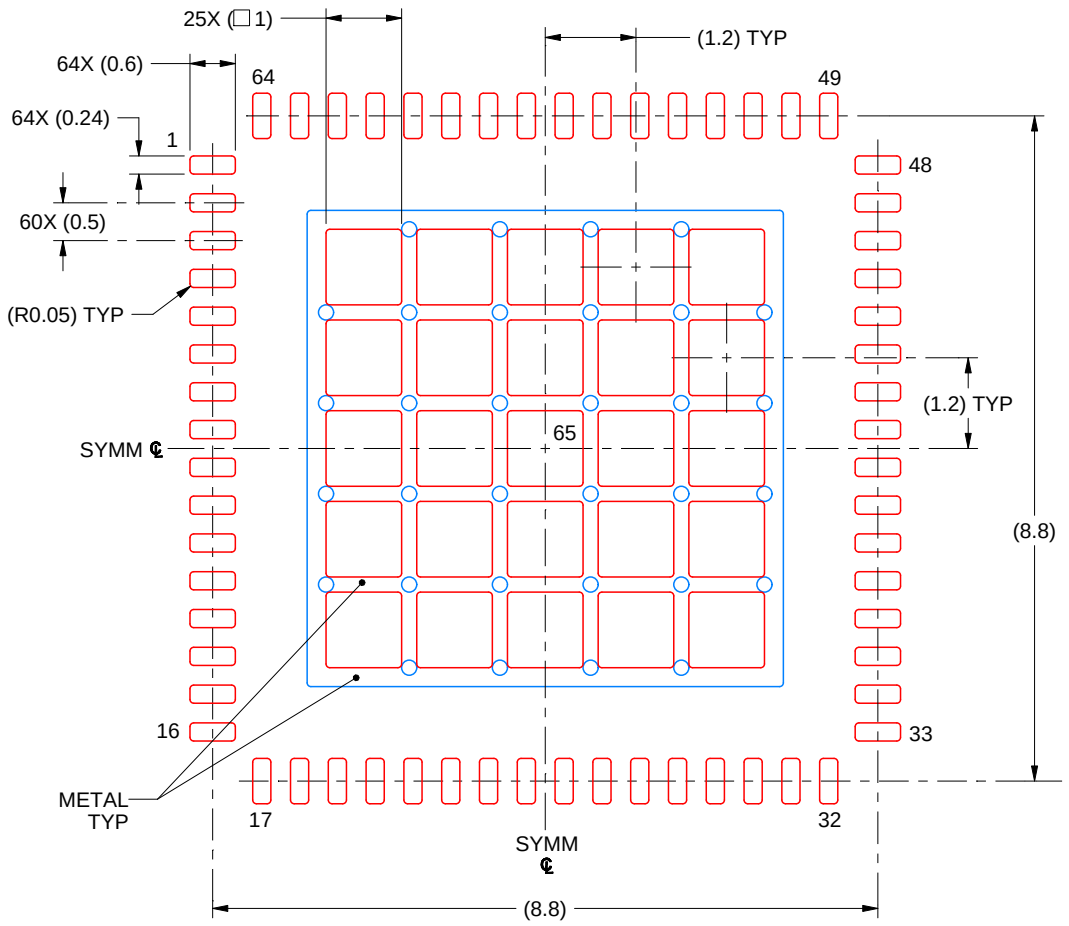
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
63% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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