18-Bit, 1.25 MSPS PulSAR® ADC

AD7643

FEATURES

Throughput: 1.25 MSPS
INL: ±1.5 LSB typical, ±3 LSB maximum (±11 ppm of full scale)
18-bit resolution with no missing codes
Dynamic range: 95 dB typical
SINAD: 93.5 dB typical @ 20 kHz (V_{REF} = 2.5 V)
THD: −113 dB typical @ 20 kHz (V_{REF} = 2.5 V)
2.048 V internal reference: typical drift 8 ppm/°C; TEMP output
Differential input range: ±V_{REF} (V_{REF} up to 2.5 V)
No pipeline delay (SAR architecture)
Parallel (18-, 16-, or 8-bit bus) and serial 5 V/3.3 V/2.5 V interface
SPI®/QSPI™/MICROWIRE™/DSP compatible
Single 2.5 V supply operation
Power dissipation
- **65 mW typical @ 1.25 MSPS with internal REF**
- **2 µW in power-down mode**

Pb-free, 48-lead LQFP and 48-lead LFCSP_VQ
Pin compatible with the AD7641 and other PulSAR ADC's

APPLICATIONS

Medical instruments
High speed data acquisition/high dynamic data acquisition
Digital signal processing
Spectrum analysis
Instrumentation
Communications
ATE

GENERAL DESCRIPTION

The AD7643 is an 18-bit, 1.25 MSPS, charge redistribution SAR, fully differential, analog-to-digital converter (ADC) that operates from a single 2.5 V power supply. The part contains a high speed, 18-bit sampling ADC, an internal conversion clock, an internal reference (and buffer), error correction circuits, and both serial and parallel system interface ports. The part has no latency and can be used in asynchronous rate applications. The AD7643 is hardware factory calibrated and tested to ensure ac parameters, such as signal-to-noise ratio (SNR), in addition to the more traditional dc parameters of gain, offset, and linearity. The AD7643 is only available in Pb-free packages with operation specified from −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

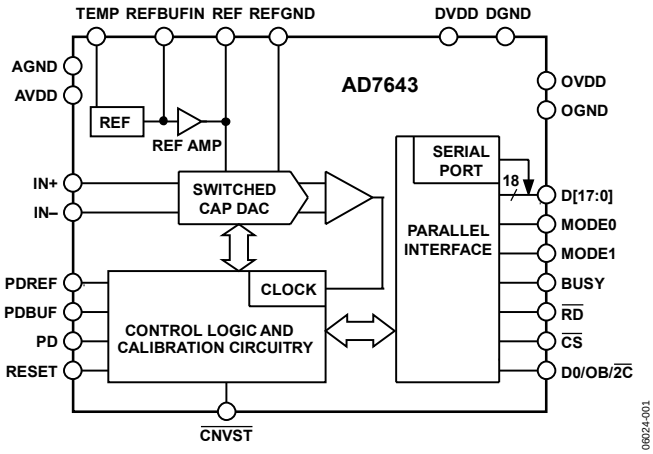


Figure 1.

Table 1. PulSAR 48-Lead Selection

Type/kSPS	100 to 250	500 to 570	650 to 1000	>1000
Pseudo Differential	AD7651, AD7660, AD7661	AD7650, AD7652, AD7664, AD7666	AD7653, AD7667	
True Bipolar	AD7610, AD7663	AD7665	AD7612, AD7671	
True Differential	AD7675	AD7676	AD7677	AD7621, AD7622, AD7623
18-Bit Multichannel/ Simultaneous	AD7631, AD7678	AD7679 AD7654	AD7634, AD7674 AD7655	AD7641, AD7643

PRODUCT HIGHLIGHTS

1. **Fast Throughput.**
   The AD7643 is a 1.25 MSPS, charge redistribution, 18-bit SAR ADC.
2. **Superior Linearity.**
   The AD7643 has no missing 18-bit code.
3. **Internal Reference.**
   The AD7643 has a 2.048 V internal reference with a typical drift of ±8 ppm/°C and an on-chip TEMP sensor.
4. **Single-Supply Operation.**
   The AD7643 operates from a 2.5 V single supply.
5. **Serial or Parallel Interface.**
   Versatile parallel (18-, 16-, or 8-bit bus) or 2-wire serial interface arrangement compatible with 2.5 V, 3.3 V, or 5 V logic.

Rev. 0
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REVISION HISTORY

4/06—Revision 0: Initial Version

SPECIFICATIONS

AVDD = DVDD = 2.5 V; OVDD = 2.3 V to 3.6 V; V_{REF} = 2.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		18			Bits
ANALOG INPUT					
Voltage Range	$V_{IN+} - V_{IN-}$	$-V_{REF}$		$+V_{REF}$	V
Operating Input Voltage	V_{IN+}, V_{IN-} to AGND	−0.1		AVDD[1]	V
Analog Input CMRR	f_{IN} = 100 kHz		58		dB
Input Current	1.25 MSPS throughput		2.5		µA
Input Impedance[2]					
THROUGHPUT SPEED					
Complete Cycle				800	ns
Throughput Rate				1.25	MSPS
DC ACCURACY					
Integral Linearity Error[3]		−3	±1.5	+3	LSB[4]
No Missing Codes		18			Bits
Differential Linearity Error		−1		+1.25	LSB
Transition Noise	V_{REF} = 2.5 V		1.7		LSB
	V_{REF} = 2.048 V		2.0		LSB
Zero Error, T_{MIN} to T_{MAX}[5]		−16		+16	LSB
Zero Error Temperature Drift			±1		ppm/°C
Gain Error, T_{MIN} to T_{MAX}[5]		−22		+22	LSB
Gain Error Temperature Drift			±1		ppm/°C
Power Supply Sensitivity	AVDD = 2.5 V ± 5%		±16		LSB
AC ACCURACY					
Dynamic Range	V_{REF} = 2.5 V		95		dB[6]
Signal-to-Noise	f_{IN} = 1 kHz, V_{REF} = 2.5 V		93.5		dB
	f_{IN} = 20 kHz, V_{REF} = 2.5 V		93.5		dB
	f_{IN} = 20 kHz, V_{REF} = 2.048 V		92		dB
	f_{IN} = 100 kHz, V_{REF} = 2.5 V		93		dB
Spurious-Free Dynamic Range	f_{IN} = 1 kHz, V_{REF} = 2.5 V		118		dB
	f_{IN} = 20 kHz, V_{REF} = 2.5 V		114		dB
	f_{IN} = 20 kHz, V_{REF} = 2.048 V		111		dB
	f_{IN} = 100 kHz, V_{REF} = 2.5 V		108		dB
Total Harmonic Distortion	f_{IN} = 1 kHz, V_{REF} = 2.5 V		−114		dB
	f_{IN} = 20 kHz, V_{REF} = 2.5 V		−113		dB
	f_{IN} = 20 kHz, V_{REF} = 2.048 V		−109		dB
	f_{IN} = 100 kHz, V_{REF} = 2.5 V		−105		dB
Signal-to-(Noise + Distortion)	f_{IN} = 1 kHz, V_{REF} = 2.5 V		93.5		dB
	f_{IN} = 20 kHz, V_{REF} = 2.5 V		93.5		dB
	f_{IN} = 20 kHz, V_{REF} = 2.048 V		91.8		dB
	f_{IN} = 100 kHz, V_{REF} = 2.5 V		92.5		dB
−3 dB Input Bandwidth			50		MHz
SAMPLING DYNAMICS					
Aperture Delay			1		ns
Aperture Jitter			5		ps rms
Transient Response	Full-scale step			250	ns
INTERNAL REFERENCE	PDREF = PDBUF = low				
Output Voltage	REF @ 25°C	2.038	2.048	2.058	V
Temperature Drift	−40°C to +85°C		±8		ppm/°C
Line Regulation	AVDD = 2.5 V ± 5%		±15		ppm/V

Parameter	Conditions	Min	Typ	Max	Unit
Turn-On Settling Time	C_{REF} = 10 µF		5		ms
REFBUFIN Output Voltage	REFBUFIN @ 25°C		1.19		V
REFBUFIN Output Resistance			6.33		kΩ
EXTERNAL REFERENCE	PDREF = PDBUF = high				
Voltage Range	REF	1.8	2.5	AVDD + 0.1	V
Current Drain	1.25 MSPS throughput		100		µA
REFERENCE BUFFER	PDREF = high, PDBUF = low				
REFBUFIN Input Voltage Range	REF = 2.048 V typical	1.05	1.2	1.30	V
REFBUFIN Input Current	REFBUFIN = 1.2 V		1		nA
TEMPERATURE PIN					
Voltage Output	@ 25°C		278		mV
Temperature Sensitivity			1		mV/°C
Output Resistance			4.7		kΩ
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		+0.6	V
V_{IH}		1.7		5.25	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format[7]					
Pipeline Delay[8]					
V_{OL}	I_{SINK} = 500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	OVDD − 0.3			V
POWER SUPPLIES					
Specified Performance					
AVDD		2.37	2.5	2.63	V
DVDD		2.37	2.5	2.63	V
OVDD		2.30[9]		3.6	V
Operating Current[10]	1.25 MSPS throughput				
AVDD[11]	With internal reference		24		mA
DVDD			1.5		mA
OVDD[12]			0.5		mA
Power Dissipation[10, 11]					
With Internal Reference	1.25 MSPS throughput		65	80	mW
With External Reference	1.25 MSPS throughput		60	75	mW
In Power-Down Mode[12]	PD = high		2		µW
TEMPERATURE RANGE[13]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] When using an external reference. With the internal reference, the input range is −0.1 V to V_{REF}.
[2] See Analog Inputs section.
[3] Linearity is tested using endpoints, not best fit.
[4] LSB means least significant bit. With the ±2.048 V input range, 1 LSB is 15.63 µV.
[5] See Voltage Reference Input section. These specifications do not include the error contribution from the external reference.
[6] All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full-scale, unless otherwise specified.
[7] Parallel or serial 18-bit.
[8] Conversion results are available immediately after completed conversion.
[9] See the Absolute Maximum Ratings section.
[10] Tested in parallel reading mode.
[11] With internal reference, PDREF and PDBUF are low; with external reference, PDREF and PDBUF are high.
[12] With all digital inputs forced to OVDD.
[13] Consult sales for extended temperature range.

TIMING SPECIFICATIONS

AVDD = DVDD = 2.5 V; OVDD = 2.3 V to 3.6 V; V_{REF} = 2.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
CONVERSION AND RESET (Refer to Figure 30 and Figure 31)					
Convert Pulse Width	t_1	15		70[1]	ns
Time Between Conversions	t_2	800			ns
$\overline{CNVST}$ Low to BUSY High Delay	t_3			23	ns
BUSY High All Modes (Except Master Serial Read After Convert)	t_4			550	ns
Aperture Delay	t_5		1		ns
End of Conversion to BUSY Low Delay	t_6	10			ns
Conversion Time	t_7			550	ns
Acquisition Time	t_8	250			ns
RESET Pulse Width	t_9	15			ns
RESET Low to BUSY High Delay[2]	t_{38}		10		ns
BUSY High Time from RESET Low[2]	t_{39}		500		ns
PARALLEL INTERFACE MODES (Refer to Figure 32 to Figure 35)					
$\overline{CNVST}$ Low to Data Valid Delay	t_{10}			550	ns
Data Valid to BUSY Low Delay	t_{11}	2			ns
Bus Access Request to Data Valid	t_{12}			20	ns
Bus Relinquish Time	t_{13}	2		15	ns
MASTER SERIAL INTERFACE MODES[3] (Refer to Figure 36 and Figure 37)					
$\overline{CS}$ Low to SYNC Valid Delay	t_{14}			10	ns
$\overline{CS}$ Low to Internal SCLK Valid Delay[3]	t_{15}			10	ns
$\overline{CS}$ Low to SDOUT Delay	t_{16}			10	ns
$\overline{CNVST}$ Low to SYNC Delay	t_{17}		135		ns
SYNC Asserted to SCLK First Edge Delay	t_{18}	2			ns
Internal SCLK Period[4]	t_{19}	8		20	ns
Internal SCLK High[4]	t_{20}	2			ns
Internal SCLK Low[4]	t_{21}	2			ns
SDOUT Valid Setup Time[4]	t_{22}	1			ns
SDOUT Valid Hold Time[4]	t_{23}	0			ns
SCLK Last Edge to SYNC Delay[4]	t_{24}	0			ns
$\overline{CS}$ High to SYNC Hi-Z	t_{25}			10	ns
$\overline{CS}$ High to Internal SCLK Hi-Z	t_{26}			10	ns
$\overline{CS}$ High to SDOUT Hi-Z	t_{27}			10	ns
BUSY High in Master Serial Read After Convert[4]	t_{28}		See Table 4		ns
$\overline{CNVST}$ Low to SYNC Asserted Delay	t_{29}		508		ns
SYNC Deasserted to BUSY Low Delay	t_{30}		13		ns
SLAVE SERIAL INTERFACE MODES (Refer to Figure 39 and Figure 40)					
External SCLK Set-Up Time	t_{31}	5			ns
External SCLK Active Edge to SDOUT Delay	t_{32}	1		8	ns
SDIN Set-Up Time	t_{33}	5			ns
SDIN Hold Time	t_{34}	5			ns
External SCLK Period	t_{35}	12.5			ns
External SCLK High	t_{36}	5			ns
External SCLK Low	t_{37}	5			ns

[1] See the Conversion Control section.
[2] See the Digital Interface section and the RESET section.
[3] In serial interface modes, the SYNC, SCLK, and SDOUT timings are defined with a maximum load C_L of 10 pF; otherwise, the load is 60 pF maximum.
[4] In serial master read during convert mode. See Table 4 for serial master read after convert mode timing specifications.

Table 4. Serial Clock Timings in Master Read After Convert Mode

DIVSCLK[1] DIVSCLK[0]	Symbol	0 0	0 1	1 0	1 1	Unit
SYNC to SCLK First Edge Delay Minimum	t_{18}	1	3	3	3	ns
Internal SCLK Period Minimum	t_{19}	8	16	32	64	ns
Internal SCLK Period Maximum	t_{19}	20	40	70	135	ns
Internal SCLK High Minimum	t_{20}	2	8	16	32	ns
Internal SCLK Low Minimum	t_{21}	2	8	16	32	ns
SDOUT Valid Setup Time Minimum	t_{22}	1	5	5	5	ns
SDOUT Valid Hold Time Minimum	t_{23}	0	0.5	10	30	ns
SCLK Last Edge to SYNC Delay Minimum	t_{24}	0	0.5	9	26	ns
BUSY High Width Maximum	t_{28}	0.84	1.14	1.72	2.88	µs

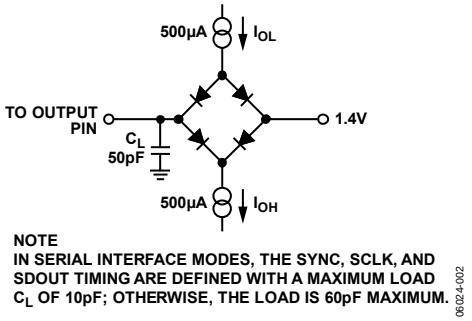


Figure 2. Load Circuit for Digital Interface Timing, SDOUT, SYNC, and SCLK Outputs, C_L = 10 pF

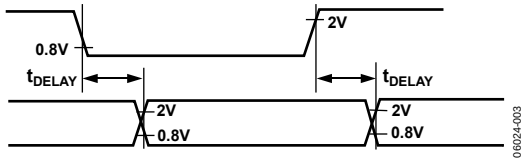


Figure 3. Voltage Reference Levels for Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Analog Inputs/Outputs	
IN+[1], IN−, REF, REFBUFIN, TEMP, INGND, REFGND to AGND	AVDD + 0.3 V to AGND − 0.3 V
Ground Voltage Differences	
AGND, DGND, OGND	±0.3 V
Supply Voltages	
AVDD, DVDD	−0.3 V to +2.7 V
OVDD	−0.3 V to +3.8 V
AVDD to DVDD	±2.8 V
AVDD, DVDD to OVDD	−3.8 V to +2.8 V
Digital Inputs	−0.3 V to +5.5 V
PDREF, PDBUF[2]	±20 mA
Internal Power Dissipation[3]	700 mW
Internal Power Dissipation[4]	2.5 W
Junction Temperature	125°C
Storage Temperature Range	−65°C to +125°C

[1] See Analog Inputs section.
[2] See Voltage Reference Input section.
[3] Specification is for the device in free air:
48-Lead LQFP; θ_{JA} = 91°C/W, θ_{JC} = 30°C/W.
[4] Specification is for the device in free air:
48-Lead LFCSP; θ_{JA} = 26°C/W.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

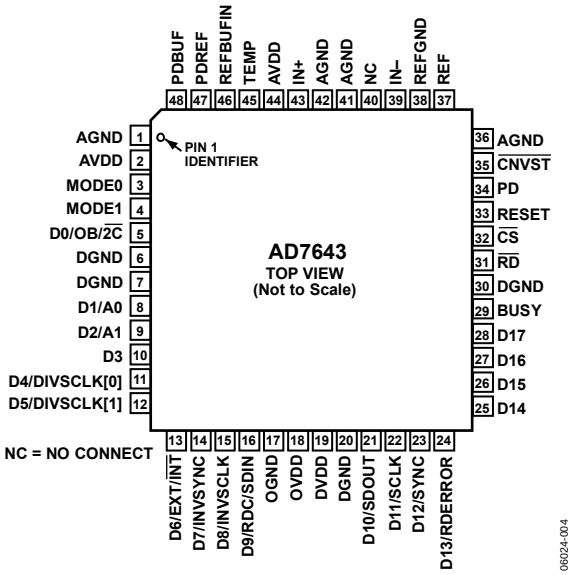


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 36, 41, 42	AGND	P	Analog Power Ground Pin.
2, 44	AVDD	P	Input Analog Power Pins. Nominally 2.5 V.
3, 4	MODE[0:1]	DI	Data Output Interface Mode Selection.
			Interface MODE# / **MODE1** / **MODE0** / **Description**
			0 / 0 / 0 / 18-bit interface
			1 / 0 / 1 / 16-bit interface
			2 / 1 / 0 / 8-bit (byte) interface
			3 / 1 / 1 / Serial interface
5	D0/OB/$\overline{2C}$	DI/O	When MODE[1:0] = 0 (18-bit interface mode), this pin is Bit 0 of the parallel port data output bus and the data coding is straight binary. In all other modes, this pin allows the choice of straight binary/twos complement. When OB/$\overline{2C}$ is high, the digital output is straight binary; when low, the MSB is inverted resulting in a twos complement output from its internal shift register.
6, 7	DGND	P	Connect to Digital Ground.
8	D1/A0	DI/O	When MODE[1:0] = 0, this pin is Bit 1 of the parallel port data output bus. In all other modes, this input pin controls the form in which data is output as shown in Table 7.
9	D2/A1	DI/O	When MODE[1:0] = 0, this pin is Bit 2 of the parallel port data output bus. When MODE[1:0] = 1 or 2, this input pin controls the form in which data is output as shown in Table 7.
10	D3	DO	When MODE[1:0] = 0, 1, or 2, this output is used as Bit 3 of the parallel port data output bus. This pin is always an output, regardless of the interface mode.
11, 12	D[4:5] or DIVSCLK[0:1]	DI/O	When MODE[1:0] = 0, 1, or 2, these pins are Bit 4 and Bit 5 of the parallel port data output bus. When MODE[1:0] = 3 (serial mode), serial clock division selection. When using serial master read after convert mode (EXT/$\overline{INT}$ = low, RDC/SDIN = low), these inputs can be used to slow down the internally generated serial clock that clocks the data output. In other serial modes, these pins are high impedance outputs.
13	D6 or EXT/$\overline{INT}$	DI/O	When MODE[1:0] = 0, 1, or 2, this output is used as Bit 6 of the parallel port data output bus. When MODE[1:0] = 3 (serial mode), serial clock source select. This input is used to select the internally generated (master) or external (slave) serial data clock. When EXT/$\overline{INT}$ = low, master mode. The internal serial clock is selected on SCLK output. When EXT/$\overline{INT}$ = high, slave mode. The output data is synchronized to an external clock signal, gated by $\overline{CS}$, connected to the SCLK input.

Pin No.	Mnemonic	Type[1]	Description
14	D7	DI/O	When MODE[1:0] = 0, 1, or 2, this output is used as Bit 7 of the parallel port data output bus.
	or INVSYNC		When MODE[1:0] = 3 (serial mode), invert sync select. In serial master mode (EXT/$\overline{\text{INT}}$ = low), this input is used to select the active state of the SYNC signal. When INVSYNC = low, SYNC is active high. When INVSYNC = high, SYNC is active low.
15	D8	DI/O	When MODE[1:0] = 0, 1, or 2, this output is used as Bit 8 of the parallel port data output bus.
	or INVSCLK		When MODE[1:0] = 3 (serial mode), invert SCLK select. In all serial modes, this input is used to invert the SCLK signal.
16	D9	DI/O	When MODE[1:0] = 0, 1, or 2, this output is used as bit 9 of the parallel port data output bus.
	or RDC		When MODE[1:0] = 3 (serial mode), read during convert. When using serial master mode (EXT/$\overline{\text{INT}}$ = low), RDC is used to select the read mode. When RDC = high, the previous conversion result is output on SDOUT during conversion and the period of SCLK changes (see the Master Serial Interface section). When RDC = low (read after convert), the current result can be output on SDOUT only when the conversion is complete.
	or SDIN		When MODE[1:0] = 3 (serial mode), serial data in. When using serial slave mode (EXT/$\overline{\text{INT}}$ = high), SDIN could be used as a data input to daisy-chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on SDOUT with a delay of 18 SCLK periods after the initiation of the read sequence.
17	OGND	P	Input/Output Interface Digital Power Ground.
18	OVDD	P	Input/Output Interface Digital Power. Nominally at the same supply as the supply of the host interface (2.5 V or 3 V).
19	DVDD	P	Digital Power. Nominally at 2.5 V.
20	DGND	P	Digital Power Ground.
21	D10	DO	When MODE[1:0] = 0, 1, or 2, this output is used as Bit 10 of the parallel port data output bus.
	or SDOUT		When MODE[1:0] = 3 (serial mode), serial data output. In serial mode, this pin is used as the serial data output synchronized to SCLK. Conversion results are stored in an on-chip register. The AD7643 provides the conversion result, MSB first, from its internal shift register. The data format is determined by the logic level of OB/$\overline{\text{2C}}$. In master mode, EXT/$\overline{\text{INT}}$ = low. SDOUT is valid on both edges of SCLK. In slave mode, EXT/$\overline{\text{INT}}$ = high: When INVSCLK = low, SDOUT is updated on SCLK rising edge and valid on the next falling edge. When INVSCLK = high, SDOUT is updated on SCLK falling edge and valid on the next rising edge.
22	D11	DI/O	When MODE[1:0] = 0, 1, or 2, this output is used as Bit 11 of the parallel port data output bus.
	or SCLK		When MODE[1:0] = 3 (serial mode), serial clock. In all serial modes, this pin is used as the serial data clock input or output, depending upon the logic state of the EXT/$\overline{\text{INT}}$ pin. The active edge where the data SDOUT is updated depends on the logic state of the INVSCLK pin.
23	D12	DO	When MODE[1:0] = 0, 1, or 2, this output is used as Bit 12 of the parallel port data output bus.
	or SYNC		When MODE[1:0] = 3 (serial mode), frame synchronization. In serial master mode (EXT/$\overline{\text{INT}}$= low), this output is used as a digital output frame synchronization for use with the internal data clock. When a read sequence is initiated and INVSYNC = low, SYNC is driven high and remains high while SDOUT output is valid. When a read sequence is initiated and INVSYNC = high, SYNC is driven low and remains low while SDOUT output is valid.
24	D13	DO	When MODE[1:0] = 0, 1, or 2, this output is used as Bit 13 of the parallel port data output bus.
	or RDERROR		When MODE[1:0] = 3 (serial mode), read error. In serial slave mode (EXT/$\overline{\text{INT}}$ = high), this output is used as an incomplete read error flag. If a data read is started and not completed when the current conversion is complete, the current data is lost and RDERROR is pulsed high.
25 to 28	D[14:17]	DO	Bit 14 to Bit 17 of the Parallel Port Data Output Bus. These pins are always outputs, regardless of the interface mode.
29	BUSY	DO	Busy Output. Transitions high when a conversion is started and remains high until the conversion is complete and the data is latched into the on-chip shift register. The falling edge of BUSY can be used as a data-ready clock signal.
30	DGND	P	Digital Power Ground.

Pin No.	Mnemonic	Type[1]	Description
31	$\overline{RD}$	DI	Read Data. When $\overline{CS}$ and $\overline{RD}$ are both low, the interface parallel or serial output bus is enabled.
32	$\overline{CS}$	DI	Chip Select. When $\overline{CS}$ and $\overline{RD}$ are both low, the interface parallel or serial output bus is enabled. $\overline{CS}$ is also used to gate the external clock in slave serial mode.
33	RESET	DI	Reset Input. When high, resets the AD7643. Current conversion, if any, is aborted. Falling edge of RESET enables the calibration mode indicated by pulsing BUSY high. Refer to the Digital Interface section. If not used, this pin can be tied to DGND.
34	PD	DI	Power-Down Input. When high, powers down the ADC. Power consumption is reduced and conversions are inhibited after the current one is completed.
35	$\overline{CNVST}$	DI	Conversion Start. A falling edge on $\overline{CNVST}$ puts the internal sample-and-hold into the hold state and initiates a conversion.
37	REF	AI/O	Reference Output/Input. When PDREF/PDBUF = low, the internal reference and buffer are enabled producing 2.048 V on this pin. When PDREF/PDBUF = high, the internal reference and buffer are disabled allowing an externally supplied voltage reference up to AVDD volts. Decoupling is required with or without the internal reference and buffer. Refer to the Voltage Reference Input section.
38	REFGND	AI	Reference Input Analog Ground.
39	IN–	AI	Differential Negative Analog Input.
40	NC		No Connect.
43	IN+	AI	Differential Positive Analog Input.
45	TEMP	AO	Temperature Sensor Analog Output. Normally, 278 mV @ 25°C with a temperature coefficient of 1 mV/°C. This pin can be used to measure the temperature of the AD7643. See the Temperature Sensor section.
46	REFBUFIN	AI/O	Internal Reference Output/Reference Buffer Input. When PDREF/PDBUF = low, the internal reference and buffer are enabled producing the 1.2 V (typical) band gap output on this pin, which needs external decoupling. The internal fixed gain reference buffer uses this to produce 2.048 V on the REF pin. When using an external reference with the internal reference buffer (PDBUF = low, PDREF = high), applying 1.2 V on this pin produces 2.048 V on the REF pin. Refer to the Voltage Reference Input section.
47	PDREF	DI	Internal Reference Power-Down Input. When low, the internal reference is enabled. When high, the internal reference is powered down and an external reference must been used.
48	PDBUF	DI	Internal Reference Buffer Power-Down Input. When low, the buffer is enabled (must be low when using internal reference). When high, the buffer is powered down.

[1] AI = analog input; AI/O = bidirectional analog; AO = analog output; DI = digital input; DI/O = bidirectional digital; DO = digital output; P = power.

Table 7. Data Bus Interface Definition

MODE	MODE1	MODE0	D0/OB/$\overline{2C}$	D1/A0	D2/A1	D[3]	D[4:9]	D[10:11]	D[12:15]	D[16:17]	Description
0	0	0	R[0]	R[1]	R[2]	R[3]	R[4:9]	R[10:11]	R[12:15]	R[16:17]	18-Bit Parallel
1	0	1	OB/$\overline{2C}$	A0 = 0	R[2]	R[3]	R[4:9]	R[10:11]	R[12:15]	R[16:17]	16-Bit High Word
1	0	1	OB/$\overline{2C}$	A0 = 1	R[0]	R[1]	All Zeros				16-Bit Low Word
2	1	0	OB/$\overline{2C}$	A0 = 0	A1 = 0	All Hi-Z		R[10:11]	R[12:15]	R[16:17]	8-Bit High Byte
2	1	0	OB/$\overline{2C}$	A0 = 0	A1 = 1	All Hi-Z		R[2:3]	R[4:7]	R[8:9]	8-Bit Mid Byte
2	1	0	OB/$\overline{2C}$	A0 = 1	A1 = 0	All Hi-Z		R[0:1]	All Zeros		8-Bit Low Byte
2	1	0	OB/$\overline{2C}$	A0 = 1	A1 = 1	All Hi-Z		All Zeros		R[0:1]	8-Bit Low Byte
3	1	1	OB/$\overline{2C}$	All Hi-Z		Serial Interface					Serial Interface

TERMINOLOGY

Integral Nonlinearity Error (INL)
Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Gain Error
The first transition (from 000…00 to 000…01) should occur for an analog voltage ½ LSB above the nominal negative full scale (−2.0479922 V for the ±2.048 V range). The last transition (from 111…10 to 111…11) should occur for an analog voltage 1½ LSB below the nominal full scale (+2.0479766 V for the ±2.048 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Zero Error
The zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Dynamic Range
It is the ratio of the rms value of the full scale to the rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Signal to (Noise + Distortion) Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD and is expressed in bits by

$$ENOB = [(SINAD_{dB} - 1.76)/6.02]$$

Aperture Delay
Aperture delay is a measure of the acquisition performance and is measured from the falling edge of the $\overline{\text{CNVST}}$ input to when the input signal is held for a conversion.

Transient Response
The time required for the AD7643 to achieve its rated accuracy after a full-scale step function is applied to its input.

Reference Voltage Temperature Coefficient

It is derived from the typical shift of output voltage at 25°C on a sample of parts maximum and minimum reference output voltage (V_{REF}) measured at T_{MIN}, T(25°C), and T_{MAX}. It is expressed in ppm/°C using

$$TCV_{REF}(\text{ppm/°C}) = \frac{V_{REF}(Max) - V_{REF}(Min)}{V_{REF}(25°\text{C}) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:

$V_{REF}(Max)$ = Maximum V_{REF} at T_{MIN}, T(25°C), or T_{MAX}

$V_{REF}(Min)$ = Minimum V_{REF} at T_{MIN}, T(25°C), or T_{MAX}

$V_{REF}(25°C)$ = V_{REF} at 25°C

T_{MAX} = +85°C

T_{MIN} = −40°C

TYPICAL PERFORMANCE CHARACTERISTICS

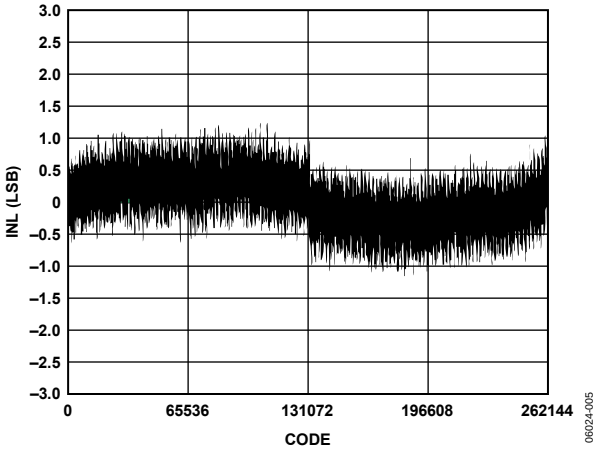


Figure 5. Integral Nonlinearity vs. Code

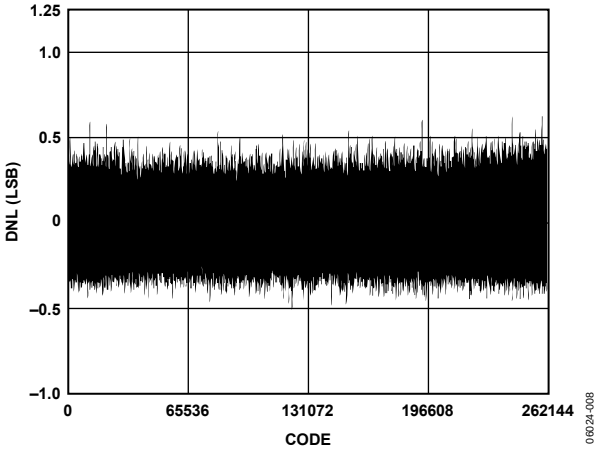


Figure 8. Differential Nonlinearity vs. Code

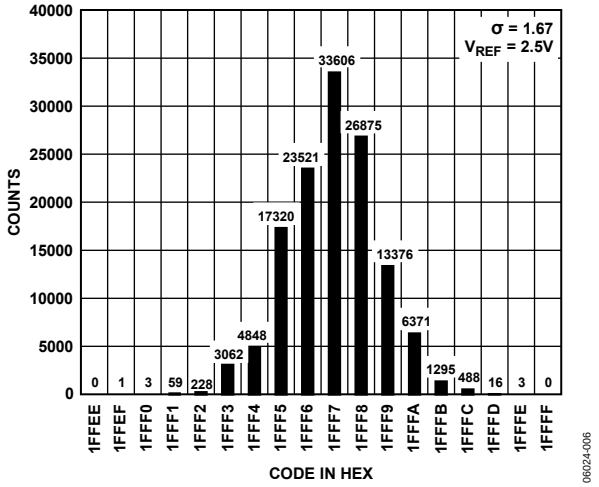


Figure 6. Histogram of 131,072 Conversions of a DC Input at the Code Center (External Reference)

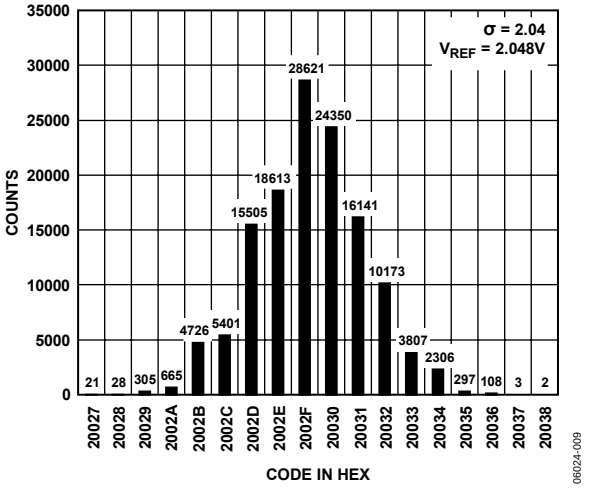


Figure 9. Histogram of 131,072 Conversions of a DC Input at the Code Center (Internal Reference)

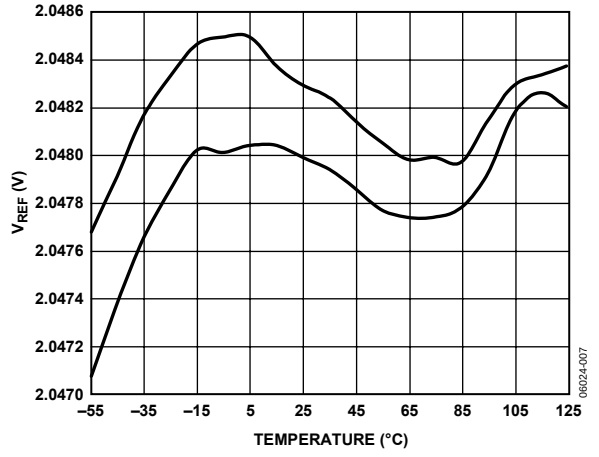


Figure 7. Typical Reference Voltage Output vs. Temperature (2 Units)

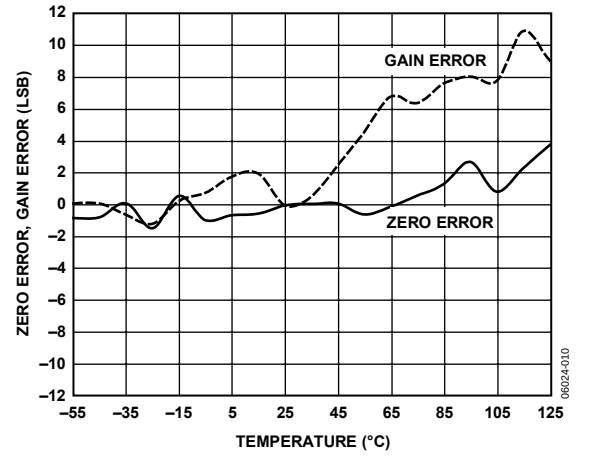


Figure 10. Zero Error, Gain Error vs. Temperature

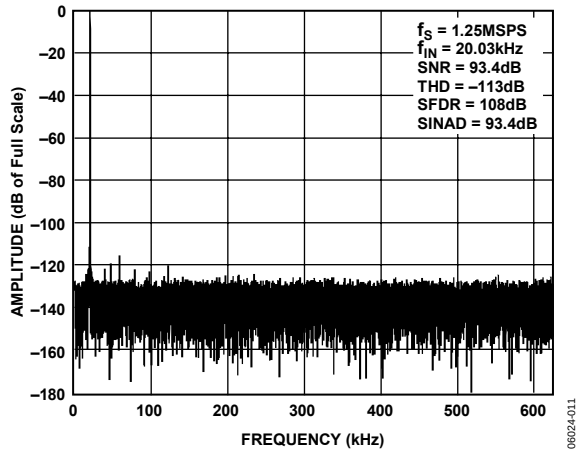


Figure 11. FFT 20 kHz

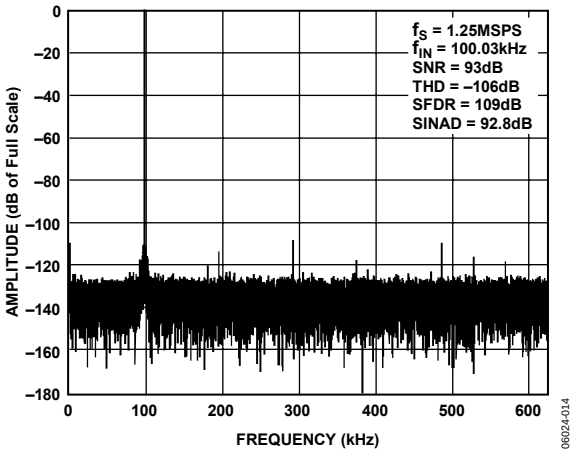


Figure 14. FFT 100 kHz

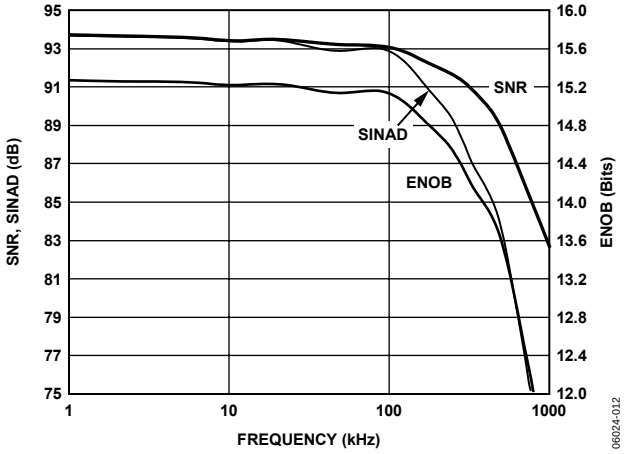


Figure 12. SNR, SINAD, and ENOB vs. Frequency

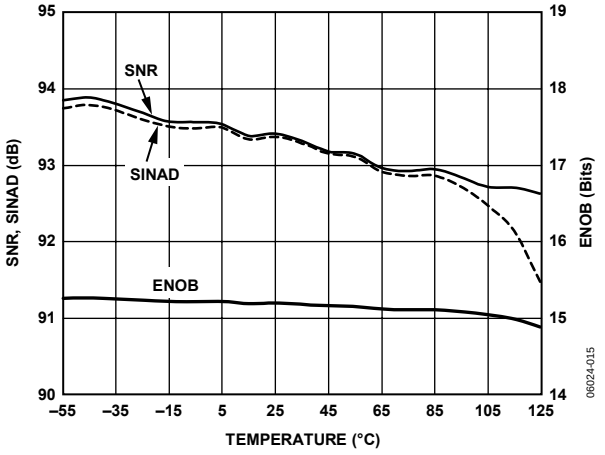


Figure 15. SNR, SINAD, and ENOB vs. Temperature

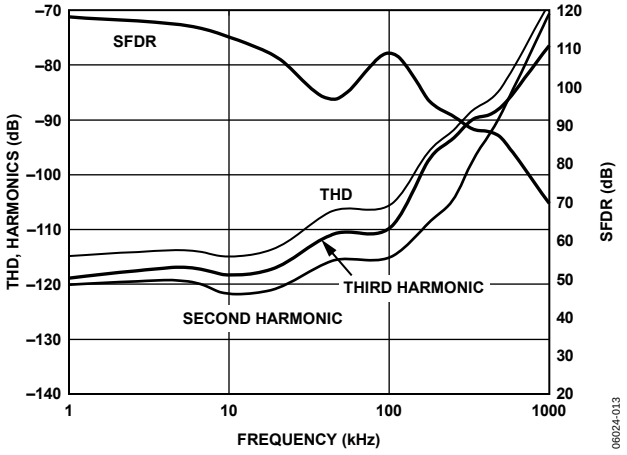


Figure 13. THD, Harmonics, and SFDR vs. Frequency

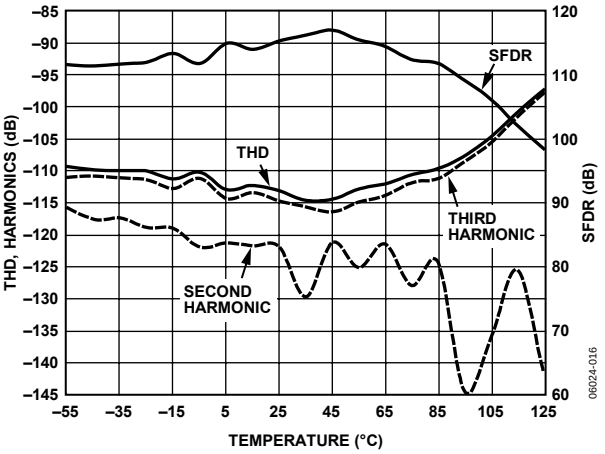


Figure 16. THD, Harmonics, and SFDR vs. Temperature

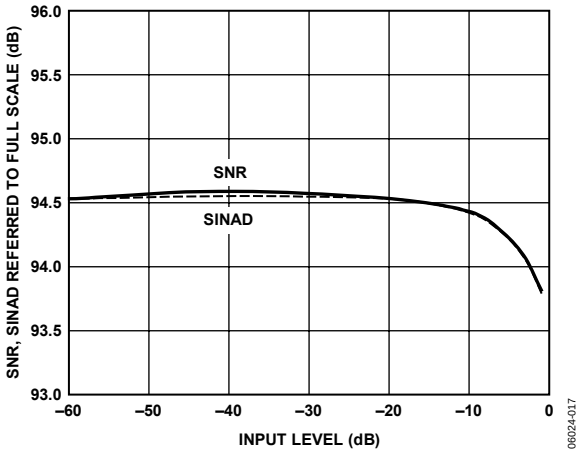


Figure 17. SNR and SINAD vs. Input Level (Referred to Full Scale)

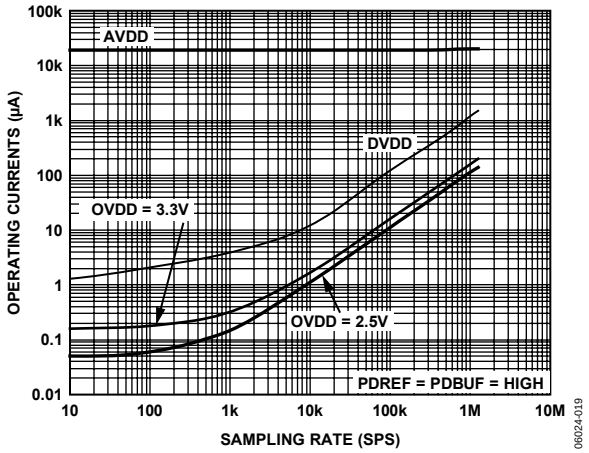


Figure 19. Operating Current vs. Sampling Rate

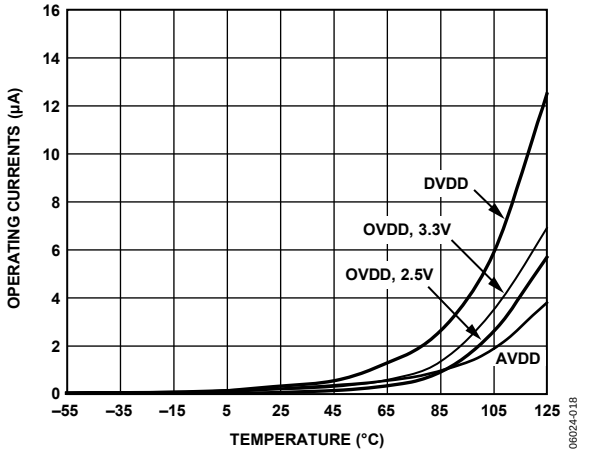


Figure 18. Power-Down Operating Currents vs. Temperature

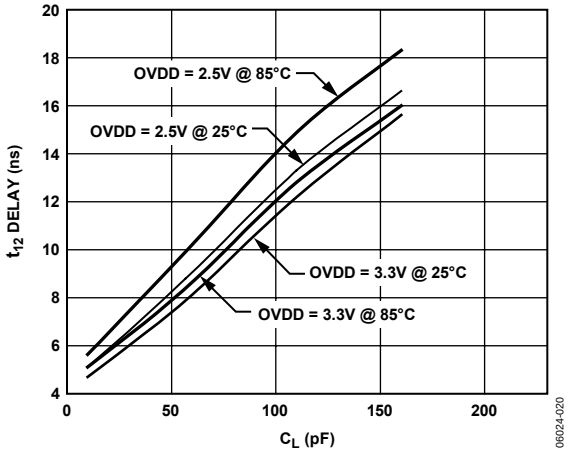


Figure 20. Typical Delay vs. Load Capacitance C_L

APPLICATIONS INFORMATION

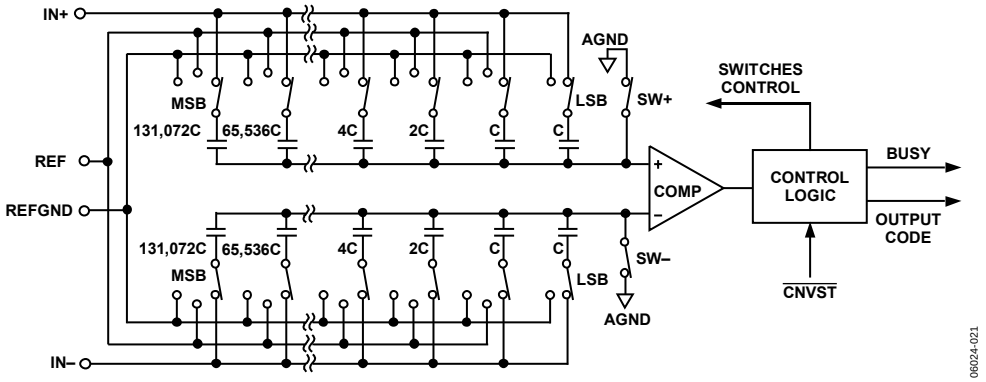


Figure 21. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7643 is a very fast, low power, single-supply, precise 18-bit ADC using successive approximation architecture. The AD7643 is capable of converting 1,250,000 samples per second (1.25 MSPS).

The AD7643 provides the user with an on-chip, track-and-hold, successive approximation ADC that does not exhibit any pipeline or latency, making it ideal for multiple multiplexed channel applications.

The AD7643 can operate from a single 2.5 V supply and interface to either 5 V, 3.3 V, or 2.5 V digital logic. It is housed in a Pb-free, 48-lead LQFP package or a tiny 48-lead LFCSP package, which combines space savings with flexibility and allows the AD7643 to be configured as either a serial or a parallel interface. The AD7643 is pin-to-pin compatible with the AD7641 and is a speed upgrade of the AD7674, AD7678, and AD7679.

CONVERTER OPERATION

The AD7643 is a successive approximation ADC based on a charge redistribution DAC. Figure 21 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors that are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to AGND via SW+ and SW−. All independent switches are connected to the analog inputs. Therefore, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN− inputs. A conversion phase is initiated once the acquisition phase is complete and the $\overline{\text{CNVST}}$ input goes low. When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the REFGND input. Therefore, the differential voltage between the inputs (IN+ and IN−) captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between REFGND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ through $V_{REF}/262144$). The control logic toggles these switches, starting with the MSB first, to bring the comparator back into a balanced condition. After the completion of this process, the control logic generates the ADC output code and brings BUSY output low.

TRANSFER FUNCTIONS

Using the OB/$\overline{2C}$ digital input, except in 18-bit interface mode, the AD7643 offers two output codings: straight binary and twos complement. The LSB size with V_{REF} = 2.048 V is 2 × V_{REF}/262,144, which is 15.623 µV. Refer to Figure 22 and Table 8 for the ideal transfer characteristic.

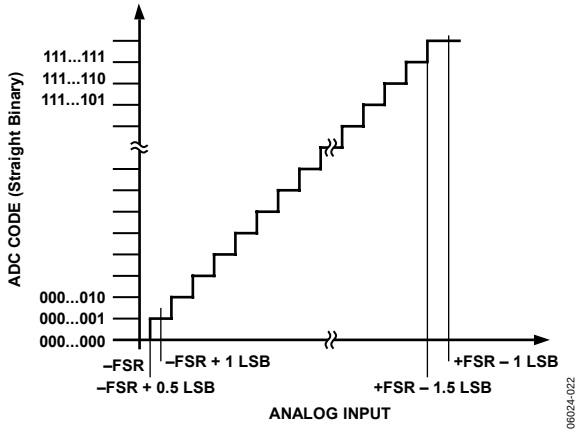


Figure 22. ADC Ideal Transfer Function

Table 8. Output Codes and Ideal Input Voltages

Description	Analog Input V_{REF} = 2.048 V	Digital Output Code (Hex)	
		Straight Binary	Twos Complement
FSR –1 LSB	+2.0479844 V	0x3FFFF[1]	0x1FFFF[1]
FSR – 2 LSB	+2.0479688 V	0x3FFFE	0x1FFFE
Midscale + 1 LSB	+15.625 µV	0x20001	0x00001
Midscale	0 V	0x20000	0x00000
Midscale – 1 LSB	–15.625 µV	0x1FFFF	0x3FFFF
–FSR + 1 LSB	–2.0479844 V	0x00001	0x20001
–FSR	–2.048 V	0x00000[2]	0x20000[2]

[1] This is also the code for overrange analog input (V_{IN+} – V_{IN-} above +V_{REF} – V_{REFGND}).
[2] This is also the code for underrange analog input (V_{IN+} – V_{IN-} below –V_{REF} + V_{REFGND}).

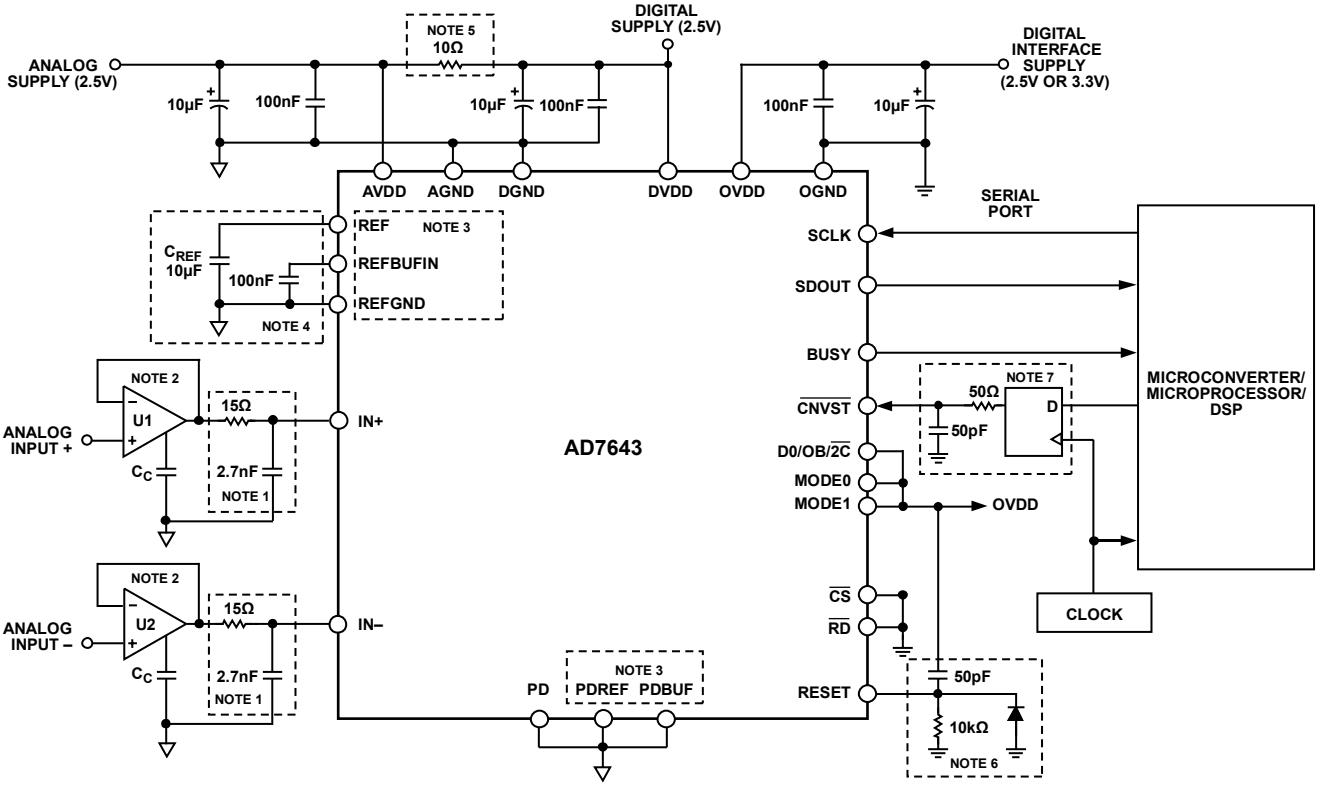


Figure 23. Typical Connection Diagram

TYPICAL CONNECTION DIAGRAM

Figure 23 shows a typical connection diagram for the AD7643. Different circuitry shown in this diagram is optional and is discussed in the following sections.

ANALOG INPUTS

Figure 24 shows an equivalent circuit of the input structure of the AD7643.

The two diodes, D_1 and D_2, provide ESD protection for the analog inputs IN+ and IN−. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V, because this causes the diodes to become forward-biased and to start conducting current. These diodes can handle a forward-biased current of 100 mA maximum. For instance, these conditions could eventually occur when the input buffer's U1 or U2 supplies are different from AVDD. In such a case, an input buffer with a short-circuit current limitation can be used to protect the part.

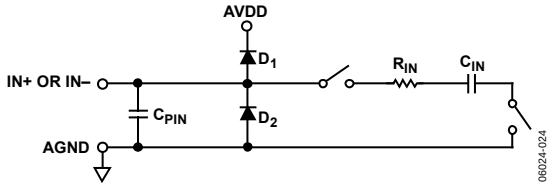


Figure 24. AD7643 Simplified Analog Input

The analog input of the AD7643 is a true differential structure. By using this differential input, small signals common to both inputs are rejected, as shown in Figure 25, representing the typical CMRR over frequency with internal and external references.

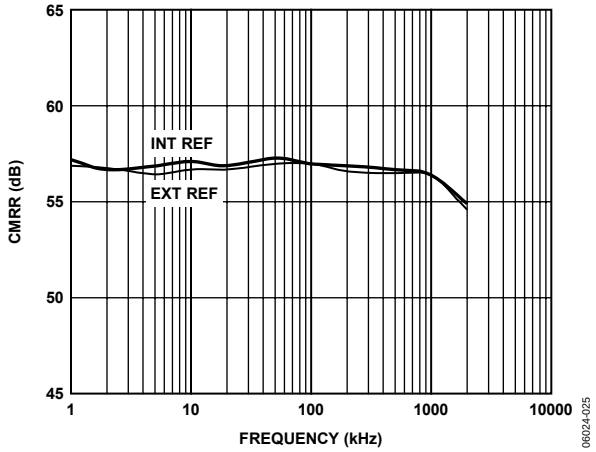


Figure 25. Analog Input CMRR vs. Frequency

During the acquisition phase for ac signals, the impedance of the analog inputs, IN+ and IN−, can be modeled as a parallel combination of capacitor C_{PIN} and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 175 Ω and is a lumped component comprised of some serial resistors and the on resistance of the switches. C_{IN} is typically 12 pF and is mainly the ADC sampling capacitor. During the conversion phase, when the switches are opened, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} make a 1-pole, low-pass filter that has a typical −3 dB cutoff frequency of 50 MHz, thereby reducing an undesirable aliasing effect and limiting the noise coming from the inputs.

Because the input impedance of the AD7643 is very high, the AD7643 can be driven directly by a low impedance source without gain error. To further improve the noise filtering achieved by the AD7643's analog input circuit, an external 1-pole RC filter between the amplifier's outputs and the ADC analog inputs can be used, as shown in Figure 23. However, large source impedances significantly affect the ac performance, especially the total harmonic distortion (THD). The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency, as shown in Figure 26.

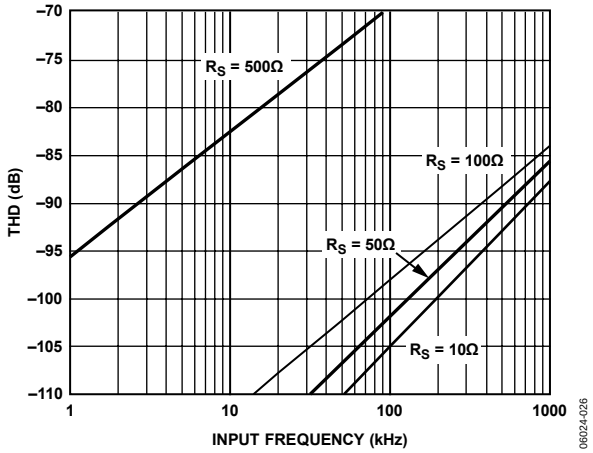


Figure 26. THD vs. Analog Input Frequency and Source Resistance

MULTIPLEXED INPUTS

When using the full 1.25 MSPS throughput in multiplexed applications for a full-scale step, the RC filter, as shown in Figure 23, does not settle in the required acquisition time, t_8. These values are chosen to optimize the best SNR performance of the AD7643. To use the full 1.25 MSPS throughput in multiplexed applications, the RC should be adjusted to satisfy t_8 (which is ~ 8.5 × RC time constant). However, lowering R and C increases the RC filter bandwidth and allows more noise into the AD7643, which degrades SNR. To preserve the SNR performance in these applications using the RC filter shown in Figure 23, the AD7643 should be run with $t_8 > 350$ ns; or approximately $1/(t_7 + t_8) \sim 1.12$ MSPS.

DRIVER AMPLIFIER CHOICE

Although the AD7643 is easy to drive, the driver amplifier needs to meet the following requirements:

- For multichannel, multiplexed applications, the driver amplifier and the AD7643 analog input circuit must be able to settle for a full-scale step of the capacitor array at an 18-bit level (0.0004%). In the amplifier's data sheet, settling at 0.1% to 0.01% is more commonly specified. This could differ significantly from the settling time at an 18-bit level and should be verified prior to driver selection. The AD8021 op amp, which combines ultralow noise and high gain bandwidth, meets this settling time requirement even when used with gains up to 13.
- The noise generated by the driver amplifier needs to be kept as low as possible to preserve the SNR and transition noise performance of the AD7643. The noise coming from the driver is filtered by the AD7643 analog input circuit 1-pole, low-pass filter made by R_{IN} and C_{IN} or by the external filter, if one is used. The SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20\log\left(\frac{30}{\sqrt{900 + \frac{\pi f_{-3dB}}{2}(Ne_{N+})^2 + \frac{\pi f_{-3dB}}{2}(Ne_{N-})^2}}\right)$$

where:

f_{-3dB} is the input bandwidth of the AD7643 (50 MHz) or the cutoff frequency of the input RC filter shown in Figure 23 (3.9 MHz), if one is used.

N is the noise factor of the amplifier (1 in buffer configuration).

e_{N+} and e_{N-} are the equivalent input voltage noise densities of the op amps connected to IN+ and IN−, in nV/√Hz. This approximation can be used when the resistances used around the amplifier are small. If larger resistances are used, their noise contributions should also be root-sum squared.

For instance, when using op amps with an equivalent input noise density of 2.1 nV/√Hz, such as the AD8021, with a noise gain of 1 when configured as a buffer, degrades the SNR by only 0.25 dB when using the RC filter in Figure 23, and by 2.5 dB without it.

- The driver needs to have a THD performance suitable to that of the AD7643. Figure 13 gives the THD vs. frequency that the driver should exceed.

The AD8021 meets these requirements and is appropriate for almost all applications. The AD8021 needs a 10 pF external compensation capacitor that should have good linearity as an NPO ceramic or mica type. Moreover, the use of a noninverting 1 gain arrangement is recommended and helps to obtain the best signal-to-noise ratio.

The AD8022 can also be used when a dual version is needed and a gain of 1 is present. The AD829 is an alternative in applications where high frequency (above 100 kHz) performance is not required. In applications with a gain of 1, an 82 pF compensation capacitor is required. The AD8610 is an option when low bias current is needed in low frequency applications.

Single-to-Differential Driver

For applications using unipolar analog signals, a single-ended-to-differential driver, as shown in Figure 27, allows for a differential input into the part. This configuration, when provided an input signal of 0 to V_{REF}, produces a differential $\pm V_{REF}$ with midscale at $V_{REF}/2$. The 1-pole filter using R = 15 Ω and C = 2.7 nF provides a corner frequency of 3.9 MHz.

If the application can tolerate more noise, the AD8139 differential driver can be used.

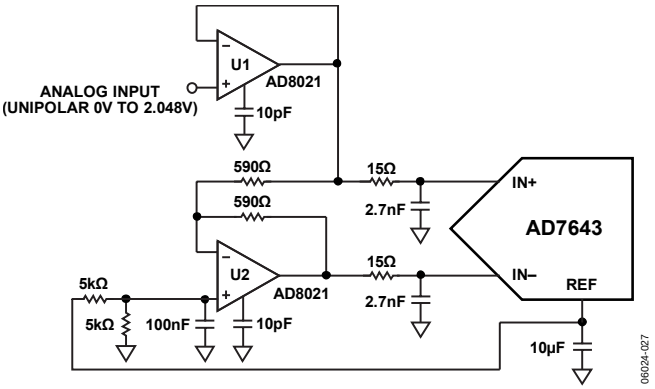


Figure 27. Single-Ended-to-Differential Driver Circuit (Internal Reference Buffer Used)

VOLTAGE REFERENCE INPUT

The AD7643 allows the choice of either a very low temperature drift internal voltage reference, an external 1.2 V reference that can be buffered using the internal reference buffer, or an external reference.

Unlike many ADCs with internal references, the internal reference of the AD7643 provides excellent performance and can be used in almost all applications.

Internal Reference (PDBUF = Low, PDREF = Low)

To use the internal reference, the PDREF and PDBUF inputs must both be low. This produces a 1.2 V band gap output on REFBUFIN, which is amplified by the internal buffer and results in a 2.048 V reference on the REF pin.

The internal reference is temperature compensated to 2.048 V ± 10 mV. The reference is trimmed to provide a typical drift of 8 ppm/°C. This typical drift characteristic is shown in Figure 7.

The output resistance of REFBUFIN is 6.33 kΩ (minimum) when the internal reference is enabled. It is necessary to decouple this with a ceramic capacitor greater than 100 nF. Therefore, the capacitor provides an RC filter for noise reduction.

Because the output impedance of REFBUFIN is typically 6.33 kΩ, relative humidity (among other industrial contaminates) can directly affect the drift characteristics of the reference. Typically, a guard ring is used to reduce the effects of drift under such circumstances. However, because the AD7643 has a fine lead pitch, guarding this node is not practical. Therefore, in these industrial and other types of applications, it is recommended to use a conformal coating, such as Dow Corning® 1-2577 or HumiSeal® 1B73.

External 1.2 V Reference and Internal Buffer (PDBUF = Low, PDREF = High)

To use an external reference along with the internal buffer, PDREF should be high and PDBUF should be low. This powers down the internal reference and allows an external 1.2 V reference to be applied to REFBUFIN, producing 2.048 V (typically) on the REF pin.

External 2.5 V Reference (PDBUF = High, PDREF = High)

To use an external 2.5 V reference directly on the REF pin, PDREF and PDBUF should both be high.

For improved drift performance, an external reference, such as the AD780 or ADR431, can be used. The advantages of directly using the external voltage reference are:

- The SNR and dynamic range improvement (about 1.7 dB) resulting from the use of a reference voltage very close to the supply (2.5 V) instead of a typical 2.048 V reference when the internal reference is used. This is calculated by

$$SNR = 20\log\left(\frac{2.048}{2.50}\right)$$

- The power savings when the internal reference is powered down (PDREF high).

PDREF and PDBUF power down the internal reference and the internal reference buffer, respectively. The input current of PDREF and PDBUF should never exceed 20 mA. This can occur when the driving voltage is above AVDD (for instance, at power-up). In this case, a 125 Ω series resistor is recommended.

Reference Decoupling

Whether using an internal or external reference, the AD7643 voltage reference input (REF) has a dynamic input impedance; therefore, it should be driven by a low impedance source with efficient decoupling between the REF and REFGND inputs. This decoupling depends on the choice of the voltage reference but usually consists of a low ESR capacitor connected to REF and REFGND with minimum parasitic inductance.

A 10 µF (X5R, 1206 size) ceramic chip capacitor (or 47 µF tantalum capacitor) is appropriate when using either the internal reference or one of the recommended reference voltages.

The placement of the reference decoupling is also important to the performance of the AD7643. The decoupling capacitor should be mounted on the same side as the ADC right at the REF pin with a thick PCB trace. The REFGND should also connect to the reference decoupling capacitor with the shortest distance.

For applications that use multiple AD7643 devices, it is more effective to use an external reference with the internal reference buffer to buffer the reference voltage. However, because the reference buffers are not unity gain, ratiometric, simultaneously sampled designs should use an external reference and external buffer, such as the AD8031/AD8032; therefore, preserving the same reference level for all converters.

The voltage reference temperature coefficient (TC) directly impacts full scale; therefore, in applications where full-scale accuracy matters, care must be taken with the TC. For instance, a ±4 ppm/°C TC of the reference changes full scale by ±1 LSB/°C.

Note that V_{REF} can be increased to AVDD + 0.1 V. Because the input range is defined in terms of V_{REF}, this would essentially increase the range to 0 V to 2.8 V with an AVDD = 2.7 V.

Temperature Sensor

The TEMP pin measures the temperature of the AD7643. To improve the calibration accuracy over the temperature range, the output of the TEMP pin is applied to one of the inputs of the analog switch (such as, ADG779), and the ADC itself is used to measure its own temperature. This configuration is shown in Figure 28.

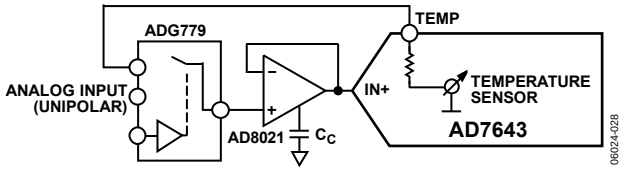


Figure 28. Use of the Temperature Sensor

POWER SUPPLY

The AD7643 uses three sets of power supply pins: an analog 2.5 V supply AVDD, a digital 2.5 V core supply DVDD, and a digital input/output interface supply OVDD. The OVDD supply allows direct interface with any logic working between 2.3 V and 5.25 V. To reduce the number of supplies needed, the digital core (DVDD) can be supplied through a simple RC filter from the analog supply, as shown in Figure 23.

Power Sequencing

The AD7643 is independent of power supply sequencing and thus free from supply induced voltage latch-up. In addition, it is insensitive to power supply variations over a wide frequency range, as shown in Figure 29.

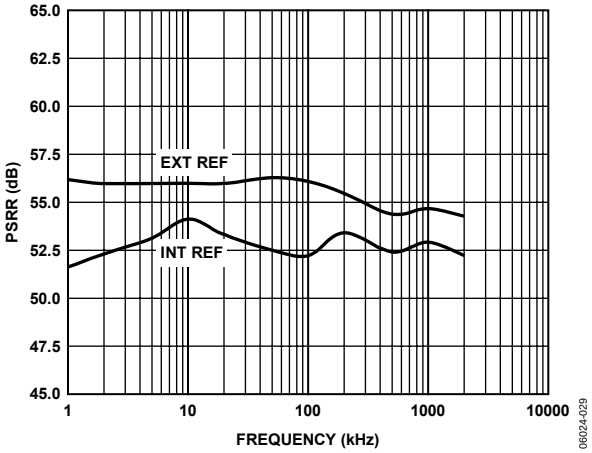


Figure 29. PSRR vs. Frequency

Power-Up

At power-up, or when returning to operational mode from the power-down mode (PD = high), the AD7643 engages an initialization process. During this time, the first 128 conversions should be ignored or the RESET input could be pulsed to engage a faster initialization process. Refer to the Digital Interface section for RESET and timing details.

A simple power-on reset circuit, as shown in Figure 23, can be used to minimize the digital interface. As OVDD powers up, the capacitor is shorted and brings RESET high; it is then charged returning RESET to low. However, this circuit only works when powering up the AD7643 because the power-down mode (PD = high) does not power down any of the supplies and as a result, RESET is low.

It should be noted that the digital interface remains active even during the acquisition phase. To reduce the operating digital supply currents even further, drive the digital inputs close to the power rails (that is, OVDD and OGND).

CONVERSION CONTROL

The AD7643 is controlled by the $\overline{\text{CNVST}}$ input. A falling edge on $\overline{\text{CNVST}}$ is all that is necessary to initiate a conversion. Detailed timing diagrams of the conversion process are shown in Figure 30. Once initiated, it cannot be restarted or aborted, even by the power-down input, PD, until the conversion is complete. The $\overline{\text{CNVST}}$ signal operates independently of $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals.

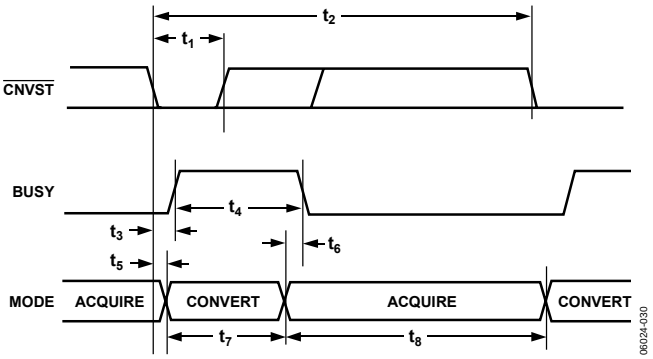


Figure 30. Basic Conversion Timing

For optimal performance, the rising edge of $\overline{\text{CNVST}}$ should not occur after the maximum $\overline{\text{CNVST}}$ low time, t_1, or until the end of conversion.

Although $\overline{\text{CNVST}}$ is a digital signal, it should be designed with special care with fast, clean edges and levels with minimum overshoot and undershoot or ringing.

The $\overline{\text{CNVST}}$ trace should be shielded with ground and a low value serial resistor (for example, 50 Ω) termination should be added close to the output of the component that drives this line. In addition, a 50 pF capacitor is recommended to further reduce the effects of overshoot and undershoot as shown in Figure 23.

For applications where SNR is critical, the $\overline{\text{CNVST}}$ signal should have very low jitter. This can be achieved by using a dedicated oscillator for $\overline{\text{CNVST}}$ generation, or by clocking $\overline{\text{CNVST}}$ with a high frequency, low jitter clock, as shown in Figure 23.

INTERFACES

DIGITAL INTERFACE

The AD7643 has a versatile digital interface that can be set up as either a serial or a parallel interface with the host system. The serial interface is multiplexed on the parallel data bus. The AD7643 digital interface also accommodates 2.5 V, 3.3 V, or 5 V logic with either OVDD at 2.5 V or 3.3 V. OVDD defines the logic high output voltage. In most applications, the OVDD supply pin of the AD7643 is connected to the host system interface 2.5 V or 3.3 V digital supply. By using the D0/OB/$\overline{2C}$ input pin, either twos complement or straight binary coding can be used.

The two signals $\overline{CS}$ and $\overline{RD}$ control the interface. When at least one of these signals is high, the interface outputs are in high impedance. Usually, $\overline{CS}$ allows the selection of each AD7643 in multicircuit applications and is held low in a single AD7643 design. $\overline{RD}$ is generally used to enable the conversion result on the data bus.

RESET

The RESET input is used to reset the AD7643 and generate a fast initialization. A rising edge on RESET aborts the current conversion (if any) and tristates the data bus. The falling edge of RESET clears the data bus and engages the initialization process indicated by pulsing BUSY high. Conversions can take place after the falling edge of BUSY. Refer to Figure 31 for the RESET timing details.

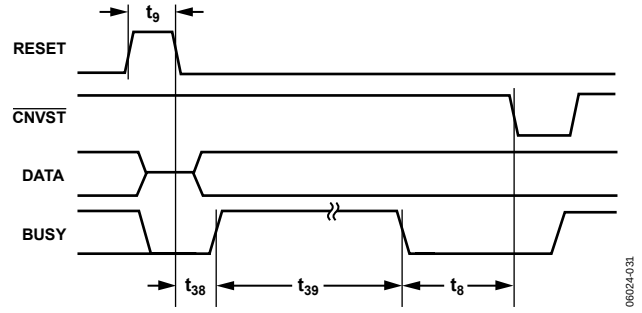


Figure 31. RESET Timing

PARALLEL INTERFACE

The AD7643 is configured to use the parallel interface for an 18-bit, 16-bit, or 8-bit bus width according to Table 7.

Master Parallel Interface

Data can be continuously read by tying $\overline{CS}$ and $\overline{RD}$ low, thus requiring minimal microprocessor connections. However, in this mode, the data bus is always driven and cannot be used in shared bus applications, unless the device is held in RESET. Figure 32 details the timing for this mode.

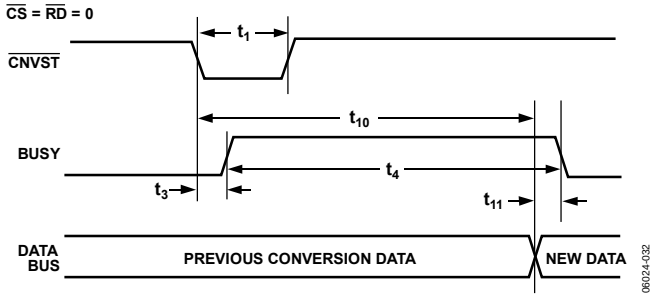


Figure 32. Master Parallel Data Timing for Reading (Continuous Read)

Slave Parallel Interface

In slave parallel reading mode, the data can be read either after each conversion, which is during the next acquisition phase, or during the following conversion, as shown in Figure 33 and Figure 34, respectively. When the data is read during the conversion, it is recommended that it is read-only during the first half of the conversion phase. This avoids any potential feedthrough between voltage transients on the digital interface and the most critical analog conversion circuitry.

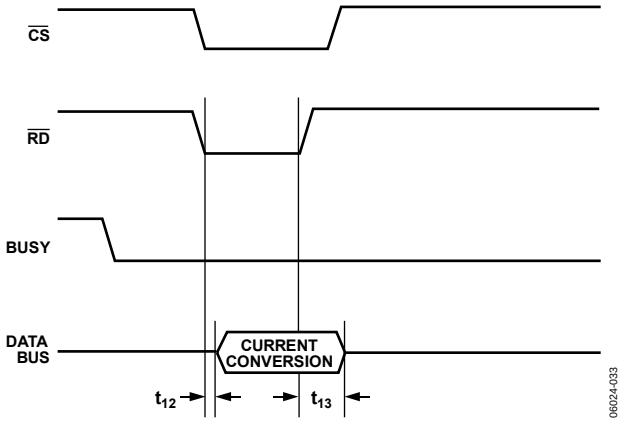


Figure 33. Slave Parallel Data Timing for Reading (Read After Convert)

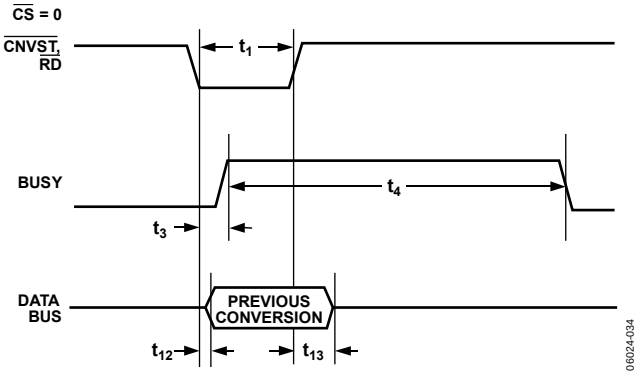


Figure 34. Slave Parallel Data Timing for Reading (Read During Convert)

16-Bit and 8-Bit Interface (Master or Slave)

In the 16-bit (MODE[1:0] = 1) and 8-bit (MODE[1:0] = 2) interfaces, the A0/A1 pins allow a glueless interface to a 16- or 8-bit bus, as shown in Figure 35. By connecting A0/A1 to an address line(s), the data can be read in two words for a 16-bit interface, or three bytes for an 8-bit interface. This interface can be used in both master and slave parallel reading modes. Refer to Table 7 for the full details of the interface.

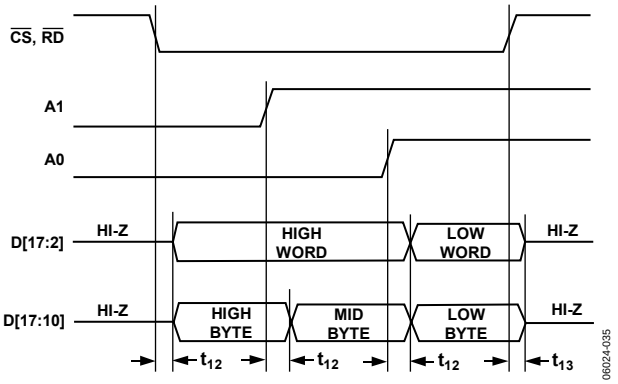


Figure 35. 8-Bit and 16-Bit Parallel Interface

SERIAL INTERFACE

The AD7643 is configured to use the serial interface when MODE[1:0] = 3. The AD7643 outputs 18 bits of data, MSB first, on the SDOUT pin. This data is synchronized with the 18 clock pulses provided on the SCLK pin. The output data is valid on both the rising and falling edge of the data clock.

MASTER SERIAL INTERFACE

Internal Clock

The AD7643 is configured to generate and provide the serial data clock SCLK when the EXT/$\overline{\text{INT}}$ pin is held low. The AD7643 also generates a SYNC signal to indicate to the host when the serial data is valid. The serial clock SCLK and the SYNC signal can be inverted. Depending on the read during convert input, RDC/SDIN, the data can be read after each conversion or during the following conversion. Figure 36 and Figure 37 show detailed timing diagrams of these two modes.

Usually, because the AD7643 is used with a fast throughput, the master read during conversion mode is the most recommended serial mode. In this mode, the serial clock and data toggle at appropriate instants, minimizing potential feedthrough between digital activity and critical conversion decisions. In this mode, the SCLK period changes because the LSBs require more time to settle and the SCLK is derived from the SAR conversion cycle.

In read after conversion mode, it should be noted that unlike other modes, the BUSY signal returns low after the 18 data bits are pulsed out and not at the end of the conversion phase, resulting in a longer BUSY width. As a result, the maximum throughput cannot be achieved in this mode.

In addition, in read after convert mode, the SCLK frequency can be slowed down to accommodate different hosts using the DIVSCLK[1:0] inputs. Refer to Table 4 for the SCLK timing details when using these inputs.

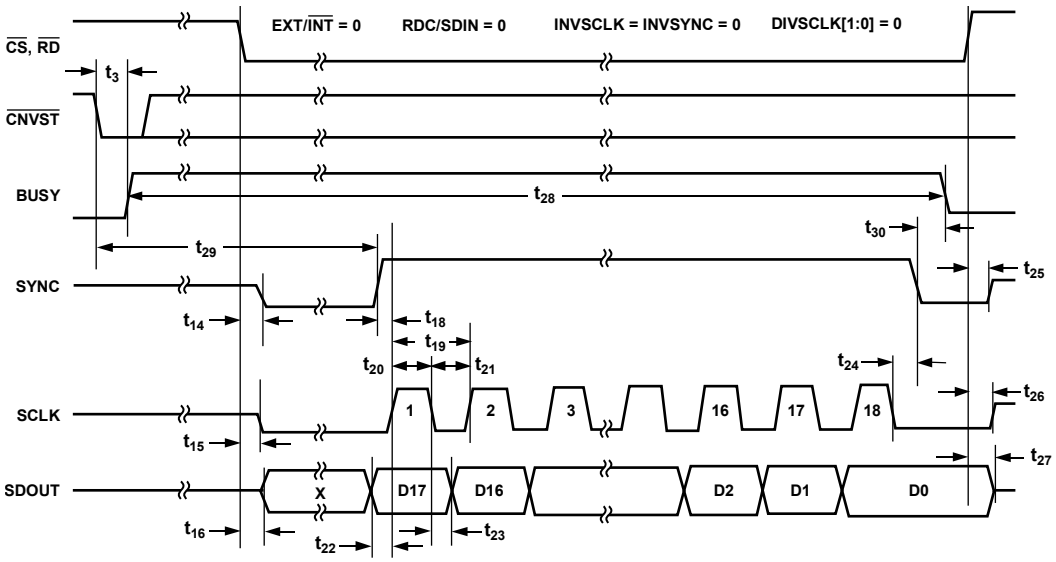


Figure 36. Master Serial Data Timing for Reading (Read After Convert)

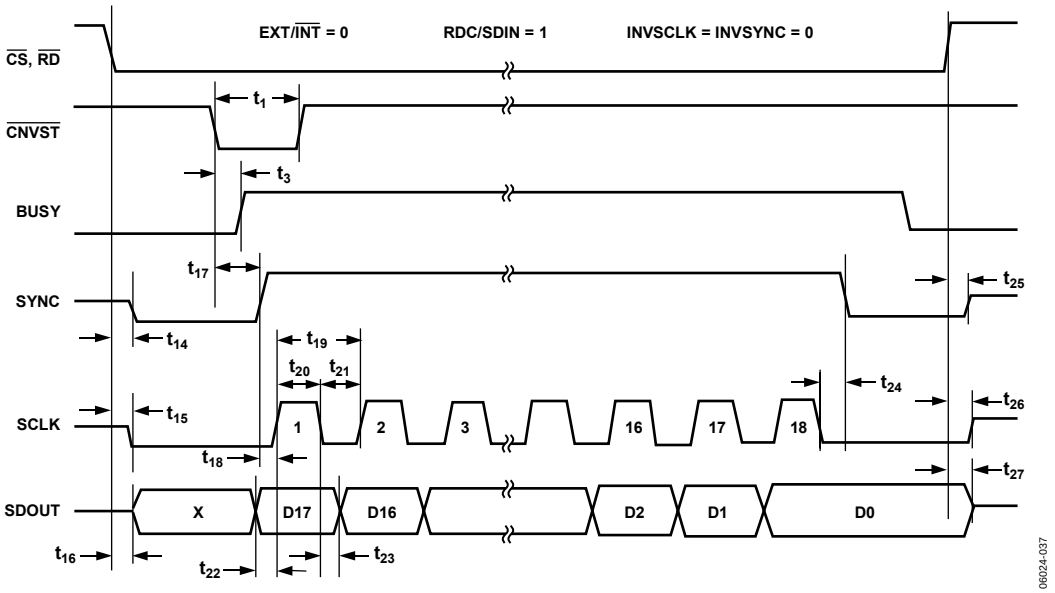


Figure 37. Master Serial Data Timing for Reading (Read Previous Conversion During Convert)

SLAVE SERIAL INTERFACE

External Clock

The AD7643 is configured to accept an externally supplied serial data clock on the SCLK pin when the EXT/$\overline{\text{INT}}$ pin is held high. In this mode, several methods can be used to read the data. The external serial clock is gated by $\overline{\text{CS}}$. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both low, the data can be read after each conversion or during the following conversion. The external clock can be either a continuous or a discontinuous clock. A discontinuous clock can be either normally high or normally low when inactive. Figure 39 and Figure 40 show the detailed timing diagrams of these methods.

While the AD7643 is performing a bit decision, it is important that voltage transients be avoided on digital input/output pins or degradation of the conversion result could occur. This is particularly important during the second half of the conversion phase because the AD7643 provides error correction circuitry that can correct for an improper bit decision made during the first half of the conversion phase. For this reason, it is recommended that when an external clock is being provided, a discontinuous clock is toggled only when BUSY is low or, more importantly, that it does not transition during the latter half of BUSY high.

External Discontinuous Clock Data Read After Conversion

Figure 39 shows the detailed timing diagrams of this method. After a conversion is complete, indicated by BUSY returning low, the conversion result can be read while both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low. Data is shifted out MSB first with 18 clock pulses and is valid on the rising and falling edges of the clock.

Among the advantages of this method is the fact that conversion performance is not degraded because there are no voltage transients on the digital interface during the conversion process. Another advantage is the ability to read the data at any speed up to 80 MHz, which accommodates both the slow digital host interface and the fast serial reading.

It is also possible to begin to read data after conversion and continue to read the last bits after a new conversion is initiated. In this reading mode, it is recommended to pause digital activity just prior to initiating a conversion (SCLK should be held high or low). Once the conversion has begun, the reading can continue. Also, in this mode, the use of a slower clock speed can be used to read the data because the total reading time is the acquisition time, t_8 + half of the conversion time, t_7 ($t_8 + ½ \times t_7$, see the External Clock Data Read During Previous Conversion section).

Finally, in this mode only, the AD7643 provides a daisy-chain feature using the RDC/SDIN pin for cascading multiple converters together. This feature is useful for reducing component count and wiring connections when desired, as, for instance, in isolated multiconverter applications.

An example of the concatenation of two devices is shown in Figure 38. Simultaneous sampling is possible by using a common $\overline{\text{CNVST}}$ signal. It should be noted that the RDC/SDIN input is latched on the edge of SCLK opposite to the one used to shift out the data on SDOUT. Therefore, the MSB of the upstream converter just follows the LSB of the downstream converter on the next SCLK cycle.

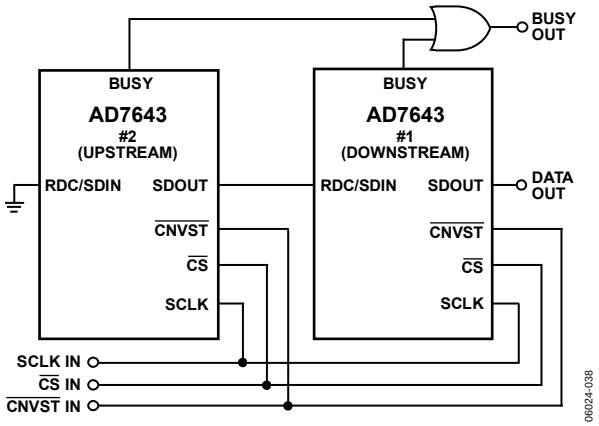


Figure 38. Two AD7643 Devices in a Daisy-Chain Configuration

External Clock Data Read During Previous Conversion

Figure 40 shows the detailed timing diagrams of this method. During a conversion, while $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both low, the result of the previous conversion can be read. The data is shifted out, MSB first, with 18 clock pulses and is valid on both the rising and falling edge of the clock. The 18 bits have to be read before the current conversion is complete; otherwise, RDERROR is pulsed high and can be used to interrupt the host interface to prevent incomplete data reading. There is no daisy-chain feature in this mode, and the RDC/SDIN input should always be tied either high or low.

To reduce performance degradation due to digital activity, a fast discontinuous clock of at least 67 MHz is recommended to ensure that all the bits are read during the first half of the SAR conversion phase, t_7, because the ADC can correct for errors introduced by digital activity during this time.

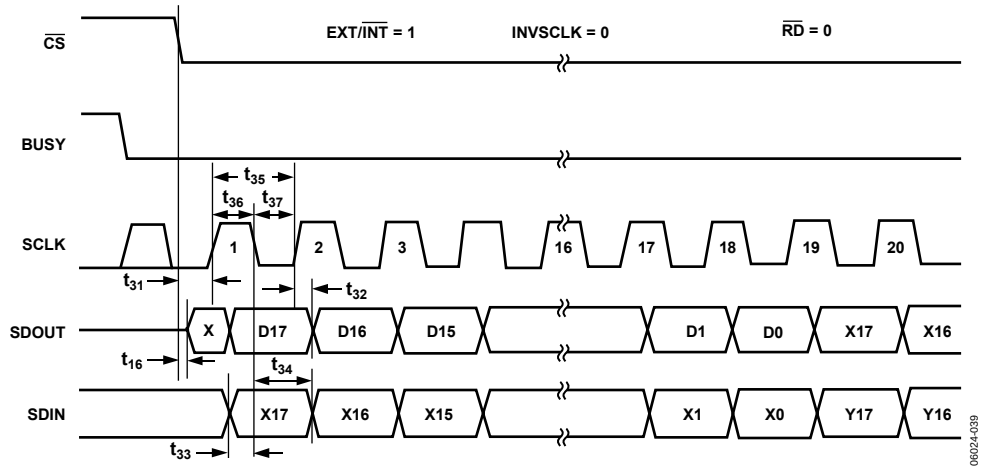


Figure 39. Slave Serial Data Timing for Reading (Read After Convert)

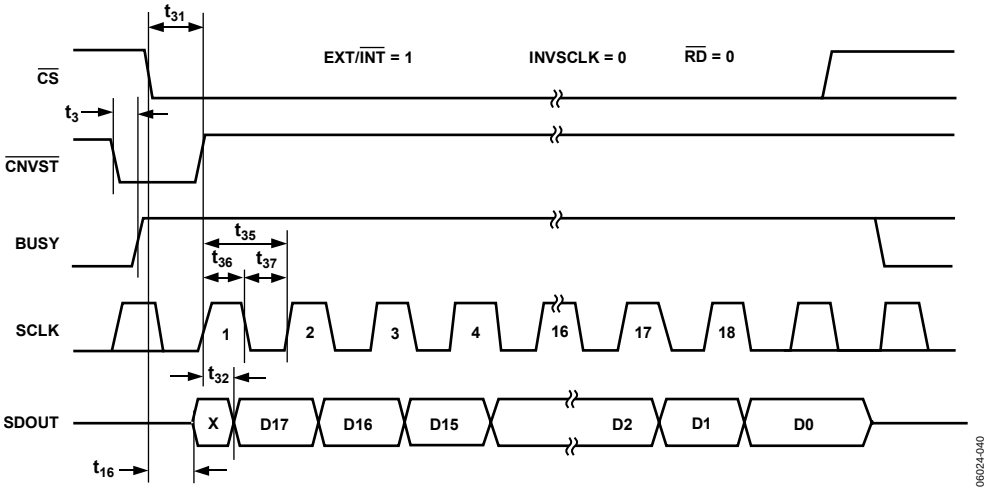


Figure 40. Slave Serial Data Timing for Reading (Read Previous Conversion During Convert)

MICROPROCESSOR INTERFACING

The AD7643 is ideally suited for traditional dc measurement applications supporting a microprocessor, and ac signal processing applications interfacing to a digital signal processor. The AD7643 is designed to interface with a parallel 8-bit or 16-bit wide interface or with a general-purpose serial port or I/O ports on a microcontroller. A variety of external buffers can be used with the AD7643 to prevent digital noise from coupling into the ADC. The SPI Interface (ADSP-219x) section illustrates the use of the AD7643 with the ADSP-219x SPI-equipped DSP.

SPI Interface (ADSP-219x)

Figure 41 shows an interface diagram between the AD7643 and an SPI-equipped DSP, the ADSP-219x. To accommodate the slower speed of the DSP, the AD7643 acts as a slave device and data must be read after conversion. This mode also allows the daisy-chain feature. The convert command can be initiated in response to an internal timer interrupt. The 18-bit output data are read with three SPI byte access. The reading process can be initiated in response to the end-of-conversion signal (BUSY going low) using an interrupt line of the DSP. The serial peripheral interface (SPI) on the ADSP-219x is configured for master mode (MSTR) = 1, clock polarity bit (CPOL) = 0, clock phase bit (CPHA) = 1, and the SPI interrupt enable (TIMOD) = 00 by writing to the SPI control register (SPICLTx). It should be noted that to meet all timing requirements, the SPI clock should be limited to 17 Mbps, allowing it to read an ADC result in less than 1 µs. When a higher sampling rate is desired, it is recommended to use one of the parallel interface modes.

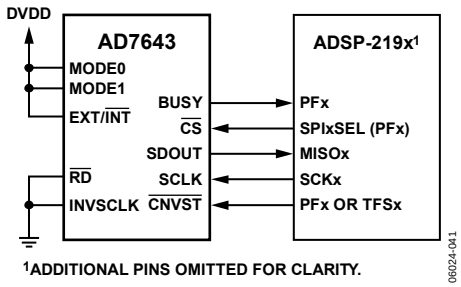


Figure 41. Interfacing the AD7643 to ADSP-219x

APPLICATION HINTS

LAYOUT

While the AD7643 has very good immunity to noise on the power supplies, exercise care with the grounding layout. To facilitate the use of ground planes that can be easily separated, design the printed circuit board that houses the AD7643 so that the analog and digital sections are separated and confined to certain areas of the board. Digital and analog ground planes should be joined in only one place, preferably underneath the AD7643, or as close as possible to the AD7643. If the AD7643 is in a system where multiple devices require analog-to-digital ground connections, the connections should still be made at one point only, a star ground point, established as close as possible to the AD7643.

To prevent coupling noise onto the die, avoid radiating noise, and reduce feedthrough:

- Do not run digital lines under the device.
- Run the analog ground plane under the AD7643.
- Shield fast switching signals, like $\overline{\text{CNVST}}$ or clocks, with digital ground to avoid radiating noise to other sections of the board, and never run them near analog signal paths.
- Avoid crossover of digital and analog signals.
- Run traces on different but close layers of the board, at right angles to each other, to reduce the effect of feedthrough through the board.

The power supply lines to the AD7643 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Good decoupling is also important to lower the impedance of the supplies presented to the AD7643, and to reduce the magnitude of the supply spikes. Decoupling ceramic capacitors, typically 100 nF, should be placed on each of the power supplies pins, AVDD, DVDD, and OVDD. The capacitors should be placed close to, and ideally right up against, these pins and their corresponding ground pins. Additionally, low ESR 10 µF capacitors should be located in the vicinity of the ADC to further reduce low frequency ripple.

The DVDD supply of the AD7643 can be either a separate supply or come from the analog supply, AVDD, or from the digital interface supply, OVDD. When the system digital supply is noisy, or fast switching digital signals are present, and no separate supply is available, it is recommended to connect the DVDD digital supply to the analog supply AVDD through an RC filter, and to connect the system supply to the interface digital supply OVDD and the remaining digital circuitry. Refer to Figure 23 for an example of this configuration. When DVDD is powered from the system supply, it is useful to insert a bead to further reduce high frequency spikes.

The AD7643 has four different ground pins: REFGND, AGND, DGND, and OGND. REFGND senses the reference voltage and, because it carries pulsed currents, should have a low impedance return to the reference. AGND is the ground to which most internal ADC analog signals are referenced; it must be connected with the least resistance to the analog ground plane. DGND must be tied to the analog or digital ground plane depending on the configuration. OGND is connected to the digital system ground.

The layout of the decoupling of the reference voltage is important. To minimize parasitic inductances, place the decoupling capacitor close to the ADC and connect it with short, thick traces.

EVALUATING THE AD7643 PERFORMANCE

A recommended layout for the AD7643 is outlined in the documentation of the EVAL-AD7643-CB evaluation board for the AD7643. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the EVAL-CONTROL BRD3.

OUTLINE DIMENSIONS

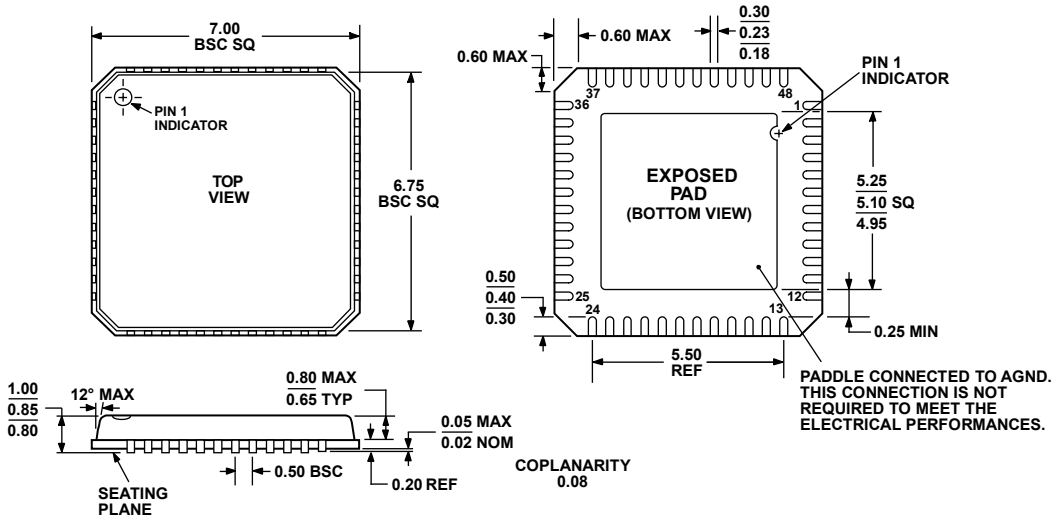


Figure 42. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm × 7 mm Body, Very Thin Quad (CP-48-1)
Dimensions shown in millimeters

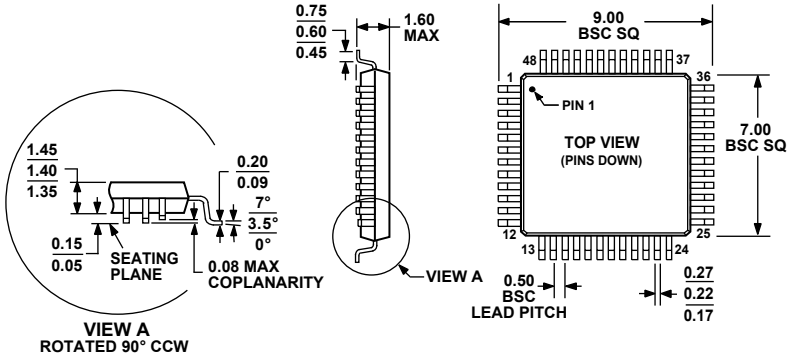


Figure 43. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7643BCPZ[1]	–40°C to +85°C	48-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-48-1
AD7643BCPZRL[1]	–40°C to +85°C	48-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-48-1
AD7643BSTZ[1]	–40°C to +85°C	48-Lead Low Profile Quad Flat Package (LQFP)	ST-48
AD7643BSTZRL[1]	–40°C to +85°C	48-Lead Low Profile Quad Flat Package (LQFP)	ST-48
EVAL-AD7643CB[2]		Evaluation Board	
EVAL-CONTROL BRD3[3]		Controller Board	

[1] Z = Pb-free part.
[2] This board can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BRD3 for evaluation/demonstration purposes.
[3] This board allows a PC to control and communicate with all Analog Devices, Inc. evaluation boards ending in the CB designators.

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