3.3V TO 18V MUX with Overcurrent Limit

Check for Samples: TPS22980

FEATURES

- **Powered From 3.3V**
- **4.5V to 19.8V High Voltage Switch**
- **3V to 3.6V Switch**
- **Adjustable Current Limit**
- **Thermal Shutdown**
- **Make Before Break Switch**
- **High Voltage Discharge Before Low Voltage Make**
- **Reverse Current Blocking**

APPLICATIONS

- **Notebook Computers**
- **Desktop Computers**
- **Power Management Systems**

DESCRIPTION

The TPS22980 is a current-limited power mux providing a connection to a peripheral device from either a low voltage supply (3.0V up to 3.6V) or a high voltage supply (5V up to 18V). The desired output is selected by digital control signals.

The high voltage (VHV) and low voltage (V3P3) switch current limits are set with external resistance. Once the current limit is reached, the TPS22980 will control the switch to maintain the current at the limit.

When the high voltage supply is not present, the TPS22980 will maintain the connection to the output from the low voltage supply. When a high voltage line and high voltage enable signal is detected by the device, the high voltage switch will be turned on in conjunction with the low voltage switch until a reverse current is detected by the low voltage switch. The low voltage switch is then disabled allowing a seamless transition from a low voltage to a high voltage supply with minimal drop and shoot-through current.

To prevent current backflow during a transition from a VHV connection to a V3P3 connection, the TPS22980 will break the VHV connection and discharge the output to approximately 3.3V. Once the output reaches 3.3V the device will connect V3P3 switch. If a load is present, the output will transition to 0V before returning to 3.3V.

The TPS22980 is available in a 4mm x 4mm x 1mm QFN package.

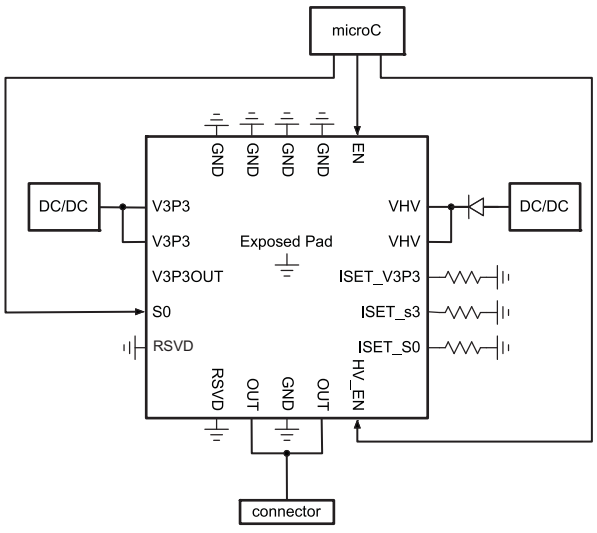


Figure 1. Typical Application

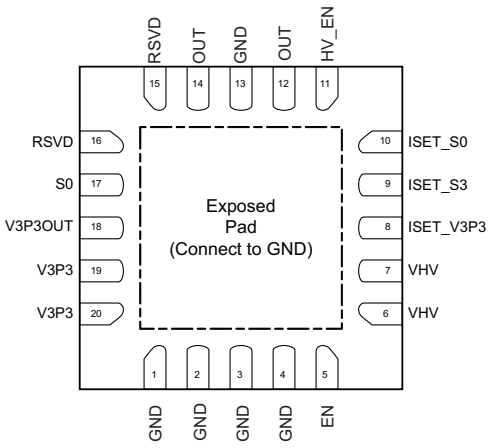
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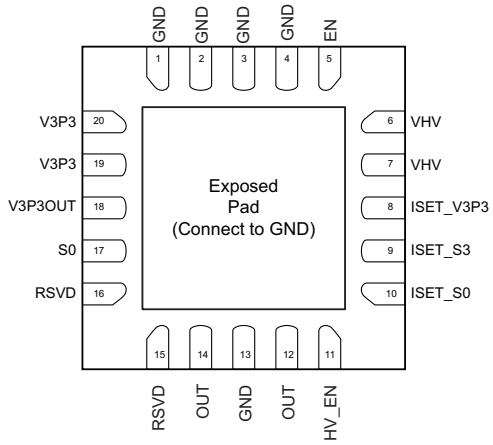
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TOP VIEW / FOOTPRINT



BOTTOM VIEW



Package Size: 4mm x 4mm x 1mm height, Pad Pitch: 0.5mm

PIN FUNCTIONS

PIN		DESCRIPTION
NO.	NAME	
1	GND	Device ground
2		
3		
4		
5	EN	Device Enable.
6	VHV	High voltage power supply input. Place a minimum of 0.1µF capacitor as close to this pin as possible.
7		
8	ISET_V3P3	Sets the current limit for V3P3. Place resistor between this pin and GND. See Equation 1 to calculate resistor value.
9	ISET_S3	Sets the current limit for VHV in S3 mode. Place resistor between this pin and GND. See Equation 1 to calculate resistor value.
10	ISET_S0	Sets the current limit for VHV in S0 mode. Place resistor between this pin and GND. See Equation 1 to calculate resistor value.
11	HV_EN	High voltage output enable.
12, 14	OUT	Power output. Place a minimum of 1µF capacitor as close to this pin as possible.
13	GND	Device ground.
15	RSVD	Reserved. Must Tie to GND.
16		
17	S0	When this pin is asserted, the device is put in S0 mode. Otherwise the device operates in S3 mode.
18	V3P3OUT	3.3V bypass output. Place a minimum of 0.1µF capacitor as close to this pin as possible.
19	V3P3	3.3V power supply input. Place a minimum of 0.1µF capacitor as close to this pin as possible.
20		
EP	GND	

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1) (2)

		VALUE	UNIT
V_I	Input voltage range on V3P3 (VDD)(3)	–0.3 to 3.6	V
	Input voltage range on EN, HVEN, ISET_V3P3, ISET_S0, ISET_S3, S0(3)	–0.3 to V3P3+0.3	
	Input voltage range on VHV(3)	–0.3 to 20	
	Output voltage range at OUT(3)	–0.3 to 20	
	Output voltage range at V3P3OUT(3)	–0.3 to V3P3+0.3	
T_A	Operating ambient temperature range	–40 to 85	°C
$T_{J\ (MAX)}$	Maximum operating junction temperature	110	°C
T_{stg}	Storage temperature range	–65 to 150	°C
ESD Rating	Charge Device Model (JESD 22 C101)	500	V
	Human Body Model (JESD 22 A114)	2	kV

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$
(3) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS22980 RGP 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	38.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	30.7	
θ_{JB}	Junction-to-board thermal resistance	11.5	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	11.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{3P3}	Supply voltage range		3.0	3.6	V
V_{HV}			4.5	19.8	V
$I_{LIM3P3OUT}$	V3P3OUT Switch current range		0	500	mA
V_{IH}	Input logic high	EN, HV_EN, S0	V3P3-0.6	V3P3	V
V_{IL}	Input logic low	EN, HV_EN, S0	0	0.6	V
R_{SET_V3P3}	3.3V switch current limit set resistance		25.3	402	kΩ
R_{SET_S0}	VHV switch current limit in S0 mode set resistance		25.3	402	kΩ
RS_{ET_S3}	VHV switch current limit in S3 mode set resistance		25.3	402	kΩ

ELECTRICAL CHARACTERISTICS

Unless otherwise noted the specification applies over the V_{DD} range and operating junction temp –40°C ≤ T_J ≤ 85°C. Typical values are for V_{3P3} = 3.3V, V_{HV} = 15V, and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS						
V_{3P3}	V3P3 Input voltage range		3	3.3	3.6	V
V_{HV}	VHV Input voltage range		4.5		19.8	V
I_{VHVACT}	Active quiescent current from VHV	HV_EN = 1, EN = 1			150	µA
I_{VHVSD}	Shutdown leakage current from VHV	HV_EN = 0, EN = 0 or 1			30	µA
I_{DDACT}	Active quiescent current from V3P3	EN = 1, HV_EN = 0			200	µA
$I_{DDACTHV}$	Active quiescent current from V3P3	EN = 1, HV_EN = 1			150	µA
I_{DDSD}	Shutdown Quiescent Current from V3P3	EN = 0, OUT = 0V			10	µA
I_{DIS}	OUT Discharge Current	EN = 1, V_{HV} = 5V HV_EN = 1 → 0	5		10	mA
I_{IN}	HV_EN, EN, S0, S3 Input pin leakage	V = 0 V			1	µA
		V = V3P3			1	µA
SWITCH AND RESISTANCE CHARACTERISTICS						
R_{SHV}	VHV Switch resistance	V_{HV} = 5 V to 18V, I_{VHV} = 1.5 A			250	mΩ
R_{S3P3}	V3P3 Switch resistance	V_{3P3} = 3.3 V, I_{V3P3} = 1.5 A			250	mΩ
$R_{S3P3BYP}$	V3P3 Bypass switch resistance	V_{3P3} = 3.3 V, I_{V3P3} = 500 mA			500	mΩ
R_{OUTDIS}	OUT Pulldown resistance when disabled	EN = 0	1.5	2.5	4	kΩ
VOLTAGE THESHOLDS						
V_{HVUVLO}	VHV Under voltage lockout	VHV Input Falling	3.6	4		V
		VHV Input Rising		4	4.3	
$V_{3P3UVLO}$	V3P3 Under voltage lockout	V3P3 Input Falling	1.8	2.25		V
		V3P3 Input Rising		2.25	2.5	
THERMAL SHUTDOWN						
T_{SD}	Shutdown Temperature		110	120	130	°C
T_{SDHYST}	Shutdown Hysteresis			10		°C

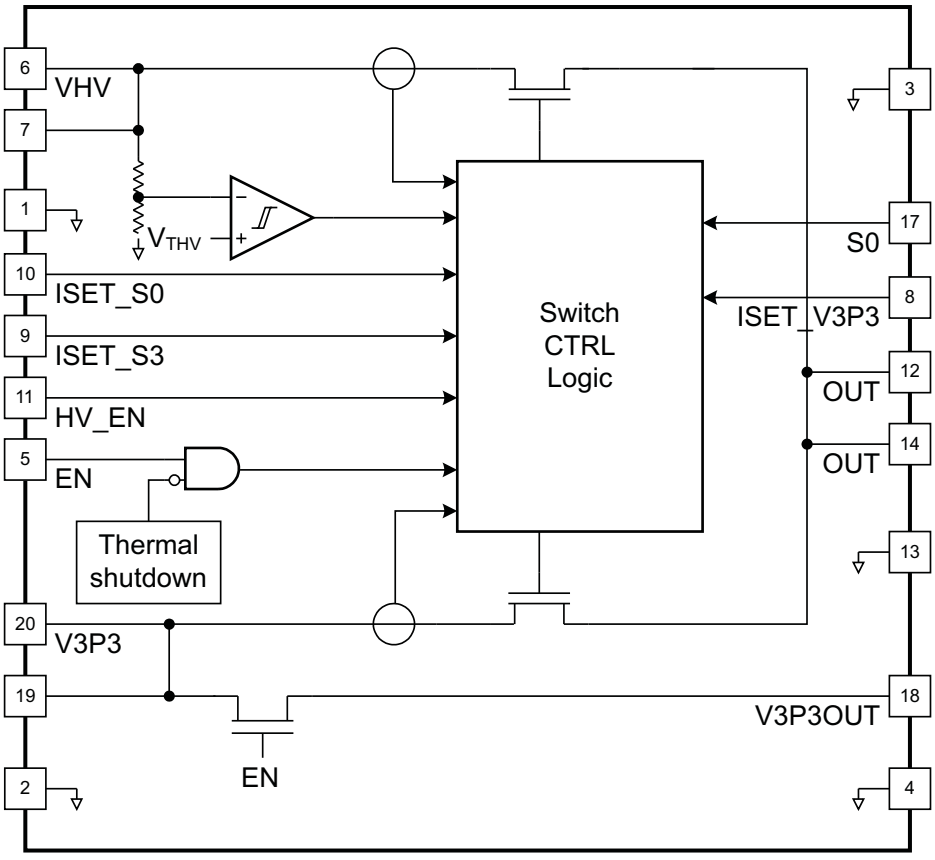
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ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted the specification applies over the V_{DD} range and operating junction temp –40°C ≤ T_J ≤ 85°C. Typical values are for V_{3P3} = 3.3V, V_{HV} = 15V, and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
I_{LIMHV}	VHV Switch current limit state S0 or S3	$R_{SET_S0,\ 3}$ = 402 kΩ	100	110	150	mA
		$R_{SET_S0,\ 3}$ = 80.6 kΩ	495	525	555	
		$R_{SET_S0,\ 3}$ = 26.7 kΩ	1515	1575	1635	
I_{LIM3P3}	V3P3 Switch current limit	R_{SET_V3P3} = 402 kΩ	100	110	150	mA
		R_{SET_V3P3} = 80.6 kΩ	495	525	555	
		R_{SET_V3P3} = 26.7 kΩ	1515	1575	1635	
I_{REV3P3}	V3P3 Switch Reverse Current Limit		10	27	45	mA
T_{V3P3RC}	V3P3 Switch Reverse Current Response Time	V_{OUT} = V_{3P3} → V_{3P3} + 20mV			100	µS
T_{VHVSC}	VHV Switch short circuit response time	C_{OUT} = 20 pF		8		µs
T_{V3P3SC}	V3P3 Switch short circuit response time	C_{OUT} = 20 pF		8		µs
TRANSITION DELAYS						
T_{3P3OFF}	VHV to V3P3 off time	C_{OUT} = 1.1µF, EN = 1, HV_EN = 1→0			6	ms
$T_{0\text{-}3.3V}$	0V to 3.3V ramp time	C_{OUT} ≤ 20 pF			6	ms
$T_{3.3V\text{-}VHV}$	3.3V to VHV ramp time	C_{OUT} ≤ 20 pF			6	ms
$T_{VHV\text{-}3.3V}$	VHV to 3.3V ramp time	C_{OUT} ≤ 20 pF			23	ms
T_{LIM}	Overcurrent response time	C_{OUT} ≤ 20 pF			0.5	ms

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

CURRENT LIMIT

The TPS22980 provides current limiting in the power switches. Both the VHV supply current limit and the V3P3 supply current limit are adjustable by external resistors.

Figure 2 shows a simplified view of the TPS22980 current limit function. Both the VHV supply current limit and the V3P3 supply current limit are adjustable by external resistors.

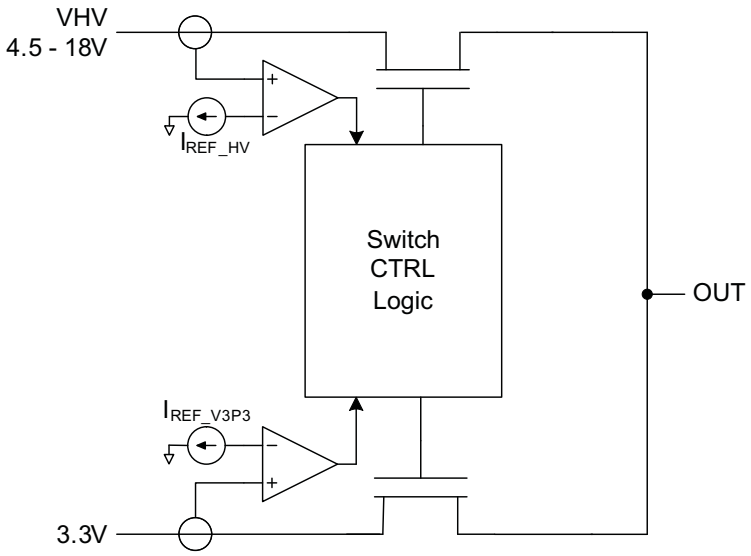


Figure 2. Simplified Current Limit Diagram

The current limit thresholds, I_{REF_HV} and I_{REF_V3P3}, are set with three external resistors as shown in Figure 3. When the TPS22980 is passes the V3P3 voltage, the current limit is set by R_{ISET_V3P3}. The VHV path has two modes that support two different current limits which are selected by the S0 pin. When S0 is asserted high, R_{ISET_S0} sets the current limit. When S0 is low, R_{ISET_S3} sets the current limit. This allows the system to have two separate VHV current limits for different modes such as active and sleep.

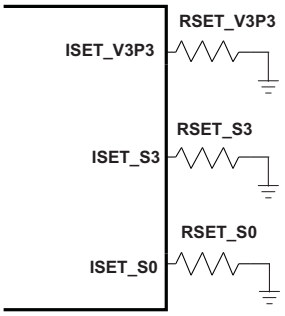


Figure 3. External R_{SET} Resistances to Set Current Limits

CURRENT LIMIT THRESHOLD

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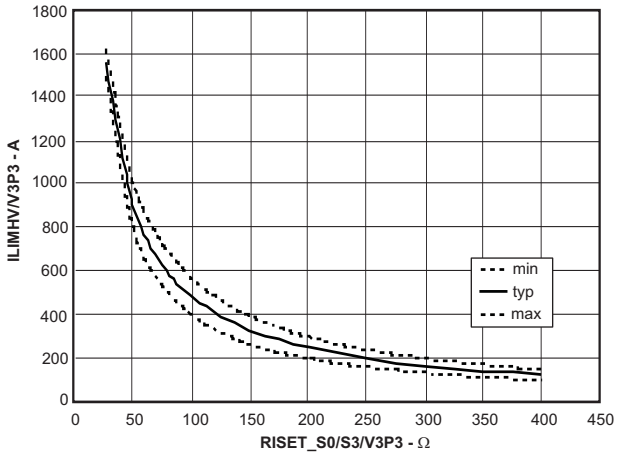


Figure 4. I_{LIM} vs R_{SET} for VHV and V3P3

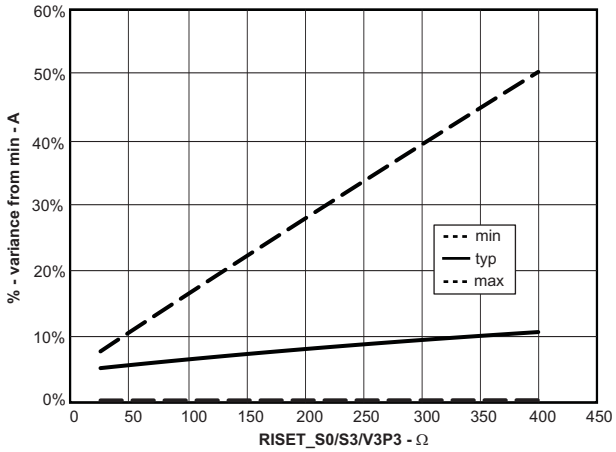


Figure 5. Percent Variance from min I_{LIM} vs R_{SET}

Figure 4 shows the minimum, typical, and maximum current limit for either supply versus its corresponding R_{ISET} value. Equation 1 is used to determine the R_{ISET} needed to set a minimum ILIM for a given supply and mode. Figure 5 shows the approximate variation from the set minimum I_{LIM} value to the typical and maximum I_{LIM} values.

$$R_{ISET} = \frac{40\ k\Omega \times Amps}{I_{LIMmin}} \quad (1)$$

where:

R_{ISET} = external resistor used to set the current limit for V3P3, VHV (S0), or VHV (S3), and
I_{LIMmin} = current limit for V3P3, VHV (S0), or VHV (S3) set by the external R_{ISET} resistor.

Each resistor is placed between the corresponding ISET pin and GND, as shown in Figure 3, providing a minimum current limit between 100mA and 1.5A.

TRANSITION DELAYS

Output transitions of the TPS22980 voltages are shown in Figure 6. When the device transitions from VHV to V3P3 at the output, the power switches both turn off until the output falls to near the V3P3 voltage. During this time, a discharge current (IDIS) pulls OUT down. If a load on the line is also pulling OUT down, the output can drop to 0V due to the switch off time of T3P3OFF. Figure 7 shows the voltage drop on the output during this transition with no output capacitance.

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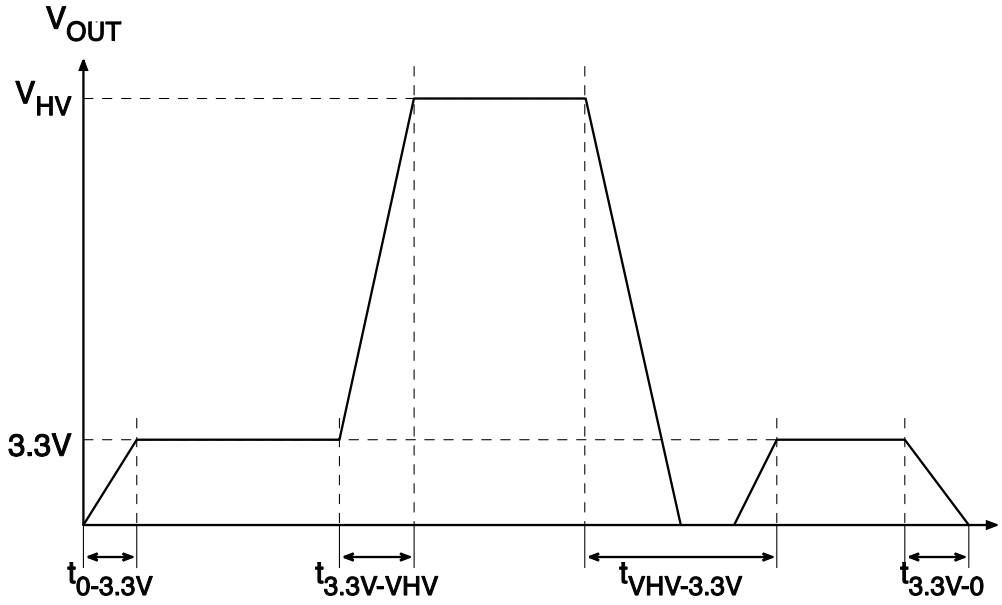


Figure 6. Allowable Voltage Transitions

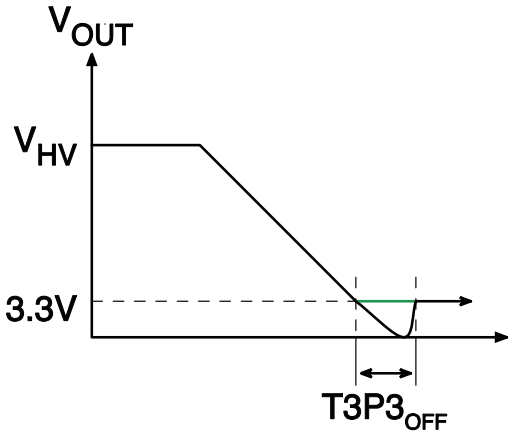


Figure 7. Voltage Drop During Transitions from VHV

DIGITAL CONTROL SIGNALS

The voltage at OUT is controlled by two digital logic input signals, EN and HV_EN. HV_EN controls the state of the VHV switch and EN controls the state of V3P3 switch. Table 1 lists the possible output states given the conditions of the digital logic signals. State PD indicates a pulldown resistance of R_{OUTDIS} to GND.

Table 1. Output State of OUT Given the States EN and HV_EN

EN	HV_EN	OUT
0	0	PD
0	1	PD
1	0	V3P3
1	1	VHV

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Figure 8 shows possible combinations of EN and HV_EN controlling OUT of the TPS22980.

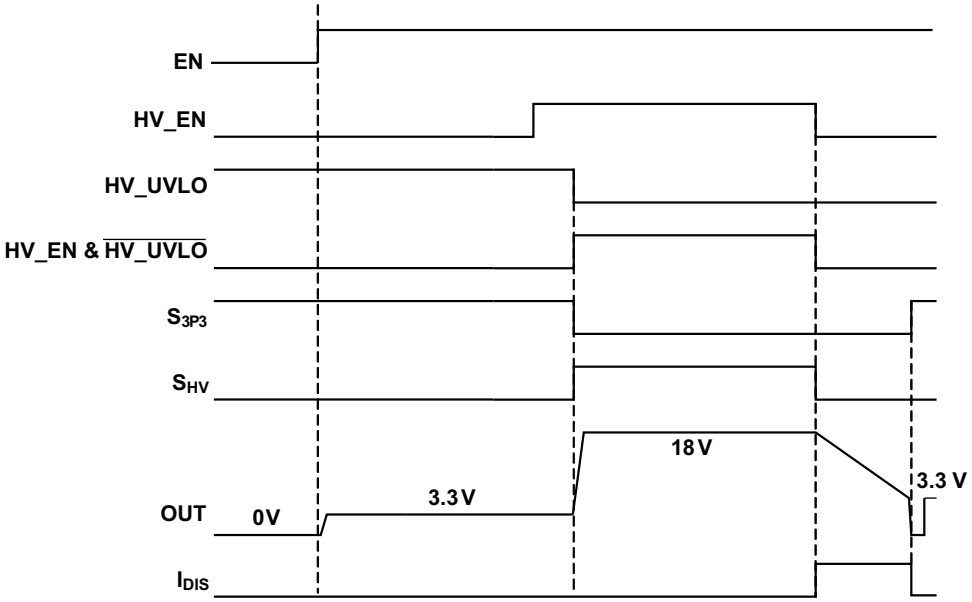


Figure 8. Logic Waveforms Displaying the Transition Between VHV and V3P3

OVER-CURRENT LIMIT AND SHORT CIRCUIT PROTECTION

When the load at OUT attempts to draw more current than the limit set by the external RISET resistors for the V3P3 switch and VHV switch (for both S0 and S3 modes), the device will operate in a constant current mode while lowering the output voltage. Figure 9 shows the delay, t_{LIM}, which occurs when an over-current fault is detected until the output current is lowered to ILIMHV tolerances for VHV or ILIM3V3 tolerances for V3P3 as shown in Figure 4.

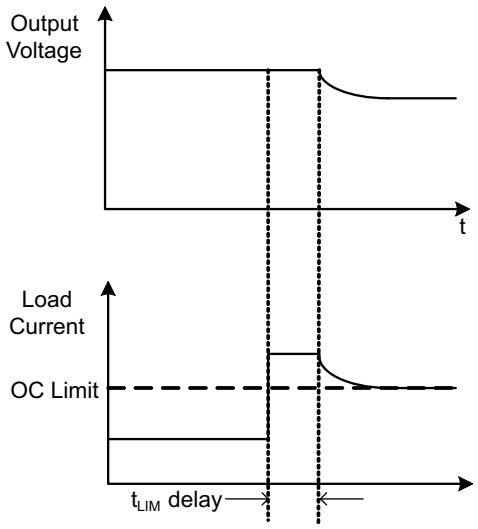


Figure 9. Overcurrent Output Response

All short circuit conditions are treated as over-current conditions. In the event of a short circuit, the device will limit the output current to the corresponding R_{SET} value and continue to do so until thermal shutdown is encountered or the short circuit condition is removed.

Reverse Current Protection

Reverse current protection for the V3P3 supply to OUT triggers at I_{REV3P3} causing the V3P3 supply switch to open. When the HV_EN signal is not asserted and reverse current protection is triggered, a discharge current source is turned on to bring the output voltage to 3.3V nominal.

Thermal Shutdown

The device enters thermal shutdown when junction temperature reaches T_{SD}. The device will resume the previous state on power up once the junction temperature has dropped by 10°C. Connect thermal vias to the exposed GND pad underneath the device package for improved thermal diffusion.

UVLO

When the VHV rail reaches the under-voltage lockout threshold of V_{HVUVLO} while HV_EN is high, the device will switch back to V3P3. Once the UVLO condition has cleared, the device will switch to VHV again. When the V3P3 rail reaches the under-voltage lockout threshold of $V_{3P3UVLO}$, regardless of the states of any digital logic controls, the device will open all switches and enter a reset condition.

Input Inductive Bounce at Short Circuit

When the TPS22980 is operating at high currents and high input voltage on VHV, a short circuit condition can cause the input to exceed the maximum safe operating condition for VHV. When a significant inductance is present at the VHV input, sudden turn off of current through the device may produce a large enough inductive voltage bounce that exceeds the maximum safe operating condition and may damage the TPS22980. To prevent this, reduce any inductance at the input. Input capacitors, such as 4.7µF, can reduce the supply bounce and are recommended.

Single Point Failure Protection

The TPS22980 current limits are set by the RISET resistances. Shorting one of these resistance would result in a single point failure that removes the current limiter for that particular input and mode. Without current limiting, an excessive current load may damage the TPS22980 and the system. To prevent a single point failure from occurring, the RISET resistances can be divided into two series resistances each as shown in Figure 10. Failure of a single resistance will not result in runaway current and damage.

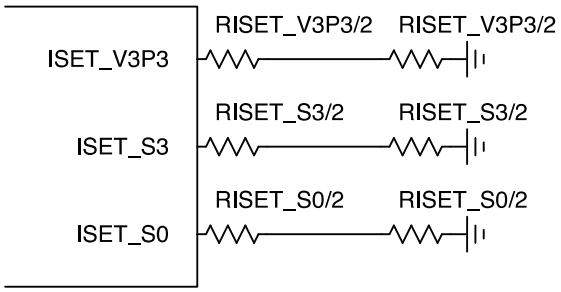


Figure 10. R_{ISET} Division to Prevent Single Point Failure

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REVISION HISTORY

Changes from Original (December 2011) to Revision A **Page**

- Changed Typical Application figure. 1
- Added bottom view pin out information. 2
- Updated Pin Functions Table. 2
- Added reverse current and thermal shutdown parameters to the ELECTRICAL CHARACTERISTICS table. 4
- Updated the APPLICATION INFORMATION section. 6

Changes from Revision A (February 2012) to Revision B **Page**

- Changed bottom view pin out information. 2

Changes from Revision B (April 2012) to Revision C **Page**

- Removed ordering information table. 2
- Added R_{OUTDIS} parameter to the Electrical Characteristics table. 4
- Updated the DIGITAL CONTROL SIGNALS section. 8

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22980RGPR	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS22980	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

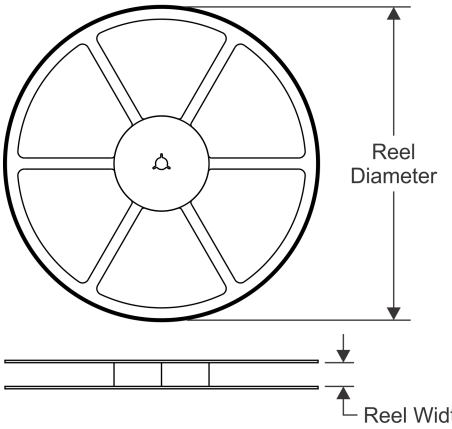
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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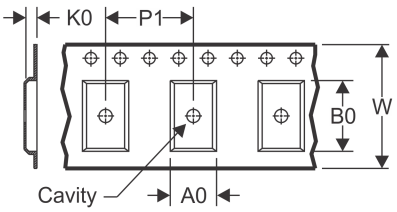
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TAPE AND REEL INFORMATION

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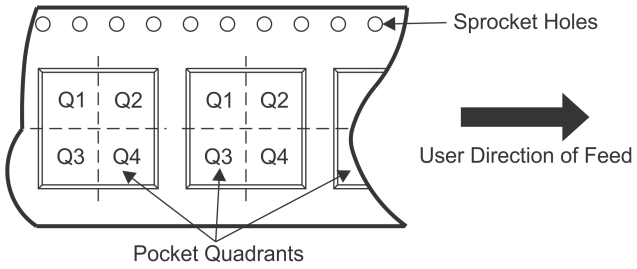


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

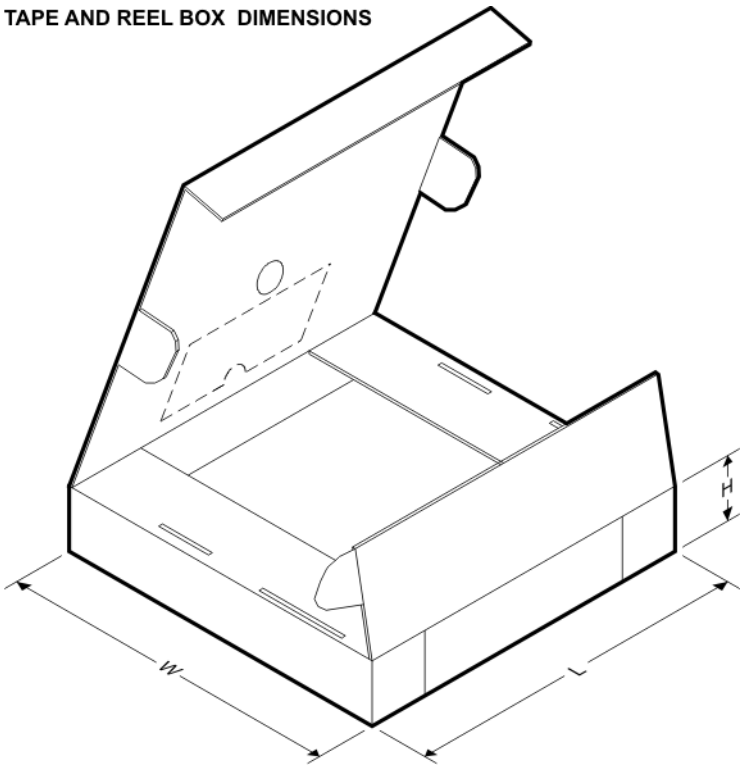
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22980RGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

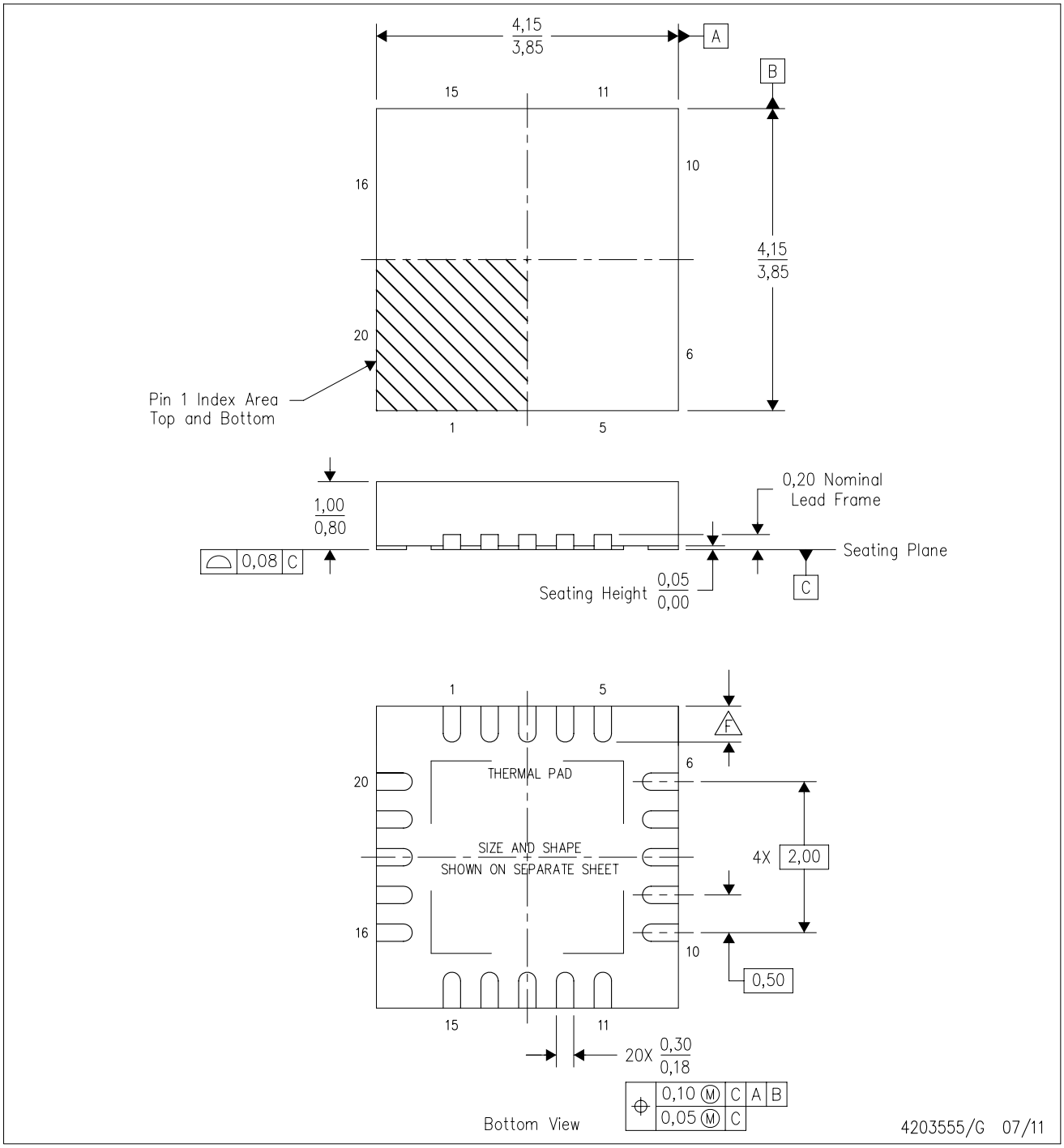
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22980RGPR	QFN	RGP	20	3000	367.0	367.0	35.0

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

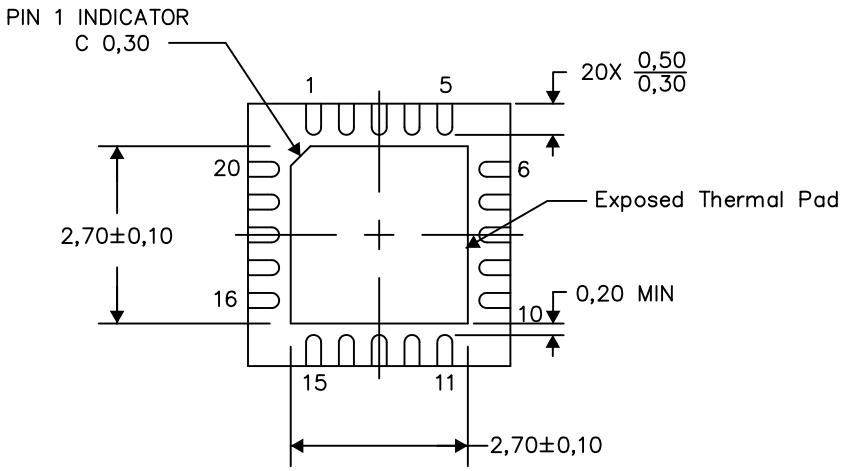
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



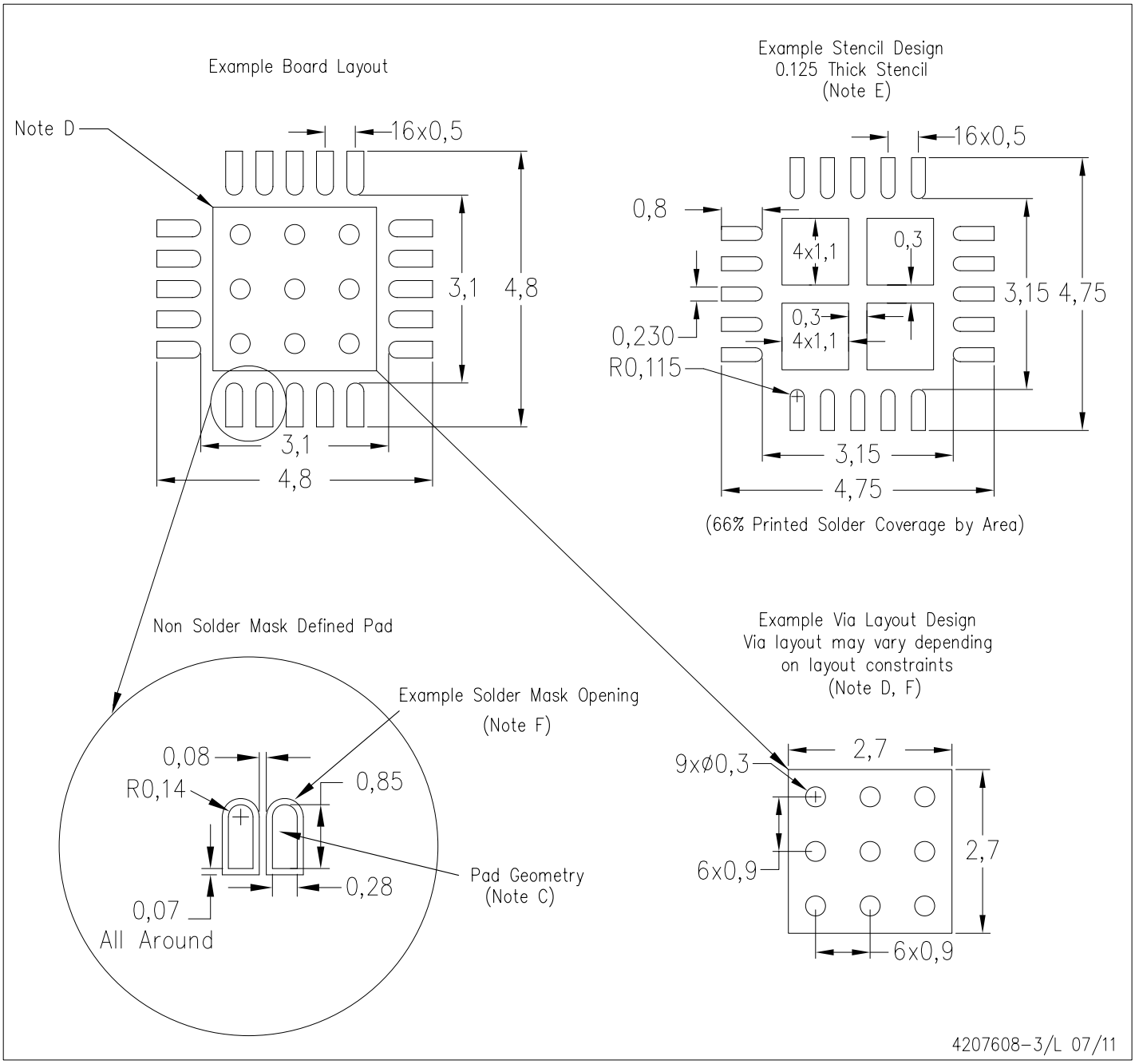
Bottom View

Exposed Thermal Pad Dimensions

4206346–3/AA 11/13

NOTES: A. All linear dimensions are in millimeters

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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