MP5018

5V, 1A-5A Current Limit Switch with Reverse Current Blocking and Output Over-voltage Clamp

The Future of Analog IC Technology

DESCRIPTION

The MP5018 is a protection device designed to protect circuitry on the output from transients on input (V_{CC}). It also protects V_{CC} from undesired shorts and transients coming from the output.

At startup, inrush current is limited by the slew rate at the output. The slew rate is controlled by a small capacitor at the SS pin. Floating the SS pin provides 13ms soft-start time.

The maximum load at the output is current limited. The magnitude of the current limit is controlled by an external resistor from ILIMIT to GND. Floating ILIMIT pin provides 3A fixed current limit. By controlling the gate voltage of a pair of N-channel MOSFETs, any current flowing from output to input is blocked.

Under Voltage Lockout (UVLO) assures that input is above the minimum operating threshold, before the power device is turned on. If input voltage goes above 5.8V, the output voltage will be limited at 5.8V with fast response.

The EN/Fault pin is a bi-directional, three-level I/O with a weak pull-up. It can be used to enable or disable MP5018, or indicate a fault condition.

The device is available in a QFN12 (2mmx3mm) package.

FEATURES

- SAS Disable to support DEVSLP or POWER_DOWN
- 4.5V to 5.5V Continued Operating Input Range
- 16V Absolute Maximum Input Voltage
- 5.8V Fast OVP Response
- Reverse Current Blocking
- Integrated 45mΩ Power FET
- Adjustable Current-Limit or Fixed Current Limit when floating ILIMIT pin
- 210μA Typical Low Quiescent Current
- Adjustable Soft Start time
- Fault Indication
- Latch-off Thermal Protection
- Available in QFN12(2mmx3mm) Package
- ESD Compliant to 2kV HBM and 1kV CDM

APPLICATIONS

- HDD, SSD
- Hot Swap Systems
- Gaming
- Set-top Boxes/Smart TV
- PCIe Cards
- Switches/Routers

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

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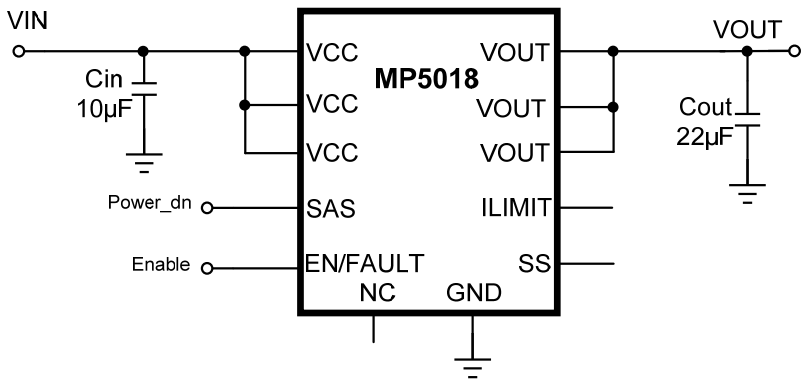
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5018GD	QFN-12 (2mmx3mm)	*See Below*

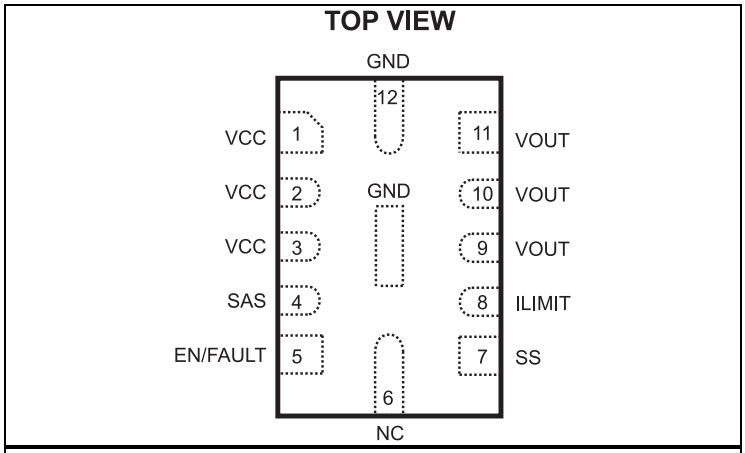
***** For Tape & Reel, add suffix –Z (e.g. MP5018GD–Z);

TOP MARKING

AMAY
LLL

AMA: product code of MP5018GD;
Y: year code;
LLL: lot number;

PACKAGE REFERENCE



QFN-12 (2mmx3mm)

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to 16V
V_{OUT}..... 6.3V
All Other Pins.....–0.3V to +6V
Junction Temperature..... -40°C to +150°C
Lead Temperature .....260°C
Continuous Power Dissipation (T_A=+25°C)**(2)**
QFN-12 (2mmx3mm)..... 1.8W

Recommended Operating Conditions (3)

Continued Operation V_{IN}.....4.5V to 5.5V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
QFN-12 (2mmx3mm).....	70	15	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J =25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Quiescent Current	I_Q	EN=1, SAS=0, I_{Load}=0		210	250	μA
		Fault latch off		170		μA
		EN=0, SAS=0 (or Float)			50	μA
		SAS=1			5	μA
Power FET						
ON Resistance	R_{DSon}	T_J=25°C		45	58	mΩ
ON Resistance(5)	R_{DSon}	T_J=80°C		54		mΩ
Turn-on Delay	T_{delay}	EN=2.5V to I_D=100mA with 1A load resistor		500		μs
Off-State Leakage Current	I_{OFF}	V_{IN}=12V, EN=0V			1	μA
Soft Start						
SS Time	t_{SS}	SS pin float, VOUT=0%-100%	10.4	13	15.6	ms
SS Current	I_{SS}	Short SS to GND or add SS cap		6.5		μA
Current Limit						
Current Limit at Normal Operation	I_{Limit_NO}	Float ILIMIT pin	2.5	3	3.5	A
		R_{set}=499Ω	1.8	2.3	2.7	A
		R_{set}=1.4kΩ	0.5	0.8	1.1	A
Short Circuit Current Limit(5)	I_{Limit_SC}	Float ILIMIT pin		3		A
Current Limit Response Time(5)	t_{CL}	I_{LIMIT}=3A, add 1Ω load resistor	5.5	10	40	μs
Secondary Current Limit(6)	I_{LimitH}	Any value of R_{ISET}		12		A
Under Voltage Protection						
Under Voltage Lockout Threshold	V_{UVLO}	UVLO Rising Threshold	3.8	4.0	4.2	V
UVLO Hysteresis	$V_{UVLOHYS}$			300		mV
Under Voltage Response(5)	t_{UV}			2		μs
Reverse Current Limit						
Reverse Current Limit	$I_{ReverseH}$	Latch off and pull EN to mid level voltage	0.9	1.2	1.5	A
Reverse Current Limit Response Time(5)	t_{SC}	Vin dv/dt = -5V/1mS	5	7	10	μs
Over Voltage Protection						
Over Voltage Clamp Voltage	V_{OVLO}		5.5	5.8	6.1	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J =25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Over Voltage Response Time(5)	t_{OV}	Cout=20uF, VIN=5V to 12V		10	40	µs
Thermal Shutdown						
Shutdown Temperature(5)	t_{STD}	Latched off until Enable = 0, SAS = 1, POR	130	175	200	°C
Enable/Fault						
Low Level Input Voltage	V_{IL}	UVLO, SAS Disable	0.35		0.8	V
Intermediate Level Input Voltage	$V_{I\ (INT)}$	Thermal fault, fast reverse current limit	0.9	1.3	1.95	V
High Level Input Voltage	V_{IH}	Output Enabled	2.1		3.3	V
Maximum High State	V_{ENH}		3.4		5.2	V
Logic Low Sink Current	I_{EH_PL}	EN=0V		-12	-20	µA
Logic Level High Current	I_H	EN = 3.3V			1	µA
Maximum Fanout for Fault Signal		Total number of chips that can be connected for simultaneous shutdown			3	Units
SAS Disable						
Low Level Input Voltage	V_{ENN_L}	EN=1, Output enabled	0.35		0.7	V
High Level Input Voltage	V_{ENN_H}	Output Disabled, EN=low	2.1			V
Maximum pin voltage	$SASH_{max}$				3.3	V
Input Impedance	R_{ENN}	To GND	350	700	1000	kΩ
Deglitch Filter	t_{SASDG}		2		50	µs

Notes:

5) Guarantee by characterization test.

6) Guarantee by design.

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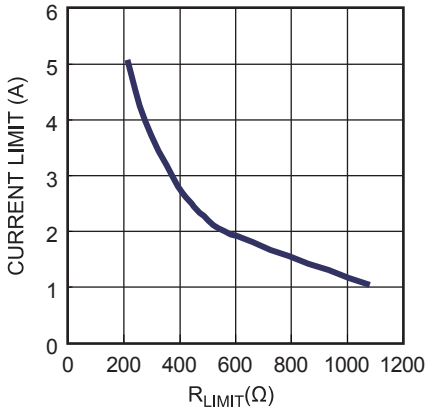
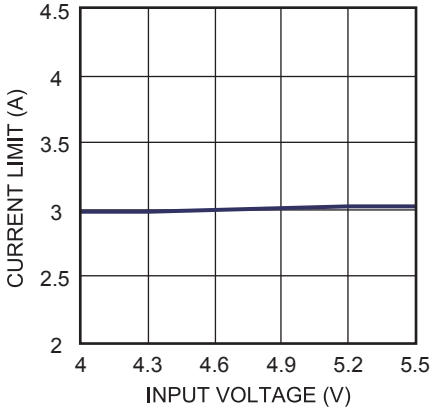
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=5V, V_{EN}=5V, I_{LIMIT} Pin Float, SS Pin Float, SAS Pin Float, C_{OUT}=22µF, T_A=25°C, unless otherwise noted.

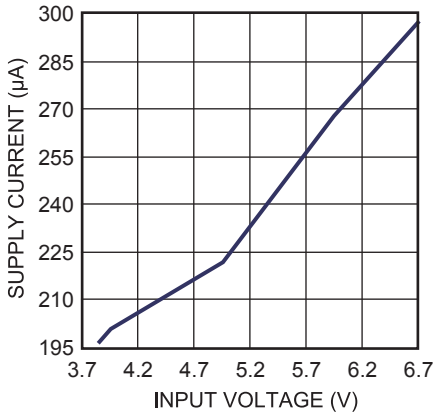
Current Limit vs.RIimit



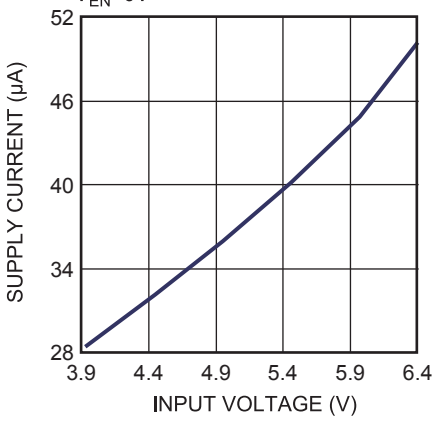
Current Limit vs. Input Voltage
R_{LIMIT} Float



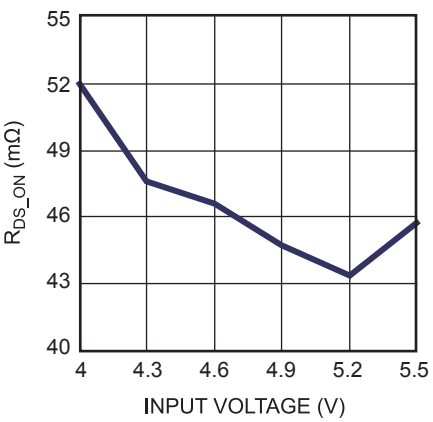
Supply Current, Output Enabled vs. Input Voltage
No load



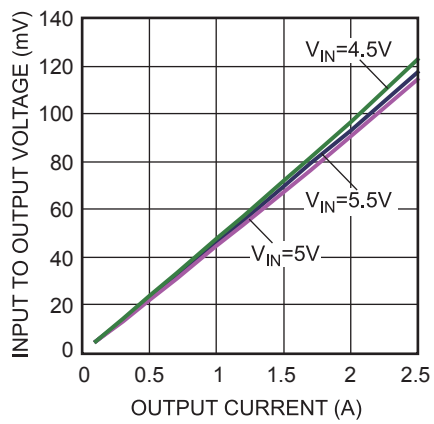
Supply Current, Output Disabled vs. Input Voltage
V_{EN}=0V



R_{DS_ON} vs. Input Voltage
I_{OUT}=0.5A



Input to Output Voltage vs. Load Current



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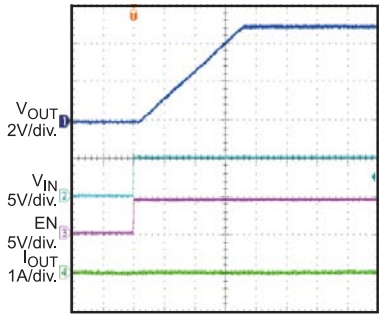
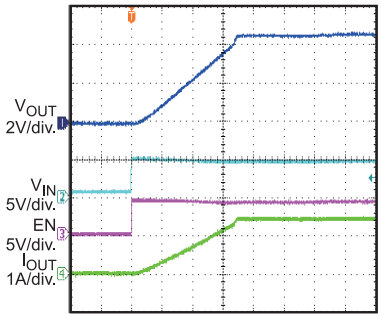
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=5V, V_{EN}=5V, I_{LIMIT} Pin Float, SS Pin Float, SAS Pin Float, C_{OUT}=22µF, T_A=25°C, unless otherwise noted.

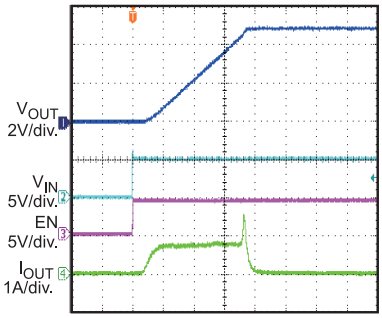
Startup through Input Voltage
En Float, No Load



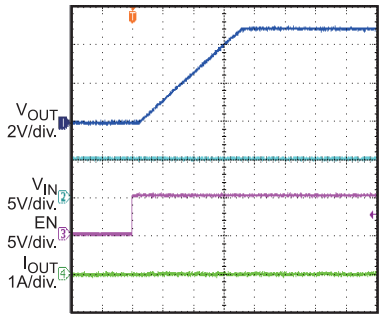
Startup through Input Voltage
En Float, R_{LOAD} = 3.3Ω



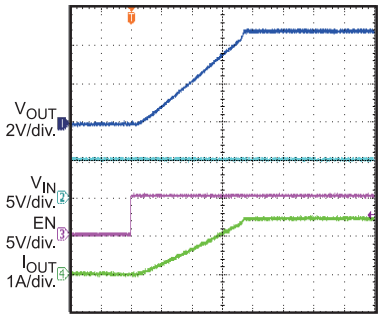
Startup through Input Voltage
En Float, No Load, C_{OUT} = 2200µF



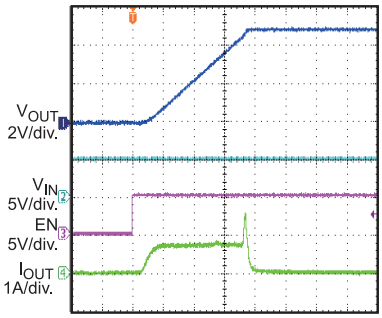
Startup through Enable
No Load



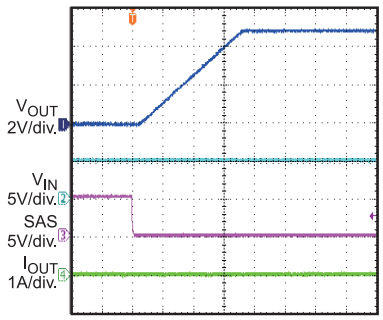
Startup through Enable
R_{LOAD} = 3.3Ω



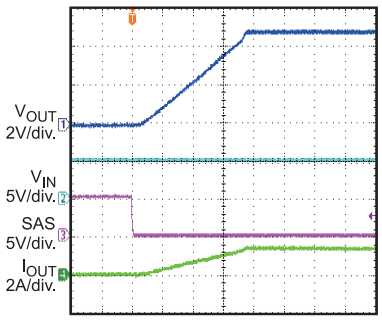
Startup through Enable
No Load, C_{OUT} = 2200µF



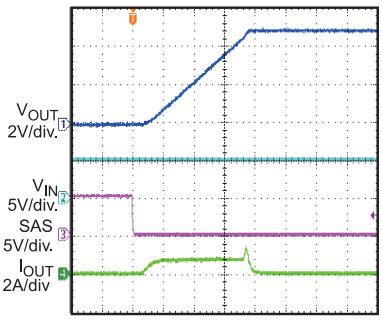
Startup through SAS
No Load



Startup through SAS
R_{LOAD}=3.3Ω



Startup through SAS
No Load, C_{OUT}=2200µF



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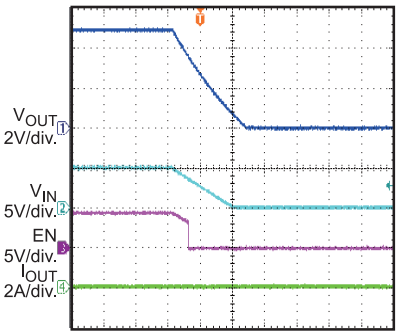
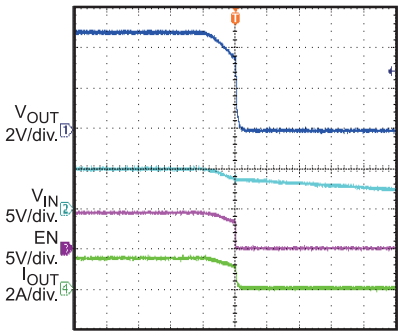
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=5V, V_{EN}=5V, I_{LIMIT} Pin Float, SS Pin Float, SAS Pin Float, C_{OUT}=22µF, T_A=25°C, unless otherwise noted.

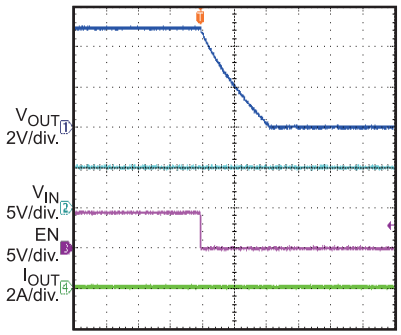
Shutdown through Input Voltage
No Load



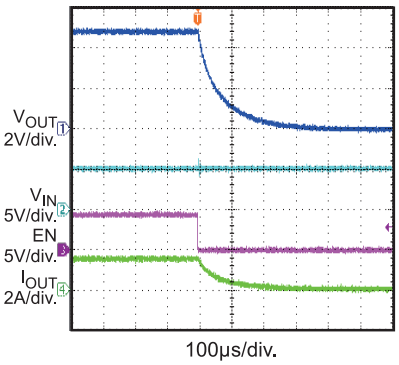
Shutdown through Input Voltage
R_{LOAD}=3.3Ω



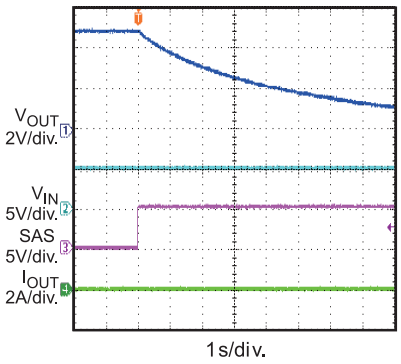
Shutdown through Enable
No Load



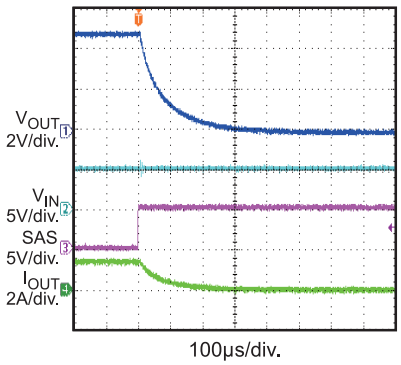
Shutdown through Enable
R_{LOAD}=3.3Ω



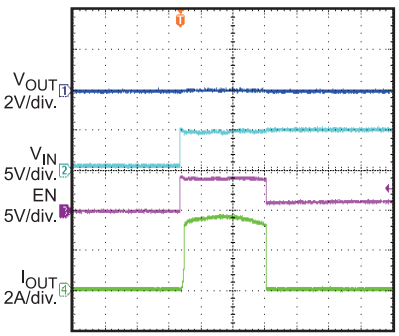
Shutdown through SAS
No Load



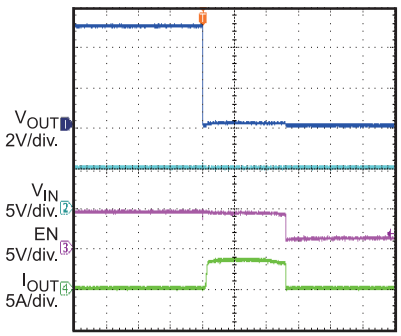
Shutdown through SAS
R_{LOAD}=3.3Ω



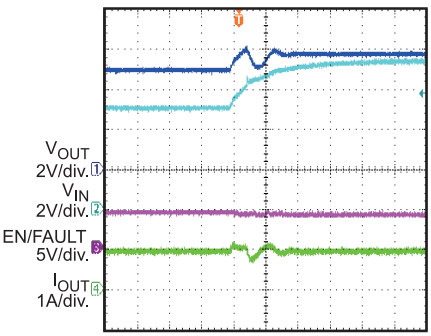
Short Circuit before Input Voltage Startup, and Thermal Shutdown



Short Circuit during Normal Operation, and Thermal Shut Down



OVP Response
V_{IN} from 5V to 7.5V



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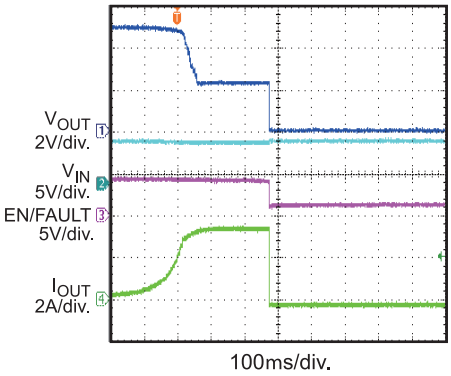
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=5V, V_{EN}=5V, I_{LIMIT} Pin Float, SS Pin Float, SAS Pin Float, C_{OUT}=22µF, T_A=25°C, unless otherwise noted.

Current Limit

Increase I_{OUT} Slowly



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PIN FUNCTIONS

Pin #	Name	Description
1, 2, 3	VCC	Supply Voltage. The MP5018 support 4.5V to 5.5V continuous input voltage and up to 16V maximum transient input voltage. Requires ceramic capacitor to decouple the input rail. Connect using a wide PCB trace.
4	SAS	SAS=low to enable the part. SAS=high to disable the part. SAS pin has internal 700kΩ pull-down resistor to ground, so it can automatically start up when SAS is floating.
5	EN/FAULT	The EN/FAULT pin is a tri-state, bi-directional interface. It can be used to enable the output of the device by floating the pin, or disable the chip by pulling it to ground (using an open drain or open collector device). If a thermal fault occurs or reverse current limit is triggered, the voltage on this pin will go to an intermediate state to signal a monitoring circuit that there is a device fault. When UVLO or SAS disable = 1, the voltage on this pin will go to a low state. It can also be connected to another device in this family to cause a simultaneous shutdown.
6	NC	No Connection.
7	SS	Soft start pin. Connect a capacitor from SS to ground to set the soft start time. Floating this pin provides 13ms soft start time.
8	ILIMIT	Current Limit Set pin. Place a resistor between this pin and ground to set the value of the current limit. Floating this pin provides 3A fixed current limit.
9, 10, 11	VOUT	The output voltage that is controlled by the IC.
12, Pad	GND	System Ground.

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FUNCTIONAL BLOCK DIAGRAM

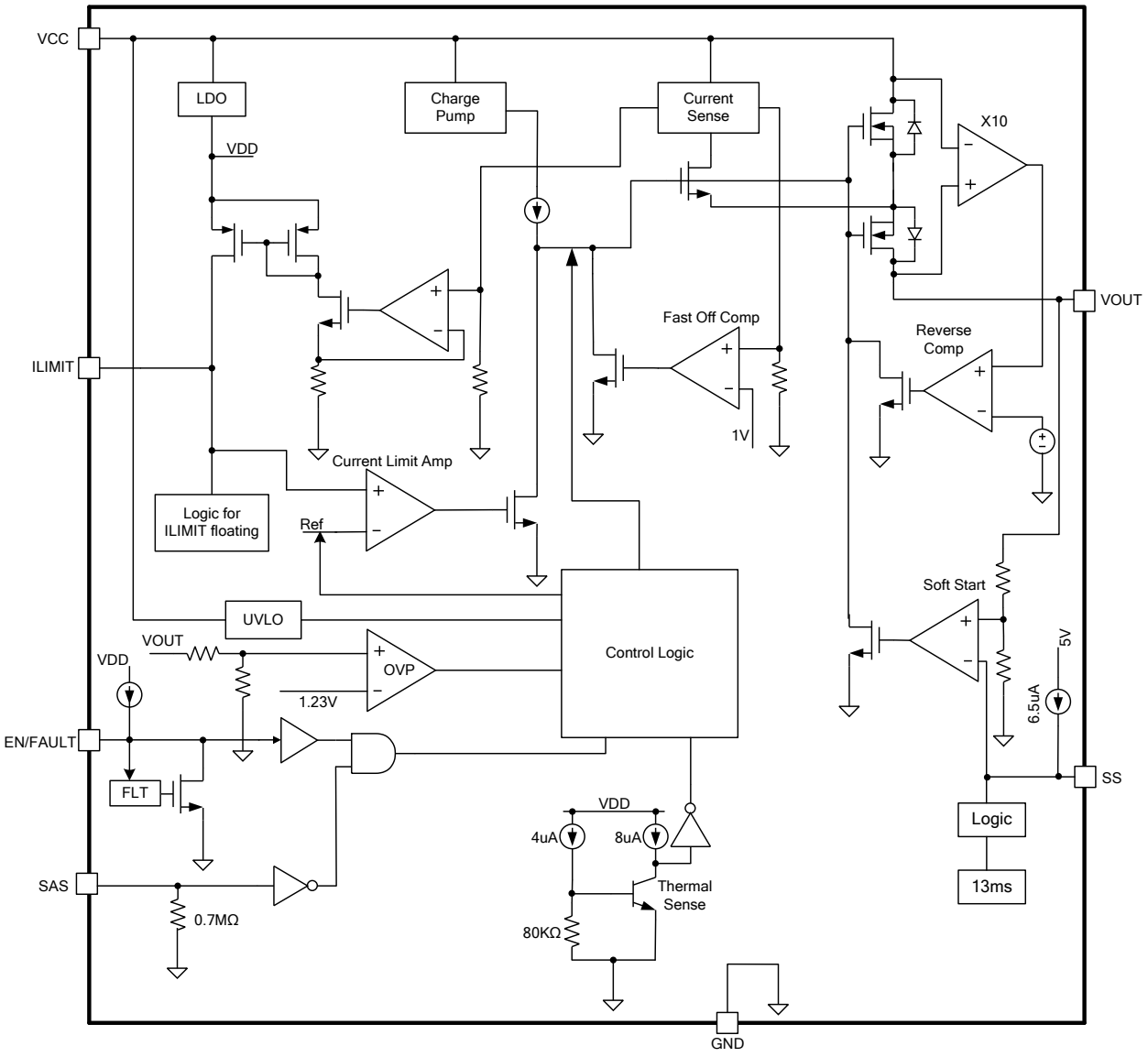

Figure 1: Functional Block Diagram

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OPERATION

The MP5018 is designed to limit the inrush current to the load when a circuit card inserts into a live backplane power source, thereby limiting the backplane's voltage drop and the dV/dt of the voltage to the load as well. It offers an integrated solution to monitor the input voltage, output voltage, output current, and die temperature which eliminates the requirement of external current sense power resistor, power MOSFET and thermal sense device.

Under-Voltage Lockout (UVLO)

If the supply voltage is below the UVLO threshold, the output is disabled, and the EN/Fault line is driven low. When the supply goes above the UVLO threshold, the output is enabled and the EN/Fault is pulled high.

The nominal input supply voltage is 5V but there are high energy transients during normal operation or during hot swap**.** Those transients depend on the parasitic inductance and resistance of the wire along with capacitor at V_{CC} node. If power clamp (TVS, Tranzorb) diode is not used, E-Fuse must be able to withstand this transient voltage. MP5018 integrates high voltage MOSFET up to 16V and also uses high voltage circuit for V_{CC} node to guarantee safe operation.

Fast Output over Voltage Clamp (OVP)

To protect the downstream loading when there is a surge voltage at input, MP5018 provides an accurate and fast comparator to monitor the over voltage condition of output. If the output voltage rises above the threshold (5.8V), the gate of internal MOSFETs is quickly pulled down and it's regulated to a certain value to maintain the output voltage clamped at 5.8V. The fast loop response speed (10μs typical) keeps the over voltage overshoot small.

Current Limit

The MP5018 provides a constant current limit and the current limit can be programmed by external resistor. Once the current limit threshold is reached, the internal circuit will regulate gate voltage to hold the current in power FET constantly. In order to limit the current, the gate to source voltage needs to be regulated from 5V to around 1V. The typical response time is about 10μs, during this period the output current may have a small overshoot.

The desired current limit is a function of the external current limit resistor.

MP5018 allows ILIMIT pin floating operation. If ILIMIT pin is floating, the current limit will be set as fixed 3A internally.

Reverse Current Blocking

The MP5018 integrates a pair of back-to-back N channel MOSFETs for reverse current protection. Once the reverse current limit threshold (-1.2A) is reached and exceed 7μs deglitch time, the internal circuit will shutdown the pair of MOSFETs. Meanwhile, the EN/Fault line is driven to middle level; reverse current is totally blocked and this state continues until VCC > VOUT-2mV. When VCC >VOUT-2mV, part resumes normal operation with soft-start control. Whenever the input voltage drops below UVLO threshold, back-to-back MOSFETs are turned off and the part is shut down; therefore, there is no reverse current during this condition.

Short Circuit Protection

If the load current increases rapidly due to short circuit event, the current may exceed the current limit threshold before control loop able to respond. If the current reaches 12A secondary current limit level, there is a fast turn off circuit active to turn off the power FET with 100mA pull-down gate discharge current, as shown in Figure 1. This can help to limit the peak current through the switch, thus keep the input voltage not drop too much. The total short circuit response time is about 1μs. After the FET is switched off, the part will restart. During the restart process, if the short still exist, MP5018 will regulate the gate voltage to hold the current at normal current limit level.

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EN Control/Fault Indication

The EN Pin enables the part when high and disables the part when low. Floating the EN pin will set the part auto startup because there is internal current source pull up EN to internal supply. The maximum internal pull up voltage source is about 5V. EN/Fault pin is also a bi-directional function node. When the part entersthermal shutdown, EN/Fault pin outputs middle level voltage ~1.3V to indicate fault condition occurred. When V_{IN}<UVLO threshold or the SAS pin is high, the EN pin will be pulled to GND through an internal resistor.

Table 1: Enable/Fault Function

Description	Enable/Fault	EFuse State	Latch
Under Voltage Lock Out	Low	Off	No
SAS = High	Low	Off	No
Thermal Shutdown	Mid	Off	Yes
Reverse Current Protection	Mid	Off	No (part restarts when V_{CC}>V_{OUT} -2mV)
SAS Floating	High	On	N/A
SAS = Low	High	On	N/A

SAS Control

The SAS pin also can control the part startup and shutdown. When floating this pin or pull it low, it enables the part and disables the part when pull high.

Soft-Start

Floating SS pin can get 13ms soft start time. While a capacitor connected to the SS pin can set the soft start time. A constant current source charges the SS capacitor and results in a linear ramping voltage on the SS pin. The output voltage rises at a similar slew rate to the SS voltage.

The soft-start time can be calculated as follows:

$$t_{ss}(ms) = \frac{1V \times C_{ss}(nF)}{6.5\mu A}$$

Where:

t_{SS}=soft start time

For example, a 22nF capacitor gives a soft start time of ~3.4ms.

If the load capacitance is extremely large, the current required to maintain the preset soft start time will exceed the current limit. In this case the rise time is controlled by the load capacitor and the current limit.

Thermal Shutdown – Latch Off

Thermal shutdown prevents the chip from operating at exceedingly high temperature. When the silicon die reaches temperature that exceeds 175°C, it shuts down the whole chip, and drives the Enable/Fault line to the middle (MID) level. The chip is latched off after trigger the thermal protection and it restarts when toggle the EN or SAS or recycle the input supply.

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APPLICATION INFORMATION

Setting the Current Limit

The MP5018 current limit value should exceed the normal maximum load current, allowing the tolerances in the current sense value. The current limit is a function of the external current-limit resistor. Table 2 and Figure 2 list examples of current limit values as a function of the resistor value.

Table 2: Current Limit vs. Current Limit Resistor

Current Limit Resistor (Ω)	1070	560	442	274	215
Current Limit (A)	1	2	2.5	4	5

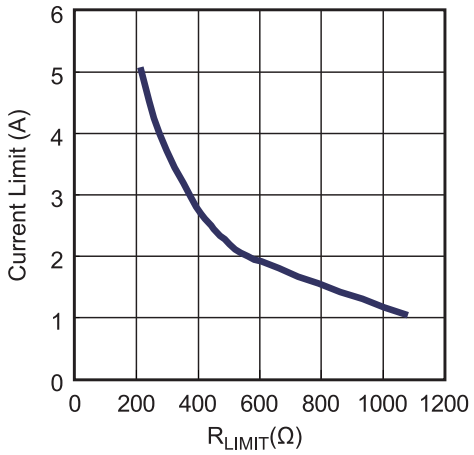

Figure 2: Current Limit vs. Current Limit Resistor

PCB Layout Guide [7]

PCB layout is benefit for better performance. Please follow these guidelines and use Figure 3 as reference.

1. Place the high-current paths (VCC and VOUT) close to the device using short, direct, and wide traces.

2. Place the input capacitors as close to the VCC and GND pins as possible.

3. Connect the VCC and VOUT pads to large copper to achieve better thermal performance.

4. Place current limit resistor R1 close to the ILIMIT pin.

5. Place SS capacitor C2 close to SS pin.

Note: The recommend layout is based on the typical application circuit shown in figure 4.

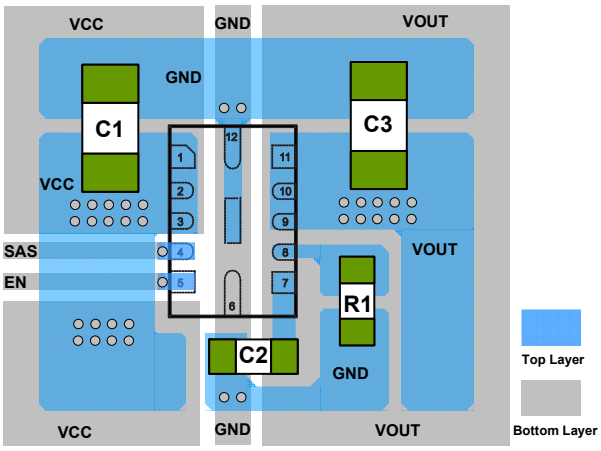

Figure 3: PCB Layout

Design Example

Below is a design example following the application guidelines for the given specifications:

Table 3: Design Example

V_{IN} (V)	5
Current Limit (A)	3
SS Time (ms)	13

The detailed application schematic is shown in Figure 4. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more detailed device applications, please refer to the related Evaluation Board Datasheets of MP5018.

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TYPICAL APPLICATION CIRCUITS

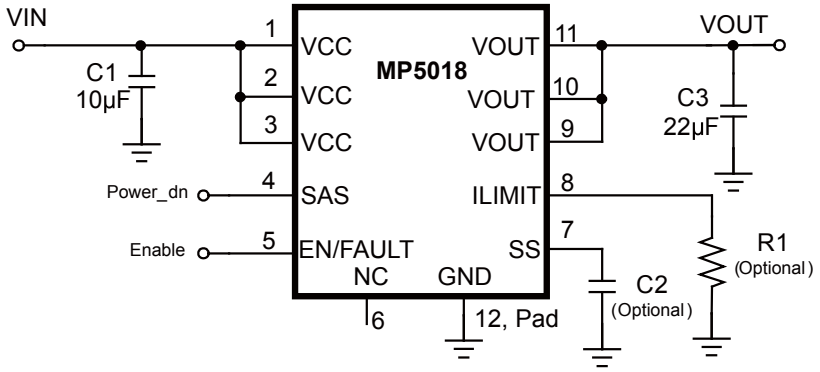

Figure 4: 5V V_{IN} Application

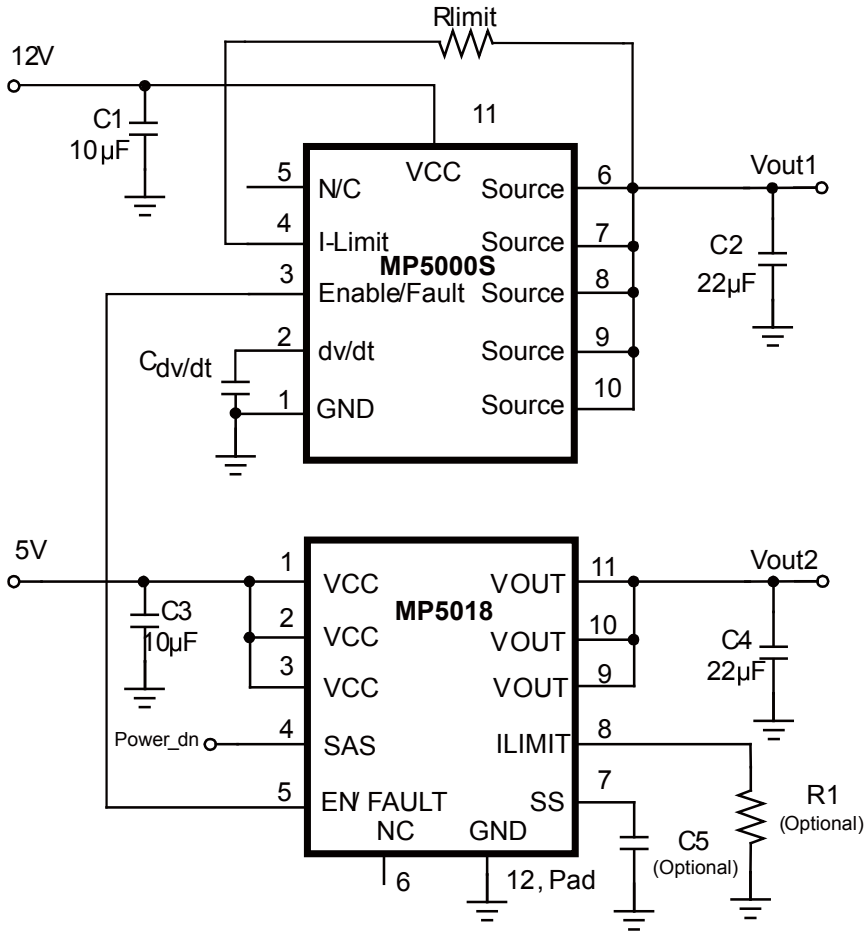

Figure 5: Simultaneous Shutdown Application

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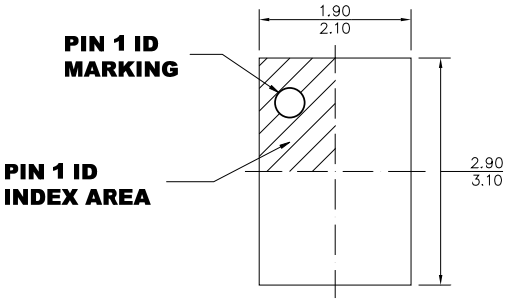
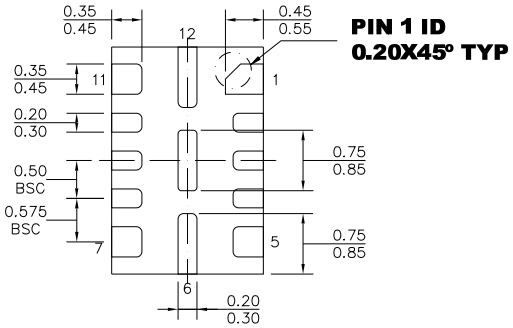
PACKAGE INFORMATION

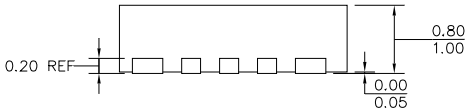
QFN-12 (2mmx3mm)



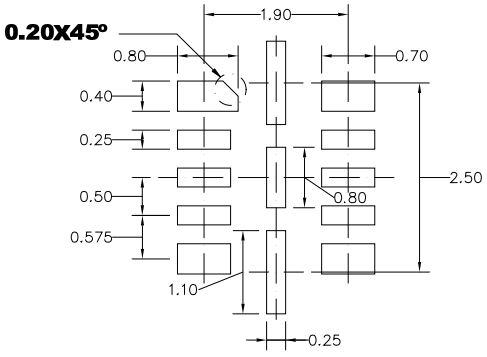
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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