SM840001

106.25MHz Ultra-Low Jitter Clock Synthesizer

General Description

The SM840001 synthesizer series were designed for Fibre Channel applications. The device design is optimized for 106.25MHz or 212.5MHz using a 26.5625MHz fundamental parallel resonant crystal, with stability and accuracy over the full operating range. The SM840001 includes a unique power reduction methodology, along with a patented RotaryWave™ architecture, that provides a stable clock with very low noise for optimized performance. This yields an overall improved Bit Error Rate (BER) and improved waveform integrity.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

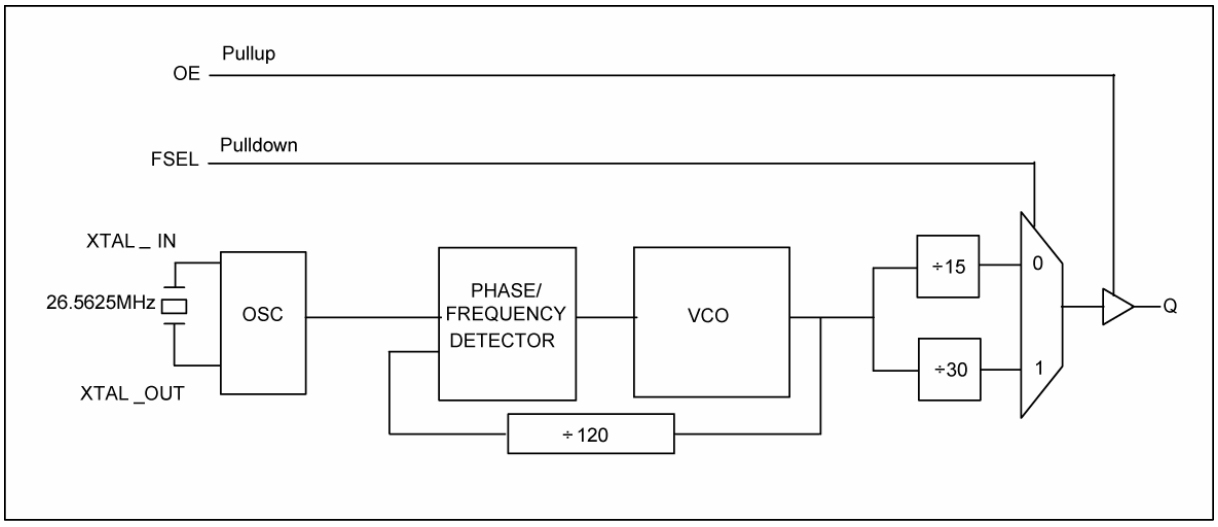
Features

- Generates a single LVCMOS/LVTTL output
- Integrated loop filter components
- RMS Phase Jitter:
  - 510 fs (typ) at 106.25MHz
  - 320 fs (typ) at 212.50MHz
- Operates with either a 3.3V or 2.5V supply
- Power consumption is <77mA @ 3.3 V
- Fundamental crystal oscillator interface
- Input frequency of 26.5625 MHz parallel resonant
- Selectable output frequency: 106.25MHz or 212.5MHz
- Temperature range: –40°C to +75°C
- Available in 8-pin TSSOP package

Applications

- Fibre Channel
- Storage

Block Diagram



RotaryWave is a trademark of Multigig, Inc.

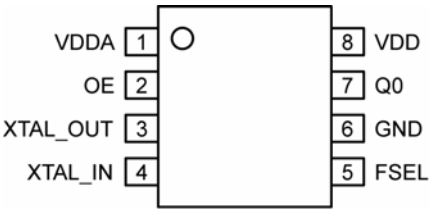
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SM840001KA	K-8	-40°C to +75°C	840001	NiPdAu
SM840001KA TR[2]	K-8	-40°C to +75°C	840001	NiPdAu

Note:

1. Devices are Green, RoHS-compliant and PFOS-compliant.
2. Tape and Reel.

Pin Configuration



8-Pin TSSOP (K-8)

Pin Description

Pin Number	Pin Name	Type	Level	Pin Function
1	VDDA	P		Analog Power.
2	OE	I	Pull-up	Output Enable: 1 = Enable, 0 = Disable.
3	XTAL OUT	O		Crystal Out.
4	XTAL IN	I		Crystal Input.
5	FSEL	I	Pull-down	Frequency Select Pin.
6	GND	P		Ground.
7	Q0	O		Single Ended LVCMOS Clock Out.
8	VDD	P		Core Power.

Frequency Select Table

FSEL	Output (MHz)
0	106.25 (Default)
1	212.5

Output Enable

OE	Output
0	Disable
1	Enable

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Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}) ..... +4.6V
Input Voltage (V_{IN}) ..... –0.50V to V_{DD}+0.5V
Output Voltage (V_{OUT}) ..... –0.50V to V_{DD}+0.5V
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{IN}) ..... +2.375V to +3.465V
Ambient Temperature (T_A) ..... –40°C to +75°C
Junction Thermal Resistance
TSSOP (θ_{JA}) ..... 150°C/W

DC Electrical Characteristics

V_{DD} = 2.5V ±5%; T_A = –40°C to +75°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Core Supply Voltage		2.375	2.50	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.50	2.625	V
I_{DD}	Core Supply Current	No load		12	20	mA
I_{DDA}	Analog Supply Current			48	55	mA

DC Electrical Characteristics

V_{DD} = 3.3V ±5%; T_A = -40°C to +75°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Core Supply Voltage		3.135	3.30	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.30	3.465	V
I_{DD}	Core Supply Current	No load		15	22	mA
I_{DDA}	Analog Supply Current			49	55	mA

LVCMOS DC Characteristics

V_{DD} = 2.5V and 3.3V ±5%; T_A = -40°C to +75°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage	V_{DD} = 3.3V ±5%	2		V_{DD} +0.3	V
		V_{DD} = 2.5V ±5%	1.7		V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage	V_{DD} = 3.3V ±5%	-0.30		0.80	V
		V_{DD} = 2.5V ±5%	-0.30		0.70	V
V_{OH}	Output HIGH Voltage	V_{DD} = 3.3V ±5%	2.6			V
		V_{DD} = 2.5V ±5%	1.8			V
V_{OL}	Output LOW Voltage				0.5	V
I_{IH}	Input HIGH Current	Output Enable input			5	µA
I_{IL}	Input LOW Current	Output Enable input	-150			µA
I_{IH}	Input HIGH Current	FSEL input			150	µA
I_{IL}	Input LOW Current	FSEL input	-5			µA

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.

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AC Electrical Characteristics

V_{DD} = 2.5V and 3.3V ±5%; T_A = -40°C to +75°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{OUT}	Output Frequency	FSEL=1	186.66	212.5	226.66	MHz
		FSEL=0	93.33	106.25	113.33	MHz
t_{JITTER}	RMS Phase Jitter	106.25MHz, Integration Range: 637kHz to 10MHz		510		fs
		212.50MHz Integration Range: 2.55MHz to 20MHz		320		fs
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		350	ps
ODC	Output Duty Cycle	106.25MHz	48		52	%
		212.50MHz	45		55	%

3.3V Carrier Frequency, 106.25MHz

Offset from Carrier	Measured Phase Noise	Unit
100Hz	-97	dBc/Hz
1kHz	-122	dBc/Hz
10kHz	-131	dBc/Hz
100kHz	-126	dBc/Hz
1MHz	-144	dBc/Hz
10MHz	-163	dBc/Hz
40MHz	-165	dBc/Hz

3.3V Carrier Frequency, 212.5MHz

Offset from Carrier	Measured Phase Noise	Unit
100Hz	-92	dBc/Hz
1kHz	-116	dBc/Hz
10kHz	-124	dBc/Hz
100kHz	-120	dBc/Hz
1MHz	-138	dBc/Hz
10MHz	-161	dBc/Hz
40MHz	-163	dBc/Hz

Crystal Characteristics

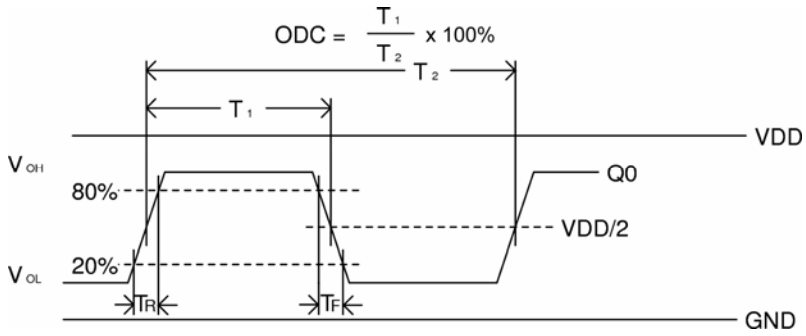
Parameter	Condition	Min	Typ	Max	Units
Mode of Oscillation		Fundamental Parallel Resonant			
Frequency			26.5625		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitor				7	pF
Drive Level				1	mW

Functional Description

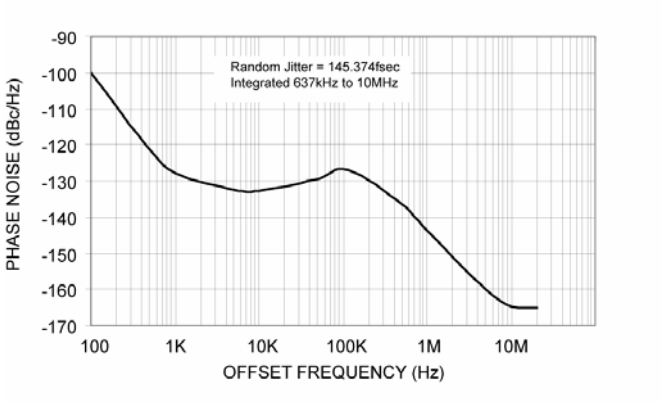
The SM840001 provides a high performance and high accuracy solution for a precision clock source at 106.25 or 212.50MHz derived from a low cost 26.5625MHz Xtal. A single 12mA LVCMOS output is provided with tri state capability, controlled via an external pin (OE).

The design of the SM840001 consumes very low power in the PLL due to a patented technology in the VCO and the associated dividers. The VCO range is ~3.2GHz to 3.5GHz providing high resolution and easy integer divide ratios. Output Divider ratios are fixed at either ÷15 or ÷30 controlled via the FSEL pin, and the feedback divider also fixed at ÷120. Duty Cycle is inherently improved and guarantees tight control and stability on this critical specification. The provides improved specifications for Duty Cycle, Jitter, Phase Noise, Power Consumption, and noise sensitivity. Additionally, the SM840001 will operate at either 3.3V or 2.5V supplies.

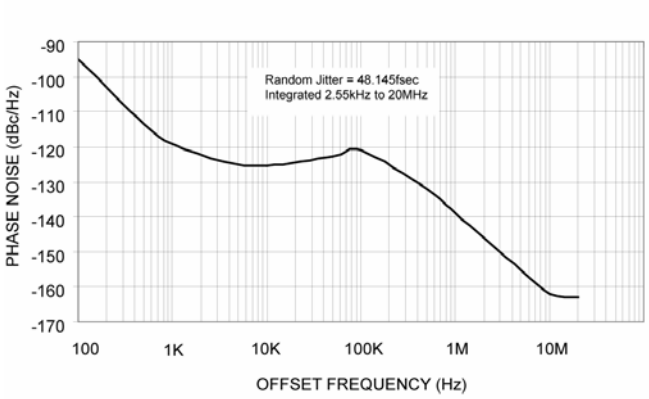
Switching Waveforms



RMS Phase Noise/Jitter



Phase Noise Plot: 106.25MHz @ 3.3V



Phase Noise Plot: 212.5MHz @ 3.3V

Power Supply Filtering

The SM840001 provides separate power supply pins to isolate any high switching noise from outputs to internal core blocks. VDD and VDDA should be individually connected to the power plane through vias. Bypass capacitors should be used for each pin. Figure 2 illustrates how the power supply filter for 3.3V and 2.5V is configured.

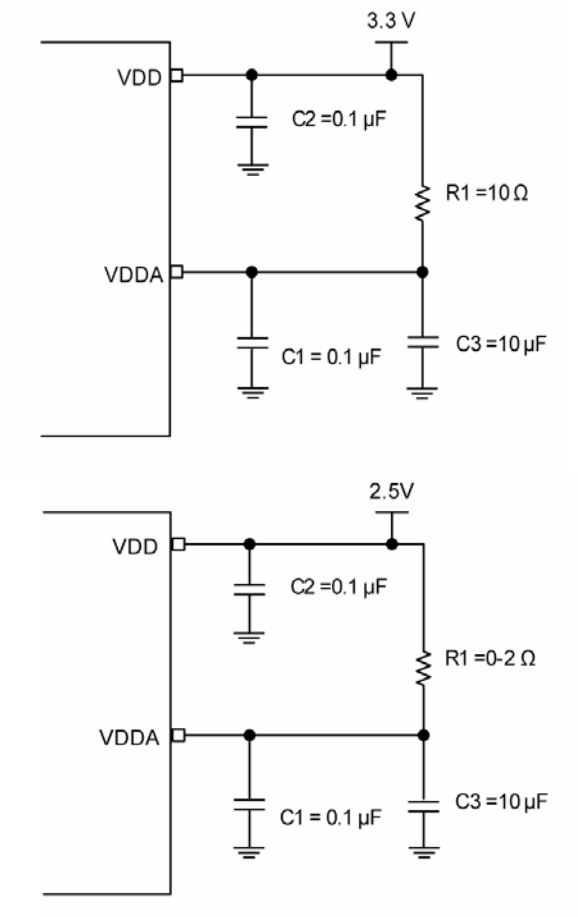
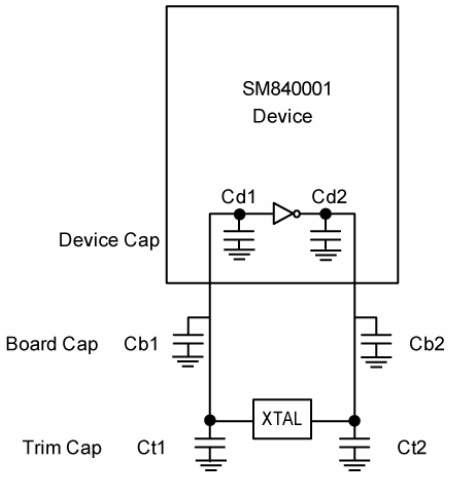


Figure 2.

Crystal Loading



Crystal Recommendations

This device requires a parallel resonance crystal. Substituting a series resonance crystal will cause this device to operate at the wrong frequency and violate the ppm specifications.

To achieve low ppm error, the total capacitance of the crystal must be considered in order to calculate appropriate capacitive loading (CL).

Load Capacitance at each side: Trim Capacitance = Ct = (2*CL-(Cb + Cd))

CL: Crystal load capacitance. Defined by manufacturer

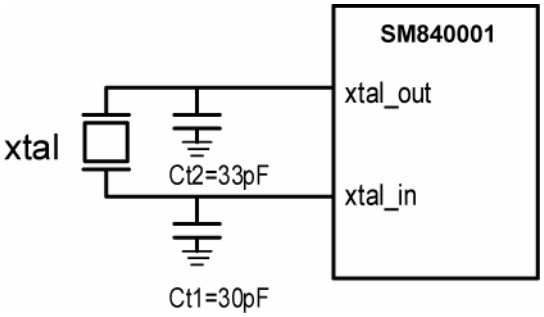
Ct: External trim capacitors. (Trimmed CL Load capacitance to get the right ppm)

Cb: Board capacitance (vias, traces, etc.)

Cd: Internal capacitance of the device (lead frame, bond wires, pin, etc.)

Equivalent Series Resistance (ESR) Max.	Cut	Load Cap.	Shunt Cap. Max.	Drive Max.
50Ω	AT	18pF	7pF	0.1mW

Crystal Input Interface



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Total capacitance seen by crystal = CL =

$$\frac{1}{\frac{1}{(Ct1 + Cb1 + Cd1)} + \frac{1}{(Ct2 + Cb2 + Cd2)}}$$

Example:

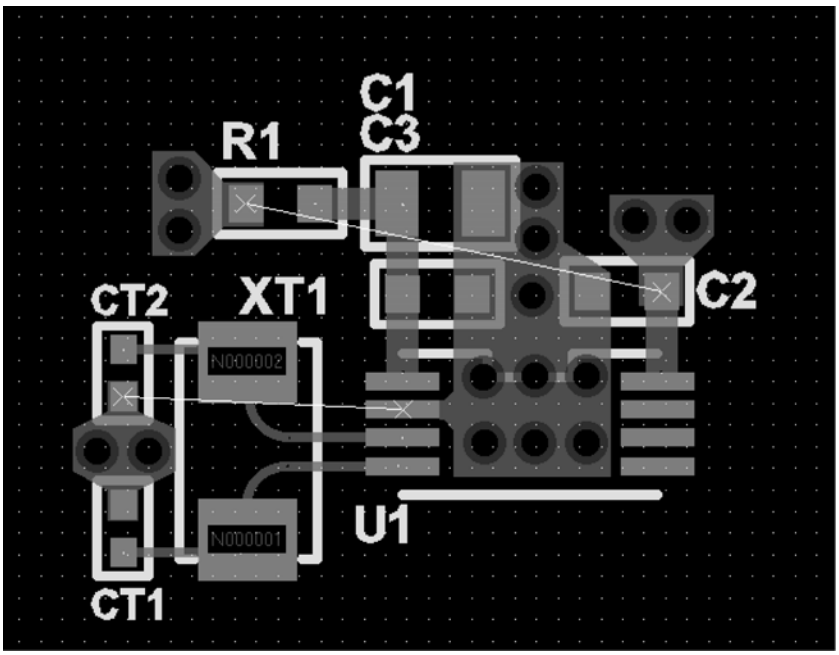
CL = 18pF, Cb = 2pF, Cd = 4pF

Trim Cap = Ct = 2 (18pF) - (2pF +4pF) = 30pF

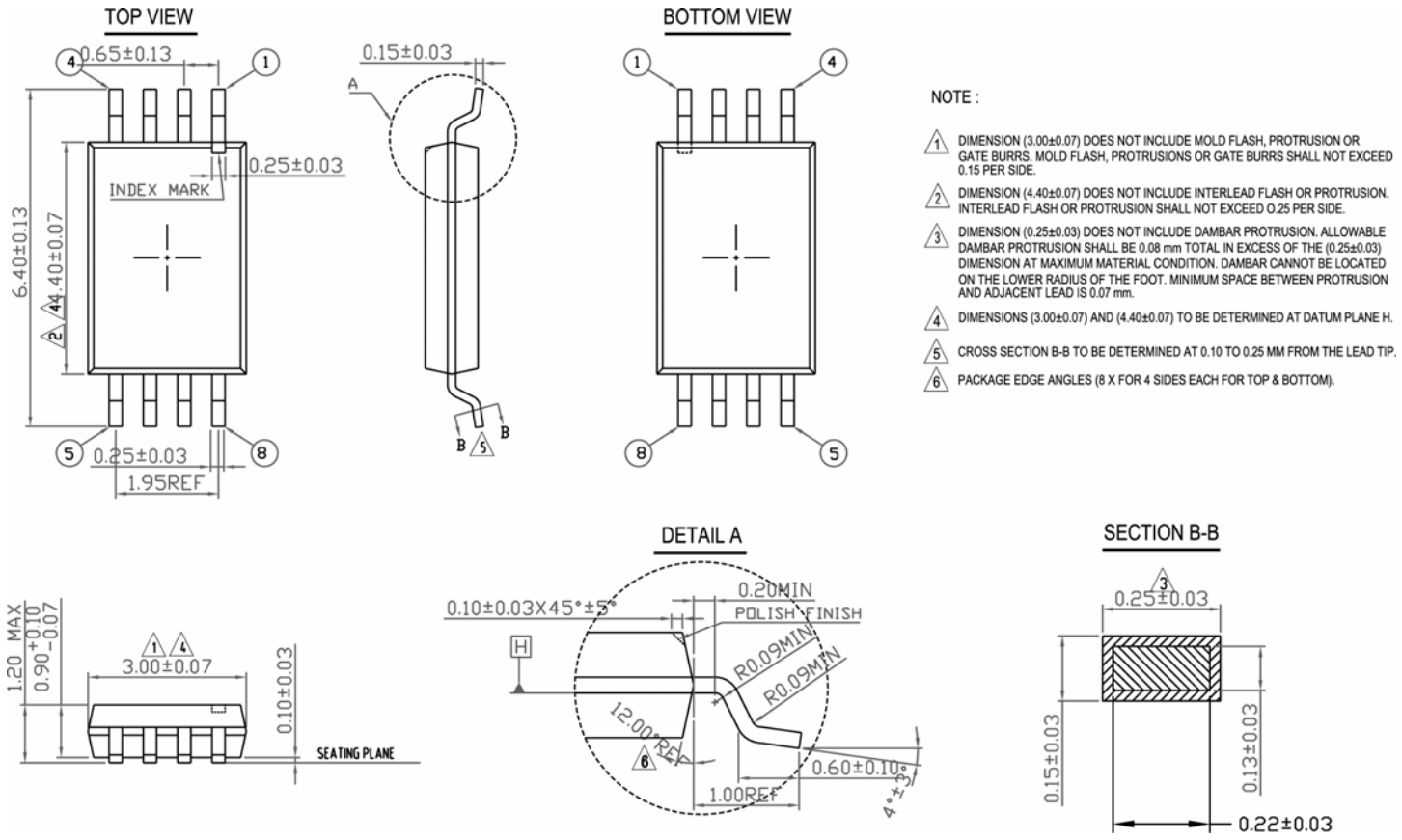
The SM843022 has been characterized with 25MHz, 18pF parallel resonant crystal. The trim capacitors Ct1 and Ct2 were optimized to minimize the ppm error.

To minimize the board capacitance, a short trace from pin to crystal footprint without vias is desirable. It is preferable to have ground shielding or distance between the crystal traces and noisy signals on the board.

Board Layout



Package Information



8-Pin TSSOP (K-8)

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