

## FEATURES

- Member of the Texas Instruments Widebus+™ Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 4.4 ns at 3.3 V
- Output Ports Have Equivalent 26- $\Omega$  Series Resistors, So No External Resistors Are Required
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Supports Mixed-Mode Signal Operation On All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## DESCRIPTION/ORDERING INFORMATION

This 32-bit buffer/driver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74LVCH322244A is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as eight 4-bit buffers, four 8-bit buffers, two 16-bit buffers, or one 32-bit buffer. It provides true outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The outputs, which are designed to sink up to 12 mA, include equivalent 26- $\Omega$  resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## ORDERING INFORMATION

| $T_A$         | PACKAGE <sup>(1)</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|---------------|-----------------------|------------------|
| –40°C to 85°C | LFBGA – GKE            | Tape and reel | SN74LVCH322244AKR     | CG244A           |
|               | LFBGA – ZKE (Pb-free)  |               | 74LVCH322244AZKER     |                  |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE (EACH 4-BIT BUFFER)

| INPUTS          |   | OUTPUT<br>Y |
|-----------------|---|-------------|
| $\overline{OE}$ | A |             |
| L               | H | H           |
| L               | L | L           |
| H               | X | Z           |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus+ is a trademark of Texas Instruments.

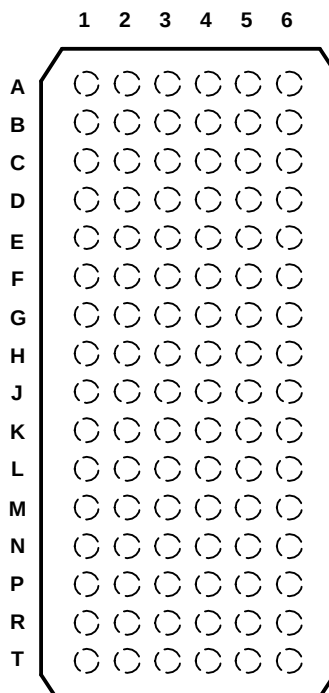
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2002–2005, Texas Instruments Incorporated

**SN74LVCH322244A**  
**32-BIT BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

SCES405B–JULY 2002–REVISED APRIL 2005

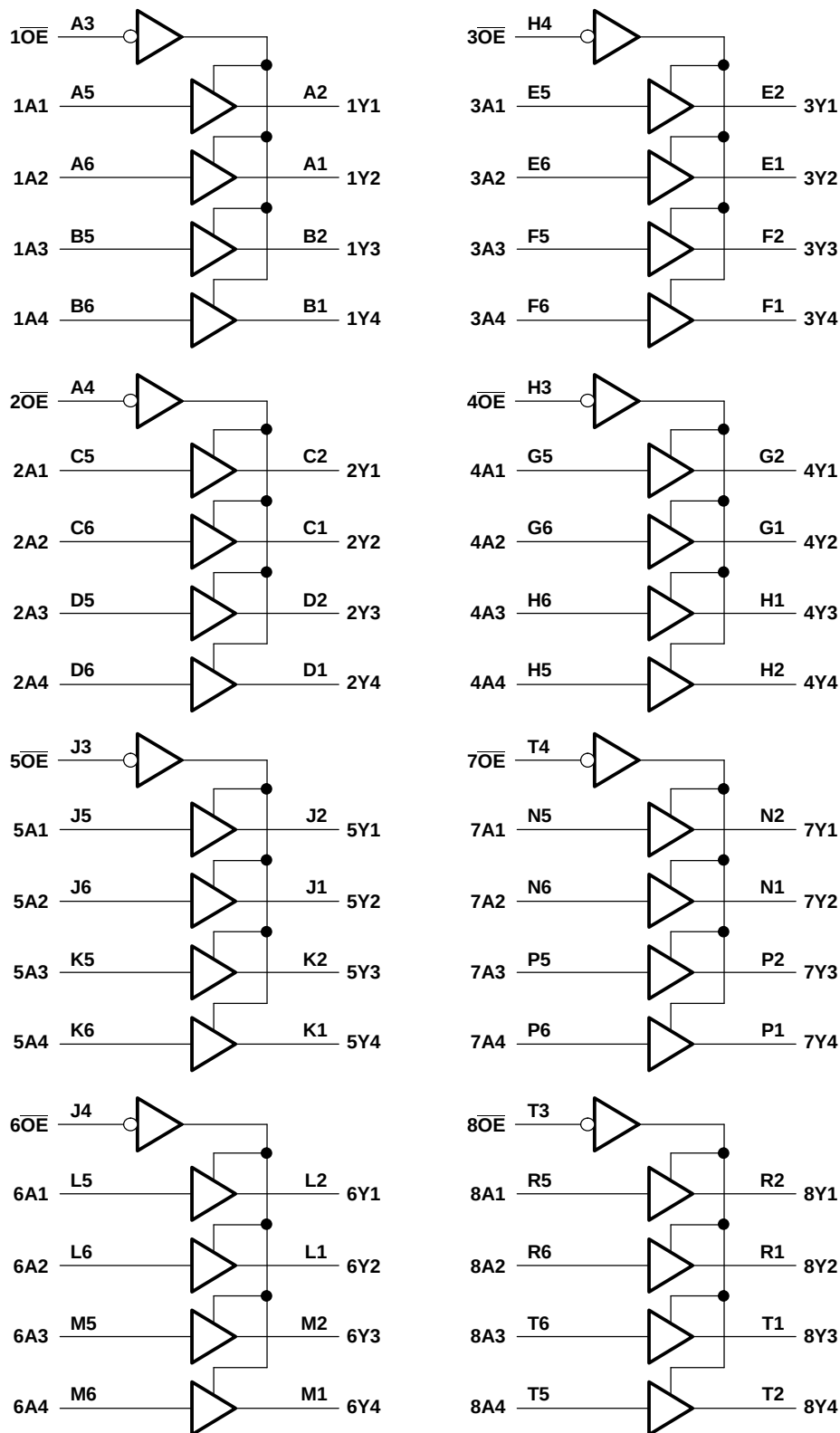
**GKE OR ZKE PACKAGE**  
**(TOP VIEW)**



**TERMINAL ASSIGNMENTS**

|          | 1   | 2   | 3                        | 4                        | 5   | 6   |
|----------|-----|-----|--------------------------|--------------------------|-----|-----|
| <b>A</b> | 1Y2 | 1Y1 | 1 $\overline{\text{OE}}$ | 2 $\overline{\text{OE}}$ | 1A1 | 1A2 |
| <b>B</b> | 1Y4 | 1Y3 | GND                      | GND                      | 1A3 | 1A4 |
| <b>C</b> | 2Y2 | 2Y1 | V <sub>CC</sub>          | V <sub>CC</sub>          | 2A1 | 2A2 |
| <b>D</b> | 2Y4 | 2Y3 | GND                      | GND                      | 2A3 | 2A4 |
| <b>E</b> | 3Y2 | 3Y1 | GND                      | GND                      | 3A1 | 3A2 |
| <b>F</b> | 3Y4 | 3Y3 | V <sub>CC</sub>          | V <sub>CC</sub>          | 3A3 | 3A4 |
| <b>G</b> | 4Y2 | 4Y1 | GND                      | GND                      | 4A1 | 4A2 |
| <b>H</b> | 4Y3 | 4Y4 | 4 $\overline{\text{OE}}$ | 3 $\overline{\text{OE}}$ | 4A4 | 4A3 |
| <b>J</b> | 5Y2 | 5Y1 | 5 $\overline{\text{OE}}$ | 6 $\overline{\text{OE}}$ | 5A1 | 5A2 |
| <b>K</b> | 5Y4 | 5Y3 | GND                      | GND                      | 5A3 | 5A4 |
| <b>L</b> | 6Y2 | 6Y1 | V <sub>CC</sub>          | V <sub>CC</sub>          | 6A1 | 6A2 |
| <b>M</b> | 6Y4 | 6Y3 | GND                      | GND                      | 6A3 | 6A4 |
| <b>N</b> | 7Y2 | 7Y1 | GND                      | GND                      | 7A1 | 7A2 |
| <b>P</b> | 7Y4 | 7Y3 | V <sub>CC</sub>          | V <sub>CC</sub>          | 7A3 | 7A4 |
| <b>R</b> | 8Y2 | 8Y1 | GND                      | GND                      | 8A1 | 8A2 |
| <b>T</b> | 8Y3 | 8Y4 | 8 $\overline{\text{OE}}$ | 7 $\overline{\text{OE}}$ | 8A4 | 8A3 |

LOGIC DIAGRAM (POSITIVE LOGIC)



# SN74LVCH322244A

## 32-BIT BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

SCES405B—JULY 2002—REVISED APRIL 2005



#### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|               |                                                                                             | MIN             | MAX            | UNIT |
|---------------|---------------------------------------------------------------------------------------------|-----------------|----------------|------|
| $V_{CC}$      | Supply voltage range                                                                        | −0.5            | 6.5            | V    |
| $V_I$         | Input voltage range <sup>(2)</sup>                                                          | −0.5            | 6.5            | V    |
| $V_O$         | Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup> | −0.5            | 6.5            | V    |
| $V_O$         | Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>              | −0.5            | $V_{CC} + 0.5$ | V    |
| $I_{IK}$      | Input clamp current                                                                         | $V_I < 0$       | −50            | mA   |
| $I_{OK}$      | Output clamp current                                                                        | $V_O < 0$       | −50            | mA   |
| $I_O$         | Continuous output current                                                                   |                 | ±50            | mA   |
|               | Continuous current through each $V_{CC}$ or GND                                             |                 | ±100           | mA   |
| $\theta_{JA}$ | Package thermal impedance <sup>(4)</sup>                                                    | GKE/ZKE package | 40             | °C/W |
| $T_{stg}$     | Storage temperature range                                                                   | −65             | 150            | °C   |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

#### Recommended Operating Conditions<sup>(1)</sup>

|                     |                                    | MIN                                          | MAX                  | UNIT     |
|---------------------|------------------------------------|----------------------------------------------|----------------------|----------|
| $V_{CC}$            | Supply voltage                     | Operating                                    | 1.65                 | 3.6      |
|                     |                                    | Data retention only                          | 1.5                  |          |
| $V_{IH}$            | High-level input voltage           | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | $0.65 \times V_{CC}$ | V        |
|                     |                                    | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$   | 1.7                  |          |
|                     |                                    | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$   | 2                    |          |
| $V_{IL}$            | Low-level input voltage            | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | $0.35 \times V_{CC}$ | V        |
|                     |                                    | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$   | 0.7                  |          |
|                     |                                    | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$   | 0.8                  |          |
| $V_I$               | Input voltage                      | 0                                            | 5.5                  | V        |
| $V_O$               | Output voltage                     | High or low state                            | 0                    | $V_{CC}$ |
|                     |                                    | 3-state                                      | 0                    | 5.5      |
| $I_{OH}$            | High-level output current          | $V_{CC} = 1.65 \text{ V}$                    | −2                   | mA       |
|                     |                                    | $V_{CC} = 2.3 \text{ V}$                     | −4                   |          |
|                     |                                    | $V_{CC} = 2.7 \text{ V}$                     | −8                   |          |
|                     |                                    | $V_{CC} = 3 \text{ V}$                       | −12                  |          |
| $I_{OL}$            | Low-level output current           | $V_{CC} = 1.65 \text{ V}$                    | 2                    | mA       |
|                     |                                    | $V_{CC} = 2.3 \text{ V}$                     | 4                    |          |
|                     |                                    | $V_{CC} = 2.7 \text{ V}$                     | 8                    |          |
|                     |                                    | $V_{CC} = 3 \text{ V}$                       | 12                   |          |
| $\Delta t/\Delta v$ | Input transition rise or fall rate |                                              | 10                   | ns/V     |
| $T_A$               | Operating free-air temperature     | −40                                          | 85                   | °C       |

- (1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                | TEST CONDITIONS                                                              |                    | V <sub>CC</sub> | MIN                   | TYP <sup>(1)</sup> | MAX  | UNIT |
|--------------------------|------------------------------------------------------------------------------|--------------------|-----------------|-----------------------|--------------------|------|------|
| V <sub>OH</sub>          | I <sub>OH</sub> = −100 μA                                                    |                    | 1.65 V to 3.6 V | V <sub>CC</sub> − 0.2 |                    |      | V    |
|                          | I <sub>OH</sub> = −2 mA                                                      |                    | 1.65 V          | 1.2                   |                    |      |      |
|                          | I <sub>OH</sub> = −4 mA                                                      |                    | 2.3 V           | 1.7                   |                    |      |      |
|                          |                                                                              |                    | 2.7 V           | 2.2                   |                    |      |      |
|                          | I <sub>OH</sub> = −6 mA                                                      |                    | 3 V             | 2.4                   |                    |      |      |
|                          | I <sub>OH</sub> = −8 mA                                                      |                    | 2.7 V           | 2                     |                    |      |      |
| I <sub>OH</sub> = −12 mA |                                                                              | 3 V                | 2               |                       |                    |      |      |
| V <sub>OL</sub>          | I <sub>OL</sub> = 100 μA                                                     |                    | 1.65 V to 3.6 V |                       |                    | 0.2  | V    |
|                          | I <sub>OL</sub> = 2 mA                                                       |                    | 1.65 V          |                       |                    | 0.45 |      |
|                          | I <sub>OL</sub> = 4 mA                                                       |                    | 2.3 V           |                       |                    | 0.7  |      |
|                          |                                                                              |                    | 2.7 V           |                       |                    | 0.4  |      |
|                          | I <sub>OL</sub> = 6 mA                                                       |                    | 3 V             |                       |                    | 0.55 |      |
|                          | I <sub>OL</sub> = 8 mA                                                       |                    | 2.7 V           |                       |                    | 0.6  |      |
| I <sub>OL</sub> = 12 mA  |                                                                              | 3 V                |                 |                       | 0.8                |      |      |
| I <sub>I</sub>           | V <sub>I</sub> = 0 to 5.5 V                                                  |                    | 3.6 V           |                       |                    | ±5   | μA   |
| I <sub>I(hold)</sub>     | V <sub>I</sub> = 0.58 V                                                      |                    | 1.65 V          | (2)                   |                    |      | μA   |
|                          | V <sub>I</sub> = 1.07 V                                                      |                    |                 | (2)                   |                    |      |      |
|                          | V <sub>I</sub> = 0.7 V                                                       |                    | 2.3 V           | 45                    |                    |      |      |
|                          | V <sub>I</sub> = 1.7 V                                                       |                    |                 | −45                   |                    |      |      |
|                          | V <sub>I</sub> = 0.8 V                                                       |                    | 3 V             | 75                    |                    |      |      |
|                          | V <sub>I</sub> = 2 V                                                         |                    |                 | −75                   |                    |      |      |
|                          | V <sub>I</sub> = 0 to 3.6 V <sup>(3)</sup>                                   |                    | 3.6 V           | ±500                  |                    |      |      |
| I <sub>off</sub>         | V <sub>I</sub> or V <sub>O</sub> = 5.5 V                                     |                    | 0               |                       |                    | ±10  | μA   |
| I <sub>OZ</sub>          | V <sub>O</sub> = 0 to 5.5 V                                                  |                    | 3.6 V           |                       |                    | ±10  | μA   |
| I <sub>CC</sub>          | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | I <sub>O</sub> = 0 | 3.6 V           |                       |                    | 40   | μA   |
|                          | 3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>(4)</sup>                                |                    |                 |                       |                    | 40   |      |
| ΔI <sub>CC</sub>         | One input at V <sub>CC</sub> − 0.6 V, Other inputs at V <sub>CC</sub> or GND |                    | 2.7 V to 3.6 V  |                       |                    | 500  | μA   |
| C <sub>i</sub>           | V <sub>I</sub> = V <sub>CC</sub> or GND                                      |                    | 3.3 V           | 5.5                   |                    |      | pF   |
| C <sub>o</sub>           | V <sub>O</sub> = V <sub>CC</sub> or GND                                      |                    | 3.3 V           | 6                     |                    |      | pF   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This information was not available at the time of publication.

(3) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(4) This applies in the disabled state only.

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | V <sub>CC</sub> = 1.8 V<br>± 0.15 V |     | V <sub>CC</sub> = 2.5 V<br>± 0.2 V |     | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     | UNIT |
|------------------|-----------------|----------------|-------------------------------------|-----|------------------------------------|-----|-------------------------|-----|------------------------------------|-----|------|
|                  |                 |                | MIN                                 | MAX | MIN                                | MAX | MIN                     | MAX | MIN                                | MAX |      |
| t <sub>pd</sub>  | A               | Y              | (1)                                 | (1) | (1)                                | (1) | 1                       | 5.6 | 1.1                                | 4.4 | ns   |
| t <sub>en</sub>  | $\overline{OE}$ | Y              | (1)                                 | (1) | (1)                                | (1) | 1                       | 6.9 | 1                                  | 5.5 | ns   |
| t <sub>dis</sub> | $\overline{OE}$ | Y              | (1)                                 | (1) | (1)                                | (1) | 1                       | 6.8 | 1.8                                | 6.3 | ns   |

(1) This information was not available at the time of publication.

# SN74LVCH322244A

## 32-BIT BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

SCES405B—JULY 2002—REVISED APRIL 2005



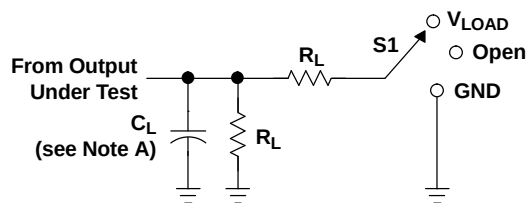
#### Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER |                                                    |                  | TEST<br>CONDITIONS  | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | UNIT |
|-----------|----------------------------------------------------|------------------|---------------------|-------------------------|-------------------------|-------------------------|------|
|           |                                                    |                  |                     | TYP                     | TYP                     | TYP                     |      |
| $C_{pd}$  | Power dissipation capacitance<br>per buffer/driver | Outputs enabled  | $f = 10\text{ MHz}$ | (1)                     | (1)                     | 35                      | pF   |
|           |                                                    | Outputs disabled |                     | (1)                     | (1)                     | 4                       |      |

(1) This information was not available at the time of publication.

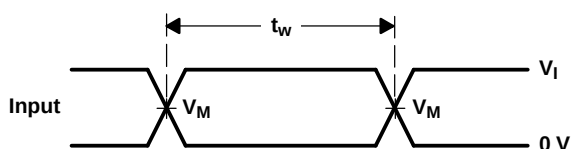
## PARAMETER MEASUREMENT INFORMATION



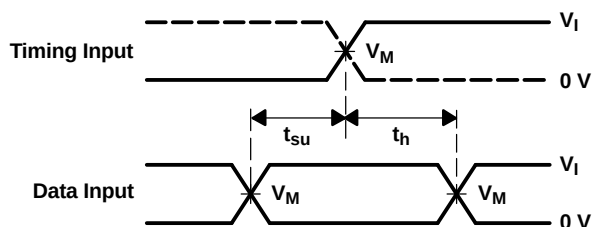
LOAD CIRCUIT

| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

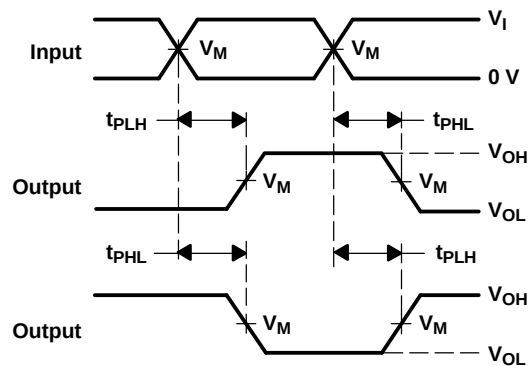
| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_r/t_f$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| 2.7 V                            | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |



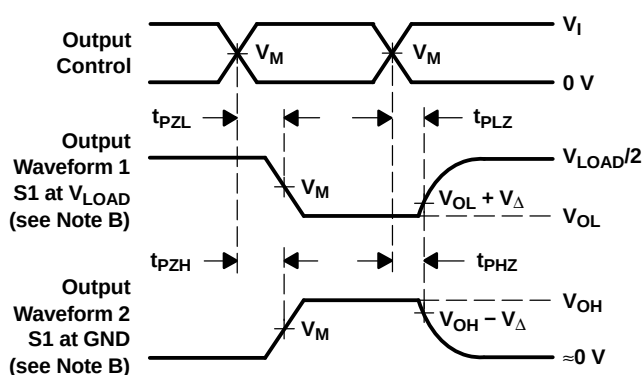
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable Device  | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|-------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|---------|
| 74LVCH322244AZKER | NRND          | LFBGA        | ZKE                | 96   | 1000           | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-3-260C-168 HR  | -40 to 85    | CG244A                  |         |
| SN74LVCH322244AKR | NRND          | LFBGA        | GKE                | 96   | 1000           | TBD                        | SNPB                    | Level-2-235C-1 YEAR  | -40 to 85    | CG244A                  |         |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

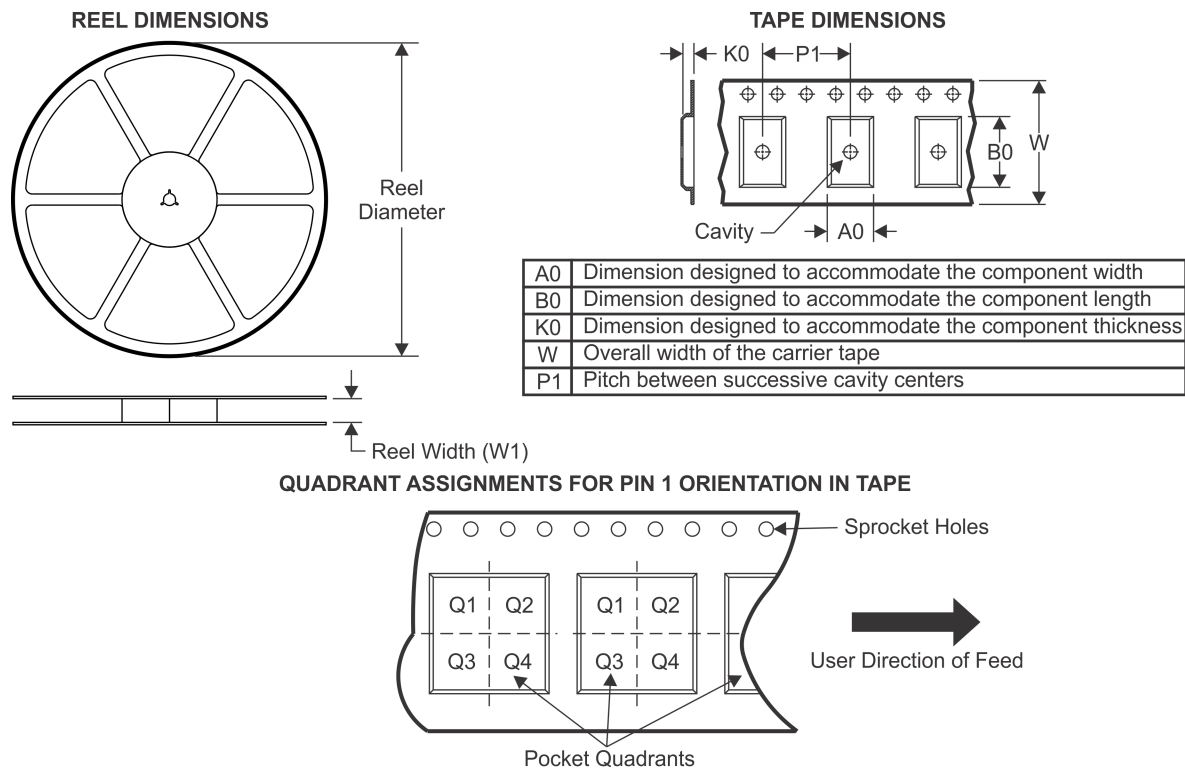
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

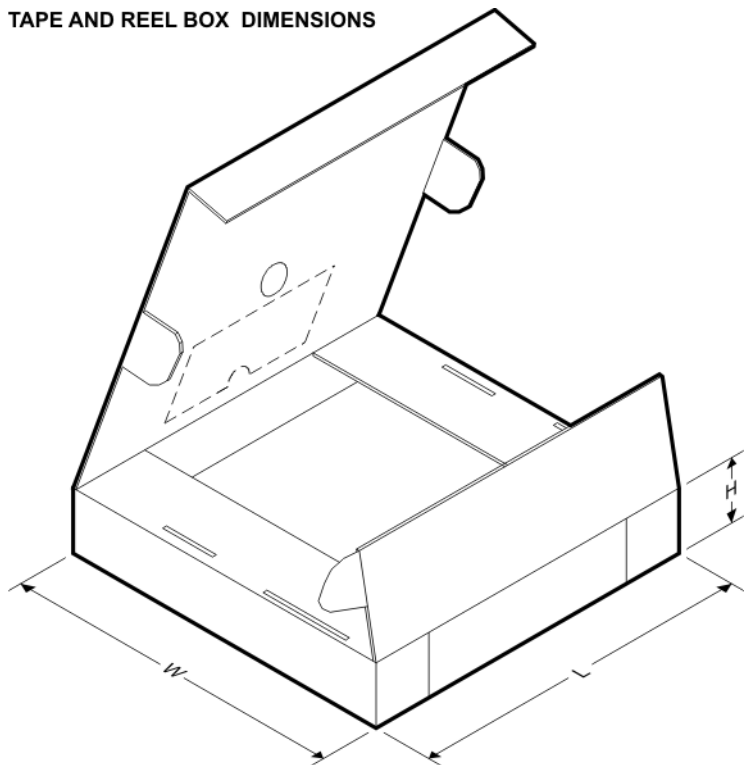


**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

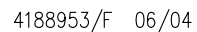
| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74LVCH322244AZKER | LFBGA        | ZKE             | 96   | 1000 | 330.0              | 24.4               | 5.7     | 13.7    | 2.0     | 8.0     | 24.0   | Q1            |
| SN74LVCH322244AKR | LFBGA        | GKE             | 96   | 1000 | 330.0              | 24.4               | 5.7     | 13.7    | 2.0     | 8.0     | 24.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

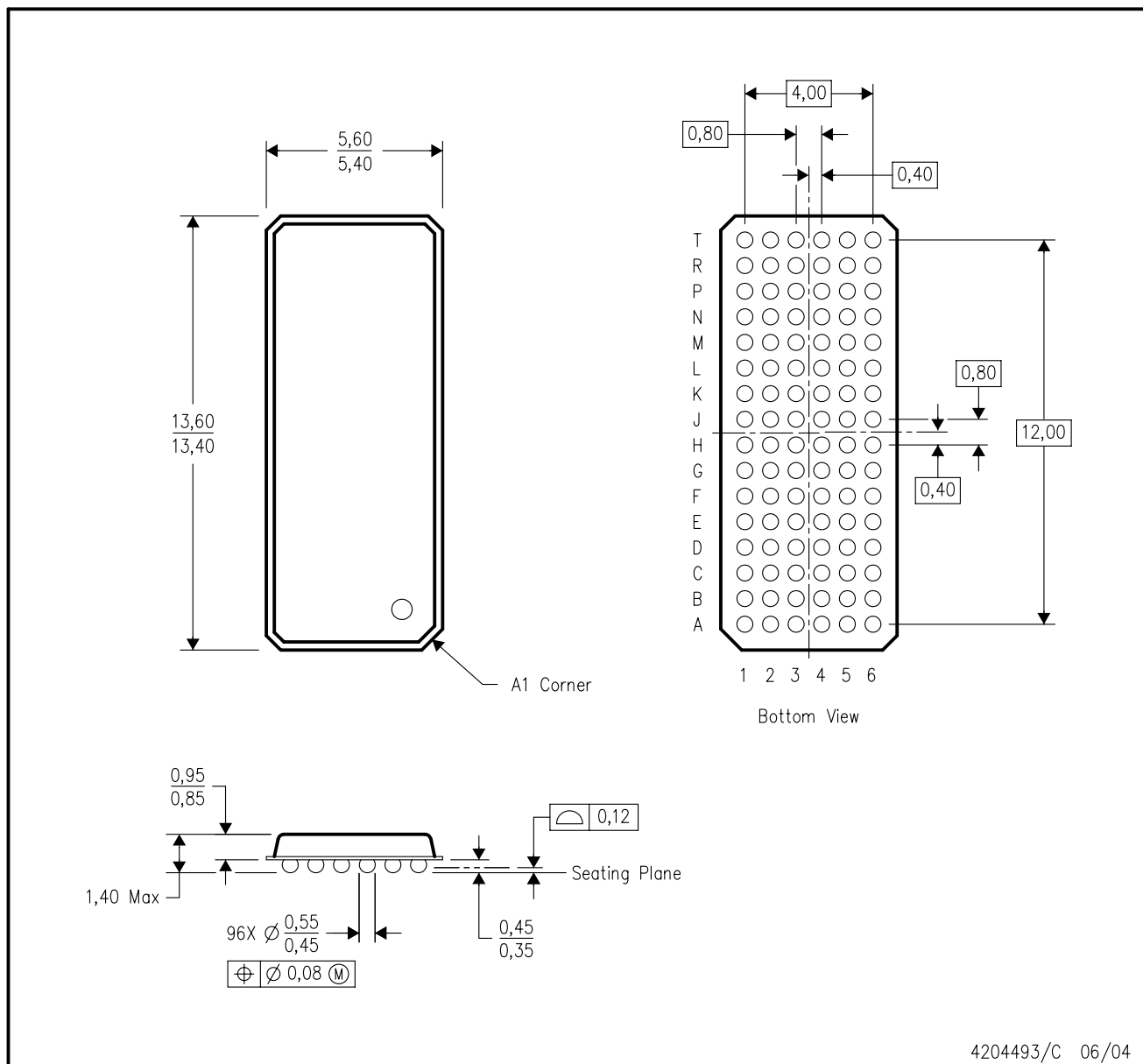
| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 74LVCH322244AZKER | LFBGA        | ZKE             | 96   | 1000 | 336.6       | 336.6      | 41.3        |
| SN74LVCH322244AKR | LFBGA        | GKE             | 96   | 1000 | 336.6       | 336.6      | 41.3        |



NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Falls within JEDEC MO-205 variation CC.  
D. This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.

ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



4204493/C 06/04

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-205 variation CC.
  - D. This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2019, Texas Instruments Incorporated