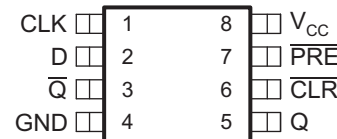


SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

FEATURES

- Qualified for Automotive Applications
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 6.9 ns at 3.3 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DCU PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This single positive-edge-triggered D-type flip-flop is designed for 1.65-V to 5.5-V V_{CC} operation.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) input sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
-40°C to 125°C	VSSOP – DCU	Reel of 3000	SN74LVC2G74QDCURQ1	C74_

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) DCU: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

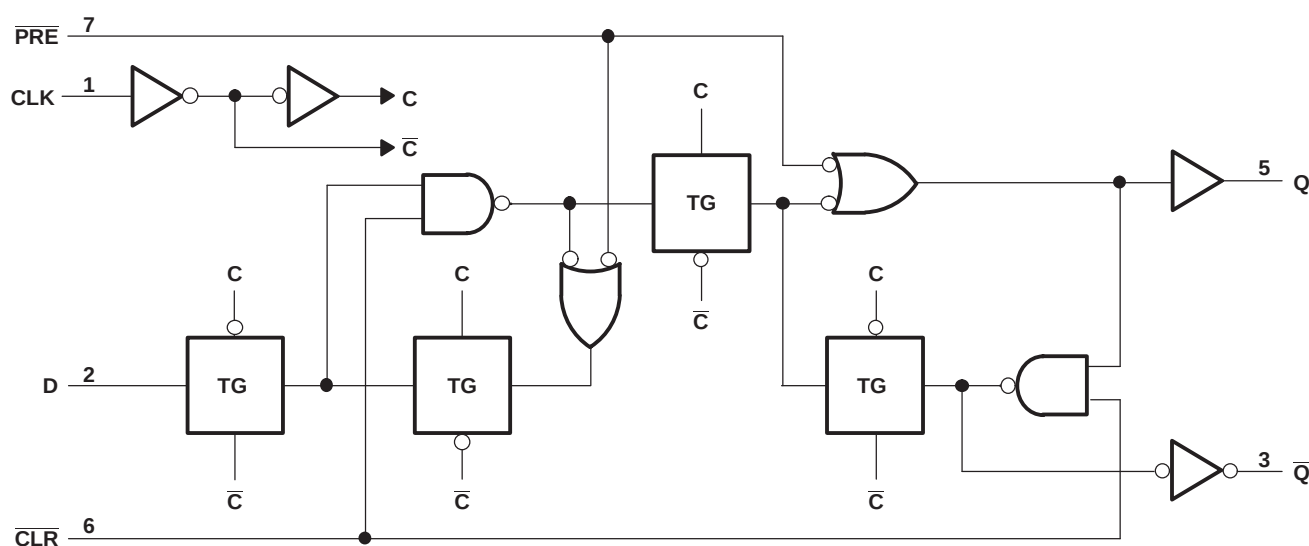


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FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H ⁽¹⁾	H ⁽¹⁾
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	$\overline{\text{Q}}_0$

- (1) This configuration is nonstable; that is, it does not persist when $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

LOGIC DIAGRAM (POSITIVE LOGIC)

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	6.5	V
V_I	Input voltage range ⁽²⁾	–0.5	6.5	
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	6.5	
V_O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	–0.5	$V_{CC} + 0.5$	
I_{IK}	Input clamp current	$V_I < 0$	–50	mA
I_{OK}	Output clamp current	$V_O < 0$	–50	
I_O	Continuous output current		±50	
	Continuous current through V_{CC} or GND		±100	
θ_{JA}	Package thermal impedance ⁽⁴⁾		227	°C/W
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the recommended operating conditions table.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 3 V to 3.6 V	2		
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 3 V to 3.6 V	0.8		
		V _{CC} = 4.5 V to 5.5 V	0.3 × V _{CC}		
V _I	Input voltage	0	5.5	V	
V _O	Output voltage	0	V _{CC}	V	
I _{OH}	High-level output current	V _{CC} = 1.65 V	–4		mA
		V _{CC} = 2.3 V	–8		
		V _{CC} = 3 V	–16		
			–24		
I _{OL}	Low-level output current	V _{CC} = 4.5 V	–24		mA
		V _{CC} = 1.65 V	4		
		V _{CC} = 2.3 V	8		
		V _{CC} = 3 V	16		
24					
Δt/Δv	Input transition rise or fall rate	V _{CC} = 4.5 V	24		ns/V
		V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V	20		
		V _{CC} = 3.3 V ± 0.3 V	10		
		V _{CC} = 5 V ± 0.5 V	5		
T _A	Operating free-air temperature	–40	125	°C	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}		I _{OH} = –100 µA	1.65 V to 5.5 V	V _{CC} – 0.1			V
		I _{OH} = –4 mA	1.65 V	1.2			
		I _{OH} = –8 mA	2.3 V	1.85			
		I _{OH} = –16 mA	3 V	2.4			
		I _{OH} = –24 mA	3 V	2.3			
			4.5 V	3.8			
V _{OL}		I _{OL} = 100 µA	1.65 V to 5.5 V			0.1	V
		I _{OL} = 4 mA	1.65 V			0.45	
		I _{OL} = 8 mA	2.3 V			0.3	
		I _{OL} = 16 mA	3 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
			4.5 V			0.55	
I _I	Data or control inputs	V _I = 5.5 V or GND	0 to 5.5 V			±5	µA
I _{off}		V _I or V _O = 5.5 V	0			±10	µA
I _{CC}		V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V			10	µA
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V			500	µA
C _I		V _I = V _{CC} or GND	3.3 V			5	pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

		V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	V _{CC} = 5 V ± 0.5 V	UNIT	
		MIN MAX	MIN MAX	MIN MAX	MIN MAX		
f _{clock}		80	120	120	140	MHz	
t _w	Pulse duration	CLK	6.2	3.5	3.5	3.3	ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	6.2	3.5	3.5	3.3	
t _{su}	Setup time before CLK↑	Data	3.5	2.3	1.9	1.7	ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	2.5	2	1.8	1.6	
t _h	Hold time, data after CLK↑		0	0.3	0.5	0.8	ns

Switching Characteristics

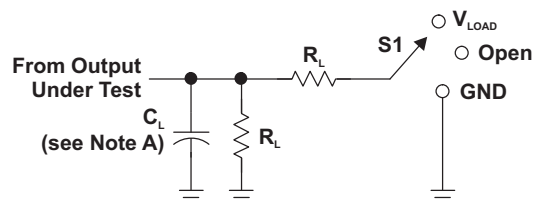
over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			80		120		120		140		MHz
t _{pd}	CLK	Q	4.8	14.4	2.2	8.1	2.2	6.9	1.4	5.1	ns
		$\overline{\text{Q}}$	6	16	3	9.7	2.6	7.2	1.6	5.4	
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	4.4	14.9	2.3	9.5	1.7	7.9	1.6	6.1	

Operating Characteristics $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	$V_{CC} = 5\text{ V}$	UNIT
		TYP	TYP	TYP	TYP	
C_{pd} Power dissipation capacitance	$f = 10\text{ MHz}$	35	35	37	40	pF

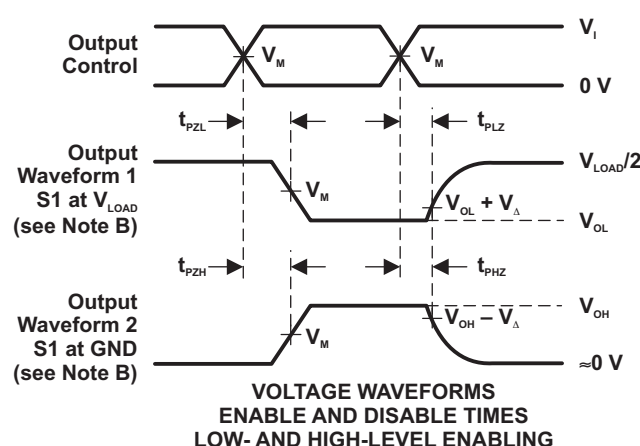
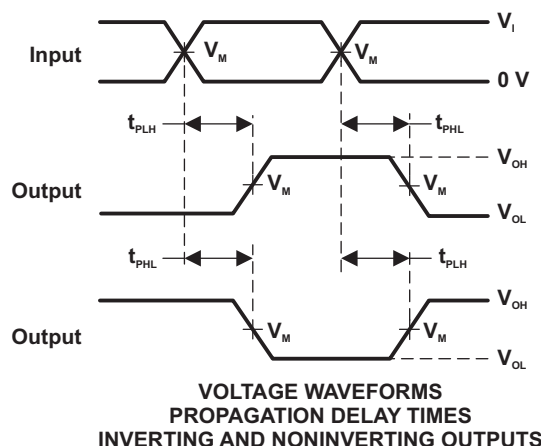
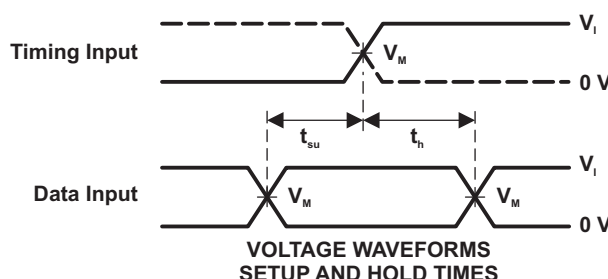
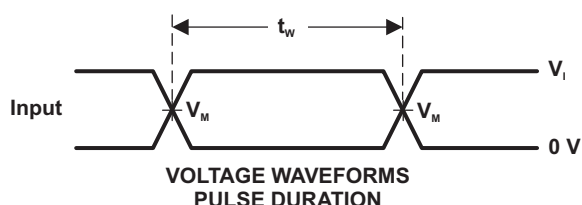
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_i/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CLVC2G74QDCURG4Q1	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74R	Samples
SN74LVC2G74QDCURQ1	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C74R	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVC2G74-Q1 :

- Catalog: [SN74LVC2G74](#)
- Enhanced Product: [SN74LVC2G74-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G74QDCURQ1	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

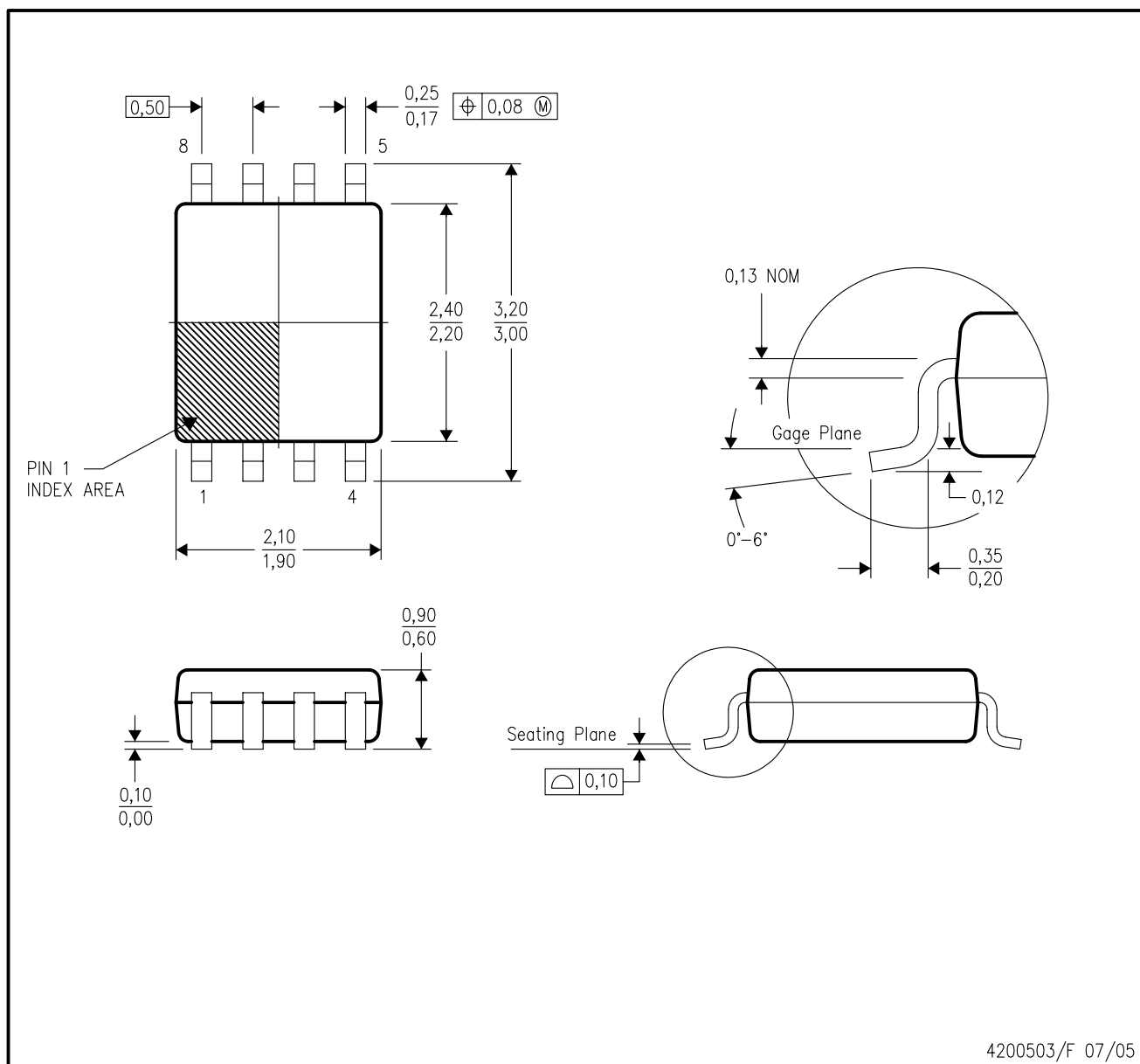


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G74QDCURQ1	VSSOP	DCU	8	3000	202.0	201.0	28.0

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)

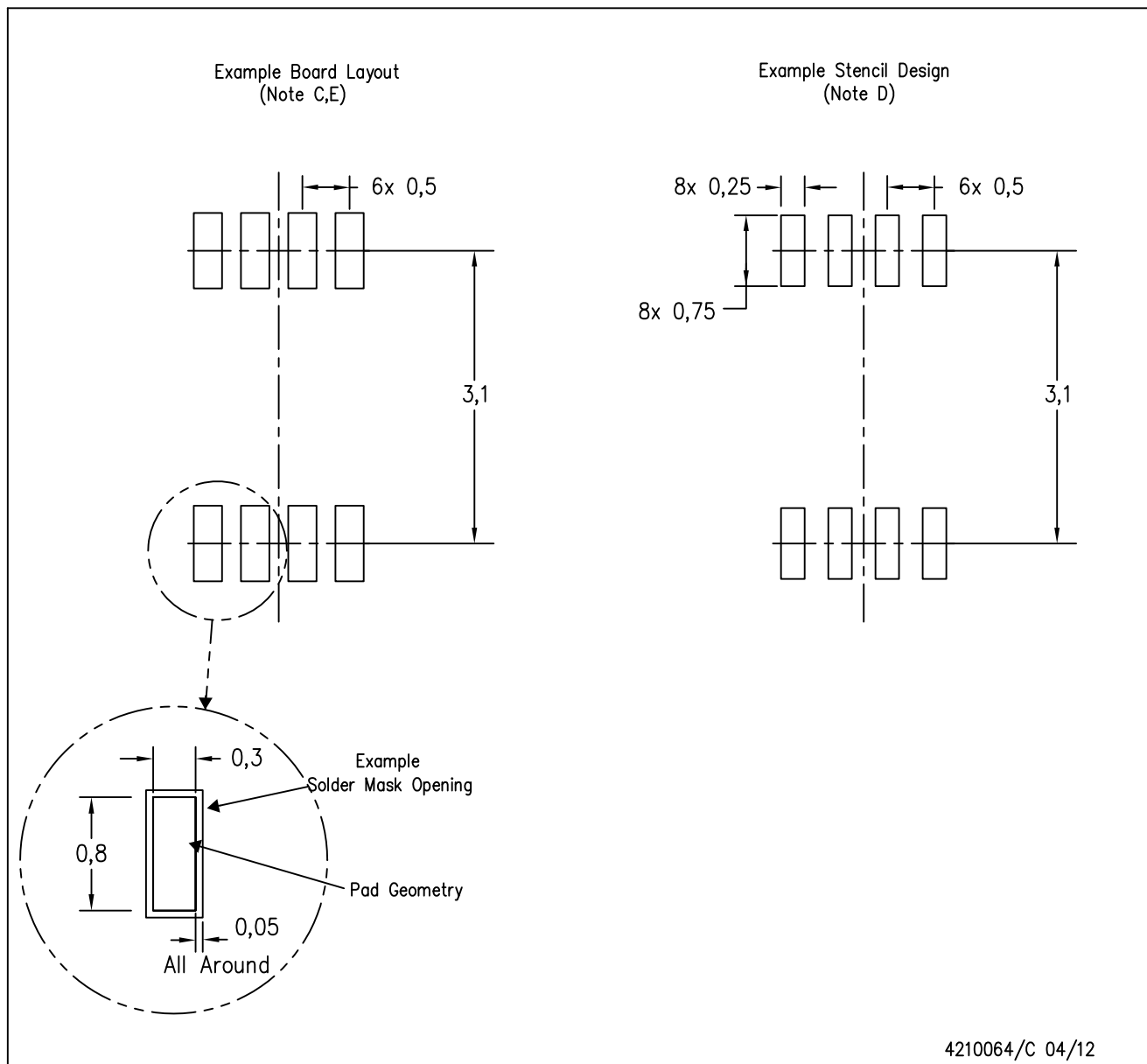


NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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