NXP Semiconductors
User Guide

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S32R274/372 EVB User Guide

by : NXP Semiconductors

1. Introduction

This user guide details the setup and configuration of the NXP S32R274/372 Evaluation Board (hereafter referred to as the EVB). The EVB is intended to provide a mechanism for easy customer evaluation of the S32Rxx family of microprocessors, and to facilitate hardware and software development.

At the time of writing this document, the S32Rxx family form the basis of the RADAR specific 55nm devices. For the latest product information, please speak to your NXP representative or consult the S32Rxx at www.nxp.com.

The EVB is intended for bench / laboratory use and has been designed using normal temperature specified components (+70°C).

1.1. List of acronyms

Table 1 provides a list and description of acronyms used throughout this document.

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Table 1. List of acronyms

Acronym	Description
1.25V_SR	Supply voltage from the 1.25 V switching regulator
3.3V_SR	Supply voltage from the 3.3 V switching regulator
5V_LR	Supply voltage from the 5.0 V linear regulator
5V_SR	Supply voltage from the 5.0 V switching regulator
ADC	Analog-to-Digital converter
RESET_B	External signal reset
EVB	Evaluation board
FEC	Fast ethernet controller module
GND	Ground
HV	High voltage (3.3 V and/or 5 V)
LED	Light emitting diode
LV	Low voltage (1.25 V)
MCU	Microcontroller
OSC	Oscillator
P12V	12 V EVB supply power domain
VREG_POR_B	Power-on reset
PWR	Power
RX	Receive
SIPI	Serial Interprocessor Interface
TBD	To be defined
TX	Transmit
VSS	Ground

1.2. Modular concept

For maximum flexibility and simplicity, the EVB has been designed as a modular development platform. The EVB main board does not contain an MCU. Instead, the MCU is fitted to an MCU daughter card (occasionally referred to as an adapter board). This approach means that the same EVB platform can be used for multiple packages and MCU derivatives within the MPC57xx and further families. High density connectors provide the interface between the EVB and MCU daughter cards as shown in the diagram below. See section 3.7 for more details on the daughter cards and section 4.8 for more details on the interface connectors.

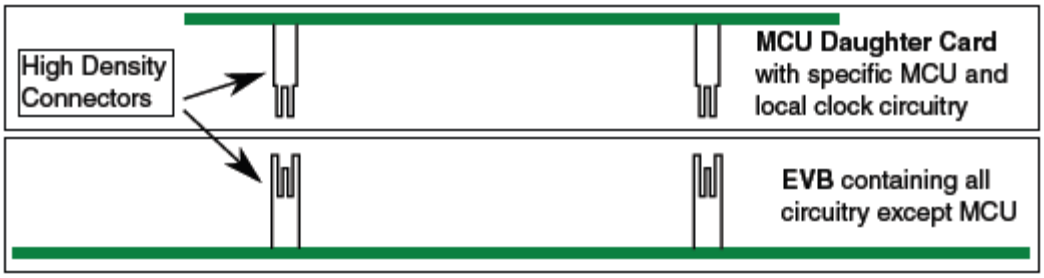

Figure 1. Modular concept – Mother board and MCU daughter card

Please consult the website at **www.nxp.com** or speak to your NXP representative for more details on the availability of MCU daughter cards.

NOTE

For details on your specific daughter card, please consult the instructions included with the daughter card.

The EVB is designed to use the motherboard and the daughter card in conjunction. However, it is possible to use the daughter cards standalone.

1.3. Daughter card availability

A number of compatible daughter cards are available for the motherboard across a number of devices. Table 2 gives an overview of daughter cards that can be used with MPC57xx motherboard and associated devices, package sizes and part numbers.

Table 2. Daughter card overview

Daughter card number	Device	Package	Socket	Nexus
S32R274RRUEVB	S32R274	257BGA	Yes	Yes
S32R372RRSEVB	S32R372	257BGA	Yes	Yes

All daughter cards will be similar in design and concept. For details on the daughter cards please refer to section 3.7. It should be noted that both daughtercards listed are the same physical board, but separate part numbers exist in order to differentiate between the silicon part included in the box. Both S32R274 and S32R372 257BGA package devices are supported by either daughtercard part number as they are pin compatible. Some features of the EVB are not supported by the S32R372 device however, please see the S32R372 device reference manual for a full list of the differences between the devices.

2. EVB features

The EVB system consists of a motherboard and a daughter card, both with distinct features.
The **mother board** provides the following key features:

- Support provided for different MCUs by utilising MCU daughter cards

- Single 12 V external power supply input with four on-board regulators providing all of the necessary EVB and MCU voltages; Power supplied to the EVB via a 2.1 mm barrel style power jack or a 2-way level connector; 12 V operation allows in-car use if desired
- Master power switch and regulator status LEDs
- Two 240-way high-density daughter card expansion connectors allowing connection of the MCU daughter card or a custom board for additional application specific circuitry
- All MCU signals readily accessible at a port-ordered group of 0.1” pitch headers
- RS232/SCI physical interface and standard DB9 female connector
- FlexRAY interface
- LINFlexD interface
- Two CAN interfaces, one configurable to be connected to one out of two CAN modules, and one connected to a dedicated third CAN module
- Ethernet interface
- Variable resistor, driving between 5 V and ground
- Four user switches and four user LEDs, freely connectable
- Liberal scattering of GND test points (surface mount loops) placed throughout the EVB

The **daughter cards** provide the following features:

- MCU (soldered or through a socket)
- Flexible MCU clocking options allow provision of an external clock via SMA connector or 40 MHz EVB clock oscillator circuit. Solder pads on the daughter card allow selection between these external clocks. SMA connectors (including differential clock input) on CLKIN signal for easy access.
- User reset switch with reset status LED
- Standard 14-pin JTAG debug connector and 34-pin Nexus Aurora connector
- 10-pin Serial Interprocessor Interface (SIPI) connector
- Gb Ethernet Physical interface IC, with RJ45 connector
- MIPI-CSI2 connector intended for use with Eagle MR3003 RADAR front end EVK (Evaluation Kit)
- Liberal scattering of ground and test points (surface mount loops) placed throughout the EVB

NOTE

To alleviate confusion between jumpers and headers, all EVB jumpers are implemented as 2 mm pitch whereas headers are 0.1 inch (2.54 mm). This prevents inadvertently fitting a jumper to a header.

CAUTION

Before the EVB is used or power is applied, please fully read the following sections on how to correctly configure the board. Failure to correctly configure the board may cause irreparable component, MCU or EVB damage.

3. Configuration

This section details the configuration of each of the EVB functional blocks.

The EVB has been designed with ease of use in mind and has been segmented into functional blocks as shown below. Detailed silkscreen legend has been used throughout the board to identify all switches, jumpers and user connectors.

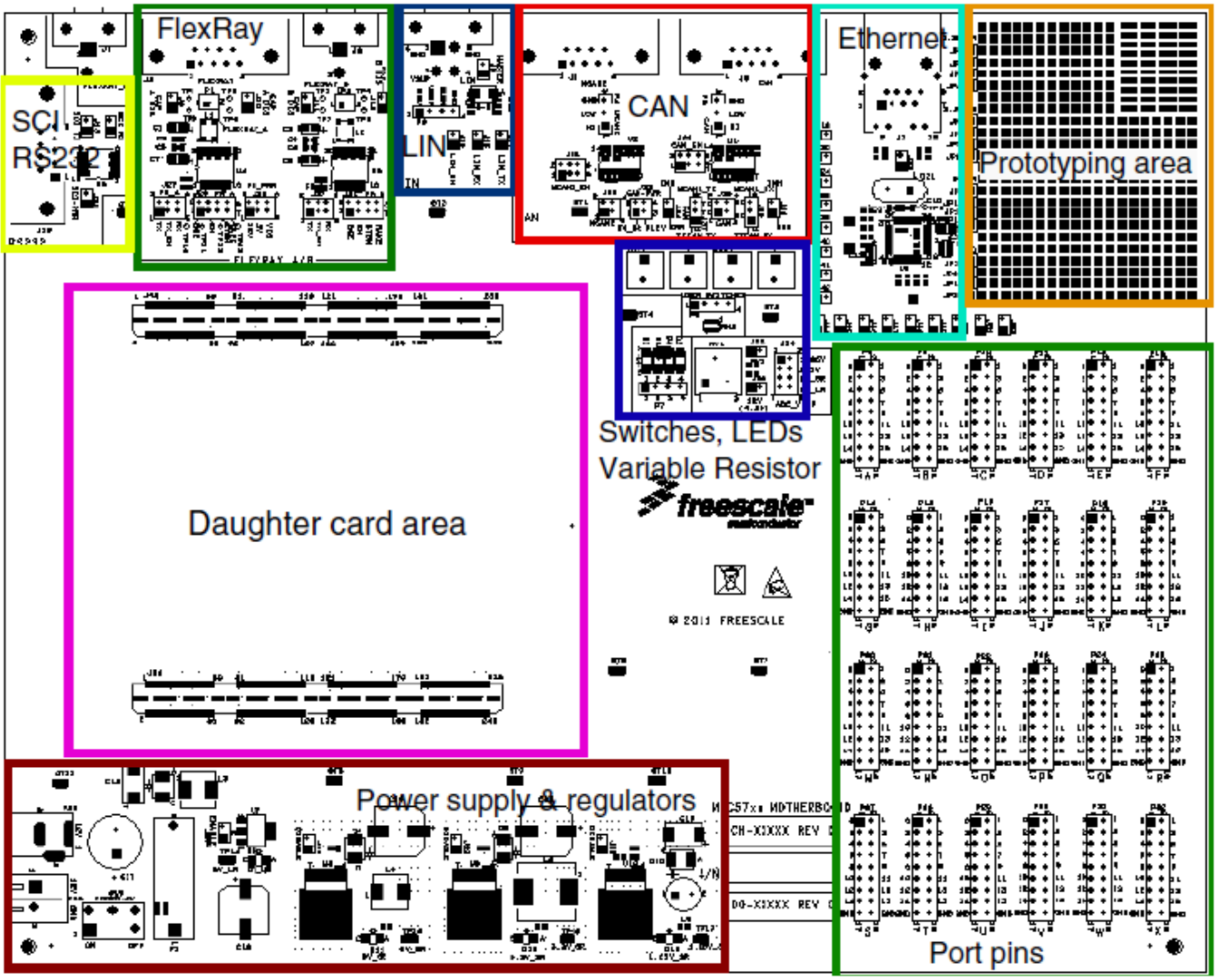

Figure 2. EVB functional blocks

3.1. Power supply configuration

The EVB requires an external power supply voltage of 12 V DC, minimum 1.5 A. This allows the EVB to be easily used in a vehicle if required. The single input voltage is regulated on-board using three switching regulators to provide the necessary EVB and MCU operating voltages of 5.0 V, 3.3 V and 1.25 V, and one 5 V linear regulator for the ADC supplies and references.

For flexibility there are two different power supply input connectors on the motherboard as detailed below. There is also a power supply option on the daughter card to use the daughter card in standalone mode. Refer to section 4.1.2 for details on the daughter card power input.

3.1.1. Motherboard powers supply connectors

2.1 mm Barrel Connector – P26:

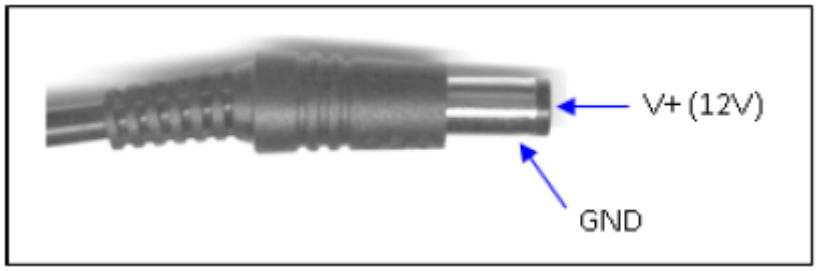

Figure 3. 2.1 mm power connector

Screw Terminal Power Connector – P33:

This can be used to connect a bare wire lead to the EVB, typically from a laboratory power supply. The polarisation of the connectors is clearly marked on the EVB (Pin 1 = +12 V). Care must be taken to ensure correct connection.

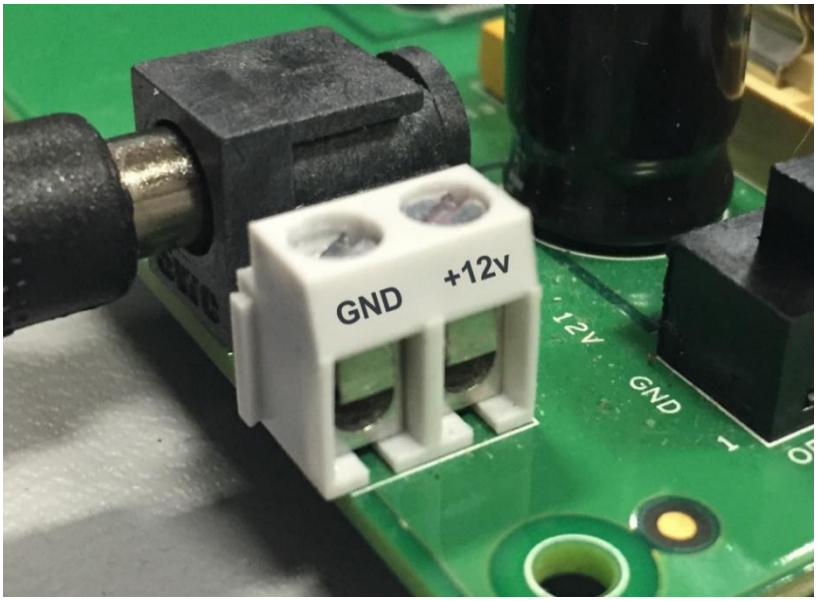

Figure 4. Screw terminal power connector

3.1.2. Regulator power jumpers

There are four power regulator circuits on the MPC57xx motherboard that supply the required voltages to operate the MCUs:

- 1.25V_SR: 1.25 V switching regulator to supply the core voltage
- 5V_SR: 5 V switching regulator to supply the power management controller, I/O and peripherals
- 3.3V_SR: 3.3 V switching regulator for Ethernet, FlexRAY, debug and I/O
- 5V_LR: 5 V linear regulator for ADC supply and reference

All of the regulators have the option of being disabled/enabled if they are not required. By default (jumpers are off), all of the switching regulators are enabled and the 5 V linear regulator is disabled. The regulators can be enabled individually by the following jumper settings:

- Connecting J57 enables the 5 V linear regulator
- Disconnecting J58 enables the 5 V switching regulator
- Disconnecting J59 enables the 3.3 V switching regulator
- Disconnecting J60 enables the 1.25 V switching regulator

The regulators supply power to the daughter cards through the board connector. The individual selection and configuration of the MCU supplies are done on the daughter cards.

NOTE

Not all the supported daughter card MCUs require all the supplies to be switched on. Please refer to the individual daughter card user guide for details.

3.1.3. Power switch, status LEDs and fuse

The main power switch (slide switch SW5) can be used to isolate the power supply input from the EVB voltage regulators if required.

- Moving the slide switch to the right (away from connector P33) will turn the EVB on
- Moving the slide switch to the left (towards connector P33) will turn the EVB off

When power is applied to the EVB, four green power LEDs adjacent to the voltage regulators show the presence of the supply voltages as follows:

- LED D9 – Indicates that the 5.0 V linear regulator is enabled and working correctly
- LED D11 – Indicates that the 5.0 V switching regulator is enabled and working correctly
- LED D12 – Indicates that the 3.3 V switching regulator is enabled and working correctly
- LED D13 – Indicates that the 1.25 V switching regulator is enabled and working correctly

If no LED is illuminated when power is applied to the EVB and the regulators are correctly enabled using the appropriate jumpers, it is possible that either power switch SW5 is in the “OFF” position or that the fuse F1 has blown. The fuse will blow if power is applied to the EVB in reverse-bias, where a protection diode ensures that the main fuse blows rather than causing damage to the EVB circuitry. If the fuse has blown, check the bias of your power supply connection then replace fuse F1 with a 20 mm 1.5 A fast blow fuse.

3.2. CAN configuration

The EVB has two NXP TJA1041T high speed CAN transceivers and two female standard DB9 connectors to provide physical CAN interfaces for the MCU.

The pinout of the DB9 connector (J2) is shown in the figure below.

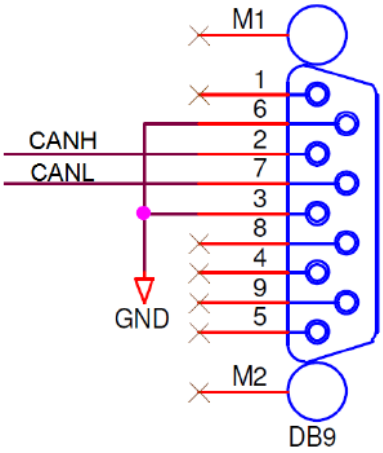

Figure 5. CAN DB9 connector pinout

For flexibility, the CAN transceiver I/Os are also connected to two standard 0.1” connectors (P4 and P5) at the top side of the PCB. The pin-out for these connectors is shown in the figure below.

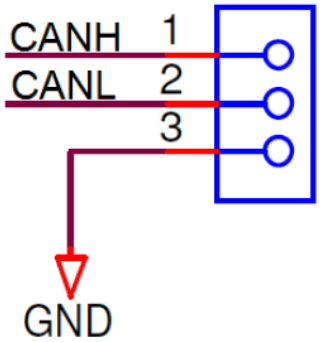

Figure 6. CAN 3pin header interface connector

By default the CAN interfaces are not enabled. To enable the CAN interfaces the jumpers detailed in Table 3 need to be placed.

Table 3. CAN control jumpers

Jumper	Label	Description
J23	CAN2_EN	PHY U2 configuration 1-2: WAKE to GND 3-4: STB to 5V 5-6: EN to 5V
J32	CAN2	1-2: PHY TX to MCU 3-4: PHY RX to MCU

Jumper	Label	Description
J33	CAN-PWR	1-2: 5.0V_SR to PHY U2 V_{CC} 3-4: 12V to PHY U2 V_{BAT}
J34	-	PHY U2 signal out 1: ERR 2: INH
J21	CAN_EN	PHY U1 configuration 1-2: WAKE to GND 3-4: STB to 5V 5-6: EN to 5V
J35	CAN	1-2: 5.0V_SR to PHY U1 V_{CC} 3-4: 12V to PHY U1 V_{BAT}
J37	CAN	PHY U1 TX to MCU 1-2: TTCAN TX 2-3: MCAN1 TX
J38	-	PHY U1 RX to MCU 1-2: TTCAN RX 2-3: MCAN1 RX
J36	-	PHY U1 signal out 1: ERR 2: INH

3.3. RS232 configuration

Female DB9 connector J19 and MAX3221E RS232 transceiver device provide a physical RS232 interface, allowing a direct RS232 connection to a PC or terminal.

The pin-out of these connectors is detailed in Figure 7. Note that hardware flow control is not supported on this implementation.

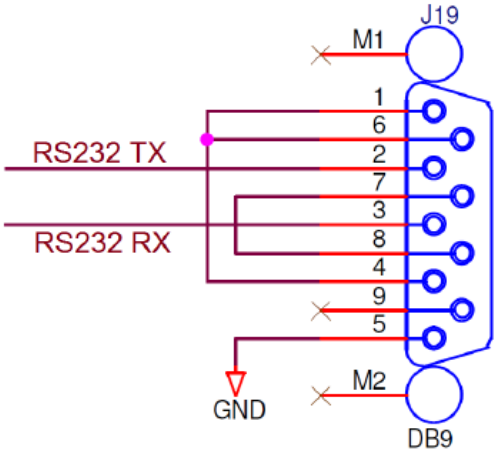

Figure 7. RS232 physical interface connector

On default the RS232 interface is not enabled. To enable the RS232 interface the user needs to place the jumpers detailed in Table 4.

Table 4. RS232 control jumpers

Jumper	Label	Description
J13	SCI TX	TX enable
J14	SCI RX	RX enable
J25	SCI_PWR	Transceiver power on

3.4. LIN configuration

The EVB is fitted with an NXP MC33661F LIN transceiver (U50) and two different style connectors: A standard LIN Molex connector (J14) at the edge of the board and a standard 0.1" connector (P3).

The pin-out of the Molex connector J4 is shown in the figure below.

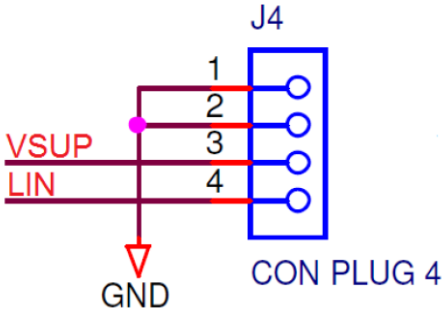

Figure 8. LIN Molex connector

For flexibility, the LIN transceiver is also connected to a standard 0.1” connector (P3) at the top side of the PCB as shown in Figure 9. For ease of use, the 12V EVB supply is fed to pin1 of P3 and the LIN transceiver power input to pin2. This allows the LIN transceiver to be powered directly from the EVB supply by simply linking pins 1 and 2 of connector P3 using a 0.1" jumper shunt.

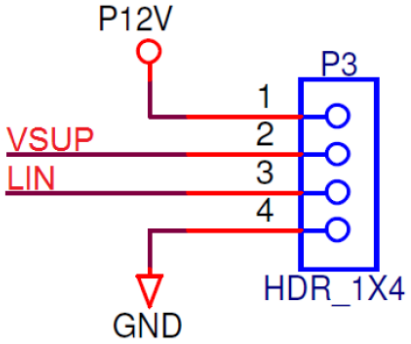

Figure 9. LIN 4pin header interface connector

By default the LIN interface is not enabled. To enable the LIN interface the jumpers detailed in Table 5 need to be placed.

Table 5. LIN control jumpers

Jumper	Label	Description
J15	LIN_EN	LIN PHY (U50) enable
J16	LIN_RX	LIN RX enable
J17	LIN_TX	LIN TX enable

3.5. FlexRAY configuration

The EVB is fitted with two FlexRAY transceivers, a female DB9 connector (for both transceivers) and two alternative connectors. Jumpers J27 and J30 are provided to route the respective MCU signals to the physical interfaces.

The pin-out of the DB9 connector (J2) is shown in the figure below.

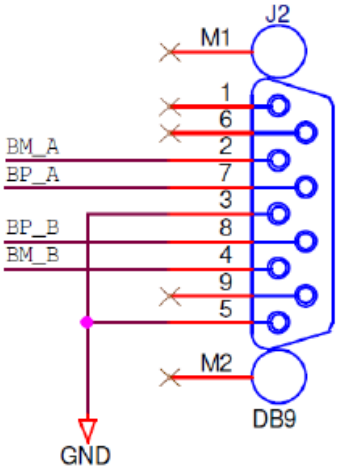

Figure 10. FlexRAY DB9 connector pinout

For flexibility, the FlexRAY transceiver is also connected to two FlexRAY connectors (P1 & P2) and two 2pin Molex connectors (J1 & J3, not populated by default) at the top side of the EVB. Figure 11 shows the connections for both types of connectors.

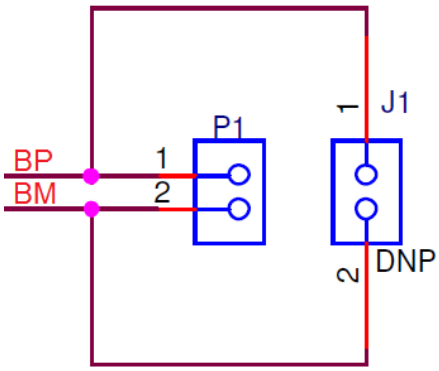

Figure 11. FlexRAY alternative connector pin-outs

By default the FlexRAY interface is not enabled. To enable the FlexRAY interface the jumpers detailed in Table 6 need to be placed.

Table 6. FlexRAY control jumpers

Jumper	Label	Description
J29	FR_PWR	FlexRay transceiver VIO selection 1-2: 12 V to V_{BAT} 3-4: 5V_SR to V_{CC} and V_{BUF} 5-6: 3.3V_SR to V_{IO}
J27	FR_A	1-2: PHY U4 TX to MCU 3-4: PHY U4 TXEN to MCU 5-6: PHY U4 RX to MCU
J28	FR_A	PHY U4 configuration: 1-2: 3.3 V (V_{IO}) to BGE 3-4: 3.3 V (V_{IO}) to EN 5-6: 3.3 V (V_{IO}) to STBY 7-8: GND to WAKE
J30	FR_B	1-2: PHY U5 TX to MCU 3-4: PHY U5 TXEN to MCU 5-6: PHY U5 RX to MCU
J31	FR_B	PHY U5 configuration: 1-2: 3.3 V (V_{IO}) to BGE 3-4: 3.3 V (V_{IO}) to EN 5-6: 3.3 V (V_{IO}) to STBY 7-8: GND to WAKE

3.6. Ethernet configuration

The EVB is fitted with a standard RJ45 Ethernet connector (J7) and a DP83848C 10/100 Ethernet transceiver (U6). This is however not used in conjunction with the S32R274RRUEVB daughter card since it is fitted with its own Gb Ethernet physical interface and RJ45 connector. Refer to section 4 for details.

3.7. Motherboard

A number of test points of different shape and functionality is scattered around the EVB to allow easy access to MCU and reference signals. This section summarizes and describes the available test points. Motherboard test points are listed and detailed in the table below.

Table 7. Test points - motherboard

Signal	TP name	Shape	Description
GND	GT1	Hook	Ground reference

Signal	TP name	Shape	Description
GND	GT2	Hook	Ground reference
GND	GT3	Hook	Ground reference
GND	GT4	Hook	Ground reference
GND	GT5	Hook	Ground reference
GND	GT6	Hook	Ground reference
GND	GT7	Hook	Ground reference
GND	GT8	Hook	Ground reference
GND	GT9	Hook	Ground reference
GND	GT10	Hook	Ground reference
GND	GT11	Hook	Ground reference
1.25V_SR	JP1	User Area Pin	1.25V_SR reference
1.25V_SR	JP2	User Area Pin	1.25V_SR reference
1.25V_SR	JP3	User Area Pin	1.25V_SR reference
1.25V_SR	JP4	User Area Pin	1.25V_SR reference
3.3V_SR	JP5	User Area Pin	3.3V_SR reference
3.3V_SR	JP6	User Area Pin	3.3V_SR reference
3.3V_SR	JP7	User Area Pin	3.3V_SR reference
3.3V_SR	JP8	User Area Pin	3.3V_SR reference
5V_SR	JP9	User Area Pin	5V_SR reference
5V_SR	JP10	User Area Pin	5V_SR reference
5V_SR	JP11	User Area Pin	5V_SR reference
5V_SR	JP12	User Area Pin	5V_SR reference
GND	JP13	User Area Pin	Ground reference
GND	JP14	User Area Pin	Ground reference
GND	JP15	User Area Pin	Ground reference
GND	JP16	User Area Pin	Ground reference
5V_SR	TP15	Hook	5V_SR reference
5V_LR	TP14	Hook	5V_LR reference
3.3V_SR	TP16	Hook	3.3V_SR reference

Signal	TP name	Shape	Description
1.25V_SR	TP17	Hook	1.25V_SR reference
FRA-INH2	TP5	Pad	FlexRAY
FRA-INH1	TP1	Pad	FlexRAY
FRA-ERRN	TP2	Pad	FlexRAY
FRA-RXEN	TP6	Pad	FlexRAY
FRB-INH2	TP7	Pad	FlexRAY
FRB-INH1	TP3	Pad	FlexRAY
FRB-ERRN	TP4	Pad	FlexRAY
FRB-RXEN	TP8	Pad	FlexRAY
FR_DBG0	TP10	Pad	FlexRAY debug0
FR_DBG1	TP11	Pad	FlexRAY debug1
FR_DBG2	TP12	Pad	FlexRAY debug2
FR_DBG3	TP13	Pad	FlexRAY debug3
FEC 25MHz	TP9	Pad	Ethernet clock

4. Configuration – Daughter card

This section details the configuration of each of the daughter card's functional blocks.

The daughter card has been designed with ease of use in mind and has been segmented into functional blocks as shown in Figure 12. Detailed silkscreen legend has been used throughout the board to identify all switches, jumpers and user connectors.

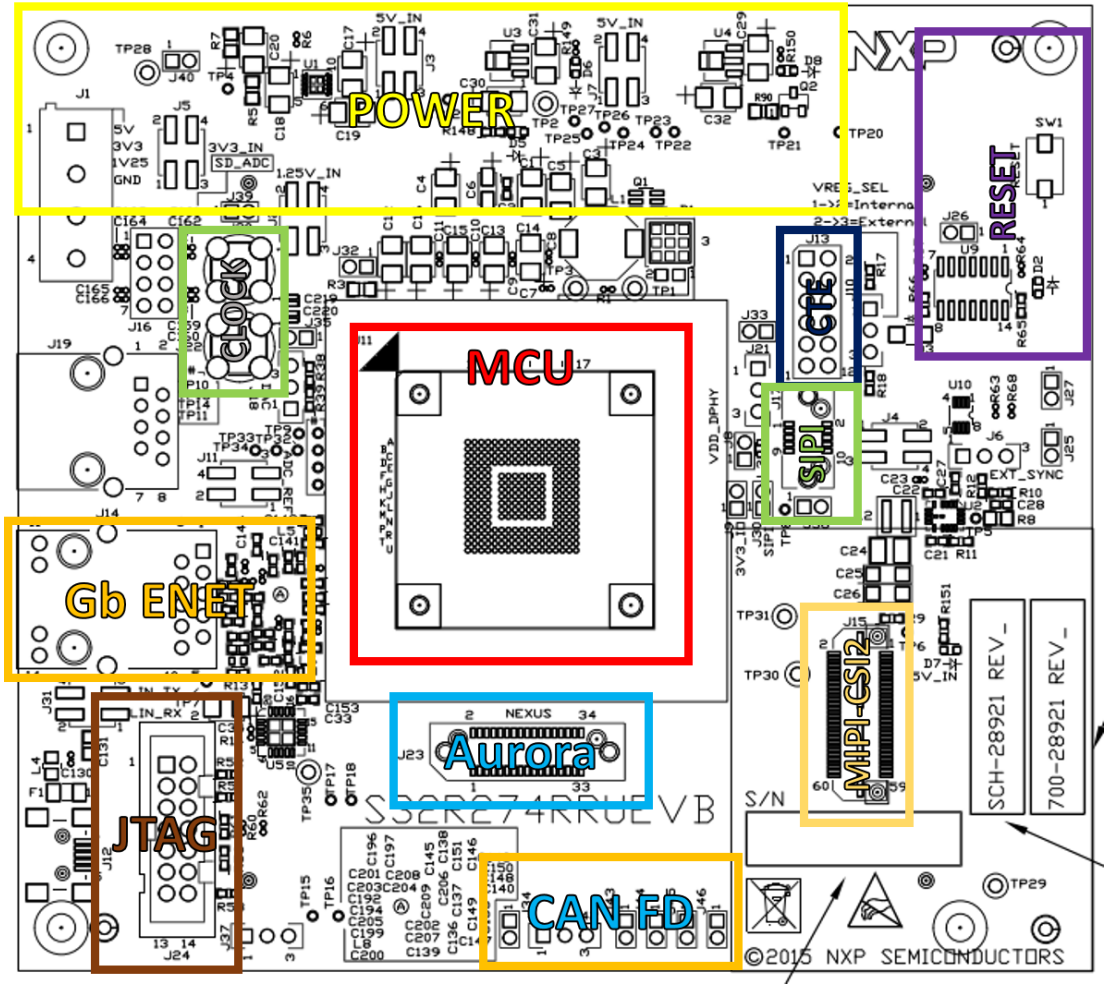

Figure 12. Daughter card - functional blocks

4.1. MCU power

4.1.1. Supply routing and jumpers

The different MCU supply inputs are connected to the regulators on the motherboard through the interface connector. Figure 13 shows how the MCU power domains are connected to the regulators.

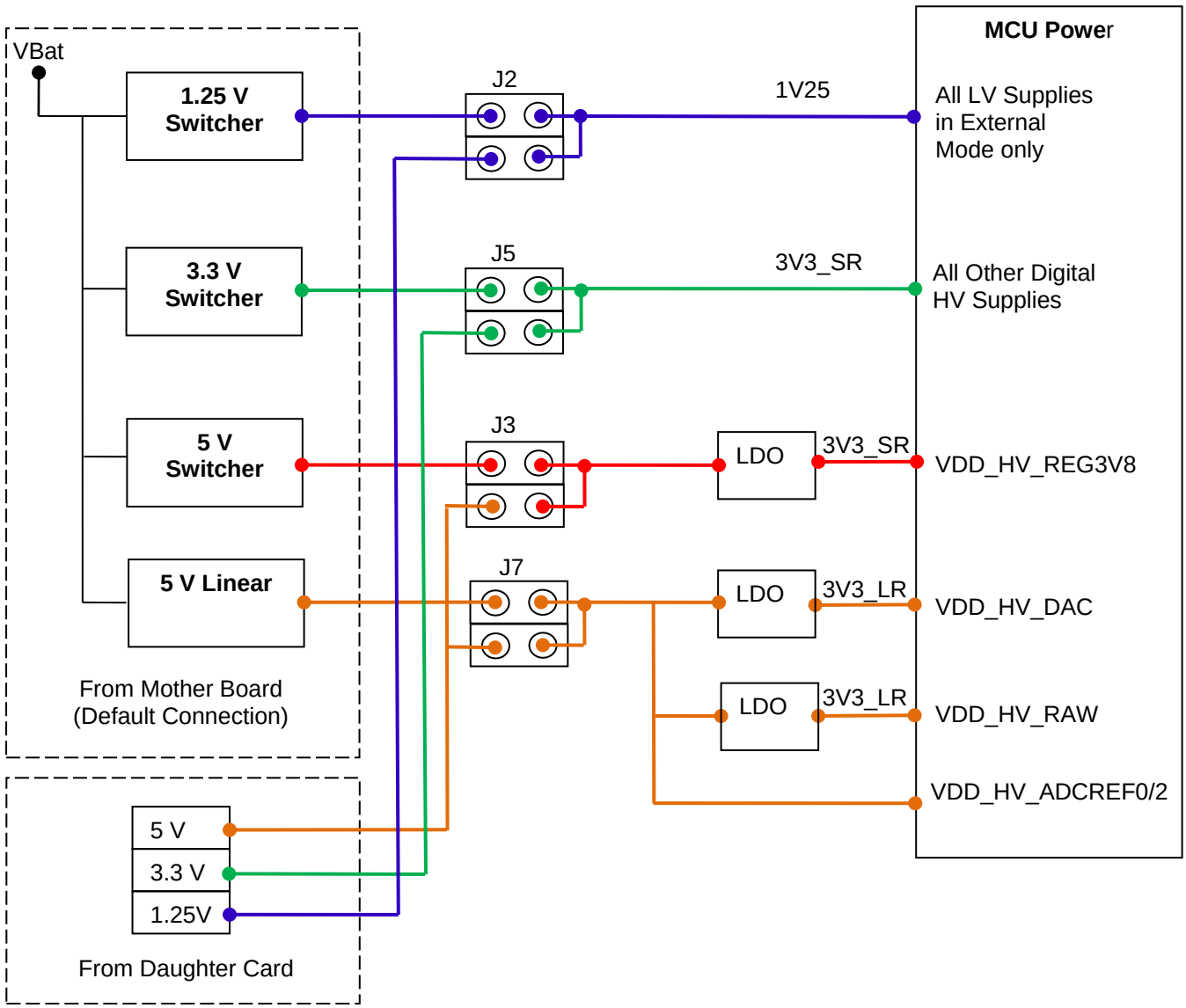

Figure 13. Daughter card power distribution

The connection of any power domain to a regulator has to be enabled by a dedicated jumper as described in the table below.

Table 8. MCU power selection jumpers

Jumper	Description
J5	Connects Digital HV supplies to 3.3V_SR
J2	Connects Digital LV supplies to 1.25V_SR
J7	Connects AFE Supply to 3.3V_LR via LDO
J3	Connects AFE Supply to 3.3V_SR via LDO

4.1.2. Daughter card standalone power input

A terminal power input is provided on the daughter card to enable use of the daughter card without the motherboard.

The connections of the power terminal are detailed in the figure below.

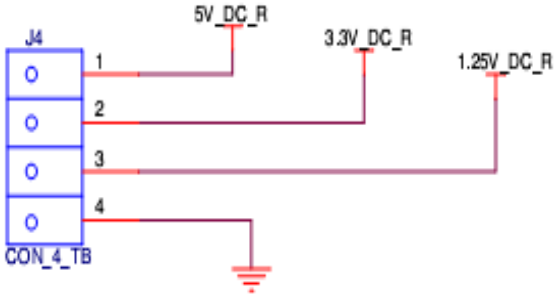

Figure 14. Terminal power input connections

NOTE

The power terminal does not connect to the 5.0V_LR power rail which is powered by the 5V linear regulator when used with the motherboard. This rail is powering the VDD_HV_DAC (DAC supply), VDD_HV_RAW (AFE supply) and VDD_HV_ADCREFxx (ADC reference voltage). When using the daughter card standalone (without the motherboard) it is required to connect the 5.0V_LR and the 5.0V_SR rail in order for the microcontroller to come out of reset. Refer to section 4.11 for more information.

4.2. Reset circuit

To enable standalone use the reset circuitry is placed on the daughter card. It consist of a reset switch that is connected to RESET_B via a jumper, and an external voltage monitoring IC connected to VREG_POR_B. The RESET_B signal is also connected to the signal RST-SW that is connected to the mother board to reset peripherals. A yellow LED (D2) is used to indicated RESET_B reset situations, and a red LED (D9) indicates VREG_POR_B reset situations.

The EVB reset circuit provides the following functionality:

The reset switch SW2 can be used to reset the MCU. The reset switch signal is connect to the MCU reset signals RESET_B (through jumper J47) and the connection can be released by lifting the according jumper. For normal operation leave jumper J47 populated. If external control of RESET_B is required then connection of a control signal to pin 2 of J47 can be made. Pushing the reset switch will also reset peripherals that are connected to the board reset signal signal RST-SW.

Since the S32R274 device offers both internal and external regulation modes this is configurable on the daughtercard, and thus an external voltage monitoring IC (U18 – Linear Devices LTC2905) is utilised to protect the device when in external regulation mode and the device low voltage detect (LVD) mechanism is disabled. This circuit monitors the 1.25 V (core supply) and 3.3 V IO supply domain and

will hold the device in reset via VREG_POR_B until these supplies are within the expected voltage range. This circuit is active in both internal and external regulation schemes.

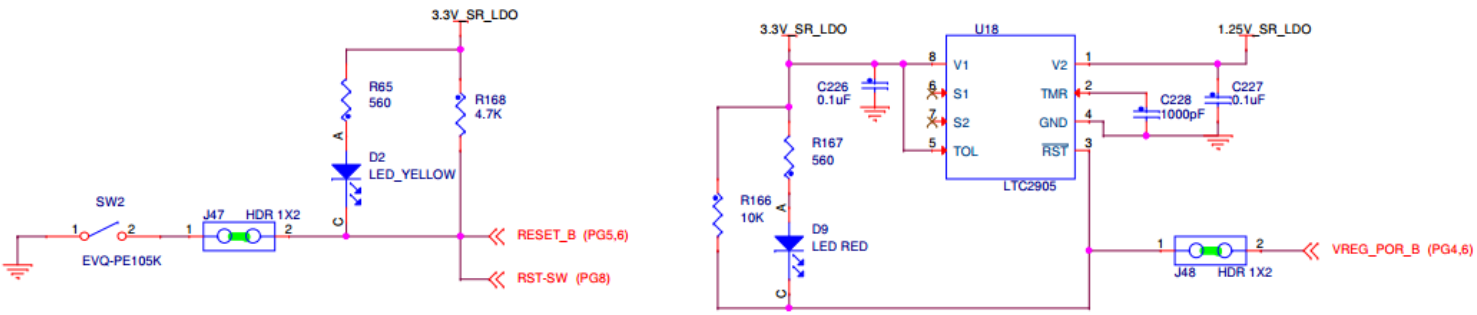

Figure 15. Voltage monitoring and reset circuit

Table 9. Reset circuit jumper settings

Jumper	Description
J47	Connect reset switch circuit to RESET_B pin
J48	Connect reset switch circuit to VREG_POR_B pin

4.3. MCU external clock circuit

In addition to the internal 16 MHz oscillator, the MCU can be clocked by different external sources. The EVB system supports four possible MCU clock sources:

1. 40 MHz crystal Y3 (The MCU only has a 40 Mhz input)
2. External clock input to the EVB via the SMA connector (J20), driving the MCU EXTAL signal
3. External differential clock input to the EVB via SMA connectors (J20 & J22), driving MCU EXTAL and XTAL with negative and positive clock signals respectively
4. External differential or single ended clock input to the EVB via the MIPI-CSI2 connector, for use with the Eagle MR3003 RF front end board.

The clock circuitry for the daughter card is shown in Figure 16. Each source is selectable via the 0-ohm links as shown, with crystal Y3 being the default factory option.

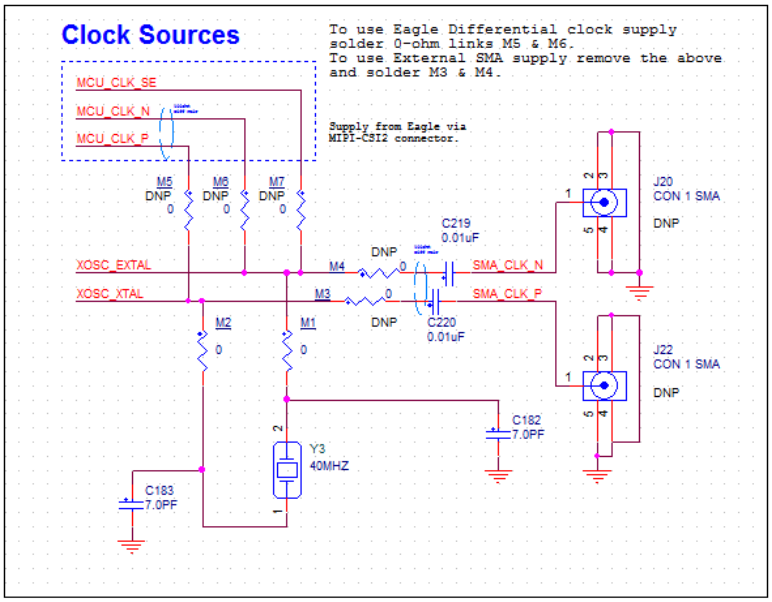

Figure 16. 40MHz crystal circuit

4.4. JTAG

The EVB is fitted with 14-pin JTAG debug connector. The following diagram shows the 14-pin JTAG connector pinout (0.1” keyed header).

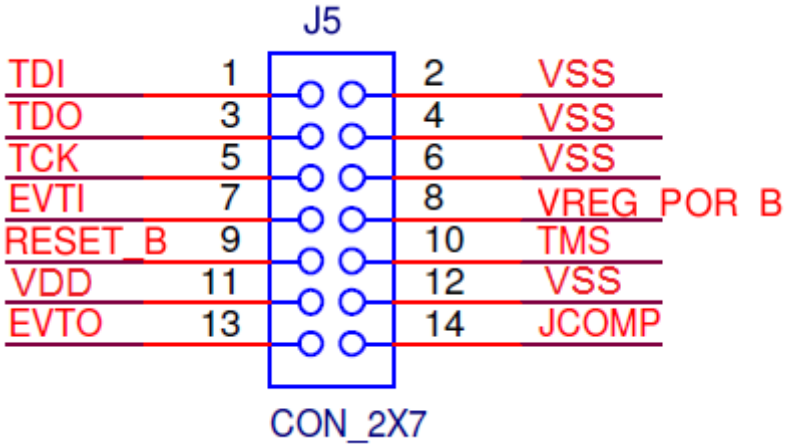

Figure 17. JTAG connector pinout

4.5. Nexus Aurora

Table 10 shows the pinout of the 34-pin Samtec connector for the S32R274.

Table 10. Aurora Trace connector pinout

Pin No	Function		Pin No	Function
1	TX0+		2	VREF
3	TX0-		4	TCK/TCKC/DRCLK
5	VSS		6	TMS/TMSC/TxDataP
7	TX1+		8	TDI/TxDataN
9	TX1-		10	TDO/RxDataP
11	VSS		12	JCOMP/RxDataN
13	TX2+		14	EVTI1
15	TX2-		16	EVTI0
17	VSS		18	EVTO0
19	TX3+		20	VREG_POR_B
21	TX3-		22	RESET_B
23	VSS		24	VSS
25	TX4+[1]		26	CLK+
27	TX4+[1]		28	CLK-
29	VSS		30	VSS
31	TX5+[1]		32	EVTO1/RDY
33	TX5+[1]		34	N/C
GND	VSS		GND	VSS

4.6. Serial Interprocessor Interface (SIPI)

A dedicated SIPI interface connector is provided on the daughter card. For signal integrity the SIPI signals are not routed to the mother board. Test points are provided on the signals so they can be accessed if required to be used as a different function.
A 10 pin Samtec connector (J17: ERF8-005-05.0-LDV-L-TR) is used for the SIPI interface. The pin-out of the connector is shown in Figure 18.

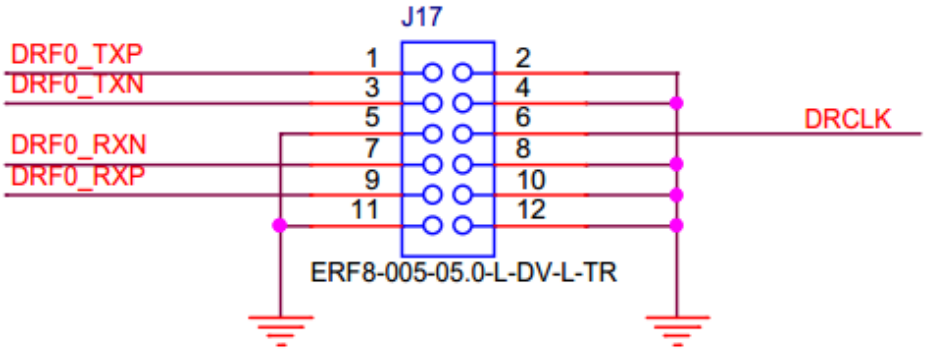

Figure 18. SIPI connector pinout

4.7. Camera Serial Interface (MIPI-CSI2)

A dedicated MIPI-CSI2 interface is provided on the daughtercard, and is designed to provide compatibility with the Eagle MR3003 Radar front end EVK. To preserve signal integrity MIPI-CSI2 signals are not routed to the motherboard.

A 60 pin Samtec connector (QTH-030-01-L-D-A-K-TR) is used for the MIPI-CSI2 interface. The pinout of the connector is shown in Figure 19.

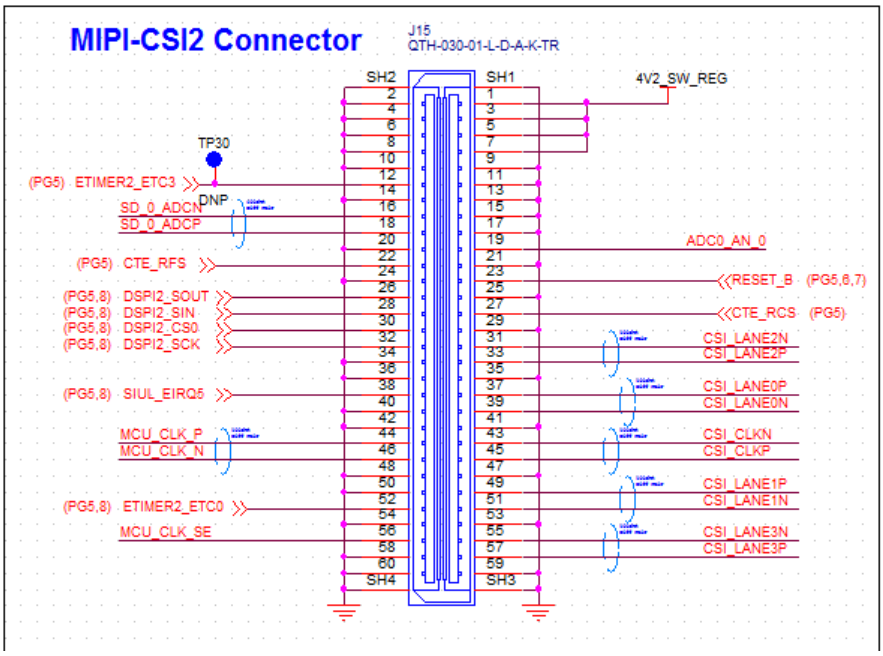

Figure 19. MIPI-CSI2 connector pinout

4.8. Gigabit Ethernet

The S32R274RRUEVB daughtercard includes support for Gb ethernet, utilizing the RGMII interface present on the S32R274 device. The daughtercard is designed with a Micrel KSZ9031RNXUA Ethernet

physical interface (U17), and associated RJ45 connector (J14 - Bel Fuse V890-1AX1-A1). This is the default configuration of the RGMII signals from the S32R274 device. If for any reason the alternate functions multiplexed on the RGMII pads are required then these signals can be routed to the motherboard by adding a 0-ohm link to the pads provided. These are not soldered by default to reduce the signal trace length and parasitic, Gb ethernet operation cannot be guaranteed if these links are in place since it adds significant length to the signal path.

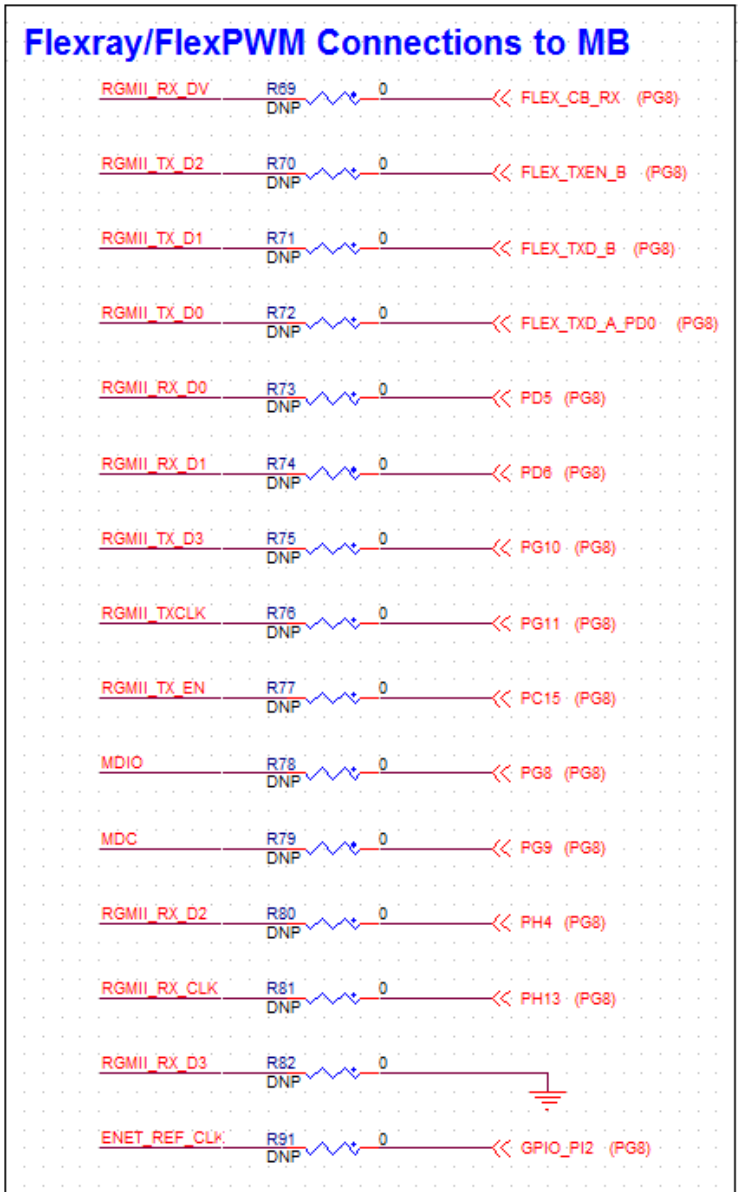

Figure 20. RGMII signal connections to motherboard

4.9. CAN FD

Although the EVB motherboard supports CAN, 2x NXP TJA1051T/3 CAN FD (Flexible Data) compliant physical interfaces are provided (U14 and U16) on the daughtercard for higher speed applications.

Since the CAN module pads have multiplexable functions these can be configured as follows:

- By default CAN0 signals will go straight to U14
- But if for any reason the motherboard physical interface or other pad functions should be used then the signals can be diverted to the motherboard by removing R155 and R156 0-ohm links
- Populating R157 and R158 respectively.

Similarly CAN2 signals can be routed to either the on-board CAN-FD phy U16 via J43 and J44, or to the motherboard Flexray physical interface via J46 and J45.

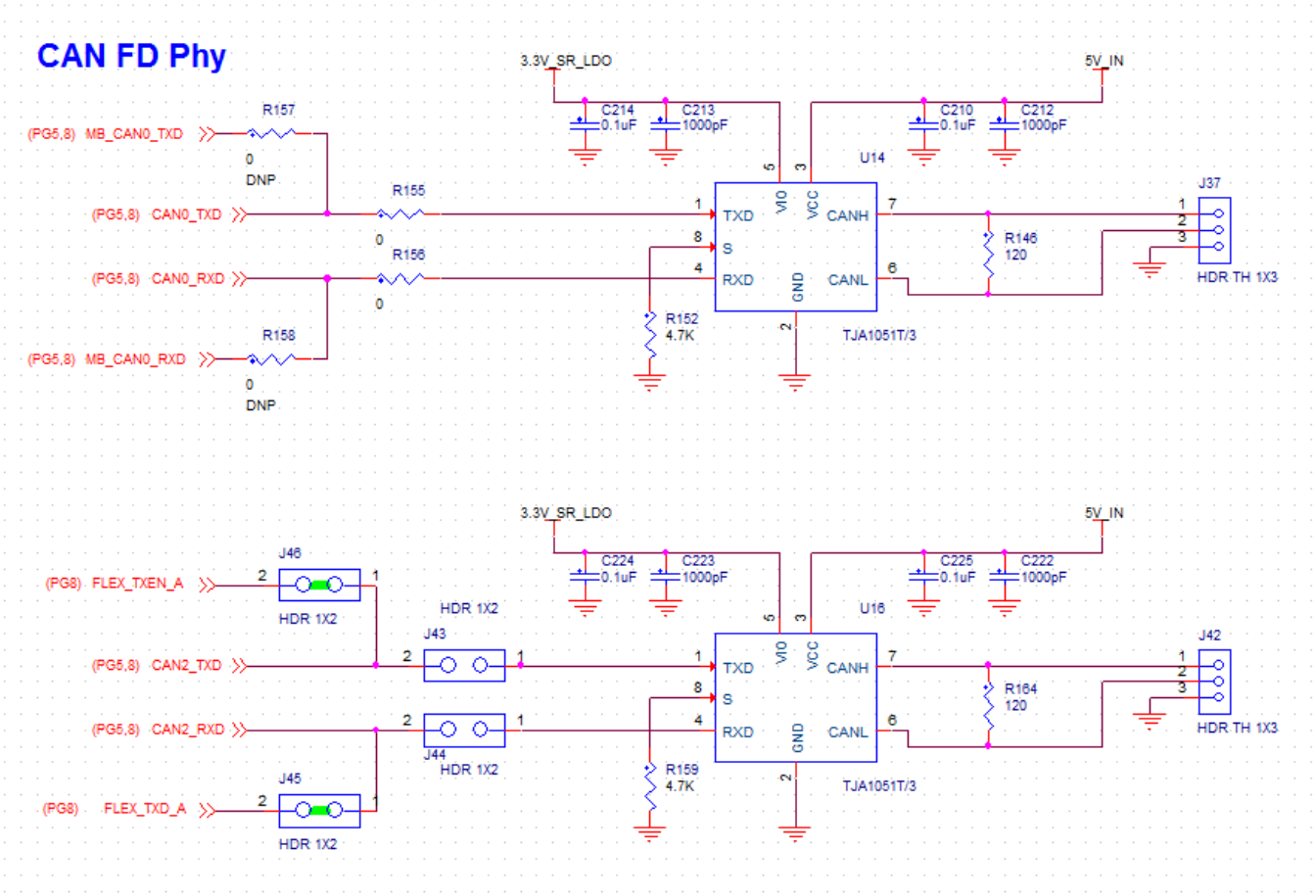

Figure 21. CAN FD physical interfaces

4.10. Test points - daughter card

Daughter card test points are listed and detailed in the table below.

Table 11. Test points – daughter card

Signal	TP name	Shape	Description
VREG_SWP	TP1	Test Loop	Driver signal for external switching transistor
3V3_HV_REG	TP2	Test Loop	3V3 Supply to external transistor
VREG_I-SENSE	TP3	Test Loop	Current sense analog input
3V3_PGOOD	TP4	Surface Pad	Power good signal from 3.3v linear regulator
4V2_PGOOD	TP5	Surface Pad	Power good signal from 4.2v switching regulator
4V2_SW_REG	TP6	Surface Pad	4.2V Switching regulator output
1V2_LR_HV	TP7	Surface Pad	1.2V Ethernet phy regulator output
1.25V_SR_LDO	TP8	Surface Pad	1.25V Core supply
VDD_LV_RADARDIG	TP9	Surface Pad	1.4V RADAR Reference
VDD_LV_RADARREF	TP10	Surface Pad	1.4V RADAR Reference
VDD_HV_RAW	TP11	Surface Pad	Analog supply for 1.4v on chip regulators
VDD_HV_DAC	TP12	Surface Pad	3.3V Analog supply for DAC
VDD_HV_DAC_2V5	TP13	Surface Pad	2.5V supply voltage for DAC
AFE_FILTER	TP14	Surface Pad	AFE filter
GND	TP28, TP29	Test Loop	Ground
ETIMER2_ETC0	TP30	Test Loop	Etimer 2 Channel 0
NPC_EVTO_B	TP31	Test Loop	PI9 (Pad G14)
VDD_LV_SDPLL	TP32	Surface Pad	1.4V Analog supply for 320Mhz PLL
VDD_LV_SDADC	TP33	Surface Pad	1.4V analog supply for SD ADCs
VDD_LV_OSC	TP34	Surface Pad	1.4V analog supply for crystal oscillator
ENET_REF_CLK	TP35	Test Loop	125MHz ENET Reference clock

4.11. Configuring the Daughter Card for Standalone Use

It is possible to use the daughter cards without the motherboard to run code on the microcontroller. Power to the daughter cards must be supplied through the terminal power connector 'J1 – PWR_IN'. It is required to connect all three voltages (1.25V, 3.3V and 5V) and ground.

Jumpers positions must be moved to allow the J1 to supply the EVB.

J3 must move to position 1-2 (5V_DC_R)

J2 must move to position 1-2 (1.25V_DC_R)

J7 must move to position 1-2 (5V_DC_R)

J5 must move to position 1-2 (3.3V_DC_R)

J4 must move to position 1-2 (5V_DC_R)

4.12. Configuring external VREG Mode

v

Table 12. Jumper Configuration for external VREG mode

Jumper Number	Default position	Function
J2	3-4	1.25 V supply
J3	3-4	5.0 V supply to create 3.3v for the AFE Regulator
J5	3-4	3.3 V supply for the device
J7	3-4	5.0 V Linear supply from Motherboard for SAR ADC Reference voltage
J8	on	1.25 V MIPI-CSI2 DPHY
J9	on	3.3 V IO
J10	2-3	Determine internal or external Vreg Mode
J11	1-2, 3-4	ACD Ref
J21	2-3	VPP TEST (always GND)
J30	on	3.3 V RGMII
J31	1-2, 3-4	Linflex Tx/Rx
J32	off	Jumper to supply to transistor
J33	on	Jumper supplies 1.25v to the core
J34	on	3.3 V supply to PMU
J35	on	1.25 V PLL supply
J36	on	3.3 V Flash supply
J39	on	3.3 V ADC supply
J40	on	3.3 V supply to MCU
J43	off	CAN2 Tx connection to PHY
J44	off	CAN2 Rx connection to PHY
J45	on	Flexray TXD A connection to motherboard

J46	on	Flexray TXEN A connection to motherboard
J47	on	RESET_B Connection to reset circuit
J48	on	VREG_POR_B Connection to reset circuit
Headers		
J13	off	CTE output
J17	off	SIPI Interface
J24	off	JTAG Interface
J16	off	SD ADC output
J18	off	DAC output
J37	off	CAN0 connections
J42	off	CAN2 connections

4.13. Configuring internal VREG Mode

The followingn table shows the jumper configuration for the EVB when in internal VREG mode.

Table 13. Jumper Configuration for internal VREG mode

Jumper Number	Default position	Function
J2	3-4	1.25 V supply
J3	3-4	5.0 V supply to create 3.3v for the AFE Regulator
J5	3-4	3.3 V supply for the device
J7	3-4	5.0 V Linear supply from Motherboard for SAR ADC Reference voltage
J8	on	1.25 V MIPI-CSI2 DPHY
J9	on	3.3 V IO
J10	1-2	Determine internal or external Vreg Mode
J11	1-2, 3-4	ACD Ref
J21	2-3	VPP TEST (always GND)
J30	on	3.3 V RGMII
J31	1-2, 3-4	Linflex Tx/Rx
J32	on	Jumper to supply to transistor
J33	on	Jumper supplies 1.25v to the core
J34	on	3.3 V supply to PMU
J35	on	1.25 V PLL supply
J36	on	3.3 V Flash supply
J39	on	3.3 V ADC supply
J40	on	3.3 V supply to MCU
J43	off	CAN2 Tx connection to PHY
J44	off	CAN2 Rx connection to PHY
J45	on	Flexray TXD A connection to motherboard
J46	on	Flexray TXEN A connection to motherboard

J47	on	RESET_B Connection to reset circuit
J48	on	VREG_POR_B Connection to reset circuit
Headers		
J13	off	CTE output
J17	off	SIPI Interface
J24	off	JTAG Interface
J16	off	SD ADC output
J18	off	DAC output
J37	off	CAN0 connections
J42	off	CAN2 connections

5. Board interface connector

This chapter provides a useful cross reference to see the connection from the motherboard to the board interface connector, and what MCU pins are connected to the interface connector on the daughter card.

Table 14 lists all the connections to the board interface connector on both motherboard and daughter card. The table on the left lists the 240 connections for the first interface connector (J28), the table on the right lists the 240 connections for the second interface connector (J29):

- The column ‘Motherboard’ shows the motherboard connections to the interface connectors like power supply connections and user area port pins.
- The column 257 BGA shows the connections from the MCU pins to the interface connector on daughter card for the 257 BGA package. It is ensured that the MCU port pins are routed to the associated user area port pin on the motherboard, but in some cases due to pin multiplexing uses this is not possible. The schematic signal name is included in brackets, but for all possible multiplexing functions of each pin please see the device reference manual.
- Green fields indicate power signals, power signals are connected to all the appropriate pins on the MCU
- Red fields indicate MCU signals that are only connected to the motherboard via 0-ohm links or jumpers that are not populated by default to preserve signal integrity. To use these signals for functions other than available on the daughter card add a jumper, or for links populate the link or short the pads with a solder blob.
- Blue fields indicate MCU signals that have dedicated connections to the motherboard peripherals through the interface connector (such as the CAN and FlexRay).
- Ground signals are not listed here. A solid ground connection is achieved through the middle bar of the interface connector.

Table 14. Board interface connector details

Connector	Motherboard	257 BGA (SCH NAME)	0-Ohm Link	Connector	Motherboard	257 BGA (SCH NAME)	0-Ohm Link
A-1	1.25V_SR	1.25V_SR		B-240	1.25V_SR	1.25V_SR	
A-2	1.25V_SR	1.25V_SR		B-239	1.25V_SR	1.25V_SR	
A-3	1.25V_SR	1.25V_SR		B-238	1.25V_SR	1.25V_SR	
A-4	1.25V_SR	1.25V_SR		B-237	1.25V_SR	1.25V_SR	
A-5	PA0	GPIO 0 (PA0)		B-236	PB0	NC#	
A-6	PA1	GPIO 1 (PA1)		B-235	PB1	NC#	
A-7	PA2	GPIO 2 (PA2)		B-234	PB2	GPIO 18 (ETIMER2_ETC0)	
A-8	PA3	GPIO 2 (PA2)		B-233	PB3	GPIO 19 (PB3)	
A-9	PA4	GPIO 4 (DSPI2_CS1)		B-232	PB4	NC#	
A-10	PA5	GPIO 5 (SIUL_EIRQ5)		B-231	PB5	NC#	
A-11	PA6	NC#		B-230	PB6	GPIO 22 (CLKOUT0)	
A-12	PA7	NC#		B-229	PB7	ADC0_AN0	
A-13	PA8	NC#		B-228	PB8	ADC0_AN1	
A-14	PA9	GPIO 9 (PA9)		B-227	PB9	ADC0_AN11	
A-15	PA10	GPIO 10 (DSPI2_CS0)		B-226	PB10	ADC0_AN12	
A-16	PA11	GPIO 11 (DSPI2_SCK)		B-225	PB11	ADC0_AN13	
A-17	PA12	GPIO 12 (DSPI2_SOUT)		B-224	PB12	ADC0_AN14	
A-18	PA13	GPIO 13 (DSPI2_SIN)		B-223	PB13	ADC1_AN0	
A-19	PA14	GPIO 14 (CAN1_TXD)		B-222	PB14	ADC1_AN1	
A-20	PA15	GPIO 15 (CAN1_RXD)		B-221	PB15	ADC1_AN2	
A-21	5.0V_SR	5.0V_SR		B-220	5.0V_SR	5.0V_SR	
A-22	5.0V_SR	5.0V_SR		B-219	5.0V_SR	5.0V_SR	
A-23	5.0V_SR	5.0V_SR		B-218	5.0V_SR	5.0V_SR	
A-24	5.0V_SR	5.0V_SR		B-217	5.0V_SR	5.0V_SR	
A-25	PC0	ADC1_AN_3		B-216	PD0	GPIO 48 (FLEX_TXD_A_PD0)	R72
A-26	PC1	ADC0_AN_2		B-215	PD1	NC#	
A-27	PC2	ADC0_AN_3		B-214	PD2	NC#	
A-28	PC3	NC#		B-213	PD3	NC#	
A-29	PC4	NC#		B-212	PD4	NC#	
A-30	PC5	NC#		B-211	PD5	GPIO 53 (PD5)	R73
A-31	PC6	NC#		B-210	PD6	GPIO 54 (PD6)	R74
A-32	PC7	NC#		B-209	PD7	NC#	

Connector	Motherboard	257 BGA (SCH NAME)	0-Ohm Link	Connector	Motherboard	257 BGA (SCH NAME)	0-Ohm Link
A-33	PC8	GPIO 17 (CAN0_RXD)	R158	B-208	PD8	GPIO 56 (PD8)	
A-34	PC9	GPIO 16 (CAN0_TXD)	R157	B-207	PD9	NC#	
A-35	PC10	NC#		B-206	PD10	NC#	
A-36	PC11	NC#		B-205	PD11	NC#	
A-37	PC12	NC#		B-204	PD12	GPIO 62 (CTU0_EXT_TRIG)	
A-38	PC13	GPIO 47 (PC15)	R77	B-203	PD13	NC#	
A-39	PC14	NC#		B-202	PD14	GPIO 59 (LIN1_TXD)	
A-40	PC15	NC#		B-201	PD15	GPIO 95 (LIN1_RXD)	
A-41	3.3V_SR	3.3V_SR		B-200	3.3V_SR	3.3V_SR	
A-42	3.3V_SR	3.3V_SR		B-199	3.3V_SR	3.3V_SR	
A-43	3.3V_SR	3.3V_SR		B-198	3.3V_SR	3.3V_SR	
A-44	3.3V_SR	3.3V_SR		B-197	3.3V_SR	3.3V_SR	
A-45	PE0	NC#		B-196	PF0	NC#	
A-46	PE1	NC#		B-195	PF1	NC#	
A-47	PE2	ADC0_AN_5		B-194	PF2	NC#	
A-48	PE3	NC#		B-193	PF3	NC#	
A-49	PE4	ADC0_AN_7		B-192	PF4	NC#	
A-50	PE5	ADC0_AN_8		B-191	PF5	NC#	
A-51	PE6	ADC0_AN_4		B-190	PF6	NC#	
A-52	PE7	ADC0_AN_6		B-189	PF7	NC#	
A-53	PE8	NC#		B-188	PF8	NC#	
A-54	PE9	NC#		B-187	PF9	NC#	
A-55	PE10	NC#		B-186	PF10	NC#	
A-56	PE11	NC#		B-185	PF11	NC#	
A-57	PE12	NC#		B-184	PF12	NC#	
A-58	PE13	NC#		B-183	PF13	NC#	
A-59	PE14	NC#		B-182	PF14	GPIO 94 (GPIO_PF14)	
A-60	PE15	GPIO 79 (GPIO_PE15)		B-181	PF15	GPIO 95 (LIN1_RXD)	
A-61	1.25V_SR	1.25V_SR		B-180	1.25V_SR	1.25V_SR	
A-62	1.25V_SR	1.25V_SR		B-179	1.25V_SR	1.25V_SR	
A-63	1.25V_SR	1.25V_SR		B-178	1.25V_SR	1.25V_SR	
A-64	1.25V_SR	1.25V_SR		B-177	1.25V_SR	1.25V_SR	
A-65	PG0	FCCU_F_0		B-176	PH0	GPIO 116 (PH4)	R80

Connector	Motherboard	257 BGA (SCH NAME)	0-Ohm Link	Connector	Motherboard	257 BGA (SCH NAME)	0-Ohm Link
A-66	PG1	FCCU_F_1		B-175	PH1	NC#	
A-67	PG2	NMI		B-174	PH2	NC#	
A-68	PG3	NC#		B-173	PH3	GPIO 51 (FLEXRAY_TXD_B)	R71
A-69	PG4	NC#		B-172	PH4	GPIO 52 (FLEXRAY_TXEN_B)	R70
A-70	PG5	NC#		B-171	PH5	NC#	
A-71	PG6	NC#		B-170	PH6	NC#	
A-72	PG7	NC#		B-169	PH7	GPIO 134 (FLEXRAY_TXD_A)	J45
A-73	PG8	GPIO 104 (PG8)	R78	B-168	PH8	GPIO 133 (FLEXRAY_TXEN_A)	J46
A-74	PG9	GPIO 105 (PG9)	R79	B-167	PH9	GPIO 49 (FLEXRAY_CA_RX)	
A-75	PG10	GPIO 106 (PG10)	R75	B-166	PH10	GPIO 50 (FLEXRAY_CB_RX)	R69
A-76	PG11	GPIO 107 (PG11)	R76	B-165	PH11	NC#	
A-77	PG12	NC#		B-164	PH12	NC#	
A-78	PG13	NC#		B-163	PH13	GPIO 125 (PH13)	R81
A-79	PG14	NC#		B-162	PH14	NC#	
A-80	PG15	NC#		B-161	PH15	NC#	
A-81	5.0V_SR	5.0V_SR		B-160	3.3V_SR	3.3V_SR	
A-82	5.0V_SR	5.0V_SR		B-159	3.3V_SR	3.3V_SR	
A-83	5.0V_SR	5.0V_SR		B-158	3.3V_SR	3.3V_SR	
A-84	5.0V_SR	5.0V_SR		B-157	3.3V_SR	3.3V_SR	
A-85	PI0	NC#		B-156	PJ0	GPIO 118 (GPIO_PH6)	
A-86	PI1	GPIO 129 (GPIO_PI1)		B-155	PJ1	GPIO 119 (I2C1_CLK)	
A-87	PI2	GPIO 130 (GPIO_PI2)		B-154	PJ2	GPIO 120 (I2C1_DATA)	
A-88	PI3	NC#		B-153	PJ3	GPIO 121 (GPIO_PH9)	
A-89	PI4	NC#		B-152	PJ4	NC#	
A-90	PI5	NC#		B-151	PJ5	NC#	
A-91	PI6	NC#		B-150	PJ6	NC#	
A-92	PI7	NC#		B-149	PJ7	NC#	
A-93	PI8	NC#		B-148	PJ8	NC#	
A-94	PI9	NC#		B-147	PJ9	NC#	
A-95	PI10	NC#		B-146	PJ10	NC#	
A-96	PI11	NC#		B-145	PJ11	NC#	

Connector	Motherboard	257 BGA (SCH NAME)	0-Ohm Link	Connector	Motherboard	257 BGA (SCH NAME)	0-Ohm Link
A-97	PI12	NC#		B-144	PJ12	NC#	
A-98	PI13	NC#		B-143	PJ13	NC#	
A-99	PI14	NC#		B-142	PJ14	NC#	
A-100	PI15	NC#		B-141	PJ15	NC#	
A-101	NC#	NC#		B-140	NC#	NC#	
A-102	NC#	NC#		B-139	NC#	NC#	
A-103	NC#	NC#		B-138	NC#	NC#	
A-104	NC#	NC#		B-137	NC#	NC#	
A-105	PK0	NC#		B-136	PL0	NC#	
A-106	PK1	NC#		B-135	PL1	NC#	
A-107	PK2	NC#		B-134	PL2	NC#	
A-108	PK3	NC#		B-133	PL3	NC#	
A-109	PK4	NC#		B-132	PL4	NC#	
A-110	PK5	NC#		B-131	PL5	NC#	
A-111	PK6	NC#		B-130	PL6	NC#	
A-112	PK7	NC#		B-129	PL7	NC#	
A-113	PK8	NC#		B-128	PL8	NC#	
A-114	PK9	NC#		B-127	PL9	NC#	
A-115	PK10	NC#		B-126	PL10	NC#	
A-116	PK11	NC#		B-125	PL11	NC#	
A-117	PK12	NC#		B-124	PL12	NC#	
A-118	PK13	NC#		B-123	PL13	NC#	
A-119	PK14	NC#		B-122	PL14	NC#	
A-120	PK15	NC#		B-121	PL15	NC#	
A-121	5.0V_LR	5.0V_LR		B-120	5.0V_LR	5.0V_LR	
A-122	5.0V_LR	5.0V_LR		B-119	5.0V_LR	5.0V_LR	
A-123	5.0V_LR	5.0V_LR		B-118	5.0V_LR	5.0V_LR	
A-124	5.0V_LR	5.0V_LR		B-117	5.0V_LR	5.0V_LR	
A-125	PM0	NC#		B-116	PN0	NC#	
A-126	PM1	NC#		B-115	PN1	NC#	
A-127	PM2	NC#		B-114	PN2	NC#	
A-128	PM3	NC#		B-113	PN3	NC#	
A-129	PM4	NC#		B-112	PN4	NC#	
A-130	PM5	NC#		B-111	PN5	NC#	
A-131	PM6	NC#		B-110	PN6	NC#	

Connector	Motherboard	257 BGA (SCH NAME)	0-Ohm Link	Connector	Motherboard	257 BGA (SCH NAME)	0-Ohm Link
A-132	PM7	NC#		B-109	PN7	NC#	
A-133	PM8	NC#		B-108	PN8	NC#	
A-134	PM9	NC#		B-107	PN9	NC#	
A-135	PM10	NC#		B-106	PN10	NC#	
A-136	PM11	NC#		B-105	PN11	NC#	
A-137	PM12	NC#		B-104	PN12	NC#	
A-138	PM13	NC#		B-103	PN13	NC#	
A-139	PM14	NC#		B-102	PN14	NC#	
A-140	PM15	NC#		B-101	PN15	NC#	
A-141	RST-SW	RST-SW		B-100	NC#	NC#	
A-142	VDD_HV_IO_FLEX	3.3v_SR_LDO		B-99	NC#	NC#	
A-143	VDD_HV_IO_FLEX	3.3v_SR_LDO		B-98	NC#	NC#	
A-144	VDD_HV_IO_FLEX	3.3v_SR_LDO		B-97	NC#	NC#	
A-145	PO0	NC#		B-96	PP0	NC#	
A-146	PO1	NC#		B-95	PP1	NC#	
A-147	PO2	NC#		B-94	PP2	NC#	
A-148	PO3	NC#		B-93	PP3	NC#	
A-149	PO4	NC#		B-92	PP4	NC#	
A-150	PO5	NC#		B-91	PP5	NC#	
A-151	PO6	NC#		B-90	PP6	NC#	
A-152	PO7	NC#		B-89	PP7	NC#	
A-153	PO8	NC#		B-88	PP8	NC#	
A-154	PO9	NC#		B-87	PP9	NC#	
A-155	PO10	NC#		B-86	PP10	NC#	
A-156	PO11	NC#		B-85	PP11	NC#	
A-157	PO12	NC#		B-84	PP12	NC#	
A-158	PO13	NC#		B-83	PP13	NC#	
A-159	PO14	NC#		B-82	PP14	NC#	
A-160	PO15	NC#		B-81	PP15	NC#	
A-161	1.25V_SR	1.25V_SR		B-80	1.25V_SR	1.25V_SR	
A-162	1.25V_SR	1.25V_SR		B-79	1.25V_SR	1.25V_SR	
A-163	1.25V_SR	1.25V_SR		B-78	1.25V_SR	1.25V_SR	
A-164	1.25V_SR	1.25V_SR		B-77	1.25V_SR	1.25V_SR	
A-165	PQ0	NC#		B-76	PR0	NC#	
A-166	PQ1	NC#		B-75	PR1	NC#	

Connector	Motherboard	257 BGA (SCH NAME)	0-Ohm Link	Connector	Motherboard	257 BGA (SCH NAME)	0-Ohm Link
A-167	PQ2	NC#		B-74	PR2	NC#	
A-168	PQ3	NC#		B-73	PR3	NC#	
A-169	PQ4	NC#		B-72	PR4	NC#	
A-170	PQ5	NC#		B-71	PR5	NC#	
A-171	PQ6	NC#		B-70	PR6	NC#	
A-172	PQ7	NC#		B-69	PR7	NC#	
A-173	PQ8	NC#		B-68	PR8	NC#	
A-174	PQ9	NC#		B-67	PR9	NC#	
A-175	PQ10	NC#		B-66	PR10	NC#	
A-176	PQ11	NC#		B-65	PR11	NC#	
A-177	PQ12	NC#		B-64	PR12	NC#	
A-178	PQ13	NC#		B-63	PR13	NC#	
A-179	PQ14	NC#		B-62	PR14	NC#	
A-180	PQ15	NC#		B-61	PR15	NC#	
A-181	5.0V_SR	5.0V_SR		B-60	5.0V_SR	5.0V_SR	
A-182	5.0V_SR	5.0V_SR		B-59	5.0V_SR	5.0V_SR	
A-183	5.0V_SR	5.0V_SR		B-58	5.0V_SR	5.0V_SR	
A-184	5.0V_SR	5.0V_SR		B-57	5.0V_SR	5.0V_SR	
A-185	PS0	NC#		B-56	PT0	NC#	
A-186	PS1	NC#		B-55	PT1	NC#	
A-187	PS2	NC#		B-54	PT2	NC#	
A-188	PS3	NC#		B-53	PT3	NC#	
A-189	PS4	NC#		B-52	PT4	NC#	
A-190	PS5	NC#		B-51	PT5	NC#	
A-191	PS6	NC#		B-50	PT6	NC#	
A-192	PS7	NC#		B-49	PT7	NC#	
A-193	PS8	NC#		B-48	PT8	NC#	
A-194	PS9	NC#		B-47	PT9	NC#	
A-195	PS10	NC#		B-46	PT10	NC#	
A-196	PS11	NC#		B-45	PT11	NC#	
A-197	PS12	NC#		B-44	PT12	NC#	
A-198	PS13	NC#		B-43	PT13	NC#	
A-199	PS14	NC#		B-42	PT14	NC#	
A-200	PS15	NC#		B-41	PT15	NC#	
A-201	3.3V_SR	3.3V_SR		B-40	3.3V_SR	3.3V_SR	

Connector	Motherboard	257 BGA (SCH NAME)	0-Ohm Link	Connector	Motherboard	257 BGA (SCH NAME)	0-Ohm Link
A-202	3.3V_SR	3.3V_SR		B-39	3.3V_SR	3.3V_SR	
A-203	3.3V_SR	3.3V_SR		B-38	3.3V_SR	3.3V_SR	
A-204	3.3V_SR	3.3V_SR		B-37	3.3V_SR	3.3V_SR	
A-205	PU0	NC#		B-36	PV0	NC#	
A-206	PU1	NC#		B-35	PV1	NC#	
A-207	PU2	NC#		B-34	PV2	NC#	
A-208	PU3	NC#		B-33	PV3	NC#	
A-209	PU4	NC#		B-32	PV4	NC#	
A-210	PU5	NC#		B-31	PV5	NC#	
A-211	PU6	NC#		B-30	PV6	NC#	
A-212	PU7	NC#		B-29	PV7	NC#	
A-213	PU8	NC#		B-28	PV8	NC#	
A-214	PU9	NC#		B-27	PV9	NC#	
A-215	PU10	NC#		B-26	PV10	NC#	
A-216	PU11	NC#		B-25	PV11	NC#	
A-217	PU12	NC#		B-24	PV12	NC#	
A-218	PU13	NC#		B-23	PV13	NC#	
A-219	PU14	NC#		B-22	PV14	NC#	
A-220	PU15	NC#		B-21	PV15	NC#	
A-221	VDD_HV_IO_MAIN	3.3v_SR_LDO		B-20	VDD_HV_IO_MAIN	3.3v_SR_LDO	
A-222	VDD_HV_IO_MAIN	3.3v_SR_LDO		B-19	VDD_HV_IO_MAIN	3.3v_SR_LDO	
A-223	VDD_HV_IO_MAIN	3.3v_SR_LDO		B-18	VDD_HV_IO_MAIN	3.3v_SR_LDO	
A-224	VDD_HV_IO_MAIN	3.3v_SR_LDO		B-17	VDD_HV_IO_MAIN	3.3v_SR_LDO	
A-225	PW0	NC#		B-16	PX0	NC#	
A-226	PW1	NC#		B-15	PX1	NC#	
A-227	PW2	NC#		B-14	PX2	NC#	
A-228	PW3	NC#		B-13	PX3	NC#	
A-229	PW4	NC#		B-12	PX4	NC#	
A-230	PW5	NC#		B-11	PX5	NC#	
A-231	PW6	NC#		B-10	PX6	NC#	
A-232	PW7	NC#		B-9	PX7	NC#	
A-233	PW8	NC#		B-8	PX8	NC#	
A-234	PW9	NC#		B-7	PX9	NC#	
A-235	PW10	NC#		B-6	PX10	NC#	
A-236	PW11	NC#		B-5	PX11	NC#	

Connector	Motherboard	257 BGA (SCH NAME)	0-Ohm Link	Connector	Motherboard	257 BGA (SCH NAME)	0-Ohm Link
A-237	PW12	NC#		B-4	PX12	NC#	
A-238	PW13	NC#		B-3	PX13	NC#	
A-239	PW14	NC#		B-2	PX14	NC#	
A-240	PW15	NC#		B-1	PX15	NC#	

Some of the port pins of the MCU have dedicated functionality or require short trace lengths to improve signal intgrity . Therefore these signal have been routed to jumper or connectors on the daughter card.

1. JTAG - (J24)
2. Nexus Aurora – (J23)
3. SIPI – (J17)
4. Sigma Delta ADC – (J16)
5. DAC – (J18)
6. CTE – (J13)
7. MIPI-CSI2 – (J15)
8. RGMII – (U8) (Gb Ethernet Physical Layer)

6. Default jumper summary table

The details for the DEFAULT jumper configuration of the EVB as set up on delivery can be found in Table 12 and Table 13 depending on the required regulation mode.

6.1. Default jumper table - motherboard

On delivery the motherboard comes with a default jumper configuration. Table 15 lists and describes briefly the jumpers on the MPC57xx motherboard and indicates which jumpers are on/off on delivery of the board.

Table 15. Default jumper table - motherboard

Jumper	Default Pos	PCB Legend	Description
J8	Off	MASTER	LIN Master/Slave select
J9	Off	CAP A DIS	Disable capacitor circuitry for FlexRAY_A signals
J10	Off	CAP A DIS	Disable capacitor circuitry for

Jumper	Default Pos	PCB Legend	Description
			FlexRAY_A signals
J11	Off	CAP B DIS	Disable capacitor circuitry for FlexRAY_B signals
J12	Off	CAP B DIS	Disable capacitor circuitry for FlexRAY_B signals
J13	Off	SCI TX	Connect SCI TX signal
J14	Off	SCI RX	Connect SCI RX signal
J15	Off	LIN_EN	Enable LIN PHY U50
J16	Off	LIN_RX	Connect LIN RX signal
J17	Off	LIN_TX	Connect LIN TX signal
J18	Off	-	Ethernet signal: RXCLK
J20	Off	-	Ethernet signal: CRS_LEDCFG
J21	Off	CAN2_EN	PHY U2 configuration: 1-2: WAKE to GND 3-4: STB to 5V 5-6: EN to 5V
J22	On	-	Ethernet phy power-on
J23	Off	CAN-EN	PHY U1 configuration: 1-2: WAKE to GND 3-4: STB to 5V 5-6: EN to 5V
J24	Off	-	Ethernet signal: RXER_MDIXEN
J25	Off	SCI-PWR	SCI phy power-on
J26	Off	-	Ethernet signal: RXDV_MIIMODE
J27	Off	FR-A	1-2: PHY U4 TX to MCU 3-4: PHY U4 TXEN to MCU 5-6: PHY U4 RX to MCU
J28	Off	FR-A	PHY U4 configuration: 1-2: 3.3V (V_{IO}) to BGE 3-4: 3.3V (V_{IO}) to EN 5-6: 3.3V (V_{IO}) to STBY 7-8: GND to WAKE
J29	Off	FR_PWR	FlexRAY transceiver VIO selection 1-2: 12V to V_{BAT} 3-4: 5V_SR to V_{CC} and V_{BUF}
J30	Off	FR_B	1-2: PHY U5 TX to MCU 3-4: PHY U5 TXEN to MCU

Jumper	Default Pos	PCB Legend	Description
			5-6: PHY U5 RX to MCU
J31	Off	FR_B	PHY U5 configuration: 1-2: 3.3V (V_{IO}) to BGE 3-4: 3.3V (V_{IO}) to EN 5-6: 3.3V (V_{IO}) to STBY 7-8: GND to WAKE
J32	Off	CAN2	1-2: PHY TX to MCU 3-4: WAKE to GND
J33	Off	CAN-PWR	1-2: 5V_SR to PHY U2 V_{CC} 3-4: 12V to PHY U2 V_{BAT}
J34	Off	-	MCAN2 signal out: 1: ERR 2: INH
J35	Off	CAN	1-2: 5V_SR to PHY U1 V_{CC} 3-4: 12V to PHY U1 V_{BAT}
J36	Off	-	CAN PHY U1 signal out
J37	Off	-	CAN TX connect
J38	Off	-	CAN RX connect
J39	Off	-	Ethernet signal: RXD0_PHYAD1
J40	Off	-	Ethernet signal: RXD1_PHYAD1
J41	Off	-	Ethernet signal: RXD2_PHYAD2
J42	Off	-	Ethernet signal: RXD3_PHYAD3
J44	Off	-	Ethernet signal: COL_PHYAD0
J45	Off	-	Ethernet signal: TXEN
J46	Off	-	Ethernet signal: TXCLK
J47	Off	-	Ethernet signal: TXD0
J48	Off	-	Ethernet signal: TXD1
J49	Off	-	Ethernet signal: TXD2
J50	Off	-	Ethernet signal: TXD3_SNIMODE
J51	Off	-	Ethernet signal: MDC
J52	Off	-	Ethernet signal: MDIO
J53	Off	RV1	Connect RV1 to analug input AN0

Jumper	Default Pos	PCB Legend	Description
J54	Off	ADC_VSUP	Connect EVB supply voltages to analog inputs
J55	Off	12V (4.3V)	Connect 12V (scaled to 4.3V) EVB power to analog input
J57	On	ENABLE	Enable 5V linear regulator
J58	Off	DISABLE	Disable 1.25V switching regulator
J59	Off	DISABLE	Disable 3.3V switching regulator
J60	Off	DISABLE	Disable 5.0V switching regulator

6.2. User qrea

There is a rectangular prototype area on the motherboard top right corner, consisting of a 0.1 inch pitch array of through-hole plated pads. Power from all the three switching regulators is readily accessible along with GND through JP1 – JP16 next to the prototyping area. This area is ideal for the addition of any custom circuitry.

There are four active low user LEDs D2, D3, D4 and D5, these are driven by connecting a logic 0 signal to the corresponding pin on 0.1” header P7 (USER LEDS). The LED inputs are pulled to VDD_HV_IO_MAIN through 10kOhm resistors.

There are f active high pushbutton switches SW1, SW2, SW3 and SW4 which will drive 5 V onto the respective pins on 0.1” connector P6 when pressed. The switch outputs are pulled to GND via 10kOhm.

Potentiometer RV1 can be connected to port pin PB[0] and is adjustable between GND and 5V from the linear regulator. Power from all regulators can be connected to port pins as through J54:

- 1-2: 1.25V_SR to PB[1]
- 3-4: 3.3V_SR to PB[2]
- 5-6: 5V_SR to PB[3]
- 7-8: 5V_LR to PB[4]

The P12V rail from the 12 V input is scaled to 4.3 V through the voltage divider of R81 and R82 and the scaled voltage can be connected to PB[5] via J55.

6.3. Known issues

No known issues.

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