Document Number: A2V07H400-04N
Rev. 1, 05/2020

RoHS

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 107 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 450 to 851 MHz.

600 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 48 Vdc, I_{DQA} = 700 mA, V_{GSB} = 1.3 Vdc, P_{out} = 107 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
595 MHz	19.4	58.4	6.8	–29.8
623 MHz	19.9	59.4	7.1	–30.1
652 MHz	19.8	57.2	7.1	–32.2

460 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 48 Vdc, I_{DQA} = 400 mA, V_{GSB} = 1.5 Vdc, P_{out} = 112 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

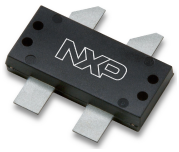
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
460 MHz	17.6	58.7	7.2	–29.7
465 MHz	17.7	58.7	7.1	–30.6
470 MHz	17.9	57.1	7.0	–32.2

Features

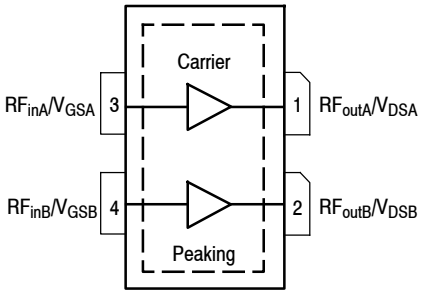
- Advanced high performance in-package Doherty
- Greater negative gate-source voltage range for improved Class C operation
- Designed for digital predistortion error correction systems

A2V07H400-04NR3

450–851 MHz, 107 W AVG., 48 V AIRFAST RF POWER LDMOS TRANSISTOR



OM-780-4L PLASTIC



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +105	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	55, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 78°C, 107 W Avg., W-CDMA, 48 Vdc, I_{DQA} = 700 mA, V_{GSB} = 1.3 Vdc, 623 MHz	$R_{\theta JC}$	0.35	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Charge Device Model (per JESD22-C101)	C3

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 105 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 55 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics - Side A, Carrier					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 137 μAdc)	$V_{GS(th)}$	1.3	1.7	2.3	Vdc
Gate Quiescent Voltage (V_{DD} = 48 Vdc, I_{DA} = 700 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	2.0	2.5	3.3	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.4 Adc)	$V_{DS(on)}$	0.1	0.24	0.5	Vdc
On Characteristics - Side B, Peaking					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 211 μAdc)	$V_{GS(th)}$	1.3	1.8	2.3	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.1 Adc)	$V_{DS(on)}$	0.1	0.24	0.5	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
4. Each side of device measured separately.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2) (In NXP Doherty Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQA} = 700 mA, V_{GSB} = 1.3 Vdc, P_{out} = 107 W Avg., f = 623 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	18.9	19.9	21.9	dB
Drain Efficiency	η_D	55.0	59.4	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.5	7.1	—	dB
Adjacent Channel Power Ratio	ACPR	—	–30.1	–28.0	dBc
Load Mismatch (2) (In NXP Doherty Test Fixture, 50 ohm system) I_{DQA} = 700 mA, V_{GSB} = 1.3 Vdc, f = 623 MHz, 12 μsec(on), 10% Duty Cycle					
VSWR 10:1 at 55 Vdc, 487 W Pulsed CW Output Power (3 dB Input Overdrive from 43 W Pulsed CW Rated Power)		No Device Degradation			
Typical Performance (2) (In NXP Doherty Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQA} = 700 mA, V_{GSB} = 1.3 Vdc, 595–652 MHz Bandwidth					
P_{out} @ 3 dB Compression Point (3)	P3dB	—	537	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 595–652 MHz frequency range)	Φ	—	–18	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	70	—	MHz
Gain Flatness in 57 MHz Bandwidth @ P_{out} = 107 W Avg.	G_F	—	0.5	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.0019	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP3dB	—	0.0022	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2V07H400-04NR3	R3 Suffix = 250 Units, 32 mm Tape Width, 13-inch Reel	OM-780-4L

1. Part internally input matched.
2. Measurement made with device in an asymmetrical Doherty configuration.
3. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

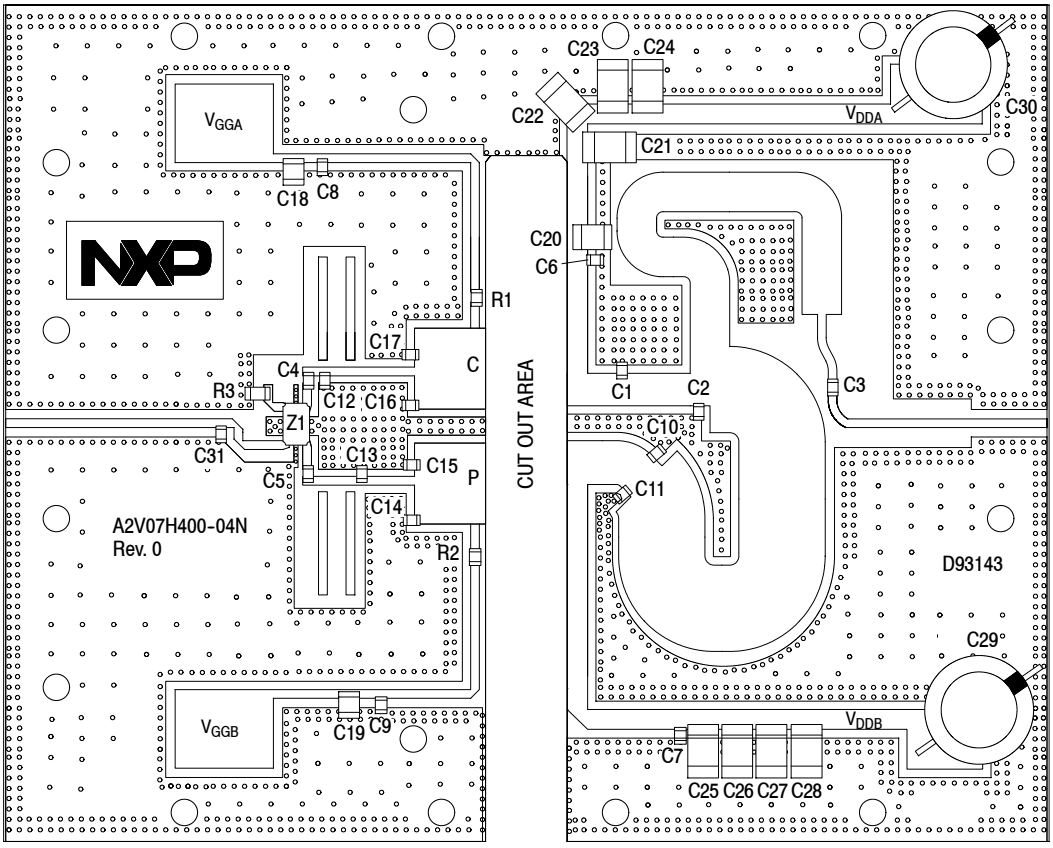


Figure 2. A2V07H400-04NR3 Test Circuit Component Layout

Table 7. A2V07H400-04NR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	3 pF Chip Capacitor	GQM2195C2E3R0BB12D	Murata
C2	8.2 pF Chip Capacitor	GQM2195C2E8R2BB12D	Murata
C3, C4, C5, C6, C7, C8, C9	150 pF Chip Capacitor	ATC600F151JT250XT	ATC
C10, C11	22 pF Chip Capacitor	GQM2195C2E220GB12D	Murata
C12, C13	10 pF Chip Capacitor	GQM2195C2E100FB12D	Murata
C14, C15	7.5 pF Chip Capacitor	GQM2195C2E7R5BB12D	Murata
C16, C17	5.1 pF Chip Capacitor	GQM2195C2E5R1BB12D	Murata
C18, C19	3.3 μF Chip Capacitor	GRM32DR71H335KA88B	Murata
C20	4.7 μF Chip Capacitor	C4532X7S2A475K230KB	TDK
C21, C22, C23, C24, C25, C26, C27, C28	15 μF Chip Capacitor	C5750X7S2A156M230KB	TDK
C29, C30	220 μF, 100 V Electrolytic Capacitor	MCGPR100V227M16X26-RH	Multicomp
C31	0.5 pF Chip Capacitor	GQM2195C2ER50BB12D	Murata
R1, R2	4.7 Ω, 1/8 W Chip Resistor	CRCW08054R70FKEA	Vishay
R3	50 Ω, 10 W Termination Chip Resistor	81A7031-50-5F	Florida Labs
Z1	690–1000 MHz Band, 90°, 2 dB Hybrid Coupler	X3C07F1-02S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D93143	MTL

TYPICAL CHARACTERISTICS — 595–652 MHz

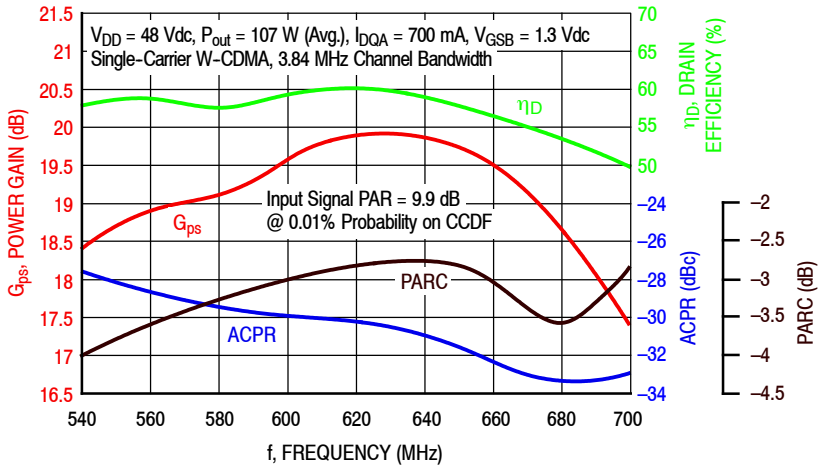


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 107 Watts Avg.

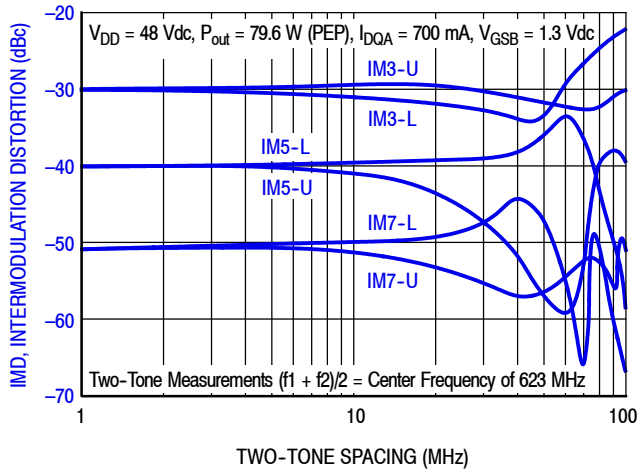


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

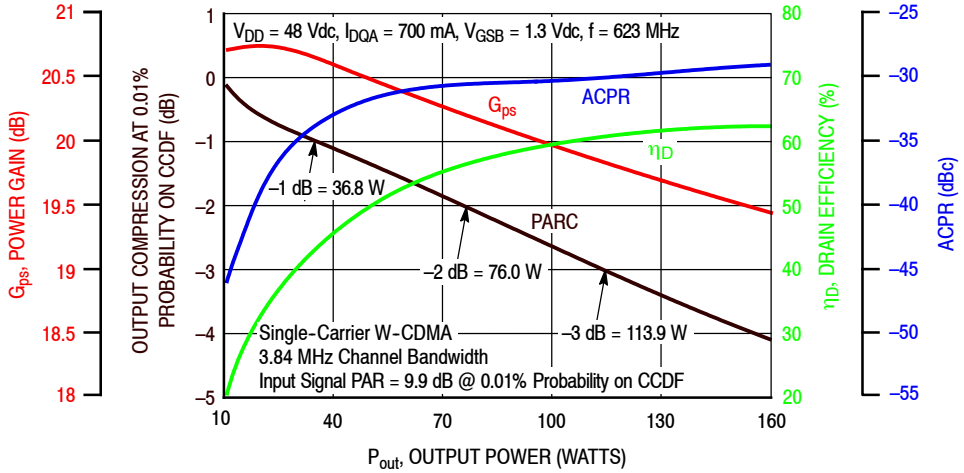


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 595–652 MHz

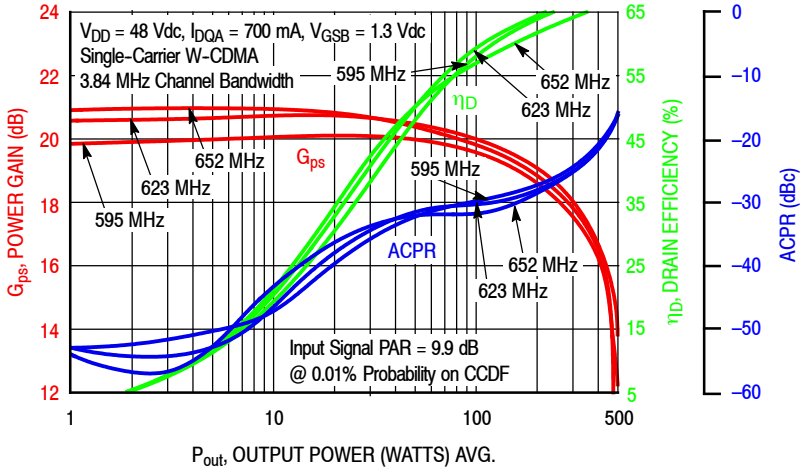


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

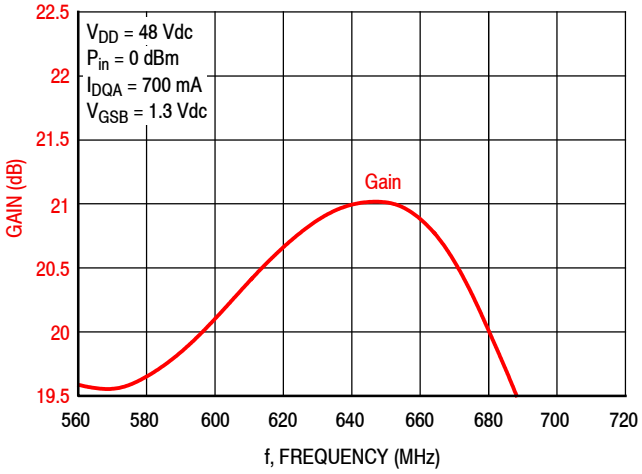


Figure 7. Broadband Frequency Response

Table 8. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, I_{DQA} = 587 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
595	5.59 – j1.07	5.63 + j1.22	3.69 – j1.30	20.2	53.7	232	57.9	–10
652	3.48 – j3.28	3.83 + j2.85	2.61 – j0.24	20.9	54.3	267	63.9	–10

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
595	5.59 – j1.07	5.24 + j1.14	3.49 – j0.71	18.6	54.7	294	65.8	–10
652	3.48 – j3.28	3.70 + j3.09	2.76 – j0.47	18.7	54.9	308	64.6	–13

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 9. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 48 Vdc, I_{DQA} = 587 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
595	5.59 – j1.07	5.09 + j1.52	4.96 + j1.21	21.9	52.6	182	68.4	–9
652	3.48 – j3.28	3.07 + j3.40	2.92 + j2.95	23.8	51.6	143	77.1	–15

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
595	5.59 – j1.07	4.52 + j1.65	4.82 + j2.83	20.6	52.7	185	75.0	–6
652	3.48 – j3.28	3.33 + j3.47	3.47 + j2.04	21.0	53.4	217	78.0	–18

(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

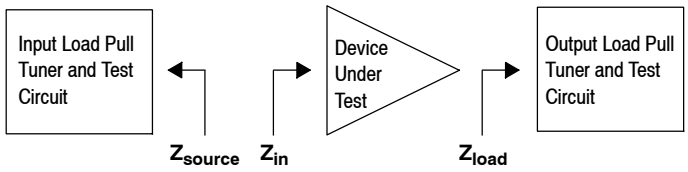


Table 10. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, V_{GSB} = 0.8 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
595	3.33 – j2.82	2.81 + j2.89	2.17 – j1.28	15.9	56.1	404	64.9	–17
652	2.46 – j5.29	2.41 + j5.25	1.89 – j0.88	16.2	56.0	396	67.0	–19

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
595	3.33 – j2.82	2.63 + j3.00	2.10 – j1.20	13.9	56.6	459	66.5	–19
652	2.46 – j5.29	2.28 + j5.45	1.99 – j1.31	13.8	56.6	454	61.7	–21

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 11. Peaking Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 48 Vdc, V_{GSB} = 0.8 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
595	3.33 – j2.82	2.67 + j2.90	3.11 + j1.23	16.6	53.7	233	77.1	–19
652	2.46 – j5.29	2.24 + j5.21	2.31 + j1.40	16.9	53.3	212	78.3	–23

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
595	3.33 – j2.82	2.52 + j3.01	3.11 + j1.11	14.6	54.3	269	76.7	–20
652	2.46 – j5.29	2.13 + j5.43	2.35 + j1.57	14.8	53.7	235	77.6	–29

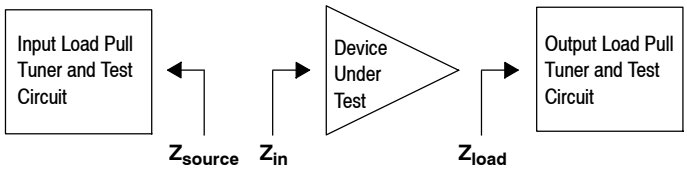
(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 652 MHz

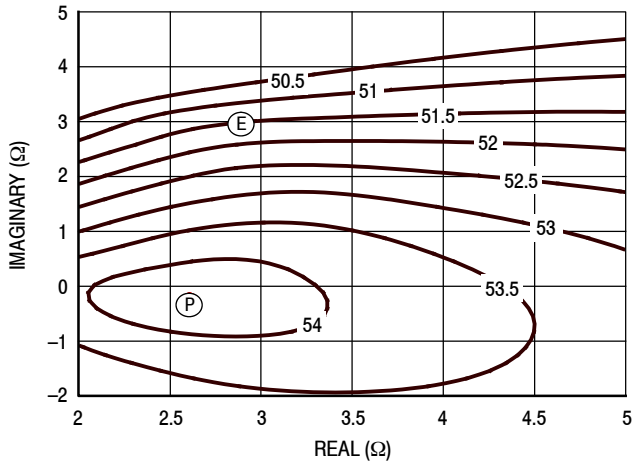


Figure 8. P1dB Load Pull Output Power Contours (dBm)

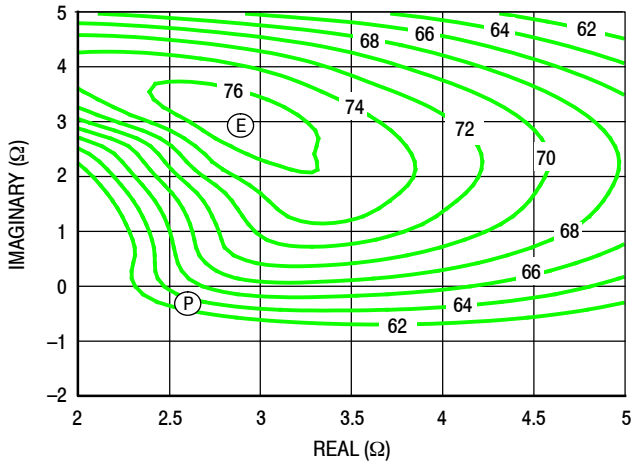


Figure 9. P1dB Load Pull Efficiency Contours (%)

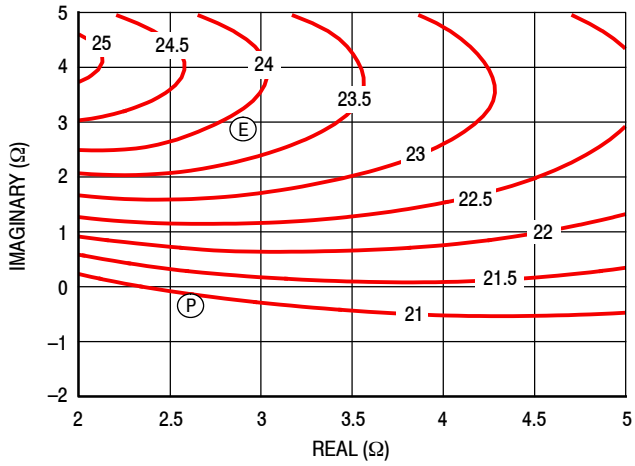


Figure 10. P1dB Load Pull Gain Contours (dB)

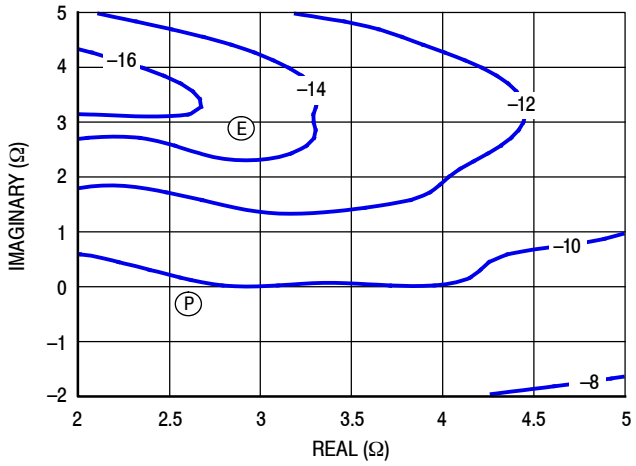


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 652 MHz

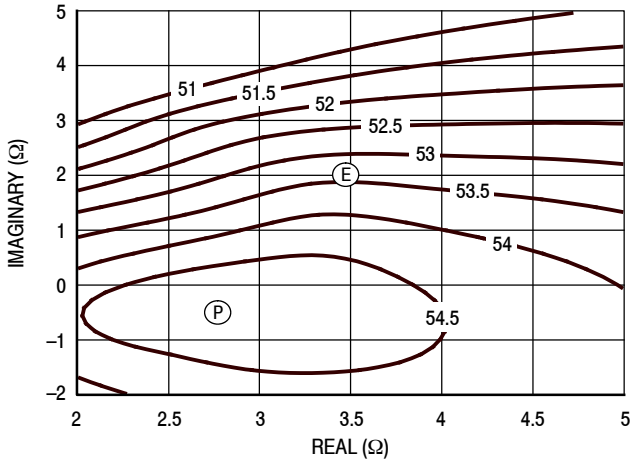


Figure 12. P3dB Load Pull Output Power Contours (dBm)

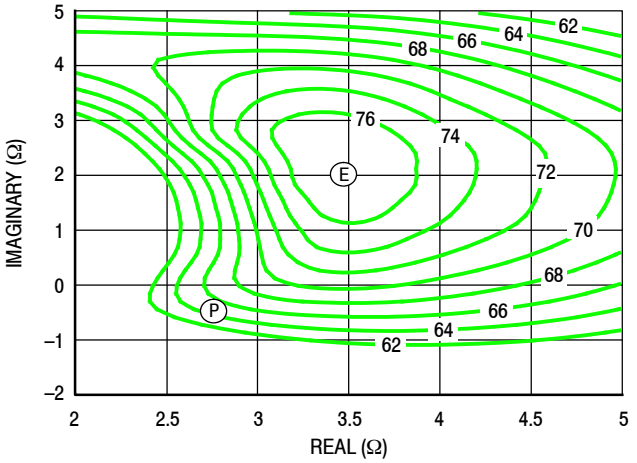


Figure 13. P3dB Load Pull Efficiency Contours (%)

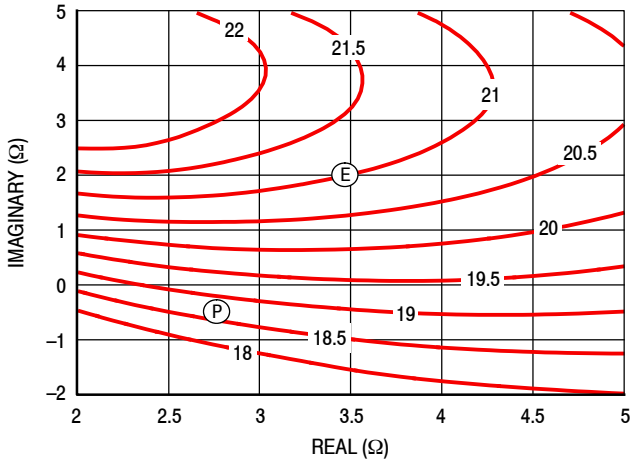


Figure 14. P3dB Load Pull Gain Contours (dB)

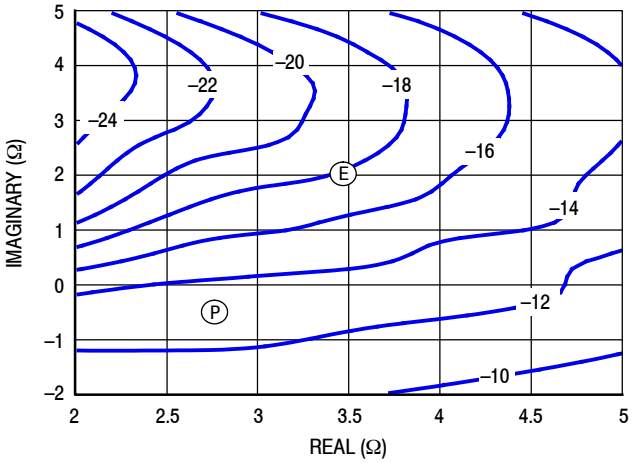


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 652 MHz

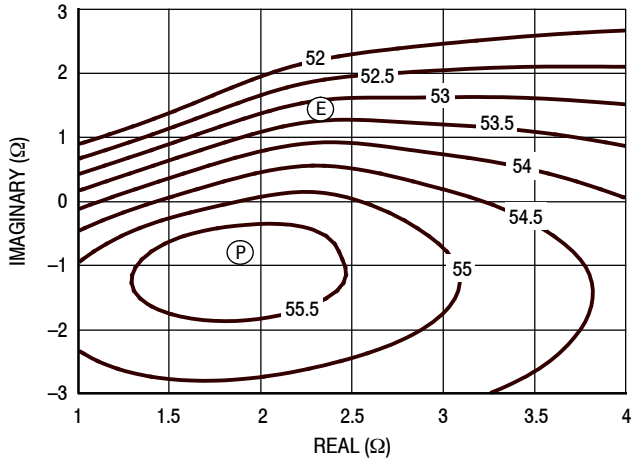


Figure 16. P1dB Load Pull Output Power Contours (dBm)

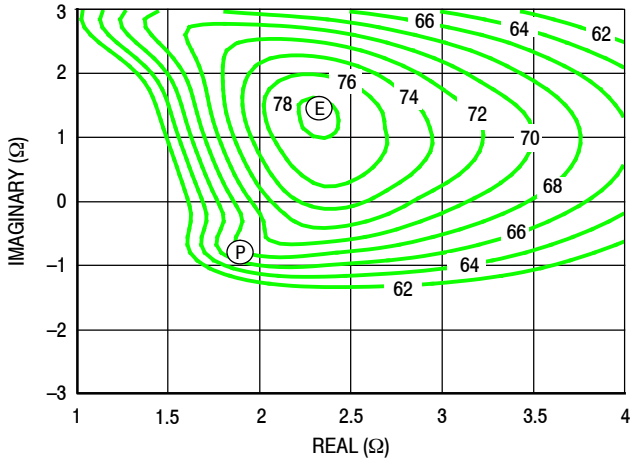


Figure 17. P1dB Load Pull Efficiency Contours (%)

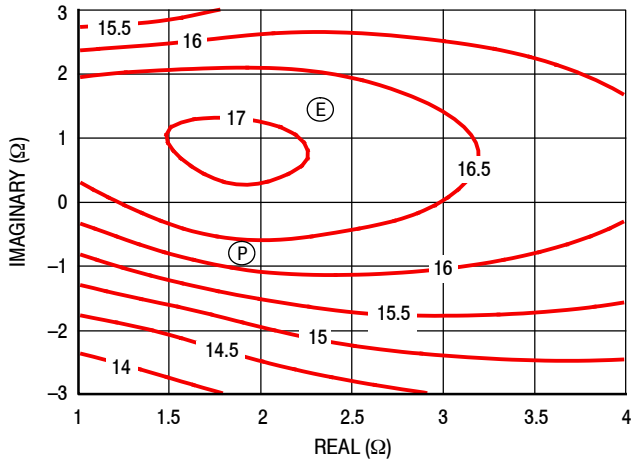


Figure 18. P1dB Load Pull Gain Contours (dB)

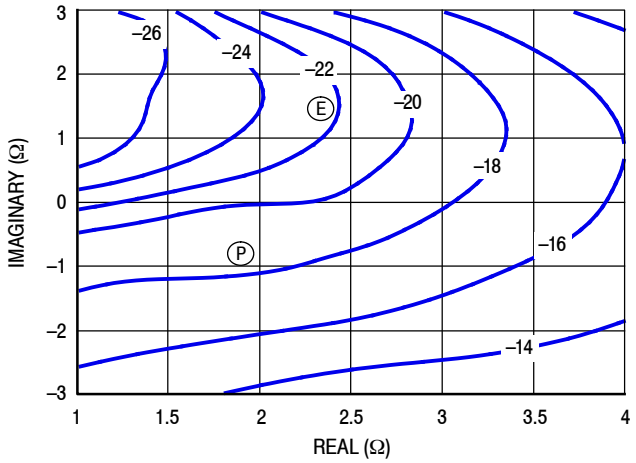


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 652 MHz

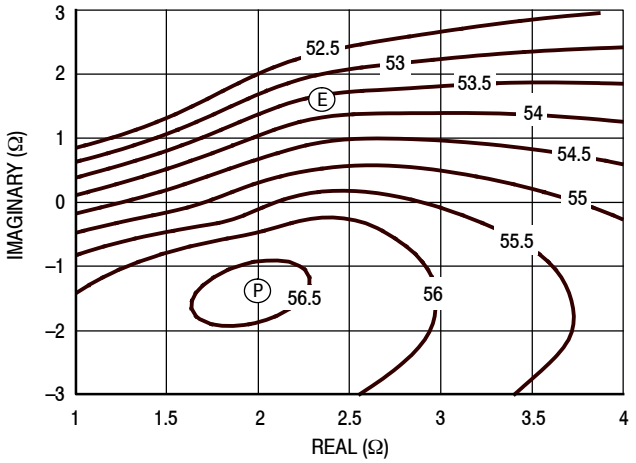


Figure 20. P3dB Load Pull Output Power Contours (dBm)

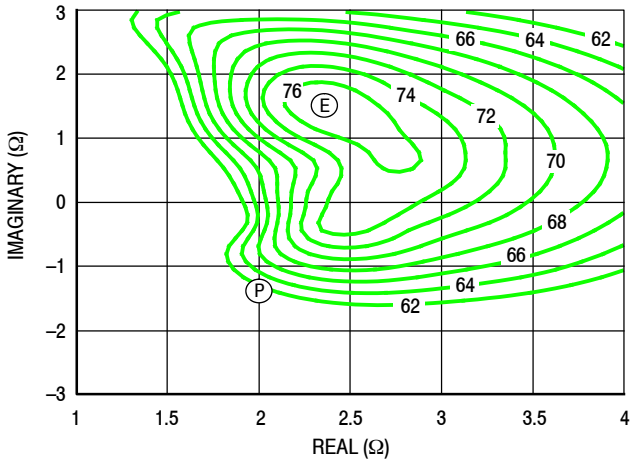


Figure 21. P3dB Load Pull Efficiency Contours (%)

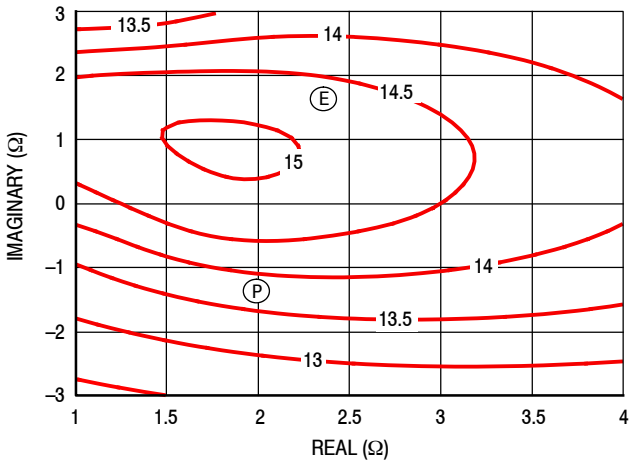


Figure 22. P3dB Load Pull Gain Contours (dB)

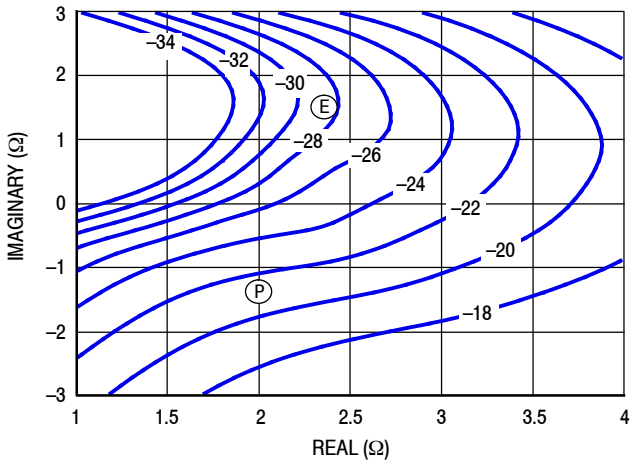


Figure 23. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

Table 12. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, I_{DQA} = 564 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
758	3.45 – j7.62	3.54 + j7.67	1.98 – j0.62	20.8	54.0	252	61.0	–10
780	3.87 – j8.86	4.00 + j8.84	1.93 – j0.70	20.5	54.0	252	61.2	–10
822	5.64 – j11.3	5.81 + j11.5	2.14 – j1.25	19.5	53.7	235	58.5	–8

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
758	3.45 – j7.62	3.48 + j7.93	2.23 – j0.78	18.7	54.9	309	65.3	–14
780	3.87 – j8.86	3.95 + j9.13	2.21 – j0.90	18.4	54.8	305	65.9	–14
822	5.64 – j11.3	5.75 + j11.8	2.31 – j1.41	17.4	54.6	289	61.3	–12

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 13. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 48 Vdc, I_{DQA} = 564 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
758	3.45 – j7.62	3.14 + j8.20	1.70 + j2.22	23.7	50.0	100	76.1	–14
780	3.87 – j8.86	3.64 + j9.40	1.65 + j1.90	23.3	50.1	104	74.5	–16
822	5.64 – j11.3	5.72 + j11.9	2.14 + j1.28	21.9	50.8	120	72.3	–12

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
758	3.45 – j7.62	3.46 + j8.53	2.55 + j2.22	21.1	51.7	149	76.0	–19
780	3.87 – j8.86	3.85 + j9.64	2.26 + j1.65	20.8	52.0	157	74.9	–20
822	5.64 – j11.3	5.71 + j12.4	2.14 + j1.24	19.8	51.6	146	72.9	–18

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

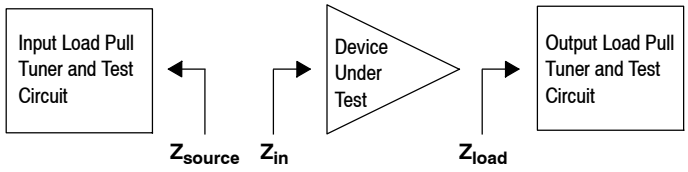


Table 14. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, V_{GSB} = 0.99 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
758	3.36 – j10.5	3.20 + j10.6	1.39 – j1.51	15.7	56.1	410	64.1	–17
780	3.99 – j12.0	3.83 + j12.0	1.36 – j1.61	15.4	56.2	413	63.2	–15
822	6.50 – j15.4	6.21 + j15.6	1.35 – j1.76	14.5	55.9	385	62.9	–13

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
758	3.36 – j10.5	3.09 + j10.8	1.51 – j1.66	13.6	56.9	492	64.3	–20
780	3.99 – j12.0	3.73 + j12.3	1.41 – j1.75	13.2	56.9	493	63.8	–19
822	6.50 – j15.4	6.16 + j16.0	1.47 – j1.91	12.3	56.6	462	64.1	–17

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 15. Peaking Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 48 Vdc, V_{GSB} = 0.99 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
758	3.36 – j10.5	2.99 + j10.4	1.48 + j0.75	16.5	52.4	174	79.1	–23
780	3.99 – j12.0	3.59 + j11.9	1.51 + j0.46	16.2	52.8	189	78.6	–21
822	6.50 – j15.4	5.67 + j15.2	0.78 + j0.33	14.3	50.2	105	76.7	–32

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
758	3.36 – j10.5	2.96 + j10.7	1.97 + j0.60	14.4	53.9	243	77.4	–25
780	3.99 – j12.0	3.61 + j12.3	2.05 – j0.40	14.3	55.3	337	78.9	–22
822	6.50 – j15.4	5.93 + j15.9	1.69 – j0.35	13.2	54.4	273	76.6	–22

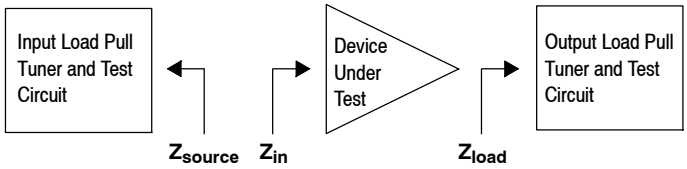
(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS – 780 MHz

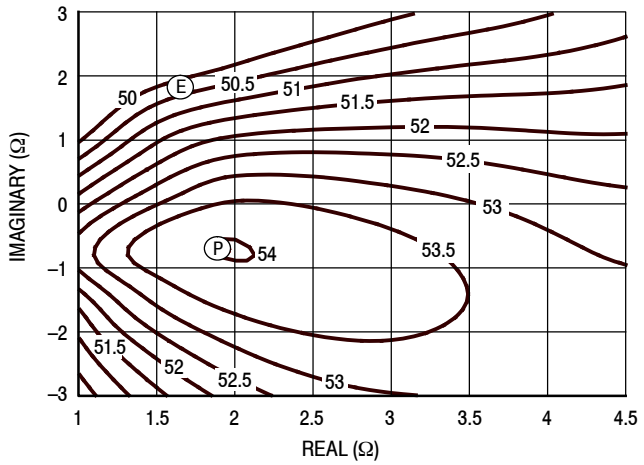


Figure 24. P1dB Load Pull Output Power Contours (dBm)

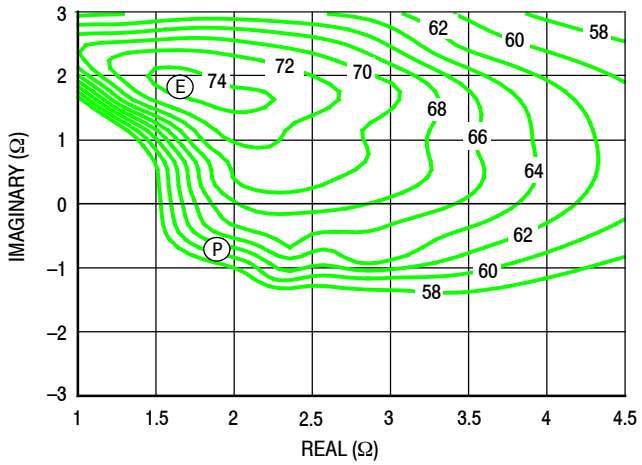


Figure 25. P1dB Load Pull Efficiency Contours (%)

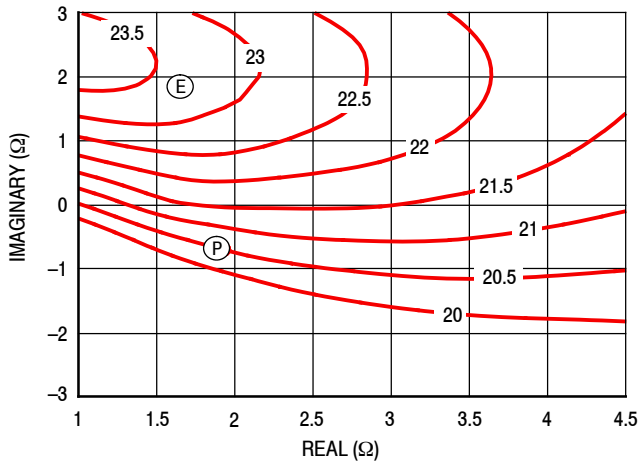


Figure 26. P1dB Load Pull Gain Contours (dB)

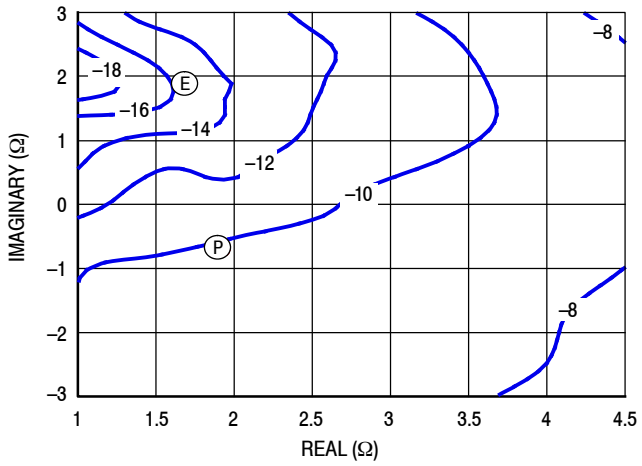


Figure 27. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS – 780 MHz

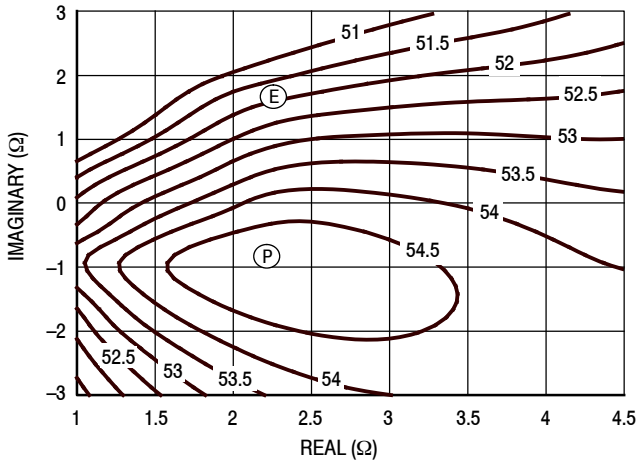


Figure 28. P3dB Load Pull Output Power Contours (dBm)

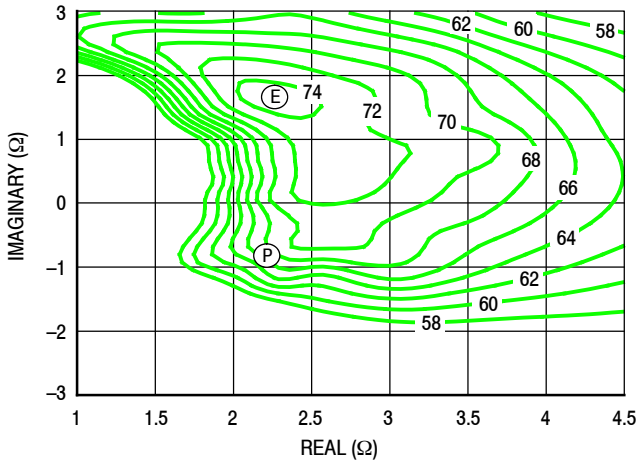


Figure 29. P3dB Load Pull Efficiency Contours (%)

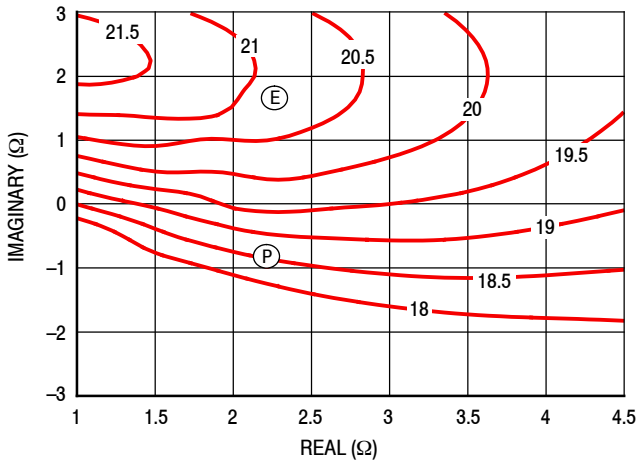


Figure 30. P3dB Load Pull Gain Contours (dB)

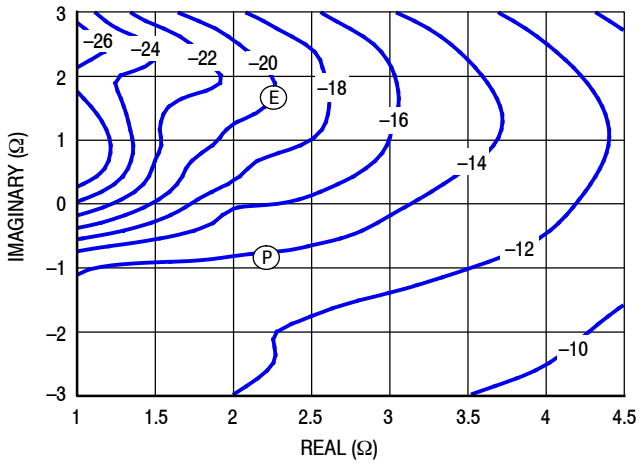


Figure 31. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS – 780 MHz

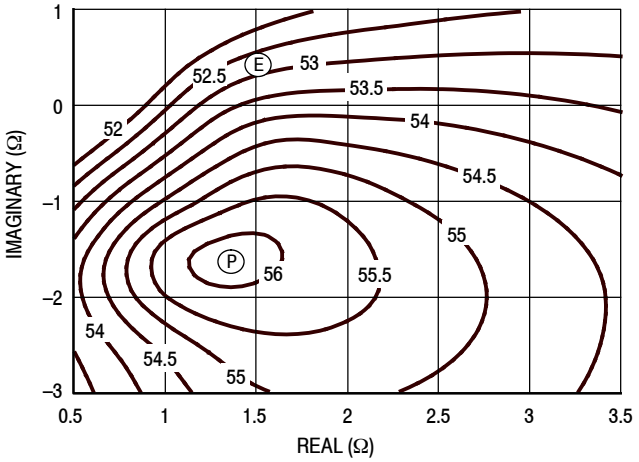


Figure 32. P1dB Load Pull Output Power Contours (dBm)

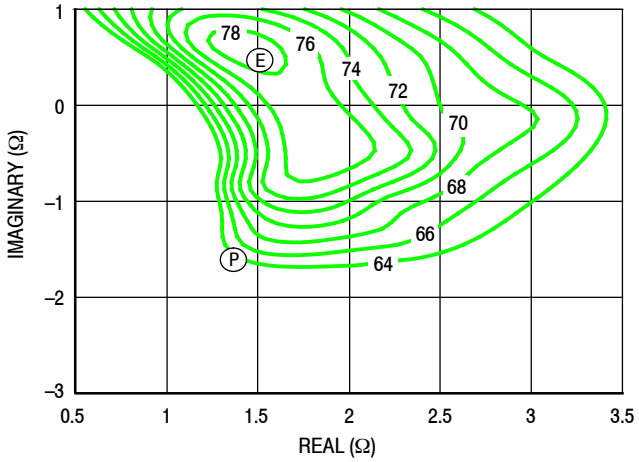


Figure 33. P1dB Load Pull Efficiency Contours (%)

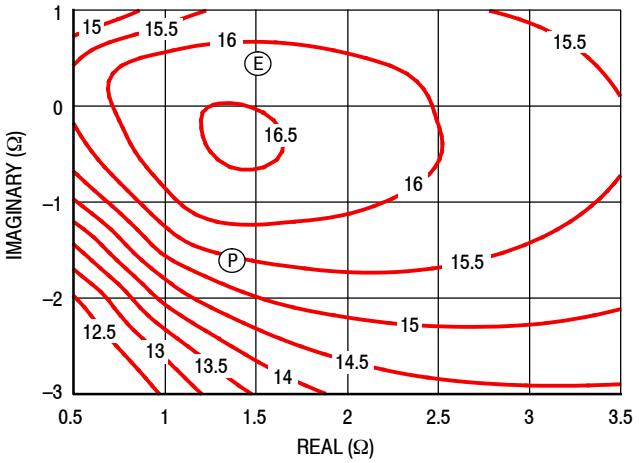


Figure 34. P1dB Load Pull Gain Contours (dB)

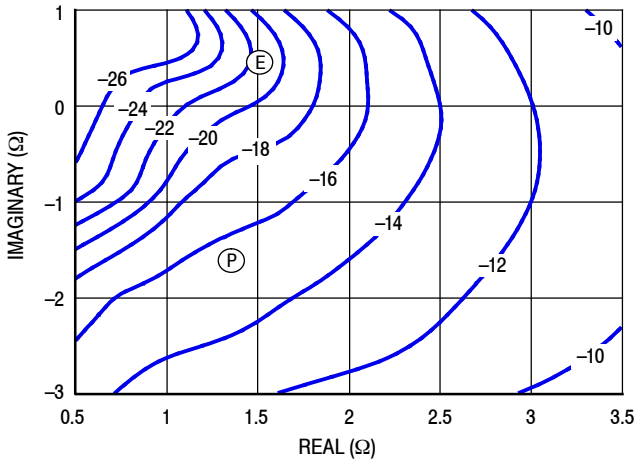


Figure 35. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS – 780 MHz

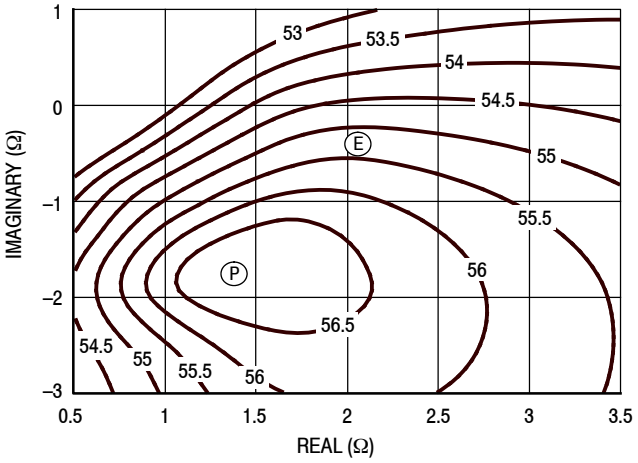


Figure 36. P3dB Load Pull Output Power Contours (dBm)

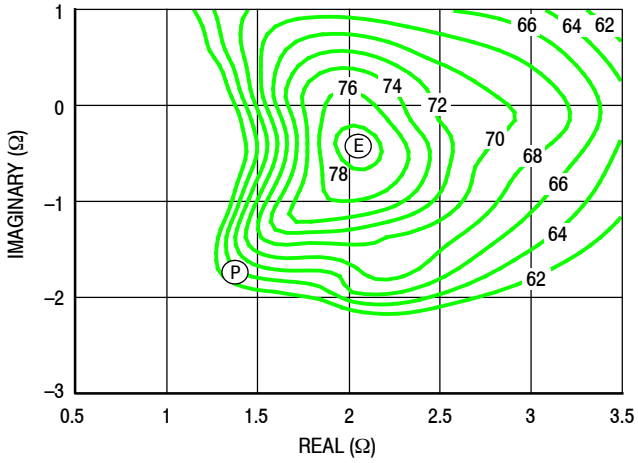


Figure 37. P3dB Load Pull Efficiency Contours (%)

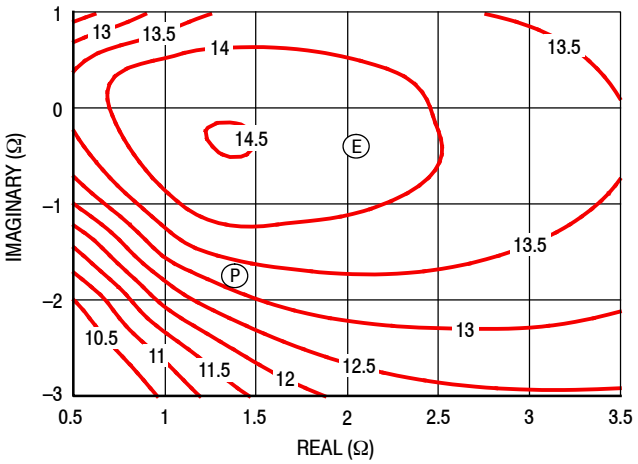


Figure 38. P3dB Load Pull Gain Contours (dB)

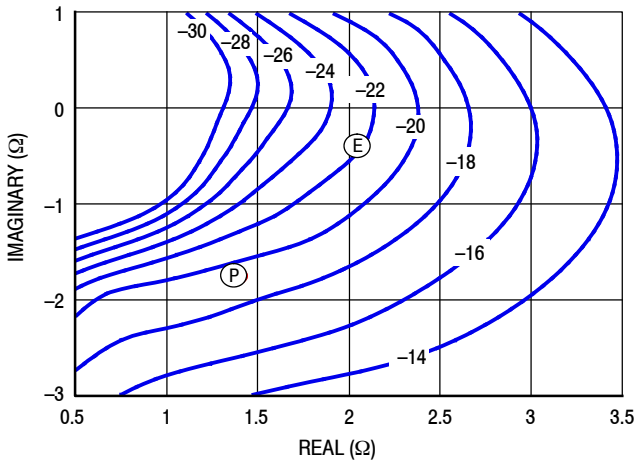


Figure 39. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

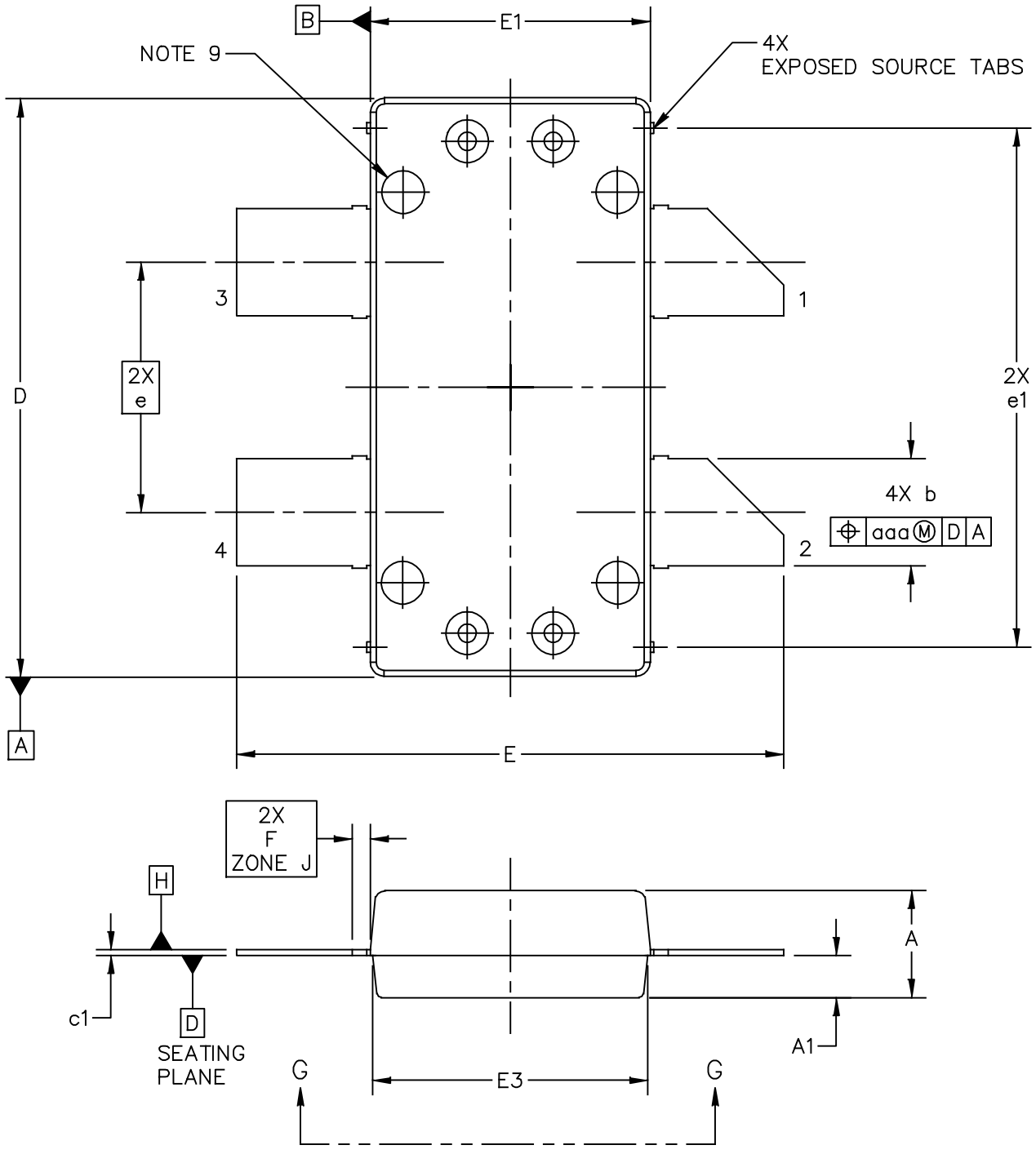
Gain

Drain Efficiency

Linearity

Output Power

PACKAGE INFORMATION



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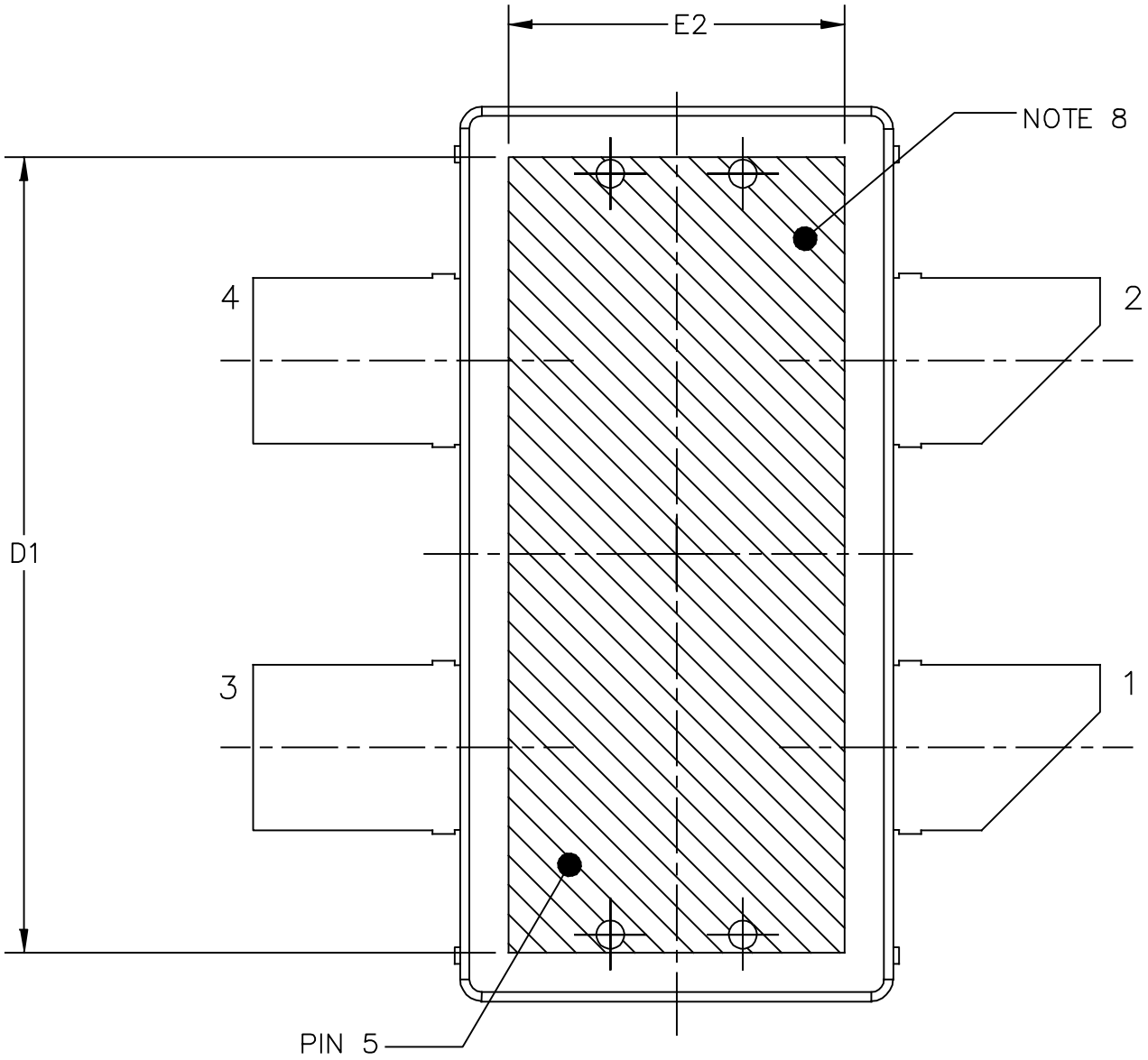
	STANDARD: NON-JEDEC	
	SOT1818-4	16 MAR 2016



BOTTOM VIEW
VIEW G–G

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	STANDARD: NON–JEDEC	
	SOT1818–4	16 MAR 2016

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. DIMENSION A1 APPLIES WITHIN ZONE "J" ONLY.

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

9. DIMPLED HOLE REPRESENTS INPUT SIDE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	0.148	.152	3.76	3.86	b	.147	.153	3.73	3.89
A1	.059	.065	1.50	1.65	c1	.007	.011	0.18	0.28
D	.808	.812	20.52	20.62	e	.350 BSC		8.89 BSC	
D1	.720	----	18.29	----	e1	.721	.729	18.31	18.52
E	.762	.770	19.36	19.56					
E1	.390	.394	9.91	10.01	aaa	.004		0.10	
E2	.306	----	7.77	----					
E3	.383	.387	9.72	9.83					
F	.025 BSC		0.635 BSC						

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TITLE:
OM780–4
STRAIGHT LEAD

DOCUMENT NO: 98ASA10833D REV: B

STANDARD: NON–JEDEC

SOT1818–4 16 MAR 2016

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Sept. 2017	• Initial release of data sheet
1	May 2020	• Changed lower frequency operation of the part from 595 MHz to 450 MHz. Added performance table with corresponding measured data, p. 1

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Rev. 1, 05/2020