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FPF1107 / FPF1108 Advance Load Management Switch

Features

- 1.2V to 4V Input Voltage Operating Range
- Typical $R_{DS(ON)}$:
 - 35m Ω at $V_{IN}=3.3V$
 - 55m Ω at $V_{IN}=1.8V$
 - 85m Ω at $V_{IN}=1.2V$
- Slew Rate Control with t_R : 130 μs
- Output Discharge Function on FPF1108
- Low <1 μA Quiescent Current at $V_{ON}=V_{IN}$
- ESD Protected: Above 4000V HBM, 2000V CDM
- GPIO/CMOS-Compatible Enable Circuitry

Description

The FPF1107/08 are low R_{DS} P-channel MOSFET load switches of the IntelliMAX™ family. Integrated slew-rate control prevents inrush current from glitch supply rails with capacitive loads common in power applications.

The input voltage range operates from 1.2V to 4V to fulfill today's lowest ultra-portable device supply requirements. Switch control is by a logic input (ON-pin) capable of interfacing directly with low-voltage CMOS control signals and GPIOs in embedded processors.

Applications

- Mobile Devices and Smart Phones
- Portable Media Devices
- Digital Cameras
- Advanced Notebook, UMPC, MID
- Portable Medical Devices
- GPS and Navigation Equipment

Ordering Information

Part Number	Part Marking	Switch (Typical) At 1.8V _{IN}	Input Buffer	Output Discharge	ON Pin Activity	t _R	 Eco Status	Package
FPF1107	QC	55m Ω	CMOS	NA	Active HIGH	130 μs	Green	4-Ball, Wafer-Level Chip-Scale Package (WLCSP), 1.0 x 1.0mm, 0.5mm Pitch
FPF1108	QD	55m Ω	CMOS	65 Ω	Active HIGH	130 μs	Green	

 For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Application Diagram

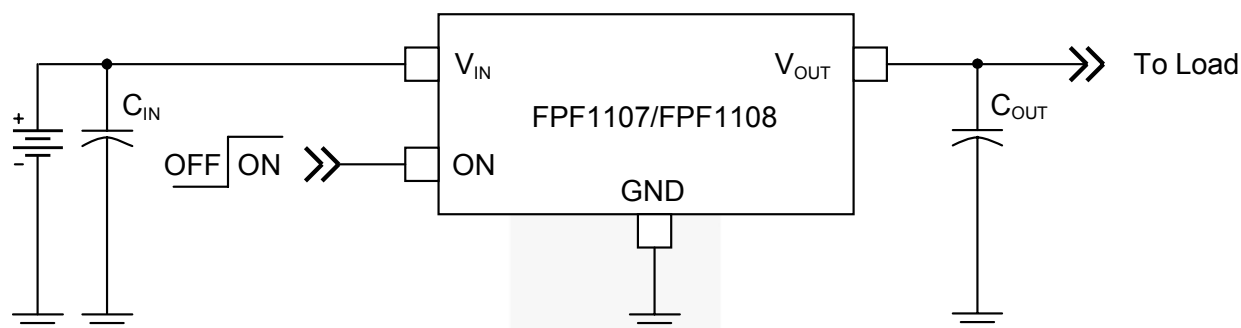


Figure 1. Typical Application

Notes:

1. $C_{IN}=1\mu F$, X5R, 0603, for example Murata GRM185R60J105KE26
2. $C_{OUT}=1\mu F$, X5R, 0805, for example Murata GRM216R61A105KA01

Block Diagram

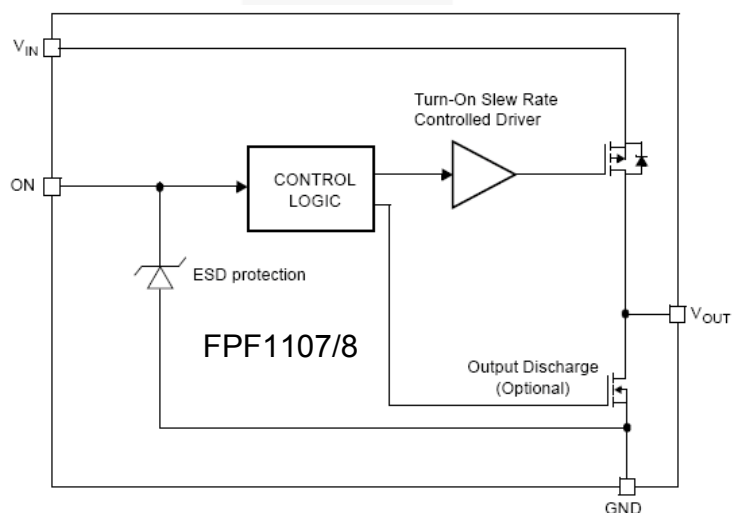


Figure 2. Block Diagram (Output Discharge for FPF1108 Only)

Pin Configurations



Figure 3. 1 x 1mm WLCSP Bumps Facing Down

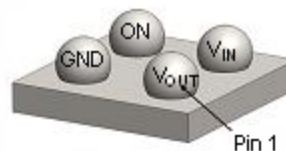


Figure 4. 1 x 1mm WLCSP Bumps Facing Up

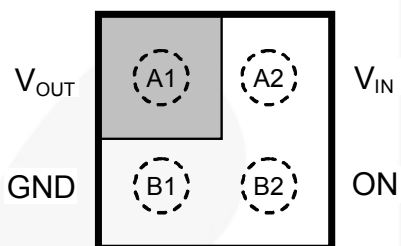


Figure 5. Pin Assignments (Top View)

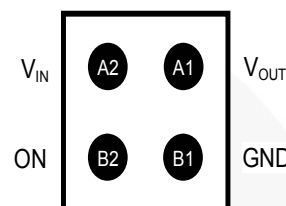


Figure 6. Pin Assignments (Bottom View)

Pin Definitions

Pin #	Name	Description
A1	V _{OUT}	Switch Output
A2	V _{IN}	Supply Input: Input to the Power Switch.
B1	GND	Ground
B2	ON	ON/OFF Control, Active HIGH

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	V_{IN} , V_{OUT} , V_{ON} to GND		-0.3	4.2	V
I_{SW}	Maximum Continuous Switch Current			1.2	A
P_D	Power Dissipation at $T_A=25^{\circ}\text{C}$			1.0	W
T_{STG}	Storage Junction Temperature		-65	+150	$^{\circ}\text{C}$
T_A	Operating Temperature Range		-40	+85	$^{\circ}\text{C}$
Θ_{JA}	Thermal Resistance, Junction-to-Ambient	1S2P with 1 Thermal Via		95	$^{\circ}\text{C/W}$
		1S2P without Thermal Via		187	
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	4		kV
		Charged Device Model, JESD22-C101	2		

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	1.2	4.0	V
T_A	Ambient Operating Temperature	-40	+85	$^{\circ}\text{C}$

Electrical Characteristics

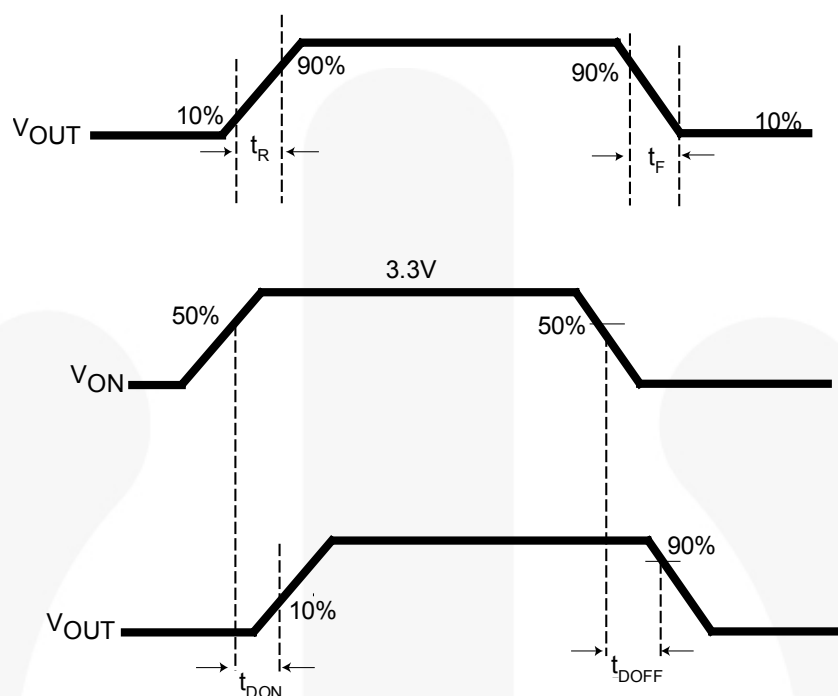
Unless otherwise noted, $V_{IN}=1.2$ to $4.0V$, $T_A=-40$ to $+85^{\circ}C$, typical values are at $V_{IN}=3.3V$ and $T_A=25^{\circ}C$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Basic Operation						
V _{IN}	Supply Voltage		1.2		4.0	V
I _{Q(OFF)}	Off Supply Current	V _{ON} =GND V _{OUT} =Open, V _{IN} =4V			1	μA
I _{SD(OFF)}	Off Switch Current	V _{ON} =GND V _{OUT} =GND			1	μA
I _Q	Quiescent Current	I _{OUT} =0mA, V _{ON} =V _{IN}			1	μA
		I _{OUT} =0mA, V _{ON} < V _{IN}			3	
R _{ON}	On Resistance	V _{IN} =3.3V, I _{OUT} =200mA, T _A =25°C		35	50	mΩ
		V _{IN} =1.8V, I _{OUT} =200mA, T _A =25°C		55	70	
		V _{IN} =1.5V, I _{OUT} =200mA, T _A =25°C		70		
		V _{IN} =1.2V, I _{OUT} =200mA, T _A =25°C		85	150	
		V _{IN} =1.8V, I _{OUT} =200mA, T _A =85°C ⁽³⁾		65	100	
R _{PD}	Output Discharge R _{PULL DOWN}	V _{IN} =3.3V, V _{ON} =0V, I _{FORCE} =20mA, T _A =25°C, PPF1108		65	110	Ω
V _{IH}	On Input Logic High Voltage	V _{IN} =1.2V to 4.0V	1.1			V
V _{IL}	On Input Logic Low Voltage	V _{IN} =1.2V to 4.0V			0.35	V
I _{ON}	On Input Leakage	V _{ON} =V _{IN} or GND	-1		1	μA
Dynamic Characteristics						
t _{DON}	Turn-On Delay ⁽⁴⁾	V _{IN} =3.3V, R _L =10Ω, C _L =0.1μF, T _A =25°C, PPF1107/8		80		μs
t _R	V _{OUT} Rise Time ⁽⁴⁾			130		μs
t _{ON}	Turn-On Time ^(4,6)			210		μs
t _{DON}	Turn-On Delay ⁽⁴⁾	V _{IN} =3.3V, R _L =500Ω, C _L =0.1μF, T _A =25°C, PPF1107/8		70	95	μs
t _R	V _{OUT} Rise Time ⁽⁴⁾			95	120	μs
t _{ON}	Turn-On Time ^(4,6)			165	215	μs
PPF1107						
t _{DOFF}	Turn-Off Delay ⁽⁴⁾	V _{IN} =3.3V, R _L =10Ω, C _L =0.1μF, T _A =25°C		2.0	2.5	μs
t _F	V _{OUT} Fall Time ⁽⁴⁾			2.2		μs
t _{OFF}	Turn-Off ^(4,7)			4.2		μs
t _{DOFF}	Turn-Off Delay ⁽⁴⁾	V _{IN} =3.3V, R _L =500Ω, C _L =0.1μF, T _A =25°C		7.0		μs
t _F	V _{OUT} Fall Time ⁽⁴⁾			110		μs
t _{OFF}	Turn-Off ^(4,7)			117		μs
PPF1108 ⁽⁵⁾						
t _{DOFF}	Turn-Off Delay ⁽⁴⁾	V _{IN} =3.3V, R _L =10Ω, C _L =0.1μF, R _{PD} =65Ω, T _A =25°C		2.0	2.5	μs
t _F	V _{OUT} Fall Time ⁽⁴⁾			1.9		μs
t _{OFF}	Turn-Off ^(4,7)			3.9		μs
t _{DOFF}	Turn-Off Delay ⁽⁴⁾	V _{IN} =3.3V, R _L =500Ω, C _L =0.1μF, R _{PD} =65Ω, T _A =25°C		2.5		μs
t _F	V _{OUT} Fall Time ⁽⁴⁾			10.6		μs
t _{OFF}	Turn-Off ^(4,7)			13.1		μs

Notes:

- This parameter is guaranteed by design and characterization; not production tested.
- $t_{DON}/t_{DOFF}/t_R/t_F$ are defined in Figure 7.
- Output discharge path is enabled during off.

Timing Diagram



Notes:

6. $t_{ON} = t_R + t_{DON}$.
7. $t_{OFF} = t_F + t_{DOFF}$.

Figure 7. Timing Diagram

Typical Performance Characteristics

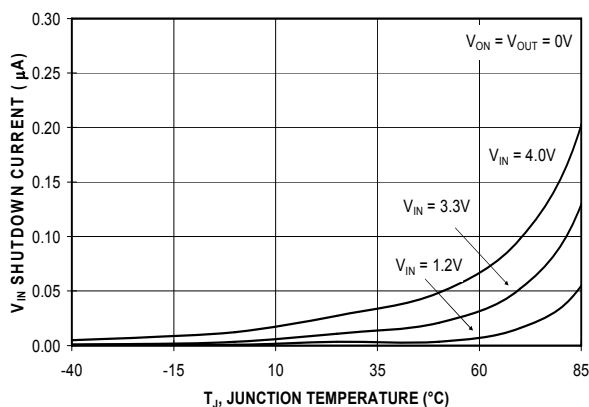


Figure 8. Shutdown Current vs. Temperature

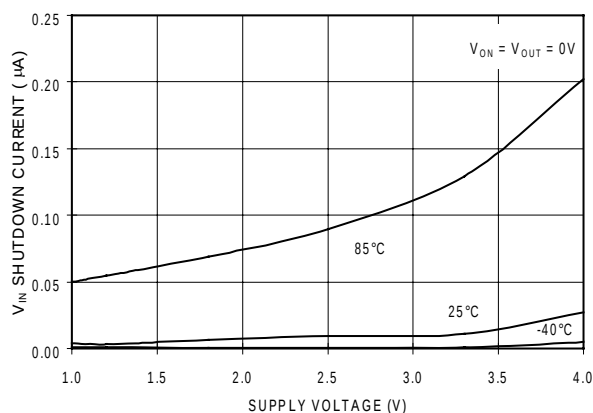


Figure 9. Shutdown Current vs. Supply Voltage

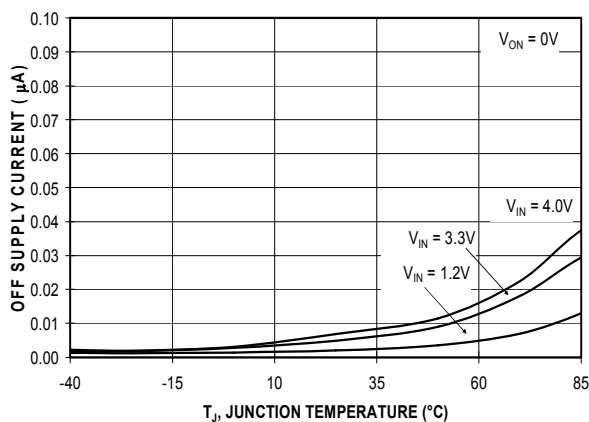


Figure 10. Off Supply Current vs. Temperature
(FPF1107, VOUT is Floating)

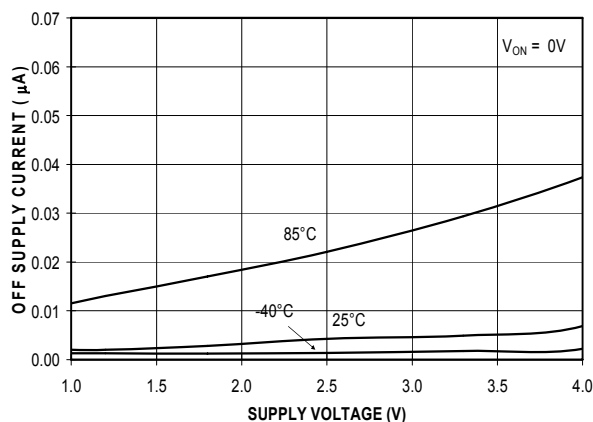


Figure 11. Off Supply Current vs. Supply Voltage
(FPF1107, VOUT is Floating)

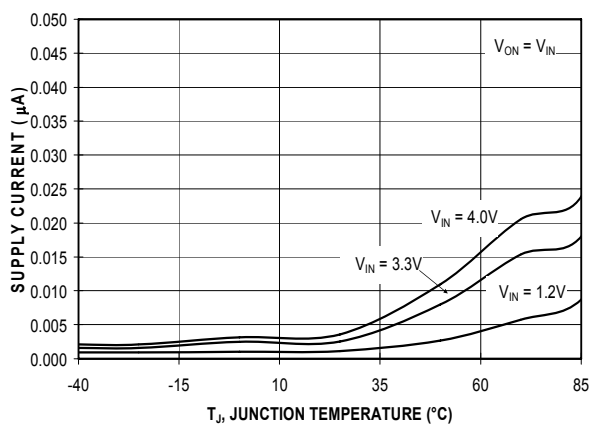


Figure 12. Quiescent Current vs. Temperature
(V_ON=V_IN)

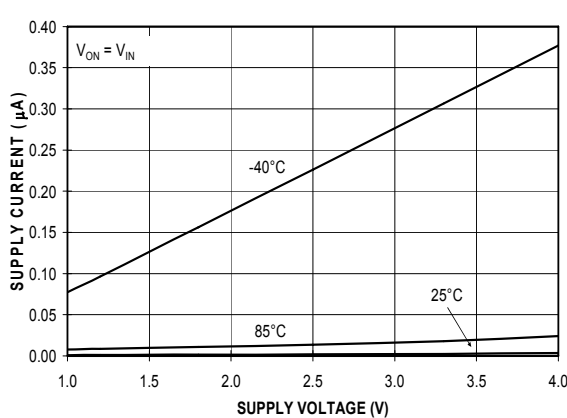


Figure 13. Quiescent Current vs. Supply Voltage

Typical Performance Characteristics

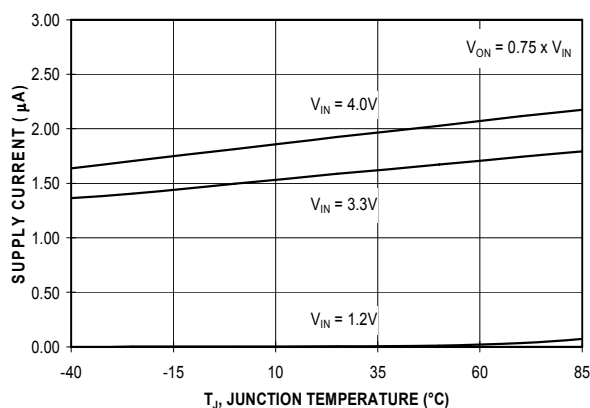


Figure 14. Quiescent Current vs. Temperature
($V_{ON}=0.75 \times V_{IN}$)

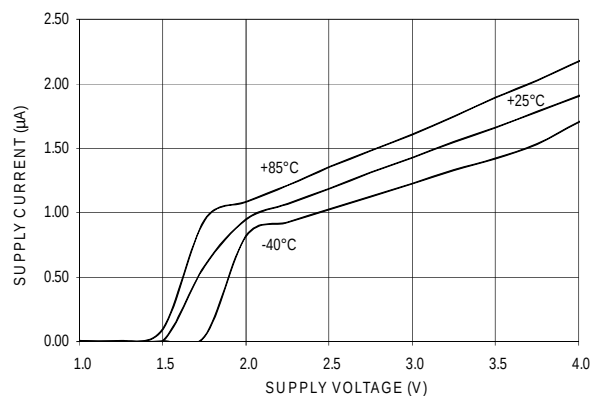


Figure 15. Quiescent Current vs. Supply Voltage
at $V_{ON}=1.2V$

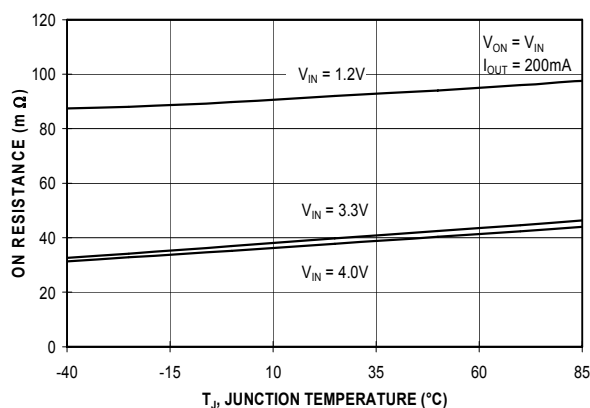


Figure 16. R_{ON} vs. Temperature

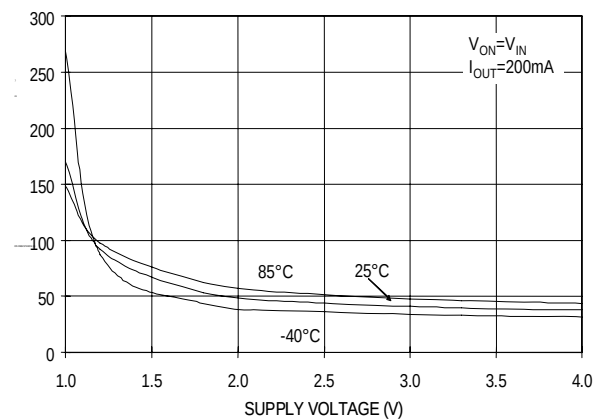


Figure 17. R_{ON} vs. Supply Voltage

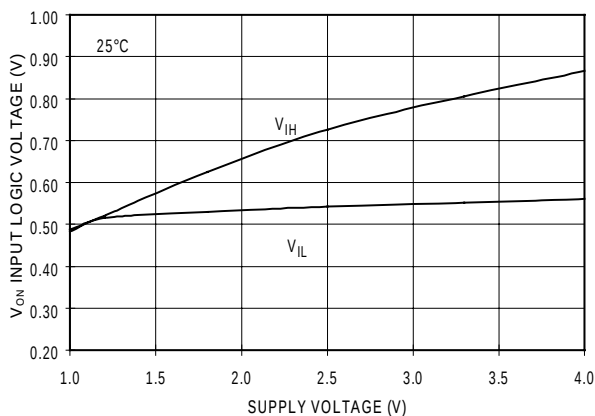


Figure 18. ON-Pin Threshold vs. V_{IN}

Typical Performance Characteristics

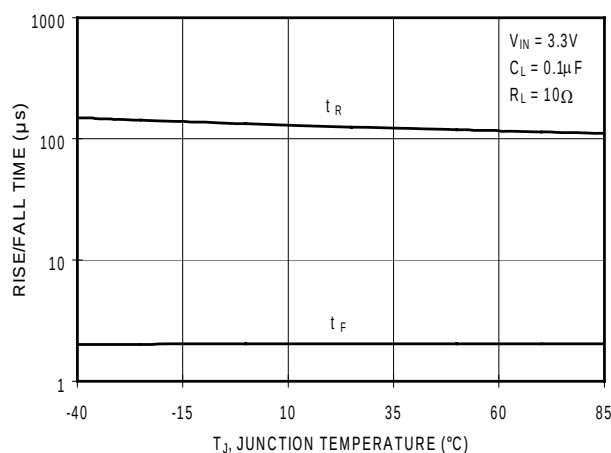


Figure 19. V_{OUT} Rise and Fall Time vs. Temperature at $R_L=10\Omega$

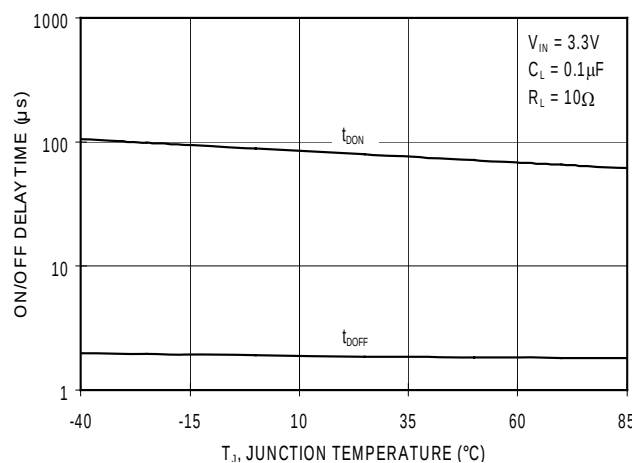


Figure 20. V_{OUT} Turn-On and Turn-Off Delay vs. Temperature at $R_L=10\Omega$

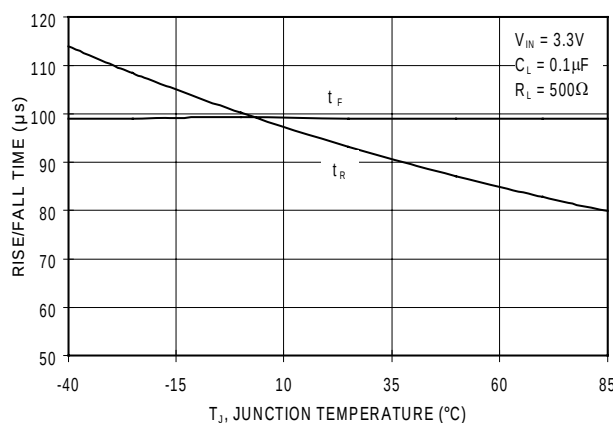


Figure 21. V_{OUT} Rise and Fall Time vs. Temperature at $R_L=500\Omega$

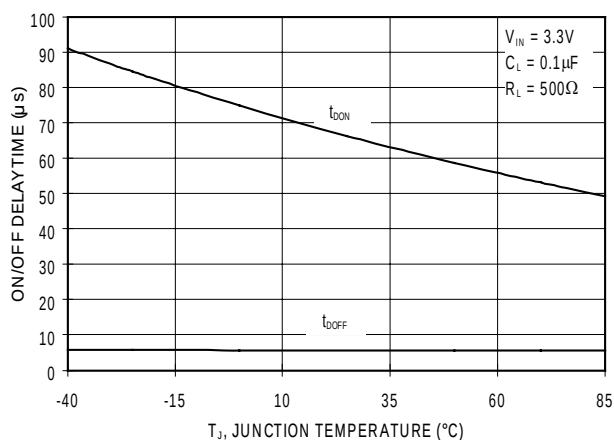


Figure 22. V_{OUT} Turn-On and Turn-Off Delay vs. Temperature at $R_L=500\Omega$

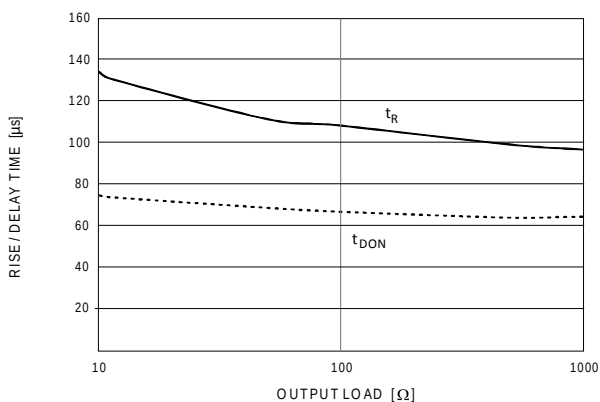


Figure 23. V_{OUT} Turn-On and Turn-Off Delay vs. Output Load at $V_{IN}=3.3V$

Typical Performance Characteristics

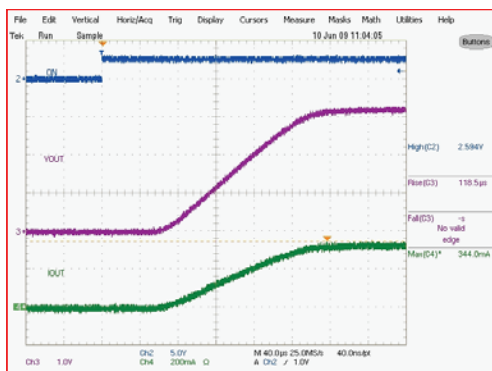


Figure 24. Turn-On Response
($V_{IN}=3.3V$, $C_{IN}=1\mu F$, $C_{OUT}=0.1\mu F$, $R_L=10\Omega$)

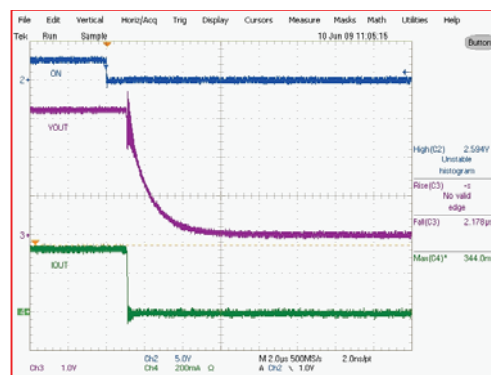


Figure 25. Turn-Off Response
($V_{IN}=3.3V$, $C_{IN}=1\mu F$, $C_{OUT}=0.1\mu F$, $R_L=10\Omega$)

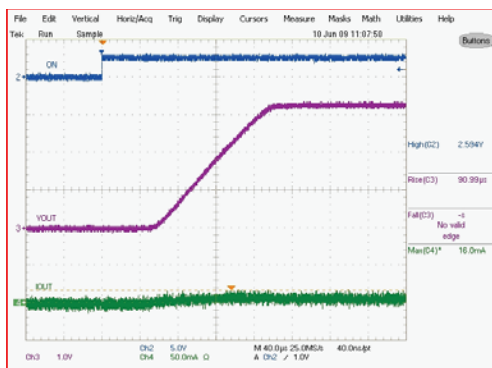


Figure 26. Turn-On Response
($V_{IN}=3.3V$, $C_{IN}=1\mu F$, $C_{OUT}=0.1\mu F$, $R_L=500\Omega$)

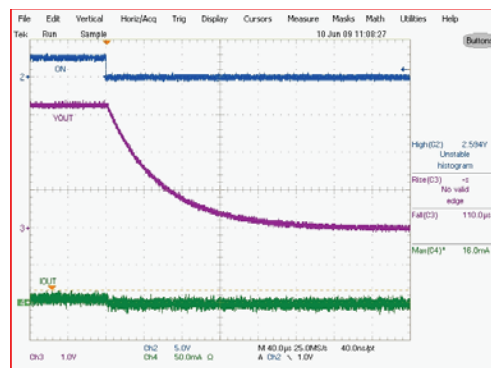


Figure 27. Turn-Off Response
(FPF1107 – No Output Pull-Down Resistor)
($V_{IN}=3.3V$, $C_{IN}=1\mu F$, $C_{OUT}=0.1\mu F$, $R_L=500\Omega$)

Application Information

Input Capacitor

The IntelliMAX™ switch doesn't require input capacitor. To reduce device inrush current effect, a 0.1μF ceramic capacitor, C_{IN}, is recommended close to the VIN pin. A higher value of C_{IN} can be used to further reduce the voltage drop experienced as the switch is turned on into a large capacitive load.

Output Capacitor

The IntelliMAX™ switch works without an output capacitor. However, if parasitic board inductance forces V_{OUT} below GND when switching off, a 0.1μF capacitor, C_{OUT}, should be placed between V_{OUT} and GND.

Fall Time

Device output fall time can be calculated based on RC constant of external components as follows:

$$t_F = R_L \times C_L \times 2.2 \quad (1)$$

where t_F is 90% to 10% fall time, R_L is output load and C_L is output capacitor.

The same equation works for a device with a pull-down output resistor, then R_L is replaced by a parallel connected pull-down and external output resistor combination, as follows:

$$t_F = \frac{R_L \times R_{PD}}{R_L + R_{PD}} \times C_L \times 2.2 \quad (2)$$

where t_F is 90% to 10% fall time, R_L is output load, R_{PD}=65Ω is output pull-down resistor, and C_L is the output capacitor.

Resistive Output Load

If resistive output load is missing, the IntelliMAX™ switch without pull-down output resistor is not discharging output voltage. Output voltage drop depends, in that case, mainly on external device leaks.

Recommended Land Pattern and Layout

For best thermal performance and minimal inductance and parasitic effects, it is recommended to keep input and output traces short and capacitors as close to the

device as possible. Below is a recommended layout for this device to achieve optimum performance.

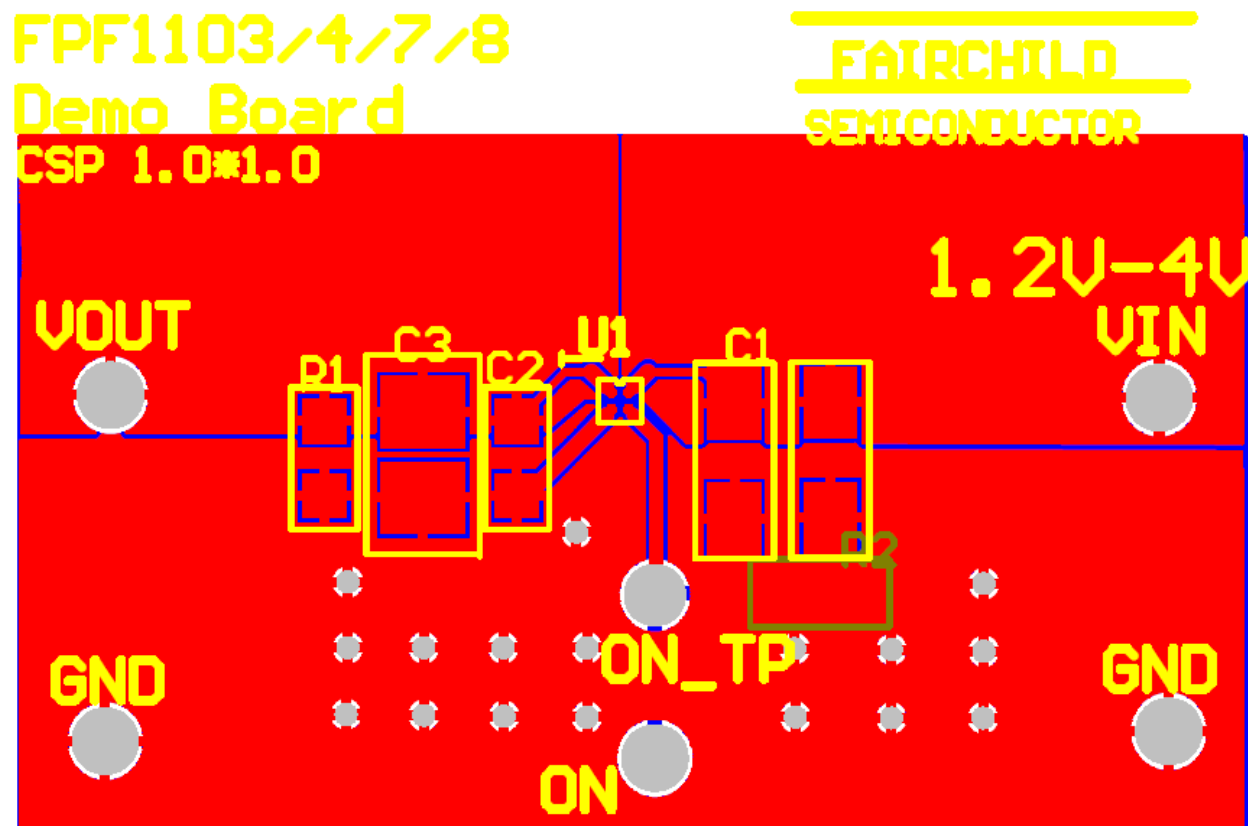
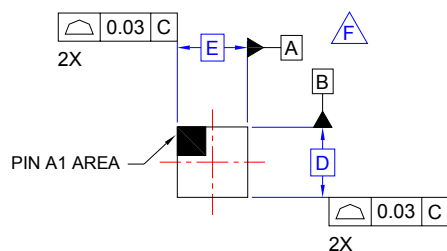
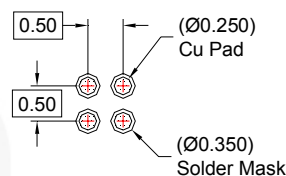


Figure 28. Recommended Land Pattern and Layout

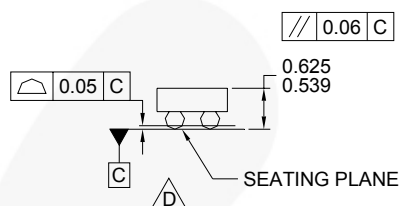
Physical Dimensions



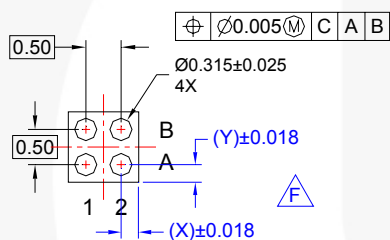
TOP VIEW



RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)



SIDE VIEWS



BOTTOM VIEW

NOTES:

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS 582 MICRONS ± 43 MICRONS (539-625 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.
- G. DRAWING FILENAME: MKT-UC004ABrev2.

Figure 29. 4 Ball, 1.0 x 1.0mm Wafer Level Chip Scale WLCSP Packaging

Product-Specific Dimensions

Product	D	E	X	Y
FPF1107	960 μ m $\pm$ 30 μ m	960 μ m $\pm$ 30 μ m	0.230mm	0.230mm
FPF1108	960 μ m $\pm$ 30 μ m	960 μ m $\pm$ 30 μ m	0.230mm	0.230mm

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FETBench™

FlashWriter®
FPS™
F-PFS™
FRFET®
Global Power Resource™
Green FPS™
Green FPS™ e-Series™
Gmax™
GTO™
IntelliMAX™
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Rev. I43

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