Getting started with the STEVAL-SCR001V1 inrush current limiter board with SCR thyristor

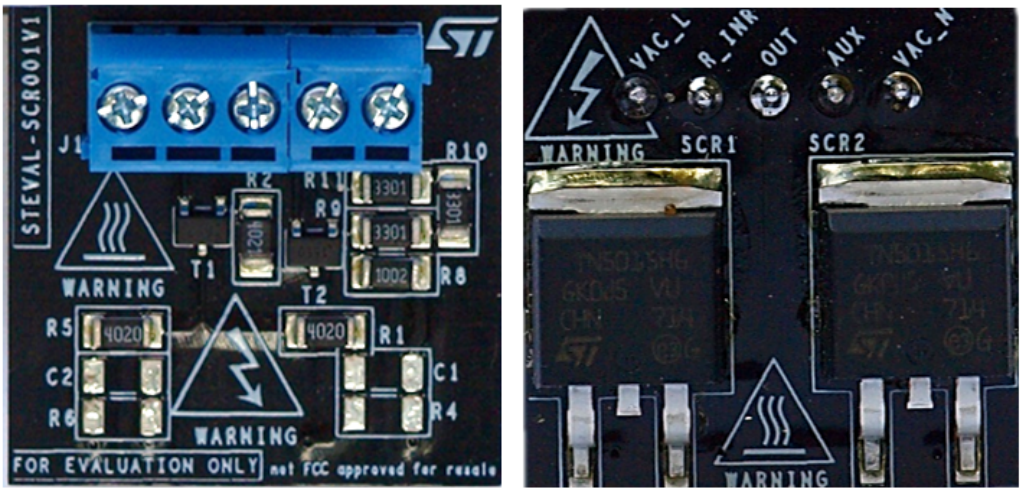
STEVAL-SCR001V1 introduction

Inrush current limiter circuits are designed to protect electrical installations and power converters.

When a power converter starts up, the high current due to the charge in the bulk capacitor can rise up to ten times the nominal system current. This inrush current induces a voltage drop on the mains supply that may affect the operation of other equipment connected to the same power network and damage serial devices like circuit breakers (or fuses) and bridge diodes.

The STEVAL-SCR001V1 evaluation board introduces a simple and innovative solution using only a few surface-mount devices (SMD) in a very compact layout. It is designed to be easily implemented on existing power factor controllers (PFC) or flyback transformers and replaces relays commonly found in power converters to bypass the inrush current limiting resistor.

Figure 1. STEVAL-SCR001V1 evaluation board (top and bottom view)



1 STEVAL-SCR001V1 evaluation board for inrush current protection

The STEVAL-SCR001V1 evaluation board lets you test ST solutions to protect circuits against high inrush currents. The inrush current limiter circuit design uses discrete components only and offers a reliable alternative to relays used in power converters to bypass inrush current limiting resistors.

The board features:

drive circuit self-synchronized to the AC line

pulse mode operation for low gate drive consumption and no SCR reverse losses

50 mA TN5015H-6G SCRs for better immunity to electrical fast transients (EFT)

While SMD SCRs (D2PAK package) are for a compact circuit design, the same circuit can be implemented with traditional through-hole devices placed on a heatsink for improved power dissipation suitable for higher power applications.

Target applications:

- compatible with PFC and flyback converters

Operating range:

- input voltage range: 90-265 VAC, 50/60 Hz
- suitable for applications from 50 W up to 800 W (230 V_{RMS}, T_{AMB} = 60 °C)
- due to board layout (70 µm copper thickness, 800 µm track width) and the technology used for the PCB (FR4 TG180), peak current should remain below 6 A at T_{AMB} = 40°C

Board characteristics:

- simple drive circuit with 2 low voltage transistors and 7 resistors (no MCU)
- requires an unregulated power supply (12 V typically; created from a secondary winding)
- robust and immune (2 kV IEC 61000-4-5, 2.5 kV IEC 61000-4-4) and low EMI noise (EN55014) solution

2 Getting started

2.1 Safety precautions



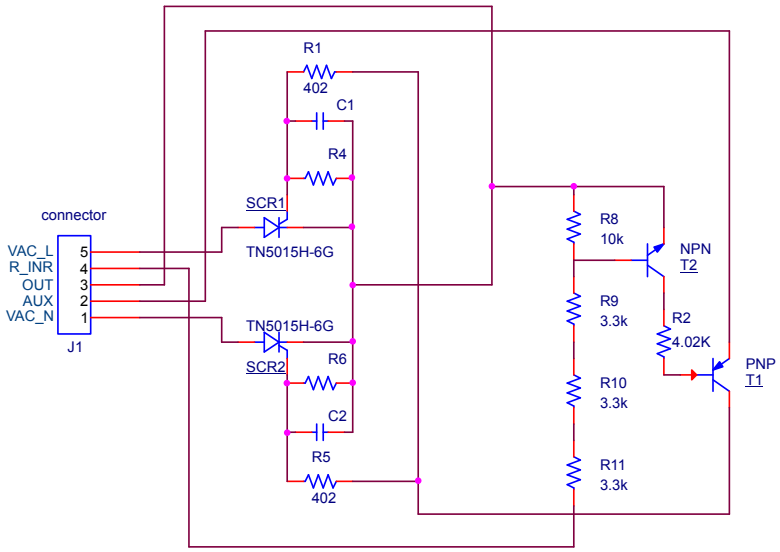
The STEVAL-SCR001V1 is intended to be connected directly on the mains. Non isolated parts at high voltage levels are present on both the top and bottom side of the PCB. This evaluation board must be used in a suitable laboratory only by qualified personnel who are familiar with installation, use and maintenance of power electrical systems.



The high current flowing through the two SCRs generates heat: the board may reach up to 150 °C at full power. Due to thermal inertia, the board may remain dangerously hot even after current has ceased to flow.

2.2 Board connection and start-up

Figure 2. STEVAL-SCR001V1 circuit schematic (C1, C2, R4, R6 not connected)



All the connections between the evaluation board and the power converter circuit are made through connector J1.

Figure 3. Connection between J1 pin connector pin and power converter circuit

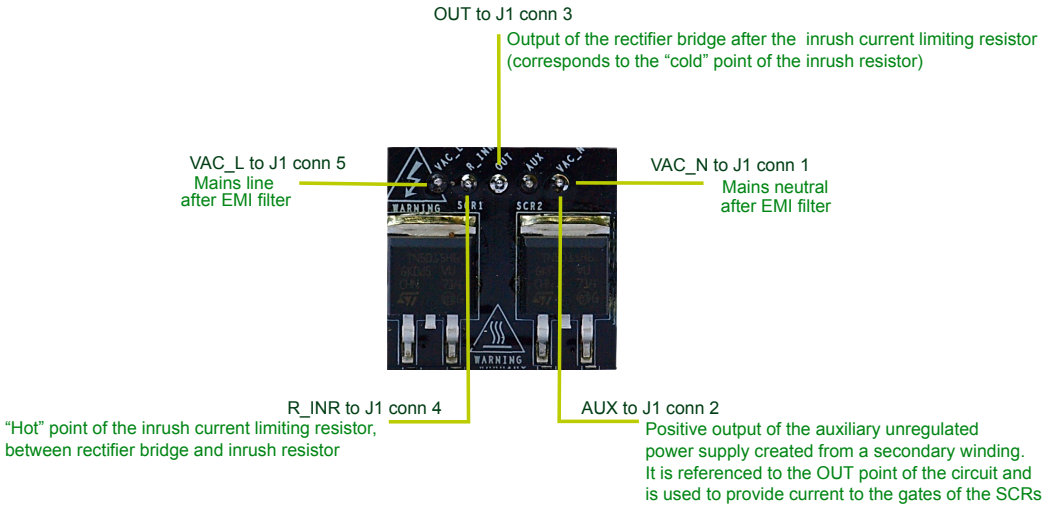


Figure 4. Connection with a boost converter (PFC)

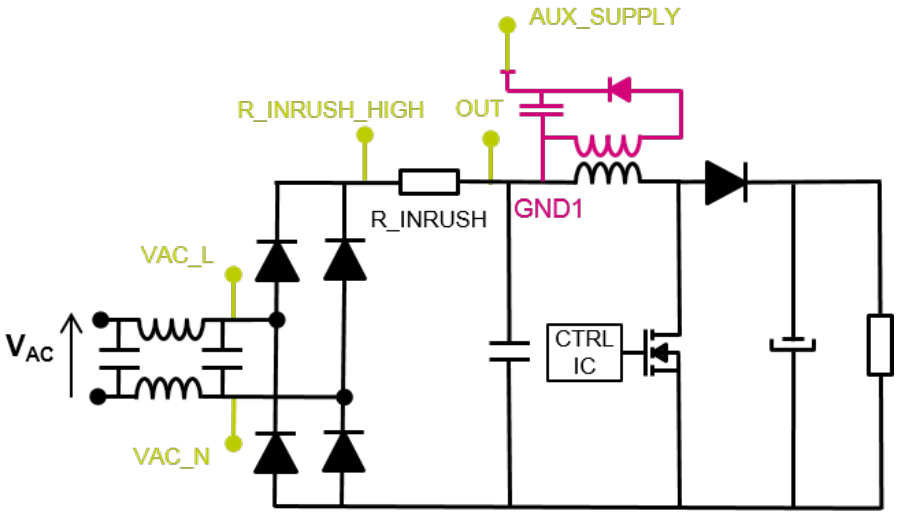
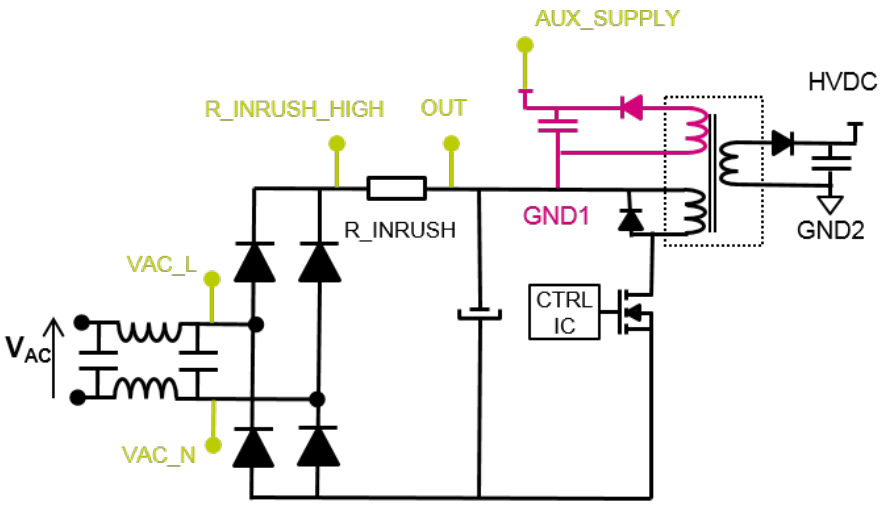


Figure 5. Connection with a Flyback converter



2.3 Adapt the board to different auxiliary voltages

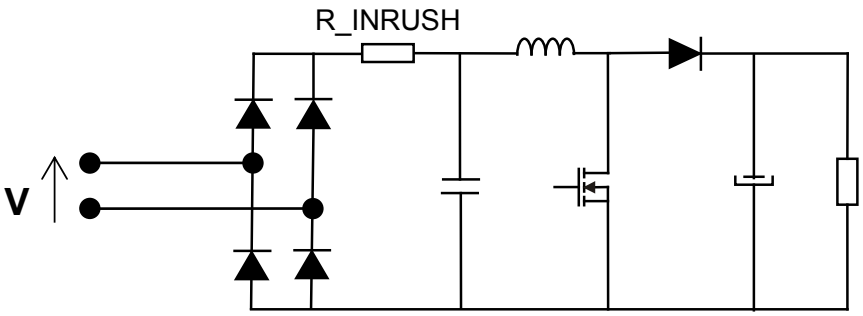
No adjustment is needed on the board when a 12 V auxiliary supply is used. To use a different auxiliary supply voltage, adjust gate resistors R1 and R5 according to the following formula:

$$R_{gate} = \frac{V_{AUX_SUPPLY}}{2 . I_{GT}} = \frac{V_{AUX_SUPPLY}}{0.03} \quad (1)$$

3 Inrush current limiter circuit design

The most common solution to limit inrush current intensity is to use a serial impedance after the rectifier bridge. To reduce power loss, the serial impedance is shorted by a mechanical relay as soon as the bulk capacitor is charged and when the converter starts up.

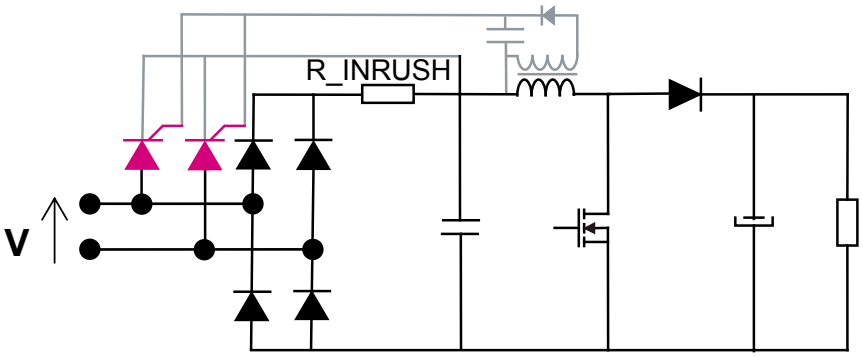
Figure 6. typical schematic of a power converter



The bulkiness of the relay and its slow response has led to an improved architecture based on a half controlled rectifier bridge.

On power up, the two SCRs are opened and the inrush current flows through the diodes of the bridge which is limited by the external inrush power resistor. As soon as the converter turns on, the gates of the two SCRs are supplied by the auxiliary winding of a boost inductor. In nominal operation mode, the two bottom diodes of the bridge and the two SCRs rectify the AC line and the inrush resistor is bypassed.

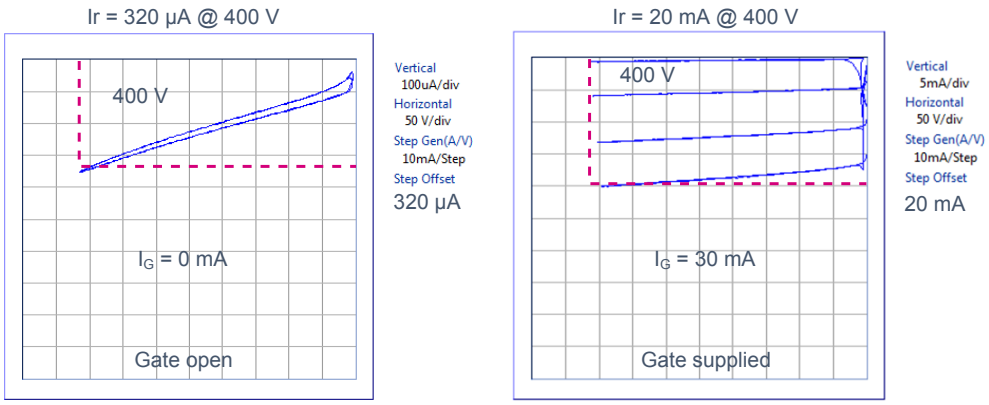
Figure 7. Power converter with half control bridge rectifier



A problem with this topology is the reverse power loss in the two SCRs. During the steady state, at each mains period, one SCR is closed and rectifies the AC line current, while the other is reverse biased and blocked. As both non-conducting and conducting SCRs are supplied with permanent DC gate current, the non-conducting SCR experiences high leakage current which, associated with a high reverse voltage, results in high power loss.

$$P_{rev-loss} = \frac{2 \times \sqrt{2} \times V_{mains(RMS)}}{\pi} \times I_{rev} = 4\ \text{W} \quad (2)$$

Figure 8. example of SCR leakage current (T_j = 125 °C)

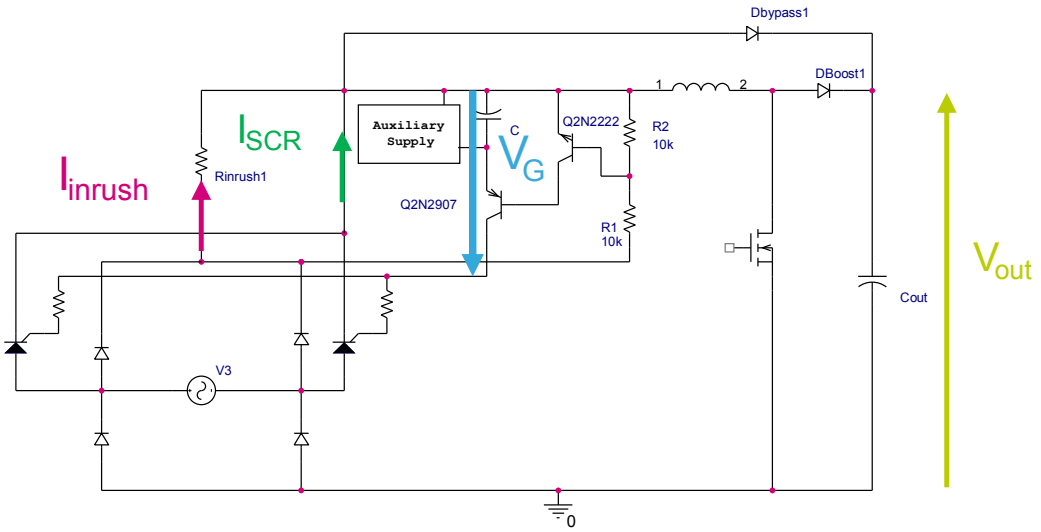


Suppliers tend to use highly sensitive SCRs to avoid this issue. While lower DC gate current involves lower leakage current, immunity to electrical fast transients is drastically reduced due to the relationship between gate sensitivity and static dV/dt.

3.1 Inrush current protection with the STEVAL-SCR001V1

Inrush current protection in the STEVAL-SCR001V1 involves the use of highly immune SCRs, while maintaining power loss close to zero.

Figure 9. power converter with bypass SCR



3.2 Inrush current and SCR activity at start-up

Figure 10. waveform at start-up

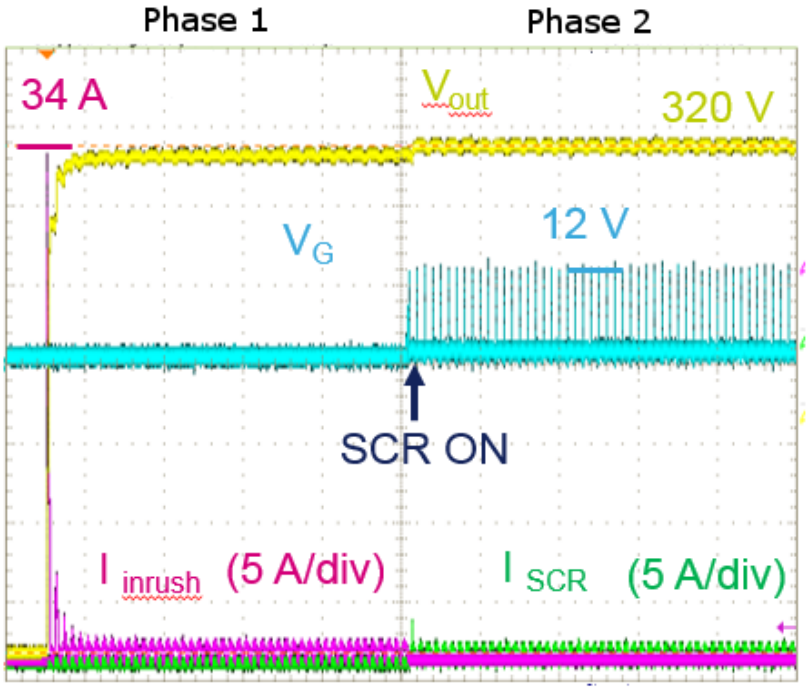


Figure 10. waveform at start-up **Phase 1**: current flows through the bridge rectifier (SCRs are off). Inrush current is limited by R_{inrush}.

$$I_{Inrush} = \frac{U_{mains(peak)}}{R_{inrush}} = 34\ A \quad (3)$$

Figure 10. waveform at start-up **Phase 2**: capacitor has finished charging. Power converter starts up, activating auxiliary supply and providing pulsed current to SCR gate. Once triggered on, the two SCRs bypass the inrush resistor.

3.3 Inrush current and SCR activity in steady state

Figure 11. waveform in steady state

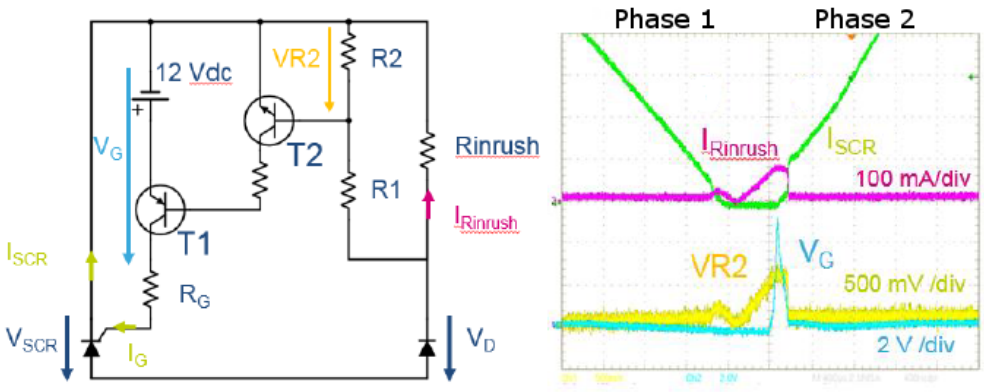


Figure 11. waveform in steady state **Phase 1**: SCR is OFF.

$$VR2 \approx \frac{R2}{R2+R1} R_{Inrush} I_{Inrush} \quad (4)$$

As current flows through R_{inrush}, VR2 rises until it reaches V_{BE} of T2. T2 triggers on, leading to T1 turn-ON. When T1 is ON, the 12 V auxiliary supply provides current I_G to the gate of the SCR and the SCR latches on.

Figure 11. waveform in steady state **Phase 2**: SCR is ON. The current passes through SCR: $V_{SCR} = V_T$

$$VR2 = \frac{R2}{R2+R1}\left(V_T - V_D\right) \text{ < } VBE \quad (5)$$

T2 turns off, which leads to T1 turn off. The auxiliary supply is no longer connected to the gate of the two SCRs, but since the current through the SCR is higher than the latching current (I_L), the SCR remains on until the next zero current crossing.

Thanks to this control circuit, the gate current is pulsed, drastically reducing reverse power losses in comparison to ordinary circuits using permanent DC gate current.

4 SCR junction temperature calculation

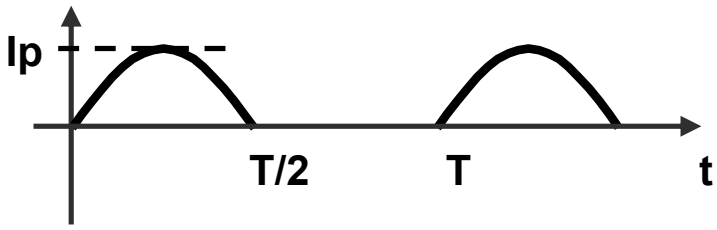
For safe and reliable operation, it is important to keep the junction temperature of the SCR below its maximum junction temperature. The STEVAL-SCR001V1 uses two TN5015H-6G high temperature 50 A SCRs that can operate up to 150°C.

Temperature junction calculation requires ambient temperature, dissipated power and thermal resistance.

4.1 Dissipated power

As current alternates through the two SCRs, the current waveform in the following figure relates to a single SCR.

Figure 12. Current waveform in SCR



The dissipated power corresponding to this half wave can be calculated with the formula(see Application note AN533 on www.st.com).

$$P_{dis} = V_{TO} \times I_{T(av)} + R_D \times {I_{TRMS}}^2 \quad (6)$$

$$I_{T(av)} = \frac{I_P}{\pi}; I_{TRMS} = \frac{I_P}{2} \quad (7)$$

Where V_{TO} and R_D correspond to threshold voltage and dynamic resistance, respectively.

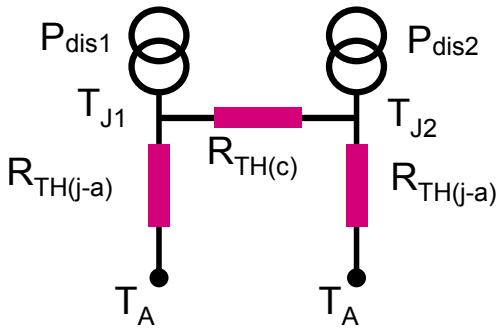
Table 1. Datasheet values for TN5015H-6G

Symbol	Test conditions			Value	Unit
V_{TO}	Threshold voltage	T_j = 150 °C	Max.	0.85	V
R_D	Dynamic resistance	T_j = 150 °C	Max.	9	mΩ

4.2 Thermal resistance

As the two SCRs are near each other on the PCB, dissipated power in one SCR influences the other. This influence is represented by a coupling path between the two SCRs called thermal resistance coupling ($R_{TH(c)}$).

Figure 13. **thermal resistance model of the two SCRs**



$$T_j = T_a + R_{TH}(j-a) \times P_{dis1} + R_{TH}(c) \times P_{dis2} \quad (8)$$

- SCR1 and SCR2 are identical, so:
  - $P_{dis1} = P_{dis2}$
  - $T_{J1} = T_{J2}$
- $R_{TH(j-a)}$ and $R_{TH(c)}$ depend on the layout, copper thickness and copper surface under the tab. For the STEVAL-SCR001V1 (e_{Cu} = 70 µm), the following thermal resistances were measured:
  - $R_{TH(j-a)}$ = 46 °C/W
  - $R_{TH(c)}$ = 11 °C/W

4.3 Example junction temperature for different power and ambient temperatures

Consider a 1000 W load at 230 V_{RMS} and an ambient temperature of 40 °C

$$I_P = \sqrt{2} \times \frac{1000}{230} = 6.1\ A,\ P_{dis} = 1.75\ W \rightarrow T_j = 140\ °C \quad (9)$$

This represents a maximum value calculated from the maximum values for V_{TO} and R_D in the relevant datasheet.

Figure 14. **Thermal camera view of the STEVAL-SCR001V1 at 1000 W and T_A = 25 °C (T_{Jmax} ≈ 102 °C)**

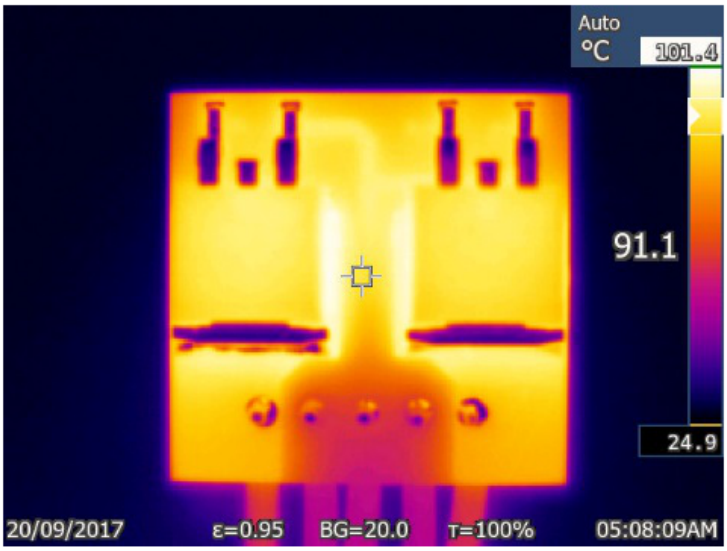


Table 2. Example junction temperatures for different power and ambient temperatures

P @ 230 V (W)	Peak current (A)	Ambient temperature (°C)	Calculated maximum junction temperature
1000	6.15	40	140
800	4.9	40	120
800	4.9	60	140
500	3.07	60	110
500	3.07	90	140

5 STEVAL-SCR001V1 board layout

Figure 15. **STEVAL-SCR001V1 board layout and silk-screen (top side)**

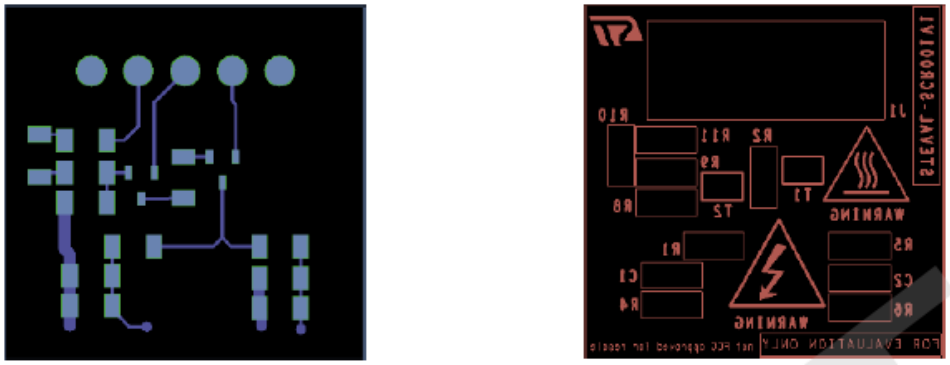


Figure 16. **STEVAL-SCR001V1 board layout and silk-screen (bottom side)**



Table 3. **STEVAL-SCR001V1 bill of materials**

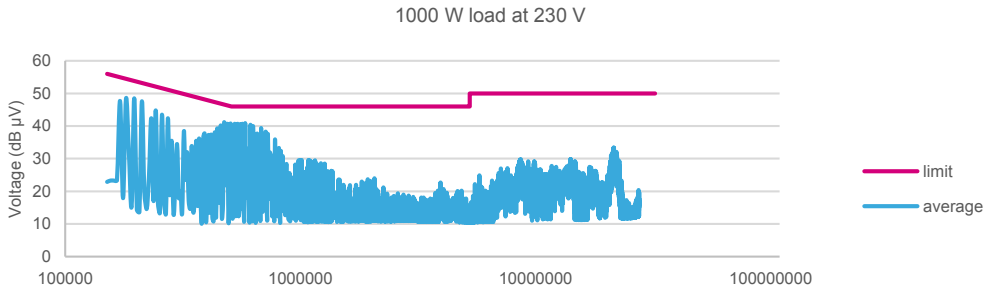
Reference	Part / Value
R1, R5	402 Ω
R2	4.02 KΩ
C1,C2	Not used
R4,R6	Not used
R8	10 KΩ
R9,R10,R11	3.3 KΩ
T1	Transistor PNP 2STR2160
T2	Transistor NPN 2STR1160
J1	Connector
SCR1, SCR2	TN5015H-6G
PCB	PCB FR4 TG180 Copper thickness 70 µm (2 mils)

6 STEVAL-SCR001V1 board performance

6.1 Conducted noise measurements

The EN55014 standard defines the maximum levels of the conducted noise due to mains current switching. The figure below illustrates EMI noise with a 1000 W load measured according to EN55014.

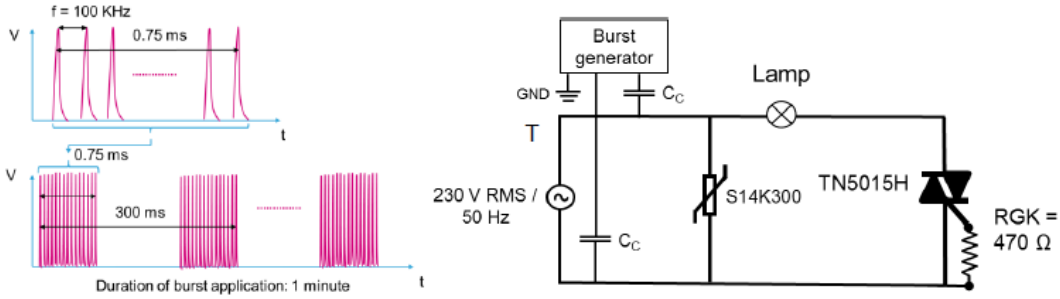
Figure 17. EN55014 standard validation (average measurement)



6.2 Electrical fast transient voltages

The immunity of electrical equipment subjected to fast transient/bursts on supply is evaluated according to the test method described in IEC 61000-4-4 standard.

Figure 18. Test schematic and waveform specification for IEC61000-4-4



The following couplings are tested:

1. between line and ground
2. between neutral and ground

For each coupling, bursts are applied in positive and negative polarity. The results are given in the following table.

Table 4. IEC61000-4-4 minimum level supported by STEVAL-SCR001V1

Coupling	L		N	
Polarities	+	-	+	-
TN5015H	2.5 KV	2.5 KV	2.5 kV	2.5 kV

6.3 Surge voltages

Lightning surge is emulated by a IEC61000-4-5 test.

The following configurations are tested:

1. positive surge with 90° phase (config a)
2. negative surge with 90° phase (config b)

Figure 19. test schematic for IEC61000-4-5 (config a)

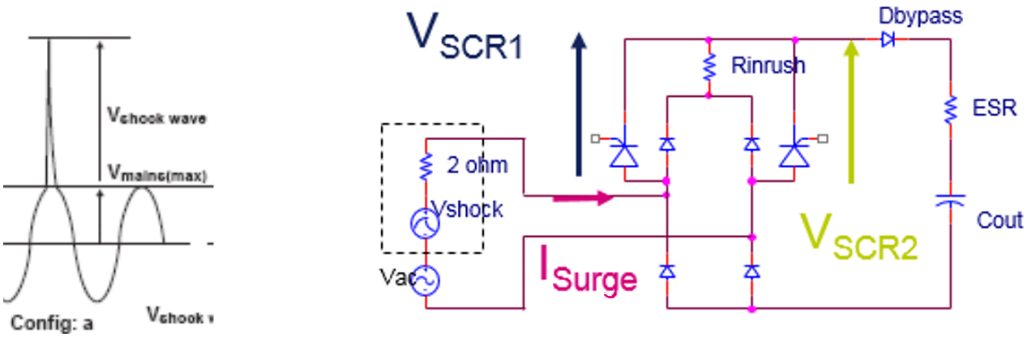


Figure 20. Resulting waveform during 2 KV IEC61000-4-5 test (config a)

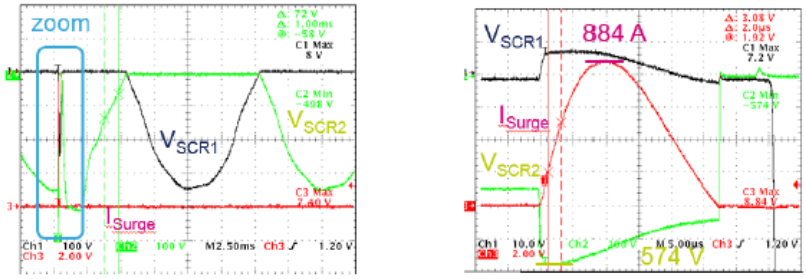


Figure 21. test schematic for IEC61000-4-5 (config b)

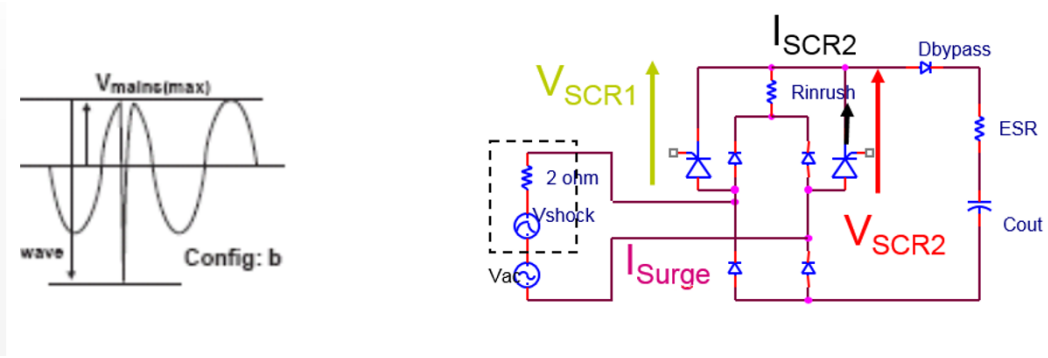
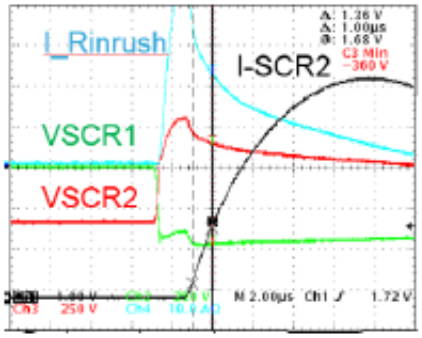


Figure 22. **Resulting waveform during 2 KV IEC61000-4-5 test (config b)**

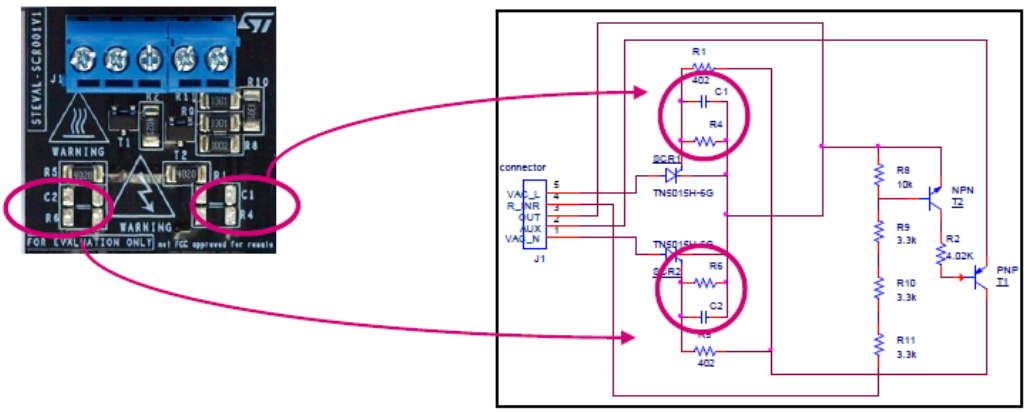


6.4 Performance improvements

For applications requiring very high immunity to fast transient voltages, it may be helpful to implement a gate filter with a capacitor and/or a resistor between the gate and cathode(see Application note AN4030 on www.st.com). The footprint for these components is available on the PCB (see Figure 23. Footprint on STEVAL-SCR001V1 to accommodate a gate filter for higher dV/dt immunity).

C_{GK} and R_{GK} should be adjusted experimentally, starting, for example, from C_{GK} = 10 nF and R_{GK} = 1 KΩ. A lower resistance and a higher capacitance will help bypass more parasitic current. If C_{GK} is used, R_{GK} must bust be included to discharge the capacitor.

Figure 23. **Footprint on STEVAL-SCR001V1 to accommodate a gate filter for higher dV/dt immunity**



Revision history

Table 5. **Document revision history**

Date	Version	Changes
01-Dec-2017	1	Initial release.
13-Mar-2018	2	Updated Figure 3. Connection between J1 pin connector pin and power converter circuit, Figure 4. Connection with a boost converter (PFC) and Figure 5. Connection with a Flyback converter.

Contents

1 **STEVAL-SCR001V1 evaluation board for inrush current protection 2**

2 **Getting started. 3**

2.1 Safety precautions 3

2.2 Board connection and start-up 3

2.3 Adapt the board to different auxiliary voltages 4

3 **Inrush current limiter circuit design 6**

3.1 Inrush current protection with the STEVAL-SCR001V1. 7

3.2 Inrush current and SCR activity at start-up 7

3.3 Inrush current and SCR activity in steady state 8

4 **SCR junction temperature calculation 10**

4.1 Dissipated power 10

4.2 Thermal resistance 10

4.3 Example junction temperature for different power and ambient temperatures 11

5 **STEVAL-SCR001V1 board layout 13**

6 **STEVAL-SCR001V1 board performance 14**

6.1 Conducted noise measurements 14

6.2 Electrical fast transient voltages. 14

6.3 Surge voltages 14

6.4 Performance improvements 16

Revision history 17

List of figures

Figure 1. STEVAL-SCR001V1 evaluation board (top and bottom view) . . . 1
Figure 2. STEVAL-SCR001V1 circuit schematic (C1, C2, R4, R6 not connected) . . . 3
Figure 3. Connection between J1 pin connector pin and power converter circuit . . . 4
Figure 4. Connection with a boost converter (PFC) . . . 4
Figure 5. Connection with a Flyback converter . . . 4
Figure 6. typical schematic of a power converter . . . 6
Figure 7. Power converter with half control bridge rectifier . . . 6
Figure 8. example of SCR leakage current (T_j = 125 °C) . . . 7
Figure 9. power converter with bypass SCR . . . 7
Figure 10. waveform at start-up . . . 8
Figure 11. waveform in steady state . . . 8
Figure 12. Current waveform in SCR . . . 10
Figure 13. thermal resistance model of the two SCRs . . . 11
Figure 14. Thermal camera view of the STEVAL-SCR001V1 at 1000 W and T_A = 25 °C (T_{Jmax} ≈ 102 °C) . . . 11
Figure 15. STEVAL-SCR001V1 board layout and silk-screen (top side) . . . 13
Figure 16. STEVAL-SCR001V1 board layout and silk-screen (bottom side) . . . 13
Figure 17. EN55014 standard validation (average measurement) . . . 14
Figure 18. Test schematic and waveform specification for IEC61000-4-4 . . . 14
Figure 19. test schematic for IEC61000-4-5 (config a) . . . 15
Figure 20. Resulting waveform during 2 KV IEC61000-4-5 test (config a) . . . 15
Figure 21. test schematic for IEC61000-4-5 (config b) . . . 15
Figure 22. Resulting waveform during 2 KV IEC61000-4-5 test (config b) . . . 16
Figure 23. Footprint on STEVAL-SCR001V1 to accommodate a gate filter for higher dV/dt immunity . . . 16

List of tables

Table 1. Datasheet values for TN5015H-6G. 10
Table 2. Example junction temperatures for different power and ambient temperatures 12
Table 3. STEVAL-SCR001V1 bill of materials. 13
Table 4. IEC61000-4-4 minimum level supported by STEVAL-SCR001V1 14
Table 5. Document revision history 17

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