HMC1096LP3E

v02.0217

GaAs pHEMT MMIC X2 ACTIVE FREQUENCY MULTIPLIER, 3.8 - 5.6 GHz OUTPUT

Typical Applications

The HMC1096LP3E is suitable for:

- Point-to-Point & VSAT Radios
- Test Instrumentation
- Military & Space

Features

High Output Power: 12 dBm

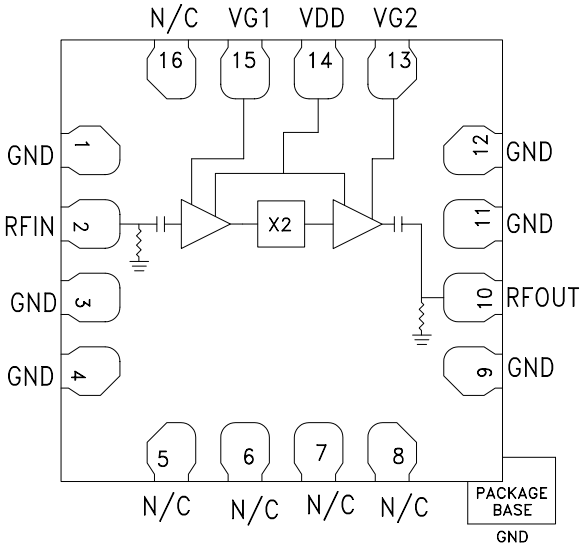
Low Input Power Drive: -2 to +5 dBm

Fo, 3 Fo Isolation: +22 dBc

Single Supply: +5V @100 mA

16 Lead 3 x 3 mm SMT Package

Functional Diagram



General Description

The HMC1096LP3E is a x2 active broadband frequency multiplier utilizing GaAs pHEMT technology in a leadless RoHS compliant Low Stress Injection Molded Plastic SMT package. When driven by a 0 dBm signal, the multiplier provides +12 dBm typical output power from 3.8 to 5.6 GHz. The Fo and 3 Fo isolations are 22 dBc with respect to the output signal level. This frequency multiplier features DC blocked I/Os, and is ideal for use in LO multiplier chains for Point-to-Point & VSAT radios yielding reduced parts count vs. traditional approaches. The HMC1096LP3E is compatible with surface mount manufacturing techniques.

Electrical Specifications, T_A = +25° C, VDD = +5 V, 0 dBm Drive Level [1]

Parameter	Min.	Typ.	Max.	Units
Frequency Range, Input	1.9		2.8	GHz
Frequency Range, Output	3.8		5.6	GHz
Output Power	9	12		dBm
Fo, 3 Fo Isolation (with respect to output level)		22		dBc
Phase Noise (@ 10 KHz Offset)		-142		dBc / Hz
Input Return Loss		12		dB
Output Return Loss		8		dB
Supply Current [1]		100		mA

[1] External resistors R1 and R2 set the typical bias level for VG1 to 1.22 Vdc, 1.4mA and VG2 to 1.04 Vdc, 1.2 mA to achieve drain current of 100mA.

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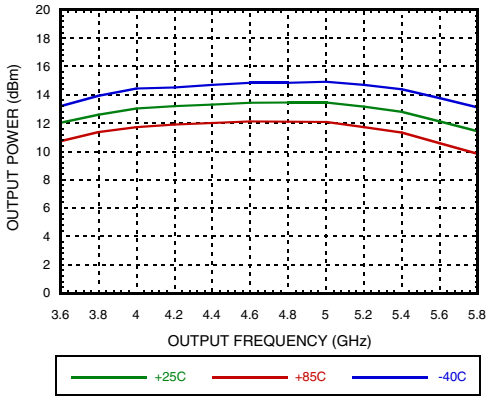
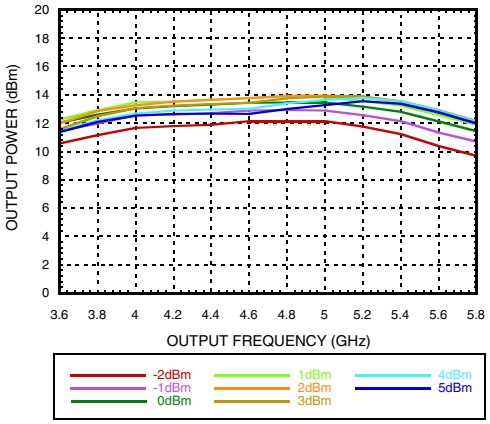
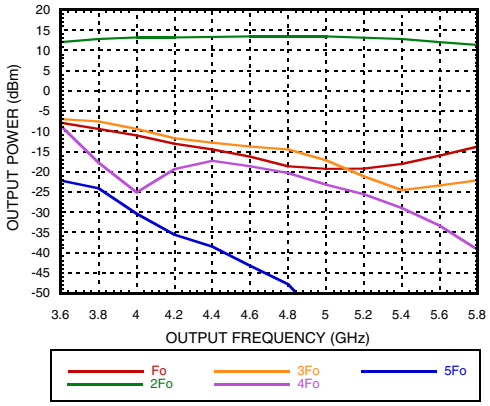
Output Power vs. Temperature @ 0 dBm Drive Level



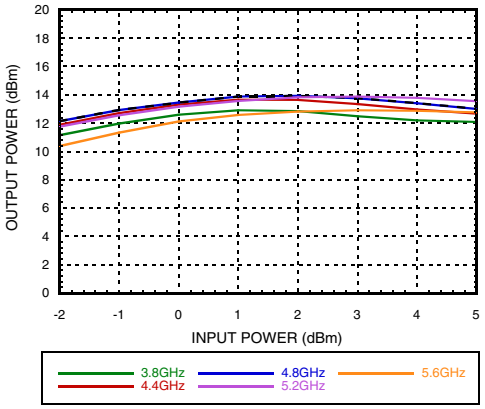
Output Power vs. Drive Level



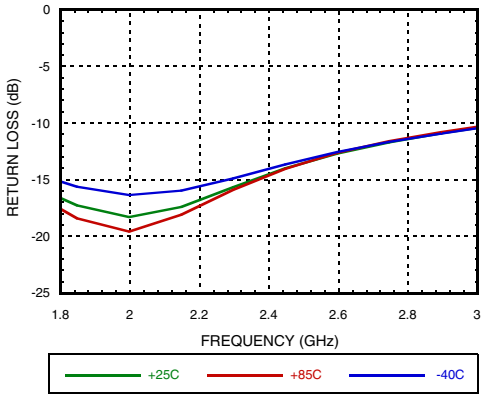
Isolation @ 0 dBm Drive Level



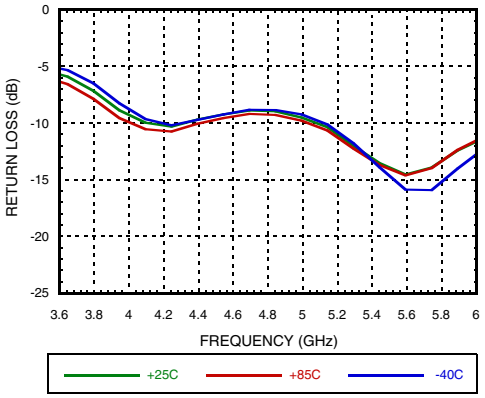
Output Power vs. Input Power



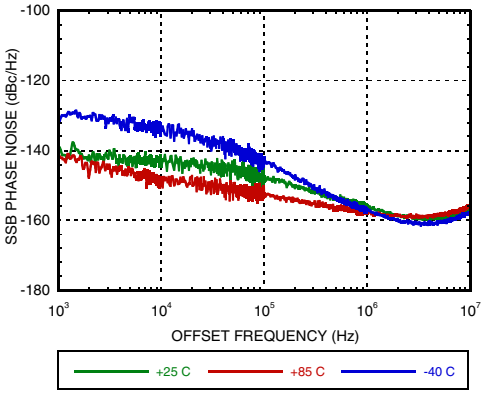
Input Return Loss vs. Temperature



Output Return Loss vs. Temperature



Phase Noise vs. Temperature @ 4.7 GHz



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Absolute Maximum Ratings

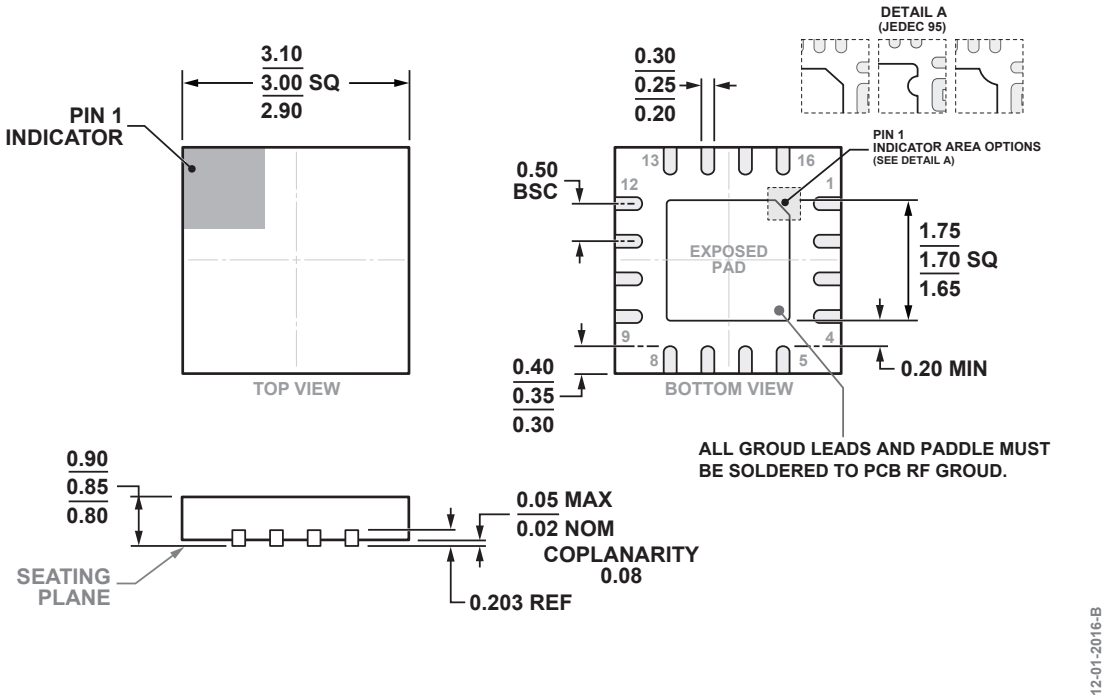
RF Input Power	+5 dBm
Supply Voltage (VDD)	+6 V
VG1, VG2 (Bias Input)	+2 V
Channel Temperature	175 °C
Continuous Pdiss (T= 85 °C) (derate 13.3 / mW / °C above 85 °C)	1.2 W
Thermal Resistance (channel to package bottom)	75 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 0, passed 150 V

Typical Supply Current vs. VDD

VDD (Vdc)	IDD (mA)
5.0	100

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing

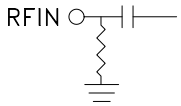
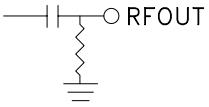
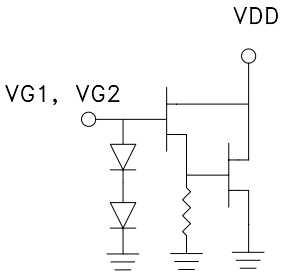


Package Information

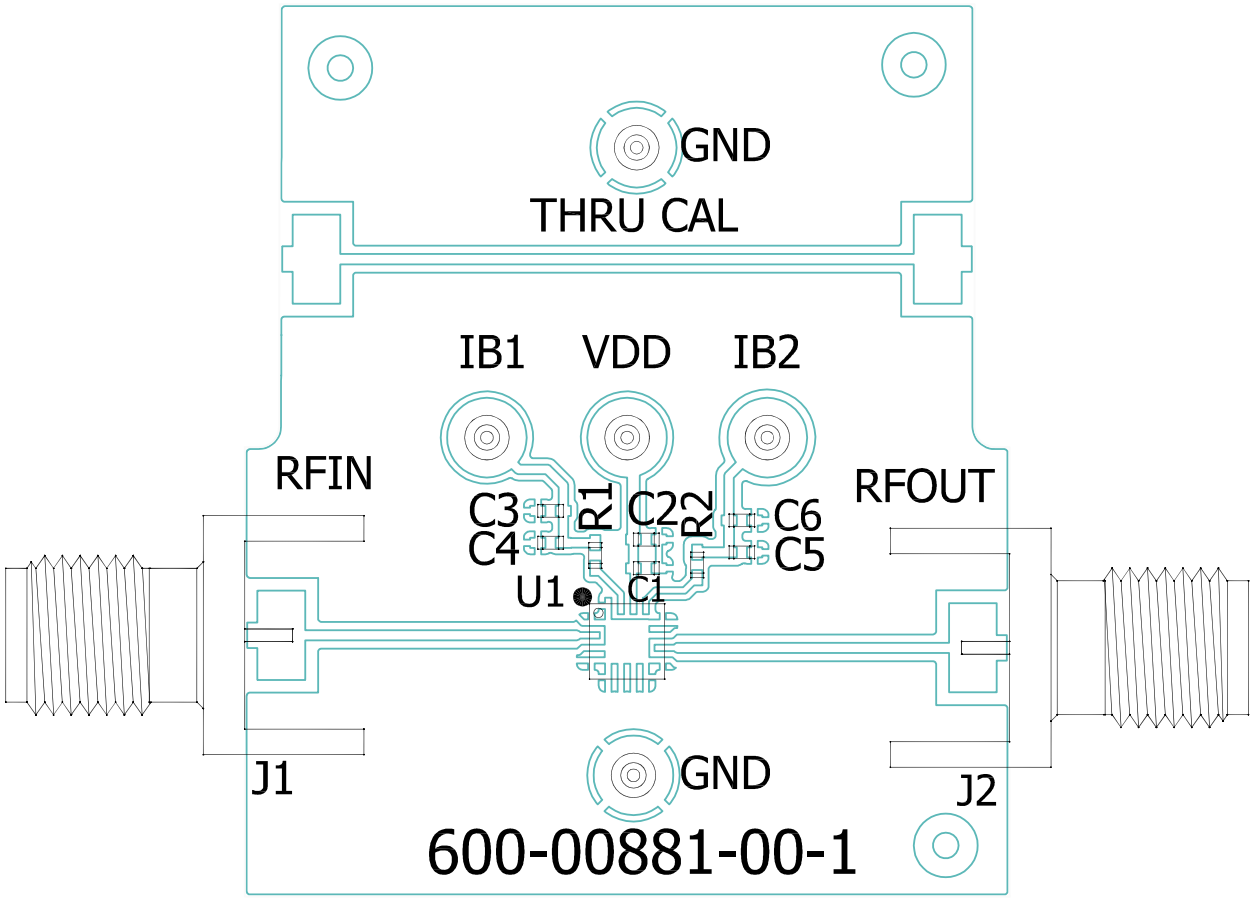
Part Number	Package Body Material	Lead Finish	MSL Rating [2]	Package Marking [1]
HMC1096LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1	H1096 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

Pin Descriptions

Pin Number	Function	Description	Pin Schematic
1, 3, 4, 9, 11, 12	GND	Package Bottom must be connected to RF/DC ground.	
5, 6, 7, 8, 16	N/C	These pins are not connected internally. However, this product was specified with these pins connected to RF/DC ground.	
2	RFIN	This pin is dc-coupled internally and matched to 50 Ohms. The resistor is used for ESD protection.	
10	RFOUT	This pin is dc-coupled internally and matched to 50 Ohms. The resistor is used for ESD protection.	
13, 15	VG2, VG1	Gate Voltage for first and second stage LO amplifier. Recommended DC voltage is +5 V at J5/J7 with bias resistors R1 and R2 applied. Typical. Refer to application circuit for required external components.	
14	VDD	Supply voltage for first and second stage LO amplifier. Recommended DC voltage is +5 V with external bypass capacitors of 100 pF and 10 nF applied. Refer to application circuit for required external components.	

Evaluation PCB



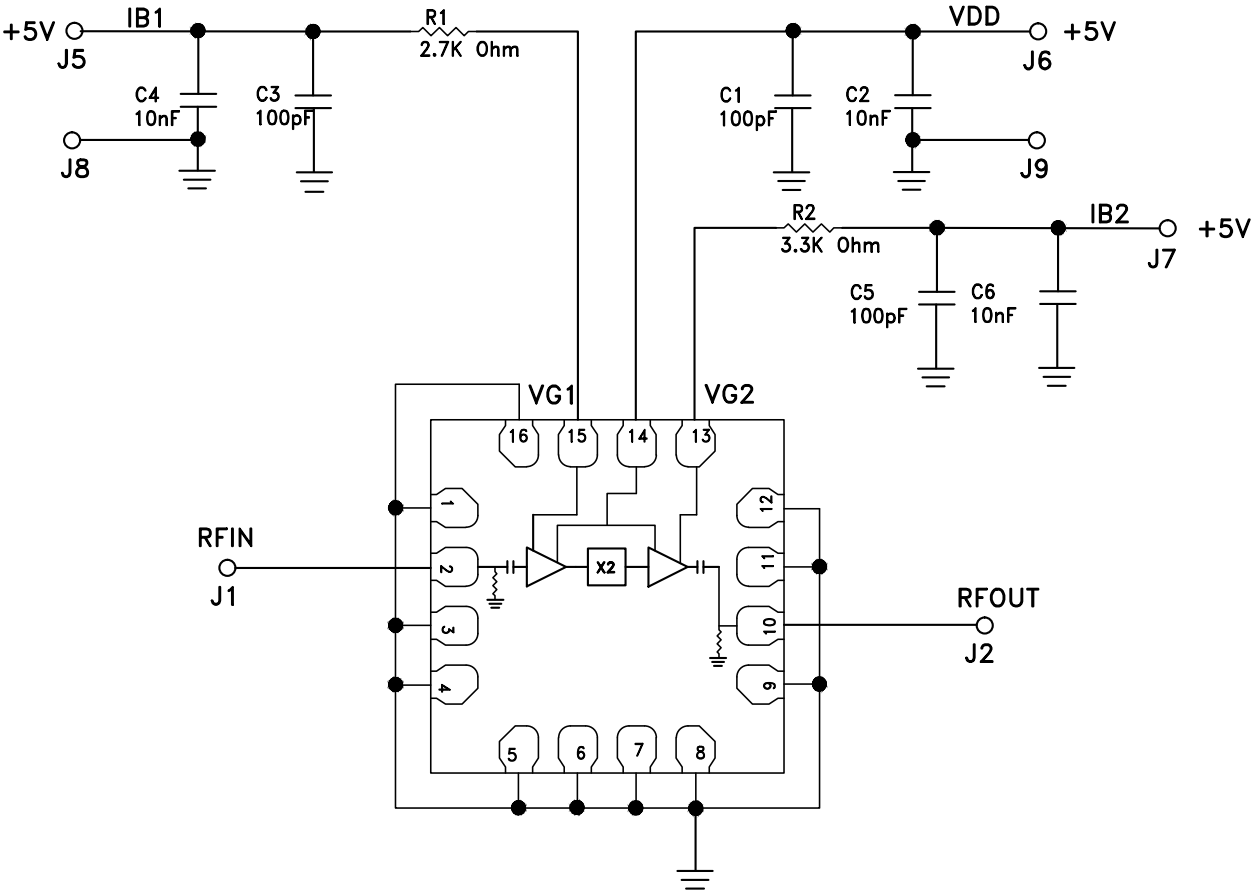
List of Materials for Evaluation PCB EV1HMC1096LP3[1]

Item	Description
J1, J2	PCB Mount SMA RF Connector
J5 - J9	DC PIN
C1, C3, C5	100 pF Capacitor, 0402 Pkg.
C2, C4, C6	10000 pF Capacitor, 0402 Pkg.
R1	2.70K Ohm Resistor, 0402 Pkg.
R2	3.30K Ohm Resistor, 0402 Pkg.
U1	HMC1096LP3E
PCB [1]	600-00881-00 Evaluation Board

[1] Circuit Board Material: Rogers 4350 or Arlon 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Application Circuit



Notes: