AN-2081 LMH6517EVAL-R1 Evaluation Board

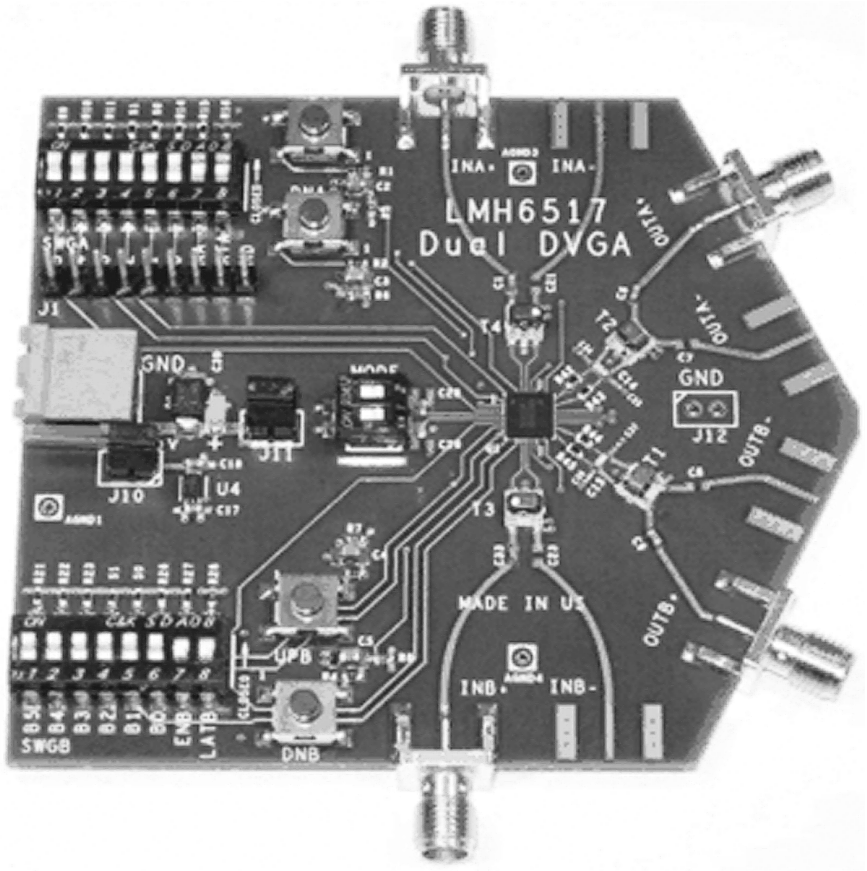

Figure 1. LMH6517EVAL-R1 Evaluation Board

1 General Description

The LMH6517EVAL-R1 evaluation board is designed to aid in the characterization of Texas Instruments' High Speed LMH6517 Digital Controlled Variable Gain Amplifier (DVGA).

The evaluation board is used as a guide for high frequency layout and as a tool to aid in device testing and characterization.

2 Basic Operation

The LMH6517 DVGA has differential inputs and differential outputs. To aid evaluation with 50Ω, single ended test equipment the LMH6517EVAL-R1 evaluation board is shipped with transformers on both the input and output signal paths. The single ended signal path uses the IN+ and OUT+ marked connectors. The IN− and OUT− signal paths are grounded and the SMA connectors are not installed.

The input and output pins of the LMH6517 will self bias to approximately mid supply (2.5V). The LMH6517EVAL-R1 board has been designed with AC coupling on both input and output signal paths to protect test equipment and to ensure proper operation of the LMH6517 DVGA. Any modifications to the board should preserve the operating points of the DVGA and protect sensitive test equipment.

Transformers T1– T4 can provide both impedance matching as well as single ended to differential conversion. The board is shipped with 2:1 turns ratio (4:1 impedance ratio) transformers that will match 50Ω equipment with the 200Ω input impedance of the LMH6517 DVGA . Do not connect the transformer secondary winding directly to ground since this will short the DVGA input voltage to ground.

For differential operation the board must be modified by hand. The copper on the grounded input must be cut as illustrated in Figure 7. and additional SMA connectors need to be soldered to the board to complete the IN- and OUT- signal paths. The LMH6517EVAL-R1 Evaluation board is 0.63” thick and uses edge mounted SMA connectors. The board is built with Emerson part #142–0701–806 end launch, nickel plated SMA connectors.

The LMH6517EVAL-R1 evaluation board comes built with 1:1 balun transformers and 10 Ohm series output resistors (R42, R43, R44 and R45). A 4.7pF load capacitor is placed between the resistors and the transformer (C14 and C15). The 10 Ohm resisters and 4.7pF capacitor form a snubber circuit that reduces high frequency peaking and enhances stability. The combination of the snubber circuit and the 1:1 balun gives very good power gain and very good OIP3 performance when driving 50Ω test equipment. The output impedance of the LMH6517 amplifier is very low (<2Ω @ 50MHz). Many load conditions can be achieved by changing out the components on the evaluation board. Not all load conditions will require a snubber circuit, but it should be included in the final circuit design unless sufficient testing has shown it to be unnecessary.

The capacitors C5, C7, C8 and C9 isolate the output transformer from the output SMA connectors and are not required if the transformer provides DC blocking. The spaces marked C34, C35, C36 and C37 are left empty by the factory. These positions are included to provide the flexibility to add extra components. Capacitors can be added to create a low pass filter. Resistors could be placed in these locations to create different load conditions for the amplifier.

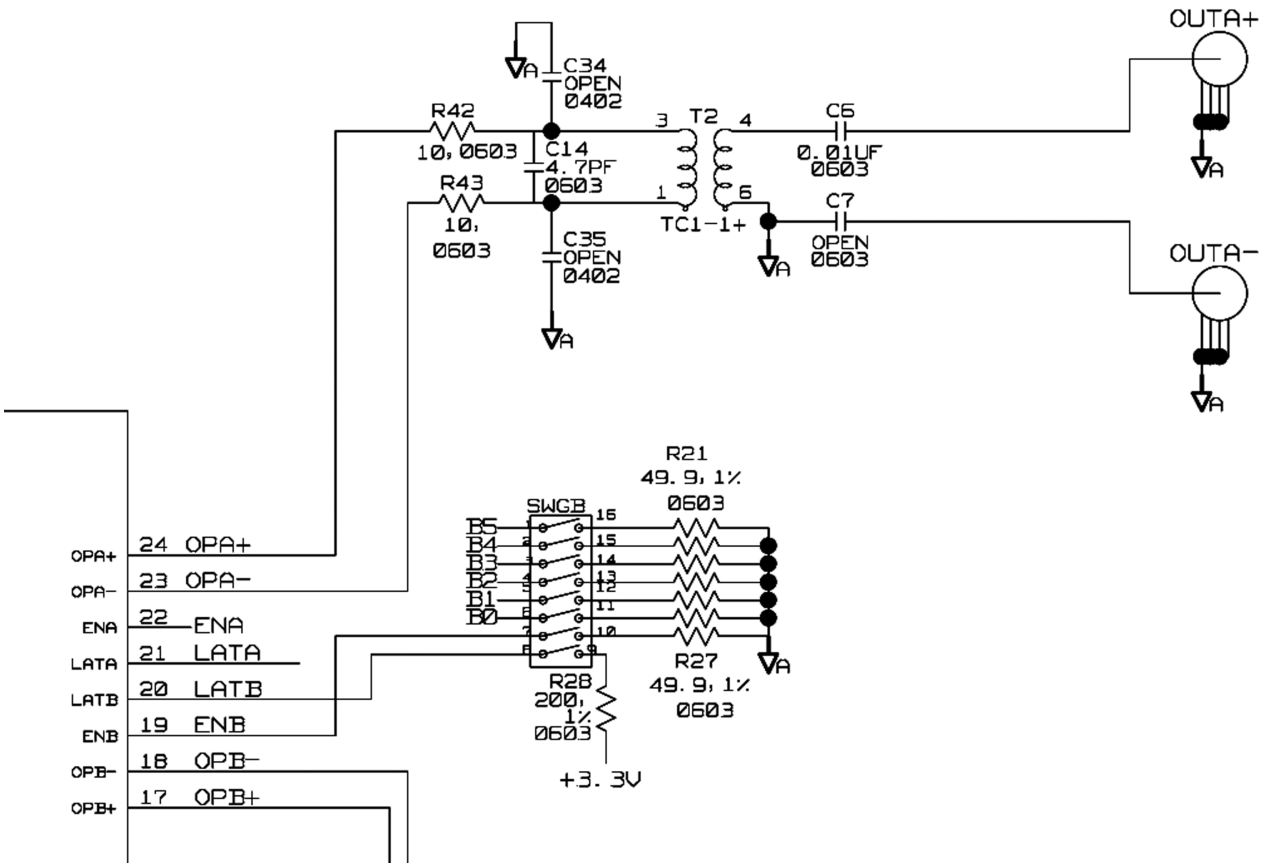

Figure 2. Output Schematic

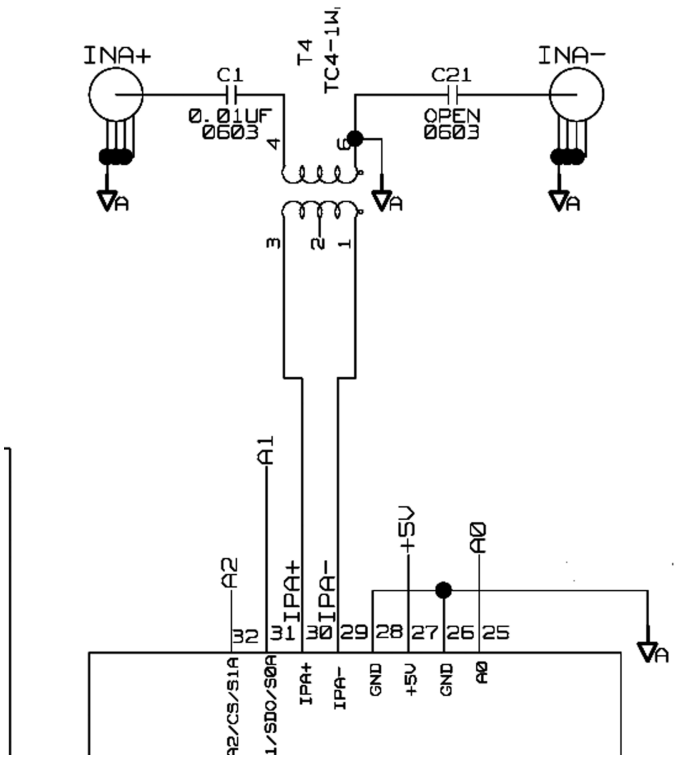

Figure 3. Input Schematic

The board was designed to be very flexible for many different configurations. Zoomed in portions of the input and output schematics are shown above in Figure 2 and Figure 3. The evaluation board, as shipped, has been optimized for ease of use with single ended 50 Ohm test equipment. This configuration may not emulate the most common application circuits. The signal path schematic is shown in Figure 8 and the full schematic in . PDF format is available upon request.

3 Using with Different Sources or Loads

The LMH6517EVAL-R1 evaluation board supports differential operation on both inputs and outputs. However they will require additional components and some board rework. For driving the evaluation board from a differential source, symmetrical signal paths are provided. Both input and output paths support fully differential test equipment.

To drive the LMH6517EVAL-R1 evaluation board from a differential source, the transformers T3 and T4 must be removed. The diagrams in Figure 6 and Figure 7 show the required connections for differential inputs. DC coupled operation is possible using differential signals. For DC coupled operation, make sure that the test equipment can provide the 2.5 V offset voltage required.

For differential output signals remove transformers T1 and T2. Wire jumpers or zero Ohm resistors must be added to complete the signal path across the transformer pads similar to the changes required for differential inputs.

4 Other Board Configurations

For other applications or experiments there are many options for changing the output circuit to simulate different circuit conditions. One option is to use a 2:1 transformer to simulate high impedance loads. In this case one would use 100 Ohm resistors for R42, R43, R44 and R45. This would present a load of 200 Ohms to the amplifier output. Many common filter circuits have 200 Ohm input impedance. Other combinations can also be used to simulate different load conditions. With a high impedance load the capacitors C14 and C15 should be decreased to 1pF to avoid losing bandwidth.

Near the power connector are a number of 0.1” pitch headers. The header labeled J1 provides off board access to the LMH6517 digital control pins. The J1 pins and functions are described below. The jack labeled J10 is normally loaded with a shorting jumper, it provides power to a 3.3V power supply used to provide 3.3V logic signals to the digital pins. The jack labeled J11 is also loaded with a shorting block and it provides the 5V power to the LMH6517. By removing the short on this jack and replacing it with an ammeter the current drawn by the DVGA can be measured. The jack labeled J12 is a ground connector and is normally left empty.

5 Additional Design Tools

The RD-179: High-IF Sub-sampling Receiver Subsystem board (SP16160CH1RB) is also available. This reference design includes the ADC16DV160 ADC, the LMH6517 DVGA, and the LMK04031B precision clock conditioner. Power regulation, filters and controlled impedance board layout are all provided in this reference design. Please visit the TI website, www.ti.com for further details.

6 Gain Control

The LMH6517 DVGA has three control modes including, parallel mode, serial (SPI compatible) mode and pulse mode. Parallel and pulse modes are fully supported on the board. Serial mode control requires the use of a PC and the SPUSI2 USB to SPI interface board (available separately) or an external signal source like a logic analyzer or a microcontroller. Each of the control modes is detailed fully below.

Mode SW1 (MOD1)	Mode SW2 (MOD0)	Gain Setting
Off	Off	Parallel
Off	On	Serial
On	Off	Pulse

7 Parallel Mode

For ease of use, dip switches are provided to set the LMH6517 gain in parallel mode. This mode is the easiest to use for basic measurements. To set the board in parallel mode, Dip-switch SW 1 which is labeled MODE must be set such that the top switch is in the OFF position and the bottom switch is in the OFF position (the top of the board is the Channel A portion). To move the MODE switches to the OFF position, slide them toward the output SMA connectors.

In Parallel mode, the switch banks are used to set the gain of the DVGA. When using the DIP switches to change gain in parallel mode ensure that the switch labeled LATA or LATB is in the ON position. With the latch switch in the ON state the device is in transparent mode and any change in the dip switches is immediately reflected in the device gain. Moving the latch pin switch to the OFF position holds the last gain setting and ignores changes in the gain control switches. When the latch switch is in the OFF position the dip switches that control the gain can be configured as desired and then implemented by momentarily switching the LATA or LATB switch. For detailed instructions on the pin functions see *Low Power, Low Noise, IF and Baseband, Dual 16 bit ADC Driver With Digitally Controlled Gain Data Sheet* (SNOSB19)

In parallel mode, the DIP switch banks SWGA and SWGB are used to set the gain of the DVGA. The gain bits are binary weighted with the LSB representing a 0.5dB gain step and the MSB representing a 16dB step. The steps increase the gain when the switch is in the ON position. For example, switching B5 from OFF to ON will increase the gain by 16dB. Between the Gain control bits and the Latch switch is an enable (ENA or ENB) switch. Setting this switch to the OFF position Enables the respective DVGA channel.

8 Pulse Mode

The DVGA is also very easy to control in Pulse mode. For system implementations Pulse mode requires fewer digital control lines than parallel mode at the expense of gain control speed. To use Pulse Mode the Mode switches should be set such that MODE 1 is in the ON position and MODE2 is in the OFF position. Gain changes are accomplished by using the UP and DN buttons. There are separate buttons for the A channel and the B channel. Gain will be indicated on the LED displays.

The dip switches that are used to control gain in parallel mode have different functions in Pulse mode. SWA, which controls the A channel should be set with the A4, A3, ENA and LATA positions in the OFF setting. The positions marked A5 and A0 need to be in the ON position. The positions marked A2 and A1 are used to set the DVGA gain step size.

Table 1. SWG Switch Settings for Pulse Mode

SWGA	A5	A4	A3	A2	A1	A0	ENBA	LATA
SWGB	B5	B4	B3	B2	B1	B0	ENBB	LATB
Position	ON	OFF	OFF	A/R	A/R	ON	OFF	OFF

The switch marked SWB controls the B channel and should be configured as follows: positions marked B4, B3, ENB and LATB set to OFF, the positions marked B5 and B0 need to be in the ON position. The positions marked B2 and B1 set the channel B gain step size. See the product data sheet for step size options. Note that if the switch marked B5 on SWGB is in the Off position the entire amplifier will be in an undefined state and will not operate correctly.

The push button switches located between the DVGA and the Parallel DIP switch banks are for use in pulse mode. The UPA and UPB buttons increment the gain up one step while the DNA and DNB buttons decrement the gain by one step. The gain step sizes are set by the DIP switches labeled S1 and S0 on the parallel control DIP switches. Each channel can have a different gain step size.

Table 2. Pulse Mode Gain Step Sizes
S1 and S0 are Located in SWGA and SWGB

S1	S0	Gain Step Size
On	On	0.5dB
On	Off	1dB
Off	On	2dB
Off	Off	6dB

9 Serial Mode

Serial mode is the most complex control mode and is considerably slower than parallel mode, but it is very flexible and requires fewer digital control lines. To use Serial Mode the Mode switches should be set such that MODE 1 is in the OFF position and MODE2 is in the ON position. Note that if the switch marked B5 on SWGB is in the Off position the entire amplifier will be in an undefined state and will not operate correctly.

Serial mode requires external logic, either from a microcontroller or logic analyzer. A 0.1” header strip is located near SWGA (J1). This strip can be used to connect a microcontroller or logic analyzer to the serial control pins, the pulse control pins and the channel A parallel control pins. The header pin functions are shown in the table below. Please refer to the product data sheet for the full description of these pin functions.

Please note that the SWGA dip switches will impact the on-board impedance for the J1 header pins. If the SWGA dip switches are set to the OFF position, there is no on-board termination for the J1 header pins and they will appear as high impedance to the logic analyzer. Make sure that this does not result in logic signals that are beyond the absolute maximum rating for the LMH6517. When the SWGA dip switches are in the ON position there are 50Ω resistors to ground connected the header pins in parallel with the LMH6517 logic pins. Some digital sources are unable to drive this load condition. If it seems that the LMH6517 is not responding to digital control signals this could be one cause.

To aid in the evaluation of SPI controlled devices, TI manufactures the SPUSI2 board and provides the TinyI2CSPI software to control it. The software and the SPUSI2 evaluation board kit can be ordered from the TI website. The software is Windows® compatible. The first step for using the board in serial mode is to place the MODE switches in the proper configuration. The MODE1 switch will be in the OFF position and the MODE2 switch will be in the ON position. Directions for installing the USB control software and evaluation board drivers are in the user's guide available on the TI website.

Once the SPUSI2 board drivers and TinyI2CSPI software are installed, the appropriate pins on the LMH6517 board need to be connected to the SPUSI2 board. Soldering jumpers is one easy method. Connect the CLK, SDI and CS pins as well as a ground wire to the SPUSI2 board. The board software should be set to SPI mode and the CS adn CKPOL columns should be set to 1. The CKPHA column needs to be set to 1and the number of bits should be set to 16. Check to the LMH6517 data sheet for details on the data to be sent to the DVGA registers. Some simple SPI commands, as well as the proper software settings are shown below in Figure 9.

Table 3. Header Jack Pin Assignments (J1)

Header Pin	LMH6517 Pin #	Parallel Function	Serial Function	Pulse Function
J1–1	3	Address bit 5	N/A	N/A
J1–2	2	Address bit 4	CLK	Up A
J1–3	1	Address bit 3	Serial Data In	Down A
J1–4	32	Address bit 2	Chip Select	Step Size MSB
J1–5	31	Address bit 1	Serial Data Out	Step Size LSB
J1–6	25	Address bit 0	N/A	N/A
J1–7	22	Enable A	Enable A	Enable A
J1–8	21	Latch A	N/A	N/A
J1–9	N/A	Ground	Ground	Ground

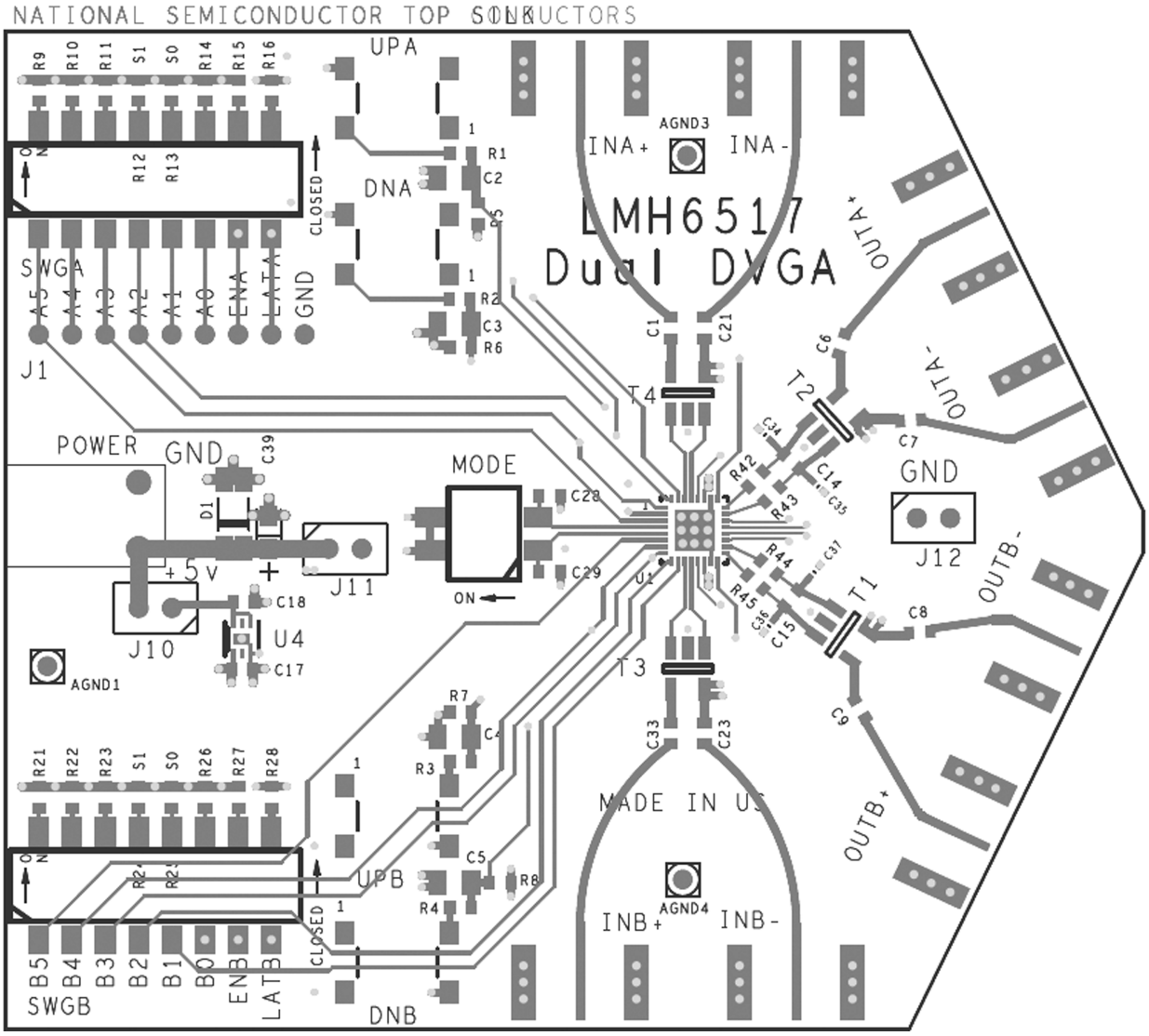

Figure 4. Evaluation Board Top Layer

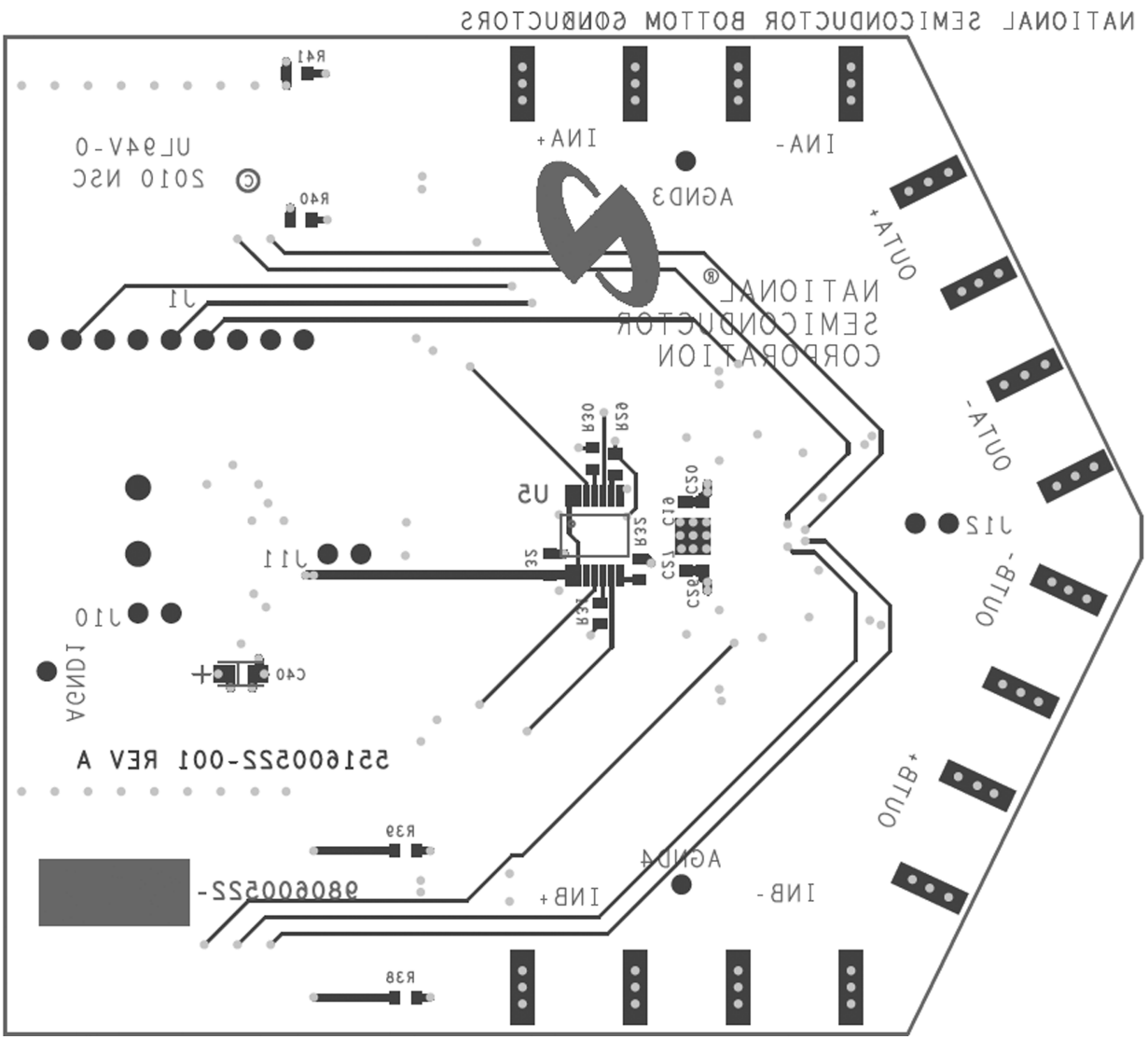

Figure 5. Evaluation Board Bottom Layer

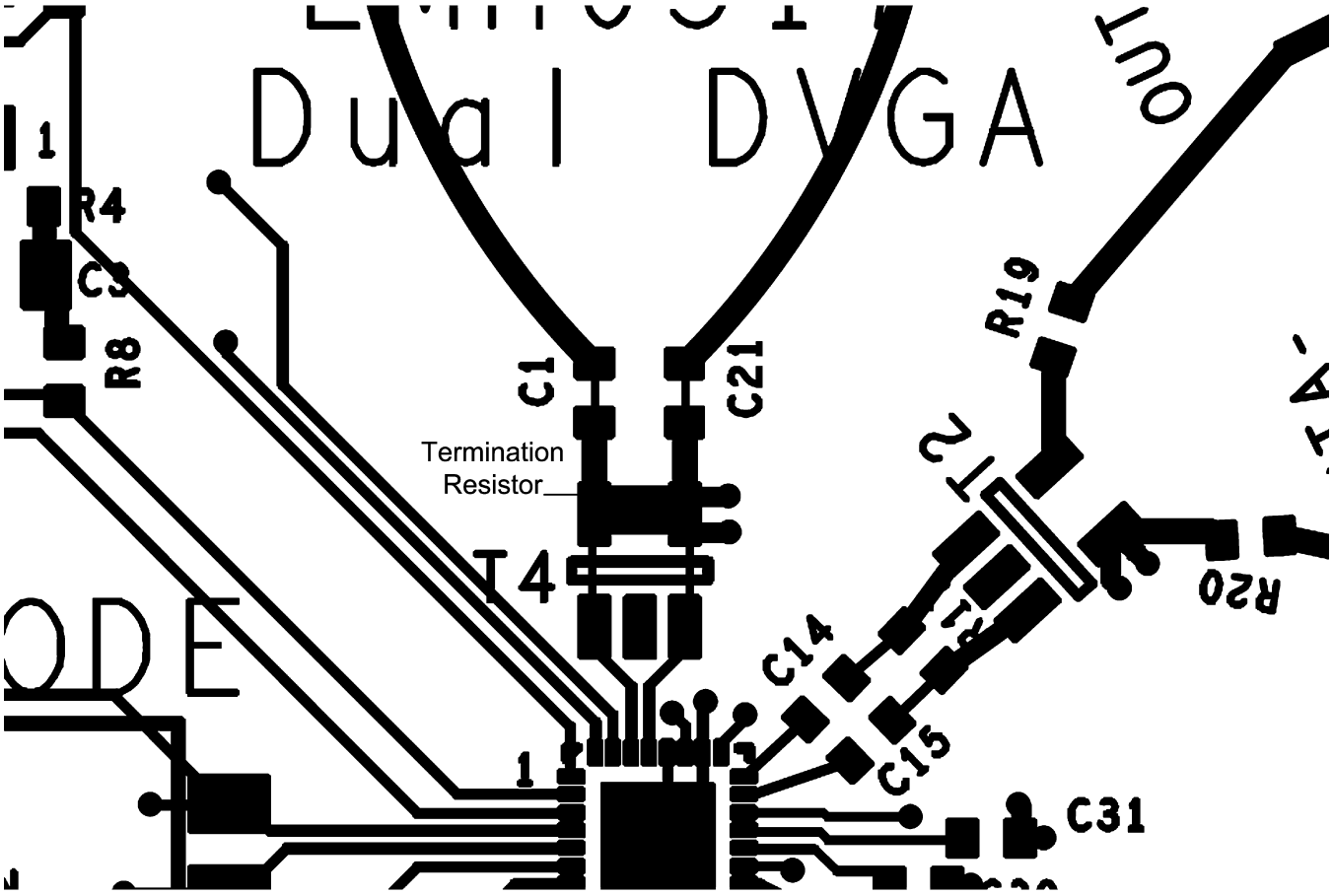

Figure 6. Connections for Differential Input

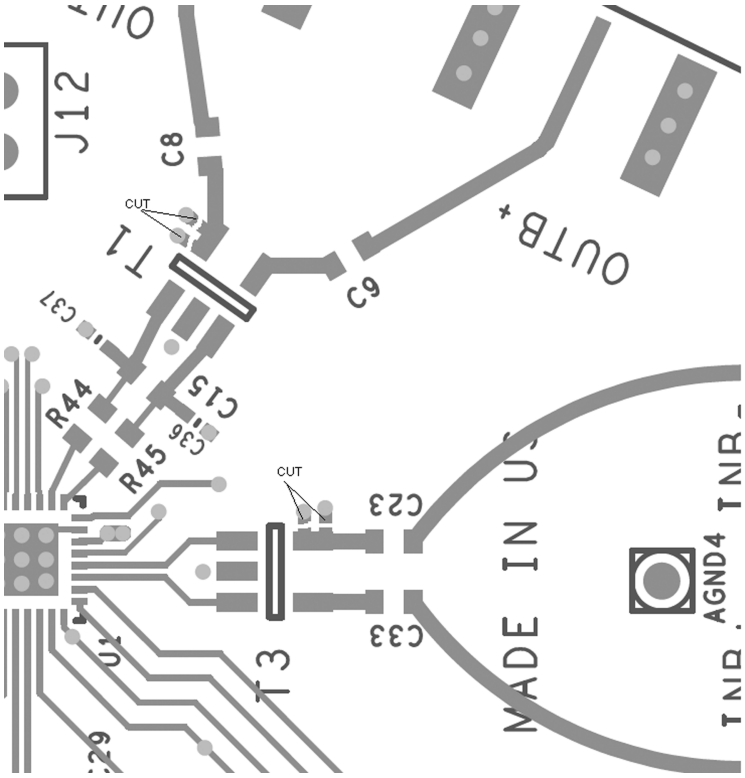

Figure 7. Trace Cuts for Differential Input and Output

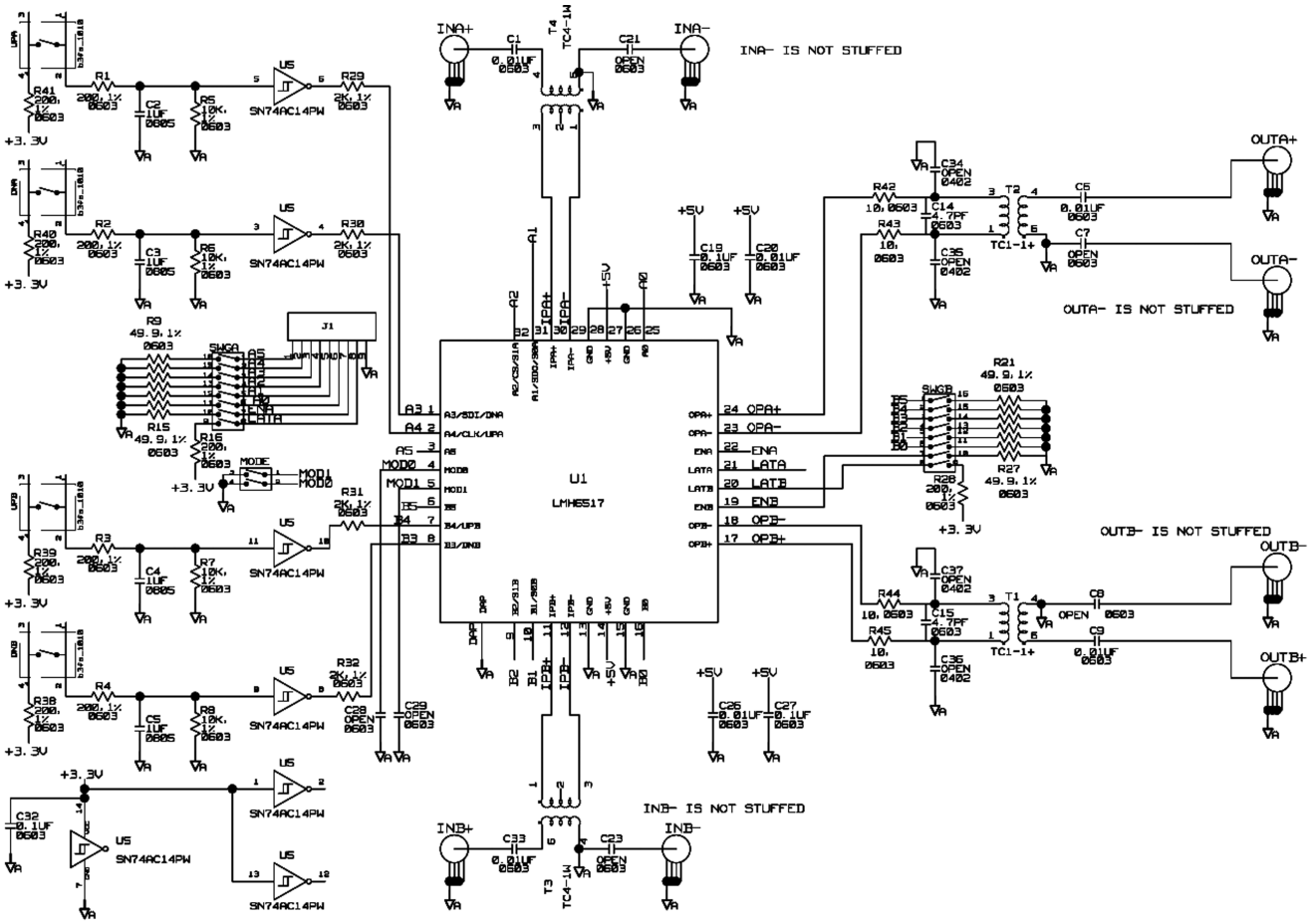

Figure 8. Signal Path Schematic

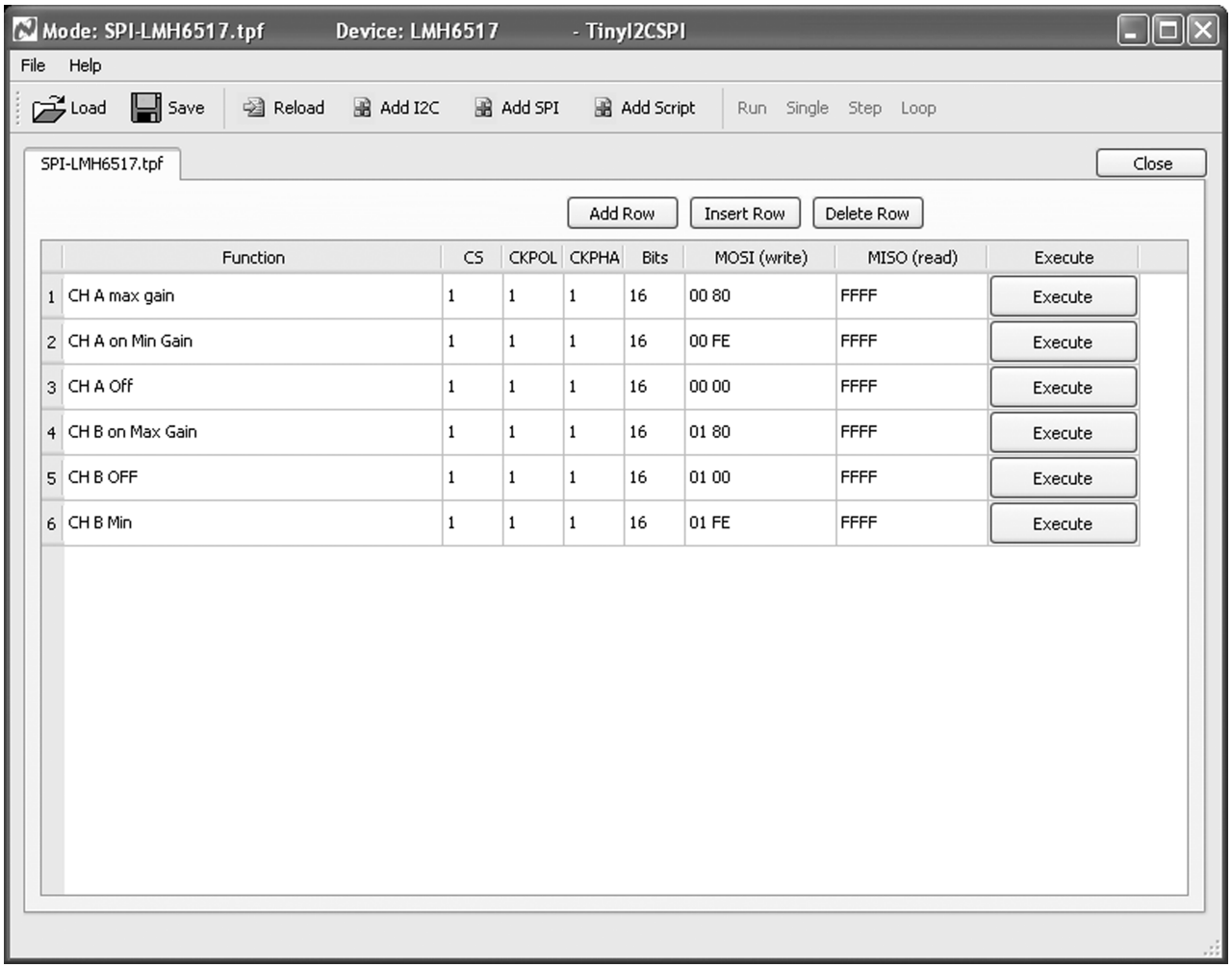

Figure 9. Software Settings for SPI Control

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