Using the TPS40100

A 12V Input, 3.3V Output, 10A Synchronous Buck Controller

System Power Management – DC/DC Controllers

1 INTRODUCTION

The TPS40100EVM-001 evaluation module (EVM) is a synchronous buck converter providing a fixed 3.3V output at up to 10A from a 12V input bus. The EVM is designed to start up from a single input supply, with no additional bias voltage required. The module uses a TPS40100 midrange input synchronous buck controller.

2 DESCRIPTION

TPS40100EVM-001 is designed to use a regulated 12V +/-10% (10.8V-13.2V) bus to produce a regulated 3.3V output at up to 10A of load current. The EVM is designed to demonstrate the TPS40100 in a typical regulated bus to low-voltage application while providing a number of test points to evaluate the performance of the TPS40100. The EVM includes features to demonstrate voltage tracking, margin up/down, enable/disable and power good. A synchronization pin is provided to allow the EVM to be synchronized to an external clock.

2.1 APPLICATIONS

- Non-Isolated Medium Current Point of Load and low voltage bus converters.
- Merchant Power Modules
- Networking Equipment
- Telecommunications Equipment
- DC Power Distributed Systems

2.2 FEATURES

- 10.8V – 13.2V input range
- 3.3V fixed output
- 10 Adc Steady State Output Current
- Output margin up and down support
- Tracking voltage input to support simultaneous sequencing
- Power good indicator
- Frequency synchronization input
- Remote sensing scheme
- 380kHz switching frequency
- Single Main Switch MOSFET and Single Synchronous Rectifier MOSFET
- Single Component Side, surface mount design on a 3.0” x 3.25” evaluation board
- Four Layer PCB with all components on top side
- Convenient test points for probing critical waveforms
- Test points for full loop analysis as well as control to output

2.2.1 USING REMOTE SENSE (J3)

TPS40100EVM-001 provides the user with remote sense capabilities. Remote sense is used to provide more accurate load regulation by compensating for losses over terminal connections and load wire resistance. When remote sense is used properly, the converter will regulate the voltage at the point where sense connections are placed. These remote sense connections are usually placed at the intended load. As the load is increased the direct output of the converter will rise to compensate for IR losses.

Caution: long wiring connections can cause the converter to act irregularly. This can show up as pulse width jitter or an oscillatory effect on the ripple voltage. If this condition occurs, check the set up and make adjustments. Please see section 5.3.2 in this users guide.

2.2.2 SIMULTANEOUS TRACKING (J3)

The EVM is equipped to provide the ability to demonstrate the tracking feature of the TPS40100. In addition, the module can be configured to have multiple TPS40100-EVMs track. The voltage tracking function allows the TPS40100 to track an external ramp (provided on EVM). This tracking feature allows single or multiple modules to track an external ramp in order to comply with the demands of many microprocessor and memory applications. Please see section 5.3.3 of the test setup section of the users guide.

2.2.3 ENABLE (SW2)

The EVM is equipped with an enable/disable switch. Please see section 5.3.4 in test set up section of the users guide. Closing S1 will disable the device by pulling the UVLO pin of the TPS40100 low. Opening the S1 will enable the device, provided that the appropriate input voltage is present. J3 pin 4 is an enable monitor pin providing a connection for user observation.

2.2.4 MARGIN UP/DOWN (J4)

The margin up and down feature of the EVM provides the user with the ability to trim or margin the output of the converter up/down by 3% or 5%. EVM is equipped with convenient jumper settings to give the user the ability to trim the output voltage. Please see section 5.3.5 in the test set up section of this users guide for more detailed test setup information.

2.2.5 POWER GOOD (J1)

The EVM contains a power good pin to provide the user with a “power ok” signal. This pin is pulled up through a resistor to the 5VBP pin of the TPS40100. If any of the following conditions occur the power good pin will pull low;

- Soft-start is active (Vss < 3.5V)
- Tracking is active (Vtrackout>.7V)
- Vfb < 0.61V
- Vfb > 0.77V
- Vuvlo < 1.33V
- Overcurrent condition exists
- Die temperature is greater than 165°C

This pin can be monitored with an oscilloscope to observe its behavior. Please see section 5.3.6 in the test setup section of the users guide.

2.2.6 SYNCHRONIZTION (J1)

To TPS40100-EVM can be synchronized to an external clock source of a higher frequency than that of the free running PWM clock. This is a feature that can aid with input filter design. It is recommended that the synchronization frequency be no more than 120% of the free running frequency. The EVM is configured to a switching frequency of 370 kHz, so the external frequency into the synchronization pin should be no more than 470 kHz. Please see section 5.3.6 of the test setup section of this users guide.

3 *ELECTRICAL PERFORMANCE SPECIFICATION*

Parameter	Notes and Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS					
Input Voltage Range		10.8		13.2	V
Max Input Current	V_{IN} = 10.8V, I_{OUT} = 10A		3.5		A
No-Load Input Current	V_{IN} = 13.2V, I_{OUT} = 0A		100		mA
OUTPUT CHARACTERISTICS					
Output Voltage		3.22	3.30	3.39	V
Output Voltage Regulation	Line Regulation (10.8V<V_{IN}<13.2V, I_{OUT} = 5A) Load Regulation (0A<I_{OUT}<10A, V_{IN} = 12V)			1 1	% %
Output Voltage Ripple	V_{IN} = 13.2V, I_{OUT} = 10A		25		mVpp
Output Load Current		0		10	A
Output Over Current			15		A
SYSTEM CHARACTERISTICS					
Switching Frequency		350	380	410	kHz
Full Load Efficiency	V_{OUT} = 3.3V, I_{OUT} = 10A V_{12V_IN} = 10.8V V_{12V_IN} = 12V V_{12V_IN} = 13.2V		93.9 93.5 93.4		%

Table 1: TPS40100EVM-001 Electrical & Performance Specifications

4 SCHEMATIC

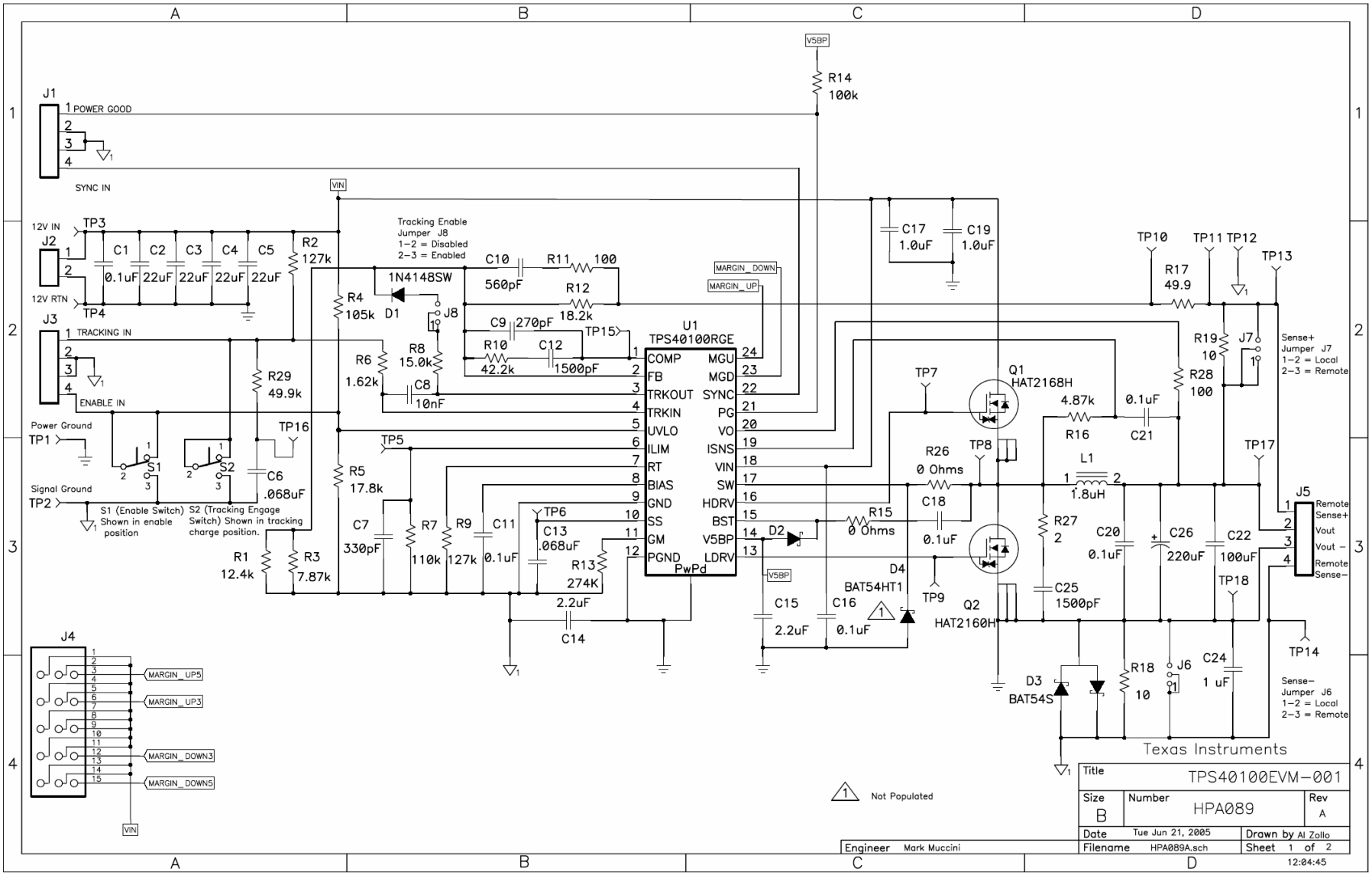

Figure 1: TPS40100EVM-001 Power Stage / Control Schematic

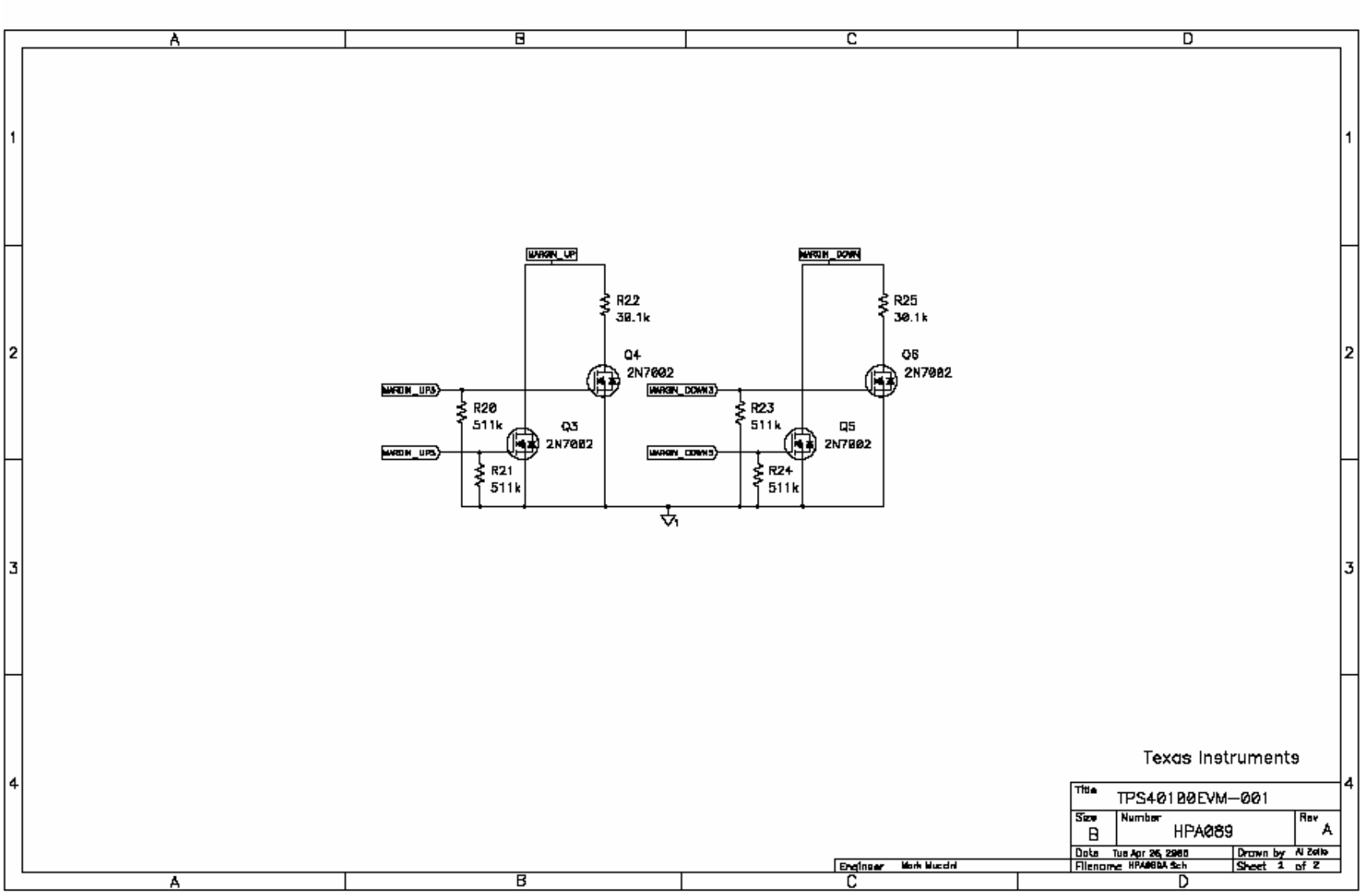

Figure 2: TPS40100EVM-001 Margin Control

Component values are for reference only.

5 TEST SET UP

5.1 EQUIPMENT

5.1.1 VOLTAGE SOURCE

VIN
The input voltage source (V_{IN}) should be a 0-15V variable DC source capable of 5Adc. Connect V_{IN} to J2 as shown in Figure 3.

5.1.2 METERS

Ammeter1: 0-5Adc, ammeter
Voltmeter1: VIN, 0-15V voltmeter
Voltmeter2: VIN, 0-5V voltmeter

5.1.3 LOADS

LOAD1
The Output Load (LOAD1) should be an Electronic Constant Current Mode Load capable of 0-10Adc @ 3.3V

5.1.4 Recommended Wire Gauge

VIN to J2.
The connection between the source voltage, VIN and J2 of EVM can carry as much as 5 Adc. The minimum recommended wire size is AWG #16. Shorter lengths of input wire will aid in reducing inductance and provide better overall performance.

J5 to LOAD1 (Power Pins 2, 3)
The power connection between J5 of EVM and LOAD1 can carry as much as 10 Adc. It is recommended that the user use AWG#16 wire. It is recommended that the load wires be kept as short as possible. This will aid in performance, most notably in transient response.

J2 to LOAD1 (Remote Sense)
If remote sense is to be used, ensure that J6 and J7 are in the remote sense enable position (shunt pins 1&2). Load wires and sense wires should be kept less than 6 inches to ensure proper functionality. The remote sense wires connecting J5 (pins 1 and 4) and LOAD1 carry less than 1Adc. The minimum recommended wire size is AWG #22, with the total length of less than 6 inches long.

5.1.5 OTHER

FAN
This evaluation module includes components that can get hot to the touch. A small fan capable of 200-400 LFM is required to reduce component surface temperatures to prevent user injury. The EVM should not be left unattended while powered or probed while the fan is not running.
OSCILLOSCOPE
A 60MHz or faster oscilloscope can be used to monitor many points on the EVM. For output ripple voltage measurements the Oscilloscope should be set for 20 MHz bandwidth limiting, 1MΩ impedance, AC coupling, 1μs/division horizontal resolution, 10-20mV/division vertical resolution for taking output ripple measurements.
FUNCTION GENERATOR
A function generator capable of source a 0-5V square wave at frequencies past 400Khz.

5.2 EQUIPMENT SETUP

5.2.1 Initial EVM Jumper and Switch Settings

Figure 4 is the basic test set up recommended for evaluating the TPS40100EVM-001. EVM is shipped with the following in the default position:

1. Enable switch (S1) open across pins 2&3. This is the enable position.
2. Tracking enable jumper (J8) has shunt positioned across pins 1&2 disabling the tracking feature.
3. Tracking engage switch (S2) open across pins 2&3. This enables the tracking ramp to charge.
4. Remote sense jumpers (J6 and J7) have shunts positioned across pins 2&3 enabling local connector sensing.
5. Margin shunts positioned in the margin disable position.

5.2.2 Procedure

1. Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
2. Prior to connecting the DC input source, VIN, it is advisable to limit the source current to 5.0A maximum. Make sure VIN is initially set to 0V and connected as shown in Figure 4.
3. Connect an ammeter between the positive output of the input supply and the positive input of the EVM. (J2, Pin 1)
4. Connect voltmeter Voltmeter #1 to TP3 and TP4 as shown in Figure 2.1. These are the EVM input supply monitoring points.
5. Connect LOAD1 to J5 as shown in Figure 2.1. Set LOAD1 to constant current mode to sink 0Adc before input voltage is applied.
6. Connect voltmeter #2 across TP13 and TP14 as shown in Figure 2.1. This is the EVM output supply monitoring point. Note: this configuration is local sensing.
7. Remove oscilloscope probe jacket and position probe as shown below in Figure 3. TP17 and TP18 are implemented to provide the user with the means to achieve good noise immune measurements of ripple voltage and transient response.

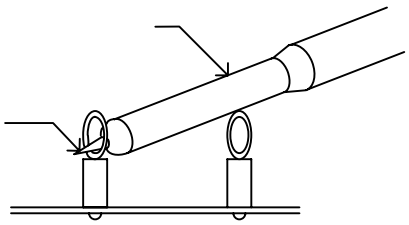

Figure 3: Probe position for ripple measurement

8. Place Fan as shown in Figure 4 and turn on, making sure air is flowing across the EVM.

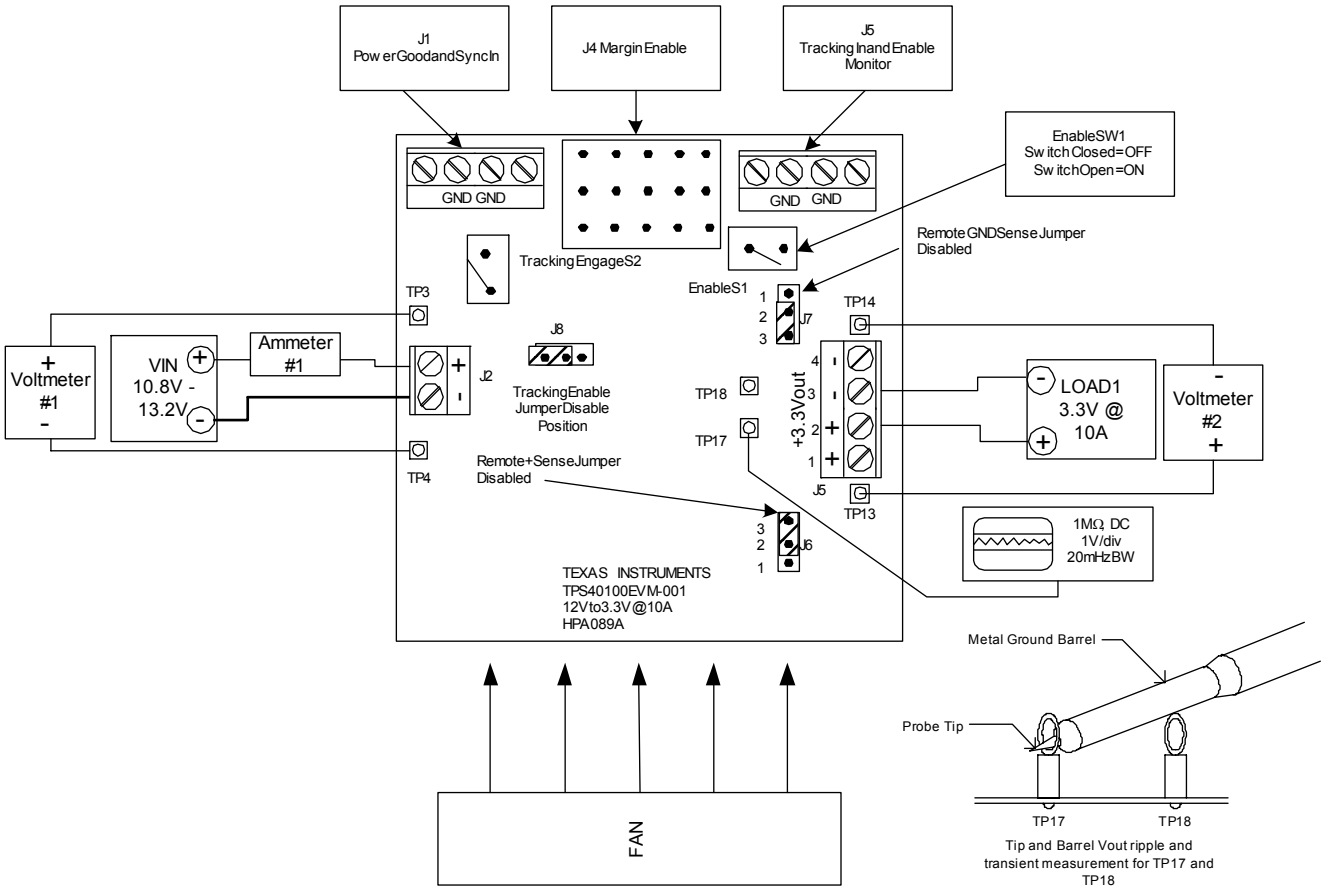

Figure 4: TPS40100EVM-001 Recommended Test Set-Up

5.2.3 START UP / SHUT DOWN PROCEDURE

1. Increase VIN (V1) from 0V to 12Vdc.
2. Observe that Vout has risen to its nominal voltage.
3. Vary LOAD1 from 0 – 10Adc
4. Vary VIN from 10.8dc to 13.2Vdc
5. Decrease LOAD1 to 0A.
6. Decrease VIN to 0V.

5.2.4 EQUIPMENT SHUTDOWN

1. Shut Down Oscilloscope
2. Shut down LOAD
3. Shut down VIN
4. Shut down FAN

5.3 OTHER TESTS

5.3.1 ADJUSTING OUTPUT VOLTAGE (R1 & R3)

The regulated output voltage can be adjusted by changing the values of the feedback resistors, R1 and R3. R19 and R17 are located in the feedback to provide the user with positive remote sense and the ability to perform loop analysis with a frequency/gain analyzer. Resistors R12 and the parallel combination of R1 and R3 are the dominant resistors associated with setting the output voltage. Listed below are the equations associated for establishing the output voltage.

$$Rparallel := \frac{(R1 \cdot R3)}{(R1 + R3)} \qquad Vout := Vref \cdot \left[\frac{(R12 + R17)}{Rparallel} + 1 \right] \qquad Rparallel := \left(\frac{Vref}{Vout - Vref} \right) \cdot (R17 + R12)$$

Where V_{VREF} = 0.690V, R17 = 49.9Ω, R12 = 18.2k Ω. R1//R3 can be adjusted to provide user defined output voltages. Table 2 contains values for R1//R3 to generate popular output voltages.

V_{OUT}	R1//R3 (Rparallel)	R1	R3
3.3V	4.82K	12.4 K	7.87 K
2.5V	6.95K	7.15 K	237 K
2.2V	8.33K	8.66 K	205 K
2.0V	9.61K	10.0 K	237 K
1.8V	11.34K	12.1 K	178 K
1.5V	15.55K	16.2 K	365 K
1.2V	24.69K	26.1 K	422 K

Table 2: Adjusting V_{out} with R1//R3

5.3.2 Remote Sense Test Set-Up

In order for the remote sense feature of the TPS40100EVM-001 to function properly, it is essential that the test setup be configured correctly. Use the following steps to set up the remote sense:

1) Ensure that the remote sense jumpers J7&J8 are shunted across pins 1&2
2) Connect load wires of a max length of 6 inches from pin 2 of J5 (+Vout) to the positive terminal of the load. Connect same length of wire from pin 3 of J5 (RTN) to the negative terminal of the load. Be sure to properly gauge the load wires for 10A. AWG#16 is recommended.
3) Connect sense wire from J5 pin 1 to the positive terminal of the load. This is the +sense line. Be sure to not exceed 6 inches in length. AWG#22 wire is recommended.
4) Connect sense wire from J5 pin 4 to the negative terminal of the load. This is the –sense line. 6 inches maximum length. AWG#22 wire is recommended.
5) Monitor voltage at TP13 and TP14 using a voltmeter. This will be the regulated voltage at the load.
6) Monitor voltage at J5 pins 2, 3. This is the voltage at the output connector. This voltage will increase based on load.
7) Set load to 0A, constant current. Both monitoring points should read very close to the same value.

8) Increase load gradually and observe the difference in voltages present at the monitoring points. The set voltage (3.3V) will be regulated at the load; this will be noted at TP13 and TP14. The direct output of the converter (J5 pin 2, 3) will read a higher voltage. As IR losses increase over load wires and terminals the direct output of the converter will compensate by raising the voltage to keep within regulation at the load.

Caution: long distance runs from the output of the converter and the load will cause erratic behavior. This can show up as pulse width jitter or an oscillatory effect on the ripple voltage. If this condition occurs, check the set up and make adjustments. Please see Figure 5 below for test up.

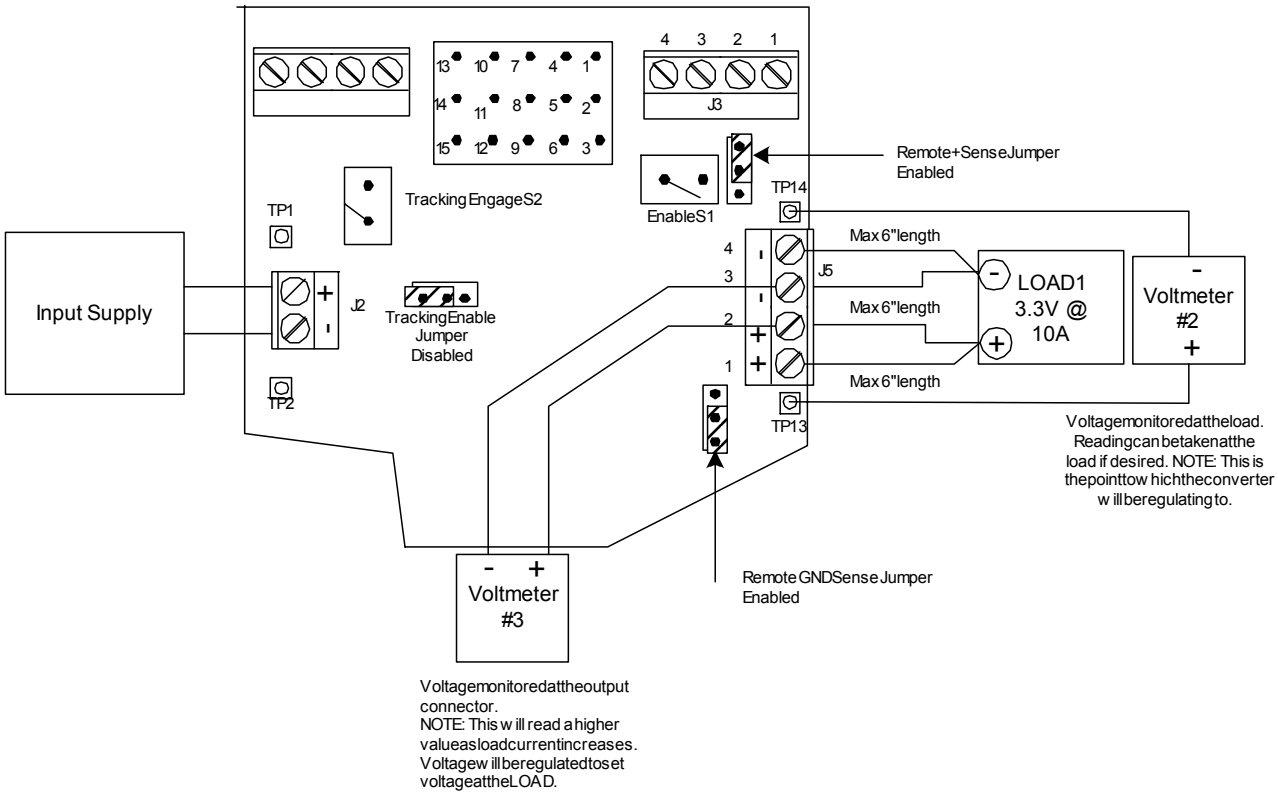

Figure 5: TPS40100EVM-001 Recommended Remote Test Set-Up

5.3.3 Voltage Tracking Test Set-Up

The following procedure is for a single EVM demonstration of the track function. Please see Figure 6 below.

1. Shunt pins 2&3 of J8 (Tracking Enable Jumper)
2. Tracking Engage Switch (S2) should be in the closed position.
3. Connect oscilloscope probe to the TRACKING IN pin (J3 pin 1) and the Vout (TP 17&18).
4. Connect load to the output of the EVM and set from 1A – 10A. (User selectable)
5. Power on the EVM with an input voltage of 10.8V – 13.2V. (Allow for SS voltage to reach 3.5V to ensure proper tracking performance or wait 1-2 seconds)
6. Open the Tracking Engage Switch (S2) (Shorting pins 1&2 open) and observe how Vout tracks the TRACKING IN pins rising voltage. Waveforms should be simultaneous.
7. Close the Tracking Engage (S2) (Shorting pins 2&3 open) and observe how Vout tracks the TRACKING IN pin's falling voltage. Waveforms should be simultaneous.

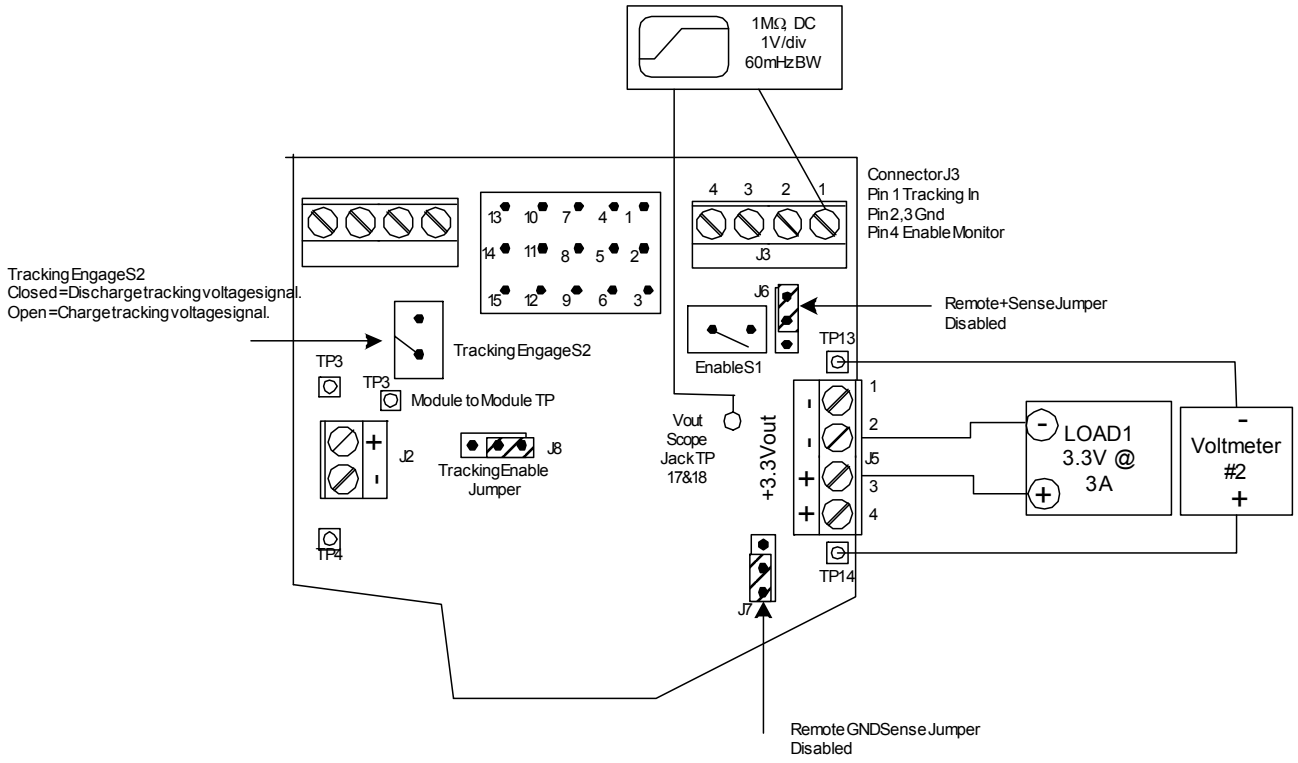

Figure 6: TPS40100EVM-001 Single EVM Tracking Test Set-Up

Single unit tracking (Charge).

Channel 1 (+3.3Vout)
Channel 4 (Tracking In).
Vin = 12V
Iout=10A

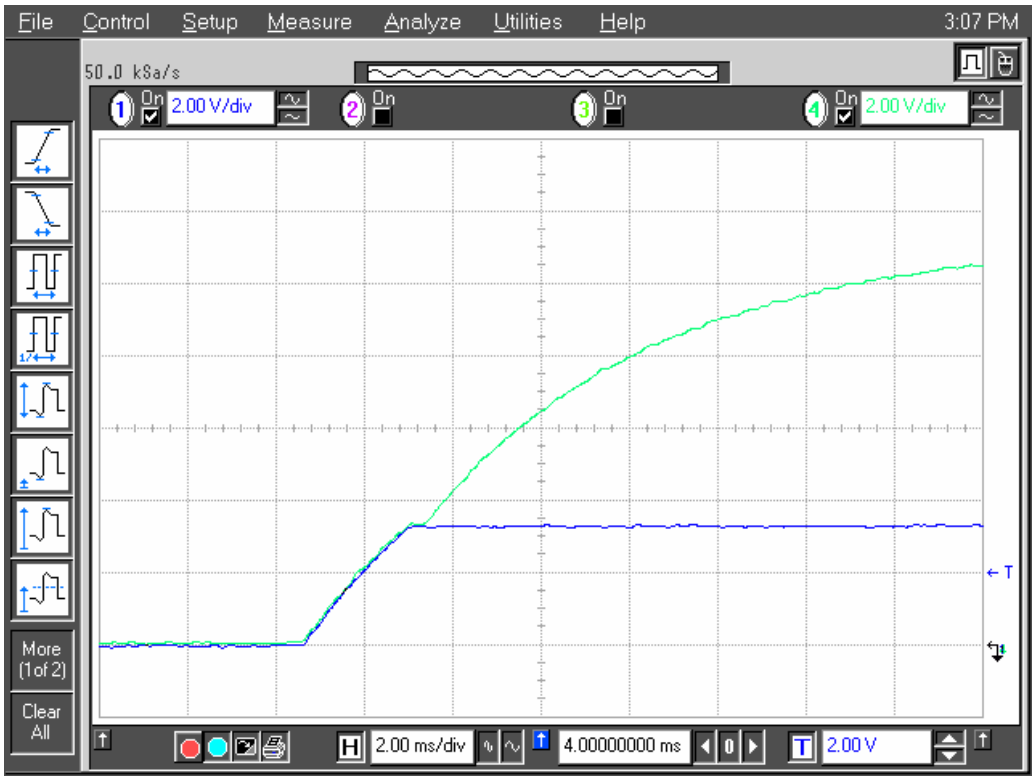

Figure 7: Single EVM tracking charging ramp

Single unit tracking (Discharge).

Channel 1 (+3.3Vout)
Channel 4 (Tracking In).
Vin = 12V
Iout=10A

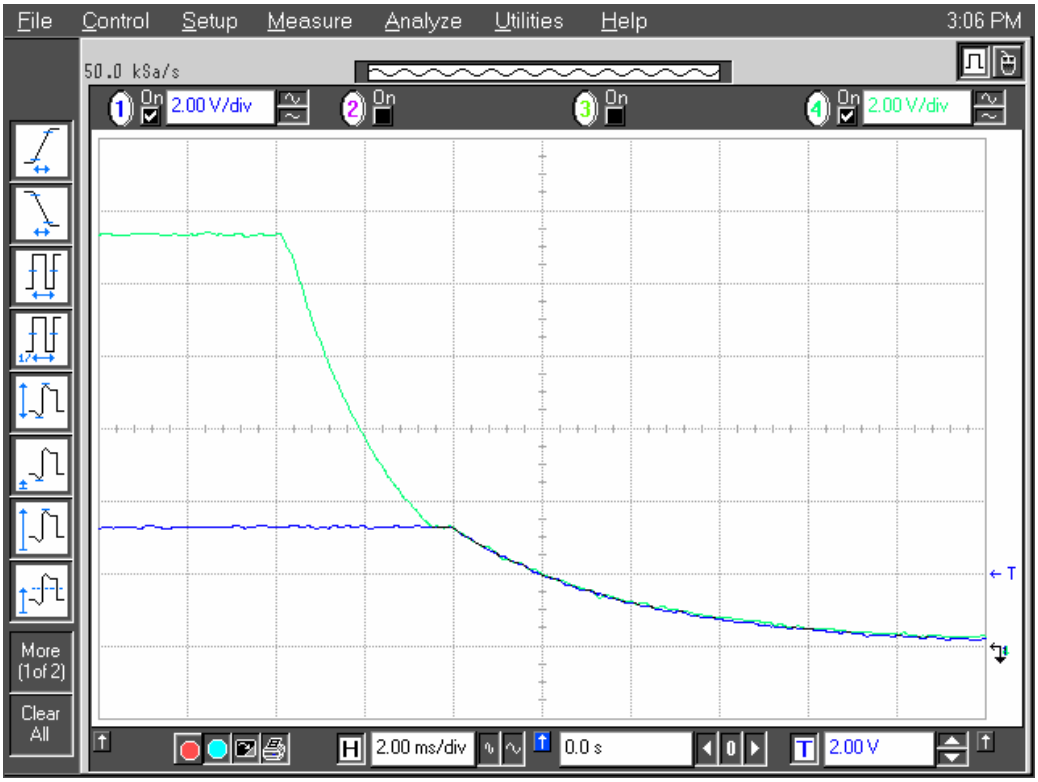

Figure 8: Single EVM tracking discharging ramp

To demonstrate multiple EVM (2 modules) tracking the following procedure must be followed to ensure proper functionality. The second TPS40100 EVM should be configured to a different output voltage.

1. Shunt pins 2&3 of the Tracking Enable Jumper (J8) for both modules.
2. Connect J3 pin 1 of each EVM.
3. Connect TP16 of each EVM. This is the module to module test point. This allows either module to be the control EVM via S2.
4. Tracking Engage Switch (S2) should be in the closed (shorting pins 2, 3) position on the control EVMs.
5. Connect oscilloscope probe to the TP17 and 18 of both modules and pin 1 of J3 of one of the modules. Modules should have a common input voltage and return.
6. Remote sense jumpers (J6&7) should have pins 2&3 shunted. Activating local output sensing.
7. Apply an input voltage of 10.8V to 13.2V.
8. Allow the SS voltage to reach 3.5V.
9. Open the control EVM Tracking Engage Switch (S2) (Opening pins 2, 3) and observe the monitored points. (Both EVM outputs and the tracking in voltage. Output voltage should follow the tracking in voltage until reaching the regulation point.
10. Close the Tracking Engage Switch (S2) (Shorting pins 2,3) of the control EVM and observe the monitored points. (Both EVM outputs and the tracking in voltage) Falling waveforms should be coincidal.

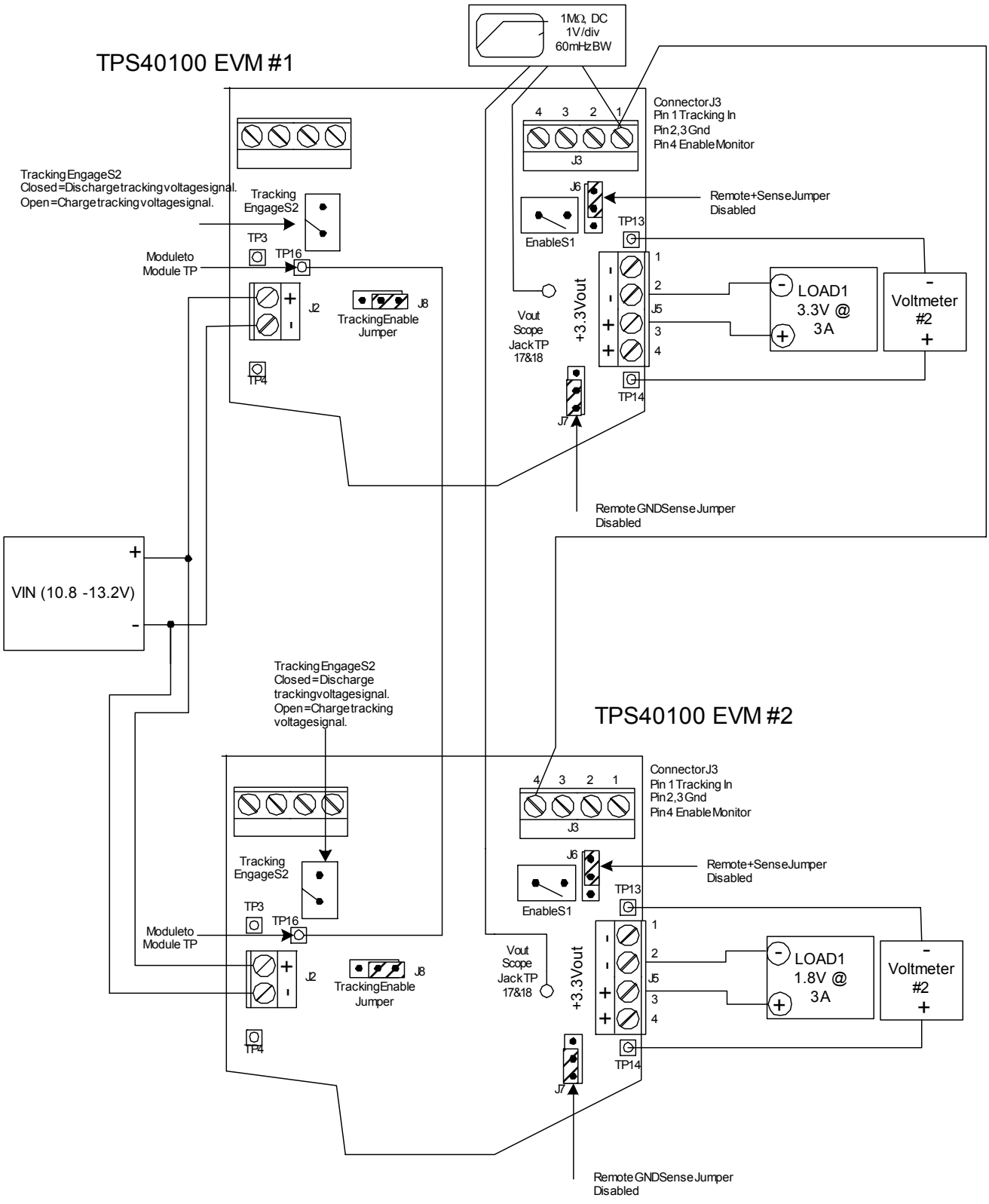

Figure 9: TPS40100EVM-001 Dual EVM Tracking Test Set-Up

5.3.4 Enable/Disable Test Set-Up

To begin testing set up EVM according to Figure 4 in the test set up section of the users guide. The switch (ENABLE S1) provides the ability to enable and disable the device. Please see Figure 10 below for illustration. Closing S1 will disable the device by pulling the UVLO pin of the TPS40100 low. Opening S1will enable the device, providing that the appropriate input voltage is present. J3 pin 4 is an enable monitor pin providing a connection for user observation.

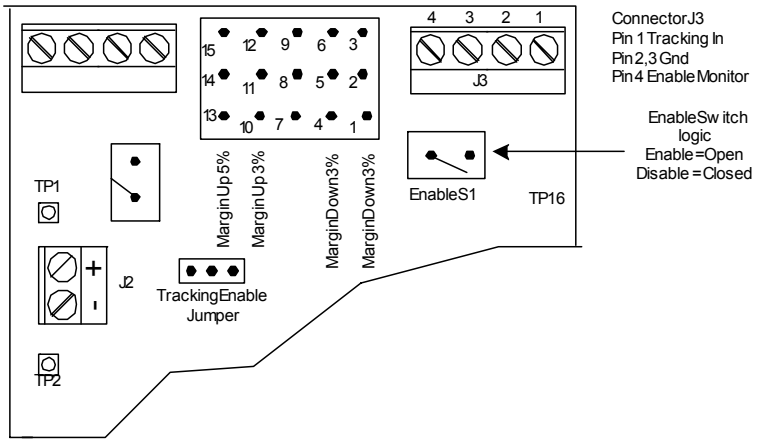

Figure 10: TPS40100EVM-001 Enable Test Set-Up Test Set-Up

Power on from enable.
Channel 1 (+3.3Vout)
Channel 3 (Power good).
Channel 4 (SS)
Vin = 12V

Iout =10A

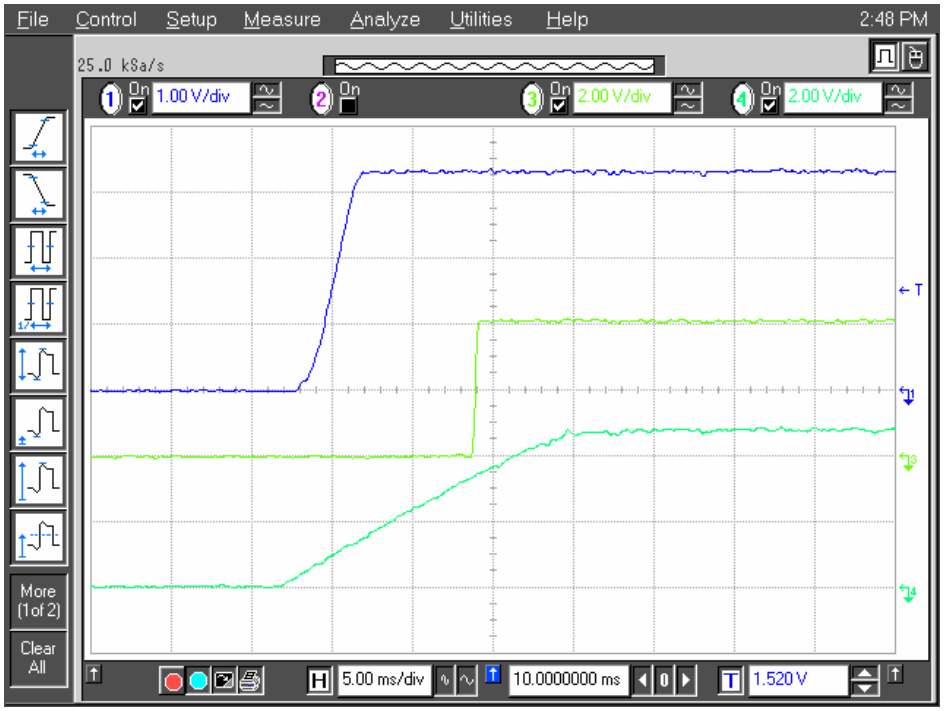

Figure 11: Power on from enable

5.3.5 Margin Test Set-Up

To begin testing set up EVM according to Figure 4. Chose the margin level desired. Connector J4 pins 3,6,12 and 15 are designated pins that can be connected to adjacent Vin pins (2, 5, 11 and 14) of J4 to enable the desired margin level. Please see Figure 12 (Margin Test Set Up). Example: To margin the unit up 5%, connect jumper across pins 2 and 3 of J4.

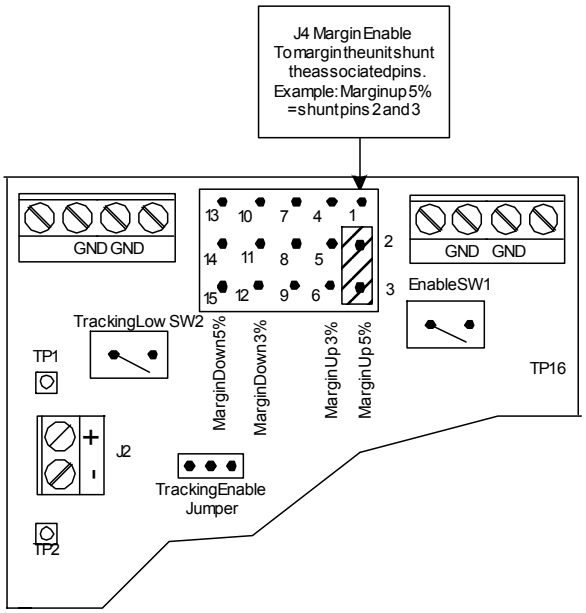

Figure 12: TPS40100EVM-001 Margin Test Set-Up

Margin up 5%.

Channel 1 Vout (looking at transition of voltage 165mV)
Channel 2 Corresponding margin pin

Vin = 12V
Iout=10A

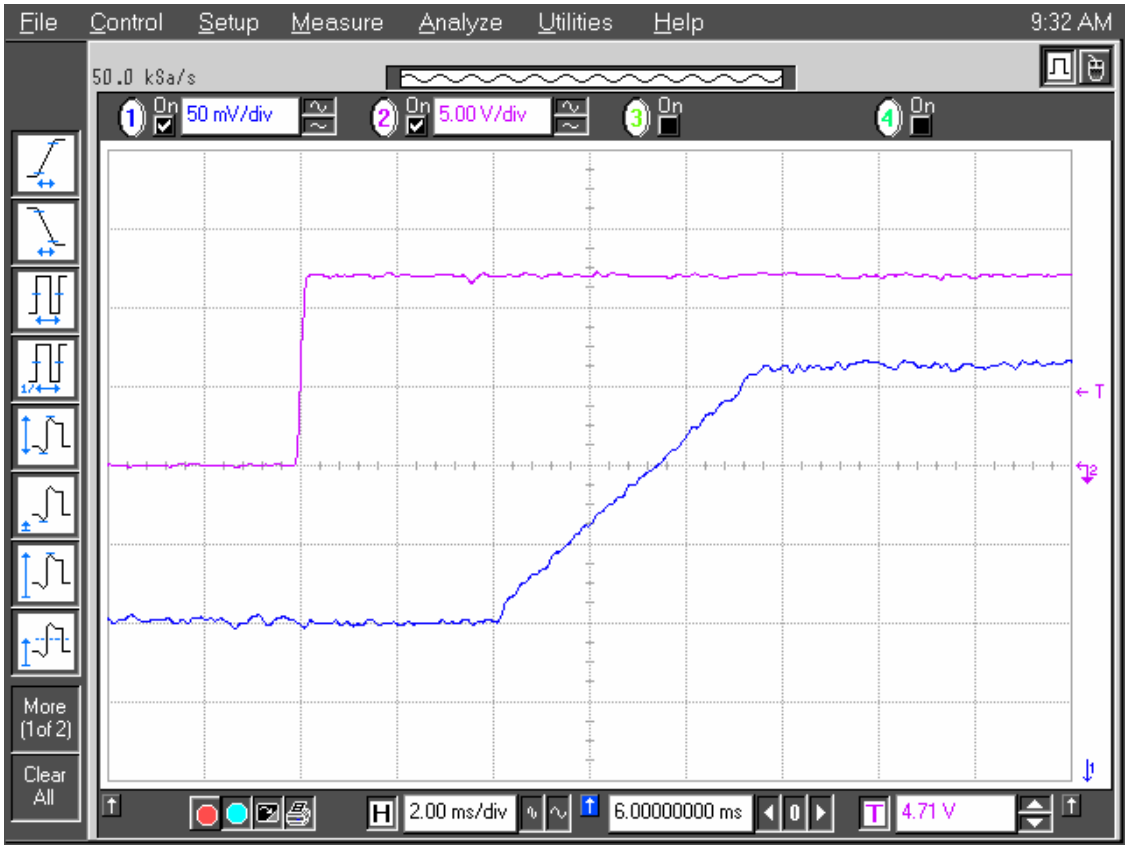

Figure 13: Margin up 5%

5.3.6 Power Good And Synchronization Test Set-Up

The TPS40100EVM-100 has the ability to be synchronized to an external clock. To begin testing, set up EVM according to Figure 4 in this users guide. Connector J1 contains both the power good pin and sync in pin. Power good can be monitored for its steady state response with a DMM or with an oscilloscope to illustrate its dynamic response. The Pgood voltage swing will range from 0 – 4.5V dependent on the condition of the output. A low on this pin dictates a power fault and a high (4.5V) conveys “power ok”.

Pin 4 of J1 is the input for an external clock frequency. To test, set up a function generator to provide a square wave at a frequency of above 410 kHz and below 480 kHz. Function generator should be set to provide a 0 to 5V square wave with a 50% duty cycle. Once power is applied to the EVM, apply the external clock to the sync in pin and observe the gate drive of the low side mosfet (Q2). This should be measured using an oscilloscope measuring at TP7. Gate drive pulse will coincide with external clock frequency. Please see Figure 14.

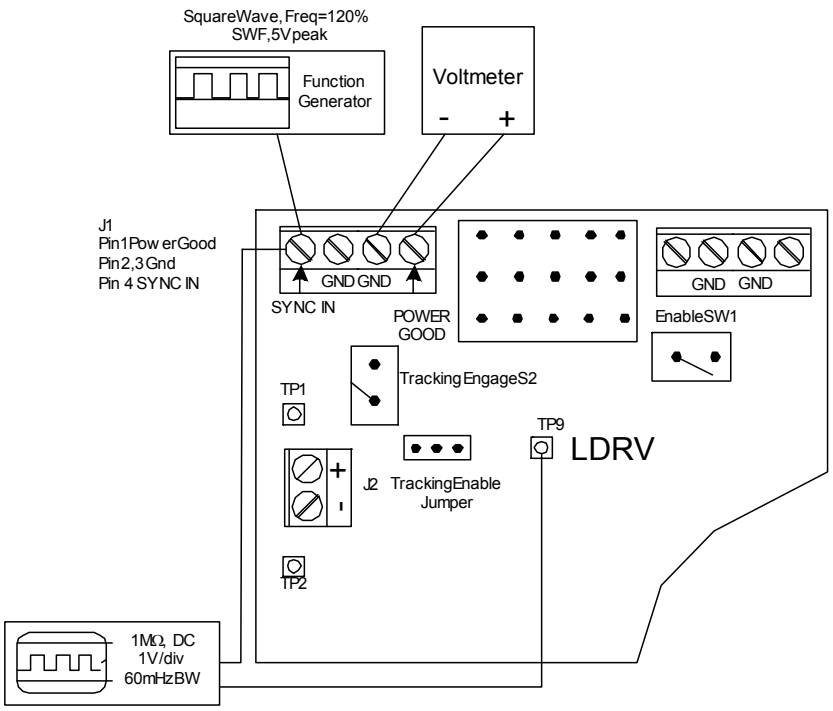

Figure 14: TPS40100EVM-001 Power Good and Synchronization Test Set-Up.

Synchronization

Channel 1 Switchnode voltage
Channel 2 External Clock Signal
Vin = 12V
Iout=10A

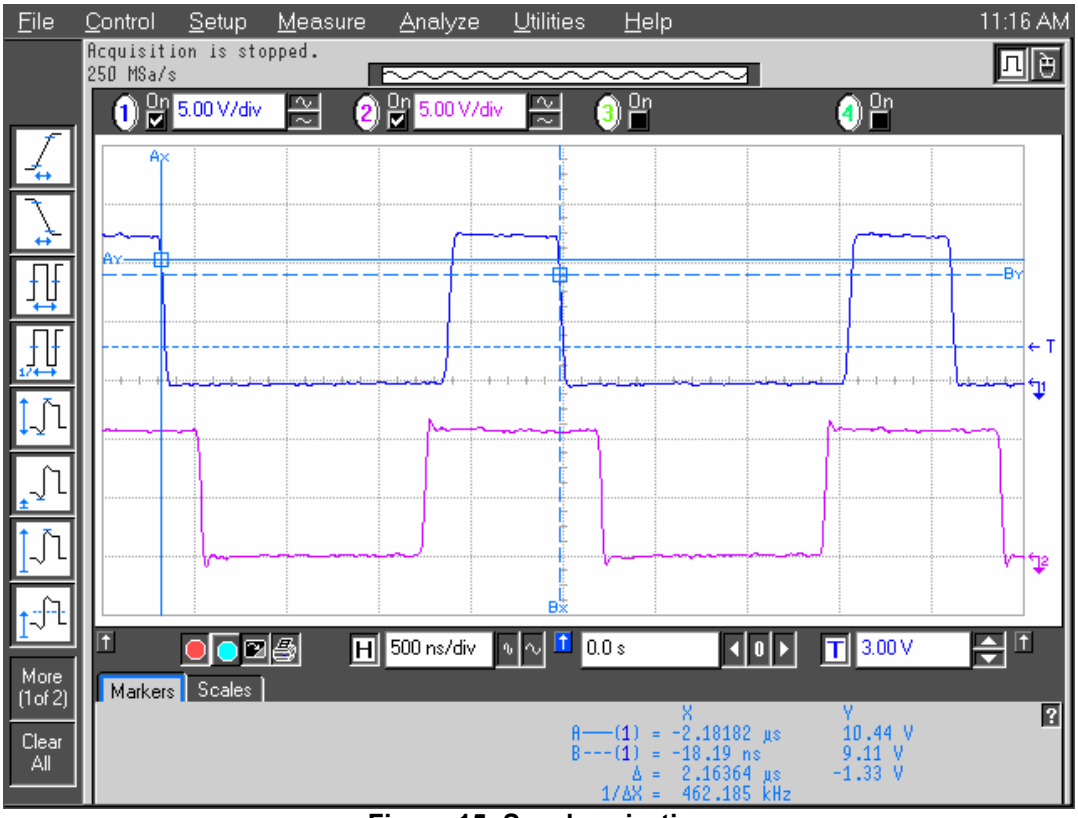

Figure 15: Synchronization

6 TPS40100EVM TYPICAL PERFORMANCE DATA & CHARACTERISTIC CURVES

Figure 16 through Figure 18 present typical performance curves for the TPS40100EVM-001. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

6.1 EFFICIENCY

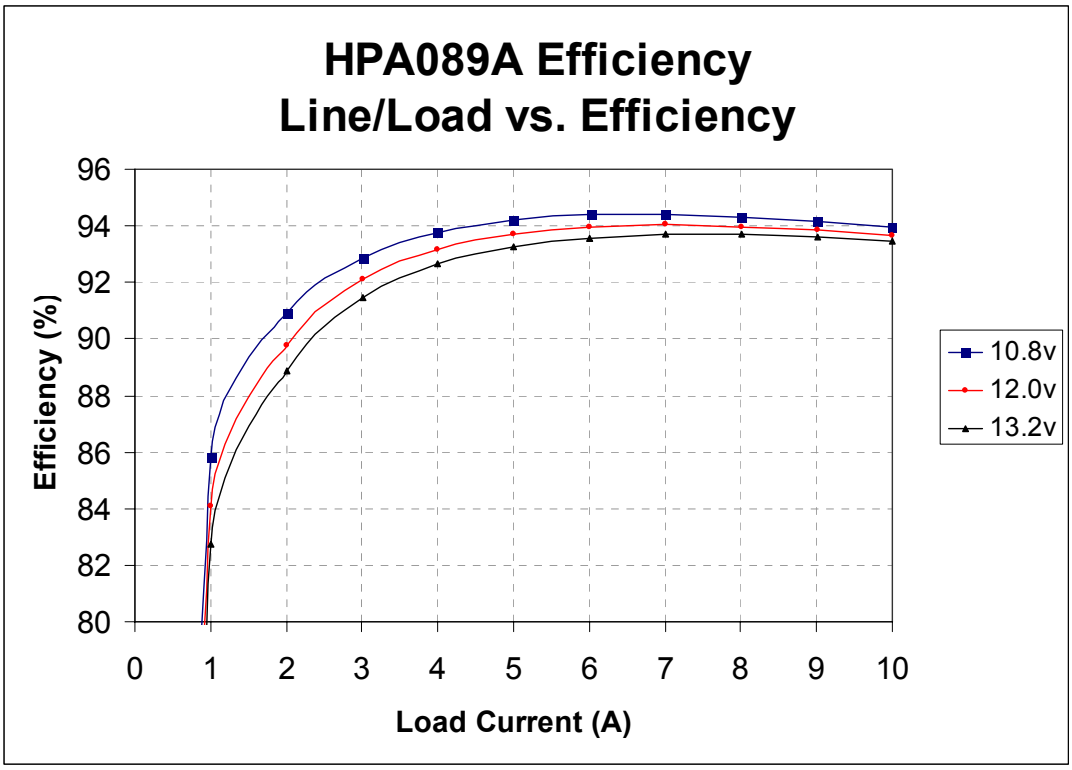

Figure 16: TPS40100EVM-001 Efficiency

V_{12V_IN} =10.8-13.2V, V_{OUT} = 3.3V I_{OUT} = 0-10A

6.2 LINE & LOAD REGULATION

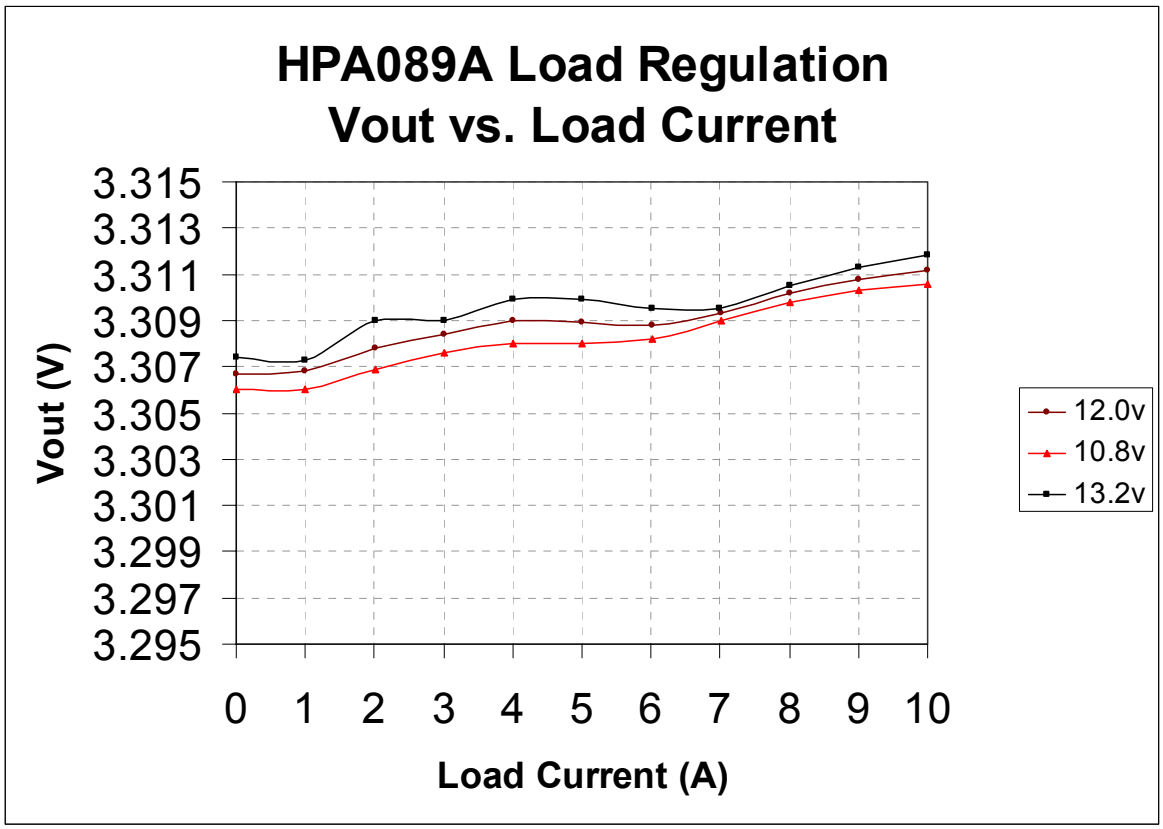

Figure 17: TPS40100EVM-001 Line Regulation I_{OUT} = 10A Vin = 10.8-13.2V

6.3 LOOP STABILITY

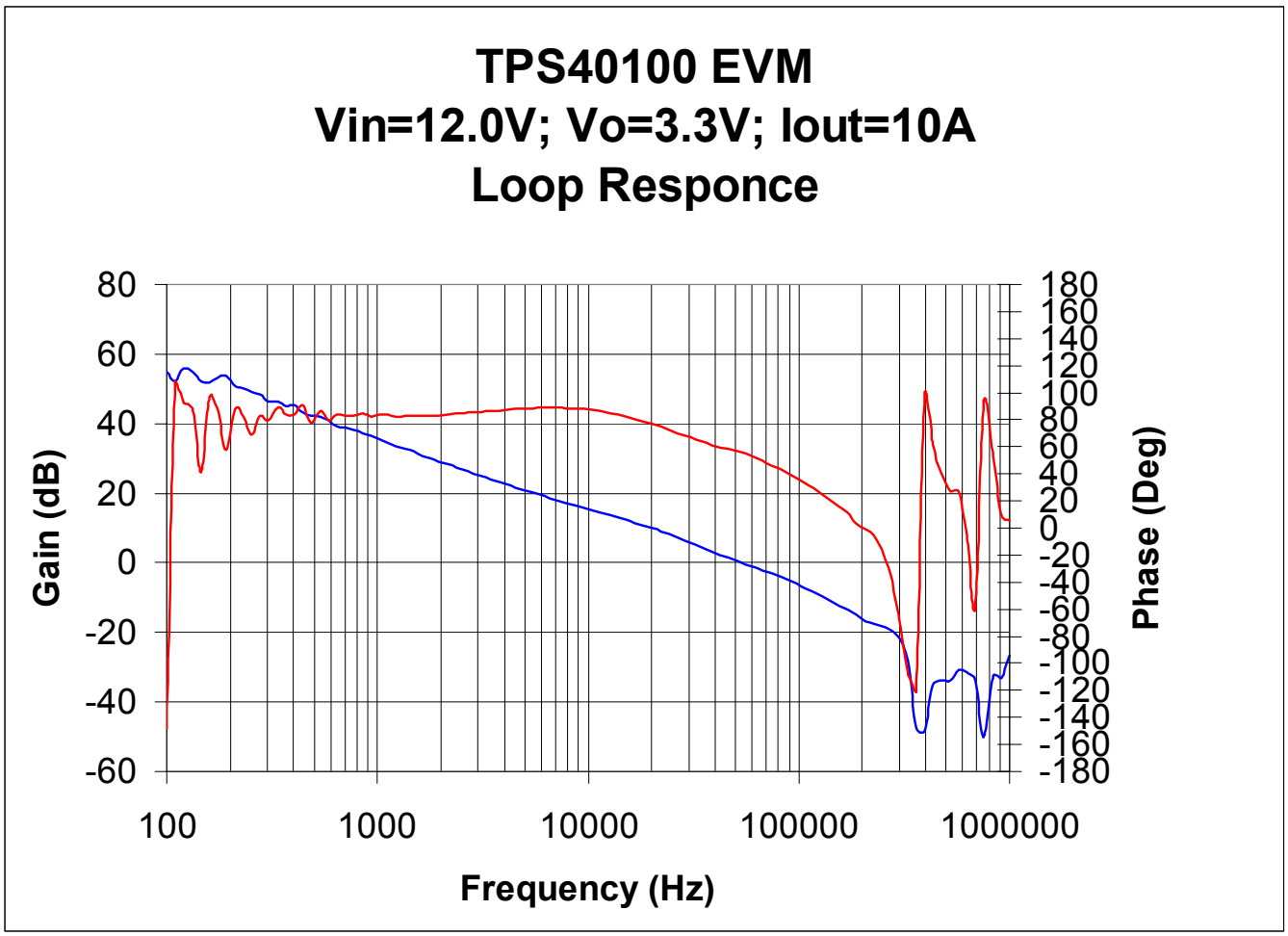

Figure 18: TPS40100EVM-001 Loop Response Vin = 12V, Vout = 3.3V, Iout = 10A

7 EVM ASSEMBLY DRAWINGS AND LAYOUT

The following figures (Figure 19 through 24) show the design of the TPS40100EVM-001 printed circuit board. The EVM has been designed using a 4-layer, 2oz copper-clad circuit board 3.0” x 3.25” with most of the components on the top side to allow the user to easily view, probe and evaluate the TPS40100 control IC in a practical application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space constrained systems.

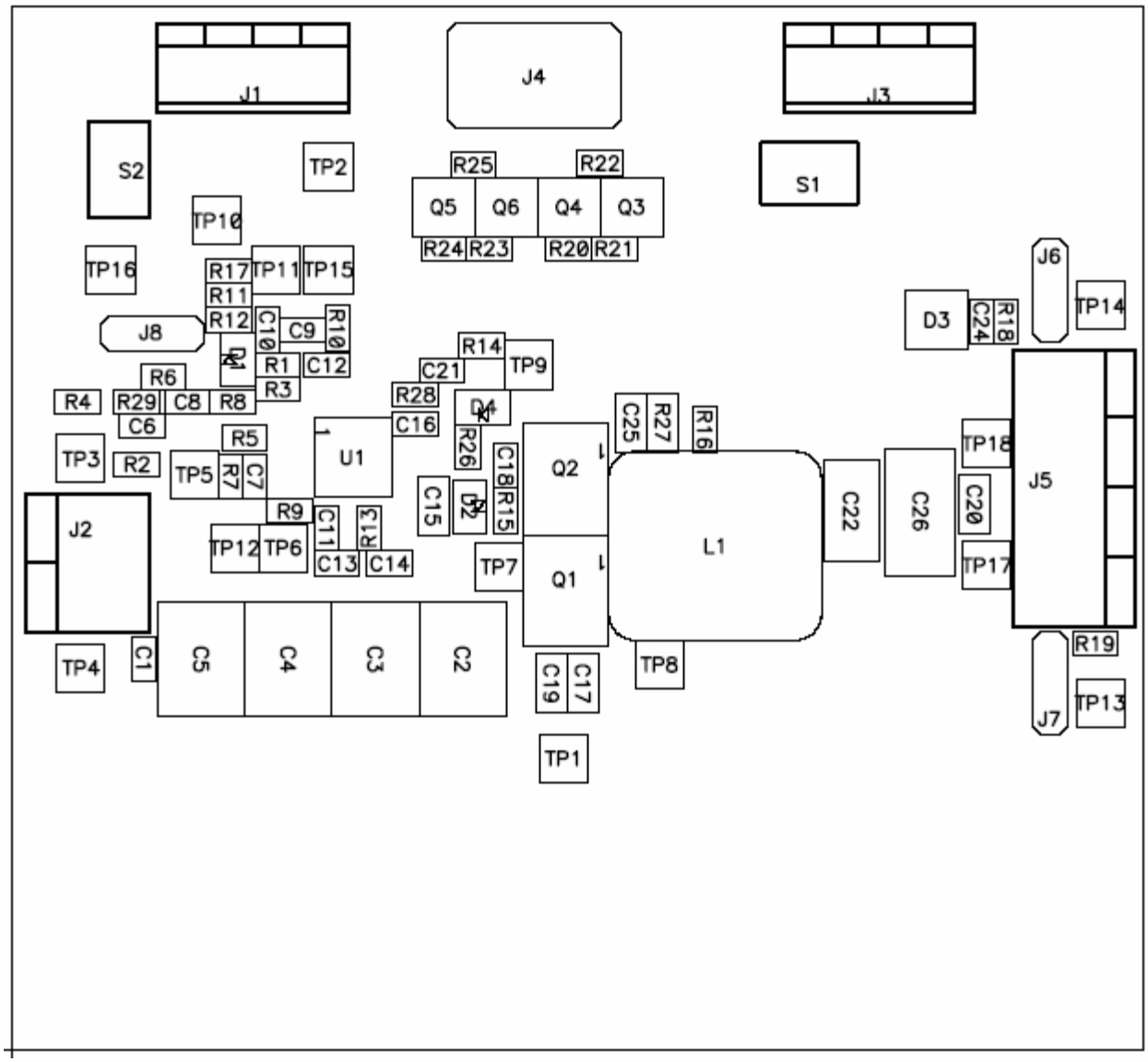

Figure 19: TPS40100EVM-001 Component Placement (Viewed from Top)

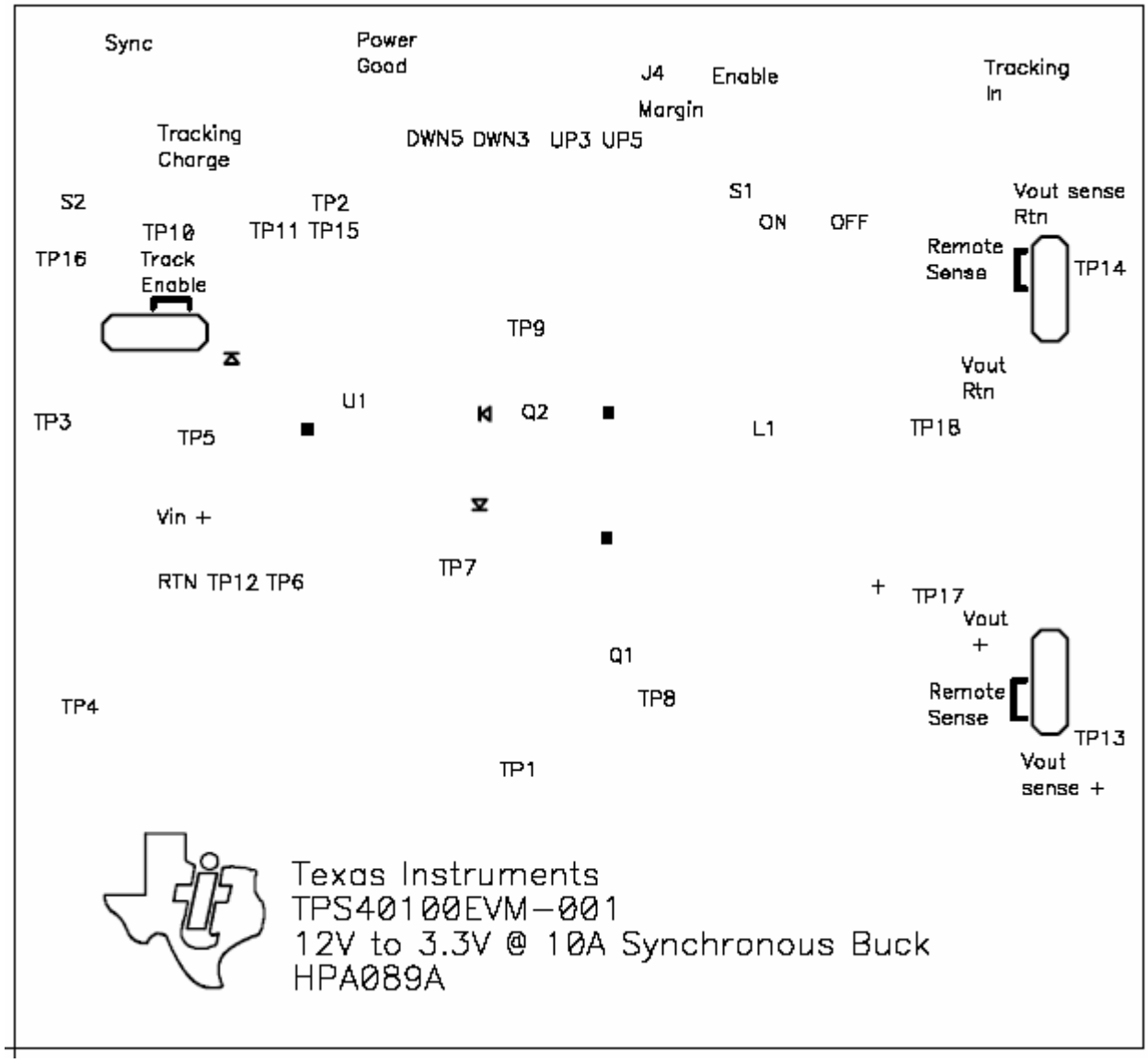

Figure 20: TPS40100EVM-001 Silkscreen (Viewed from Top)

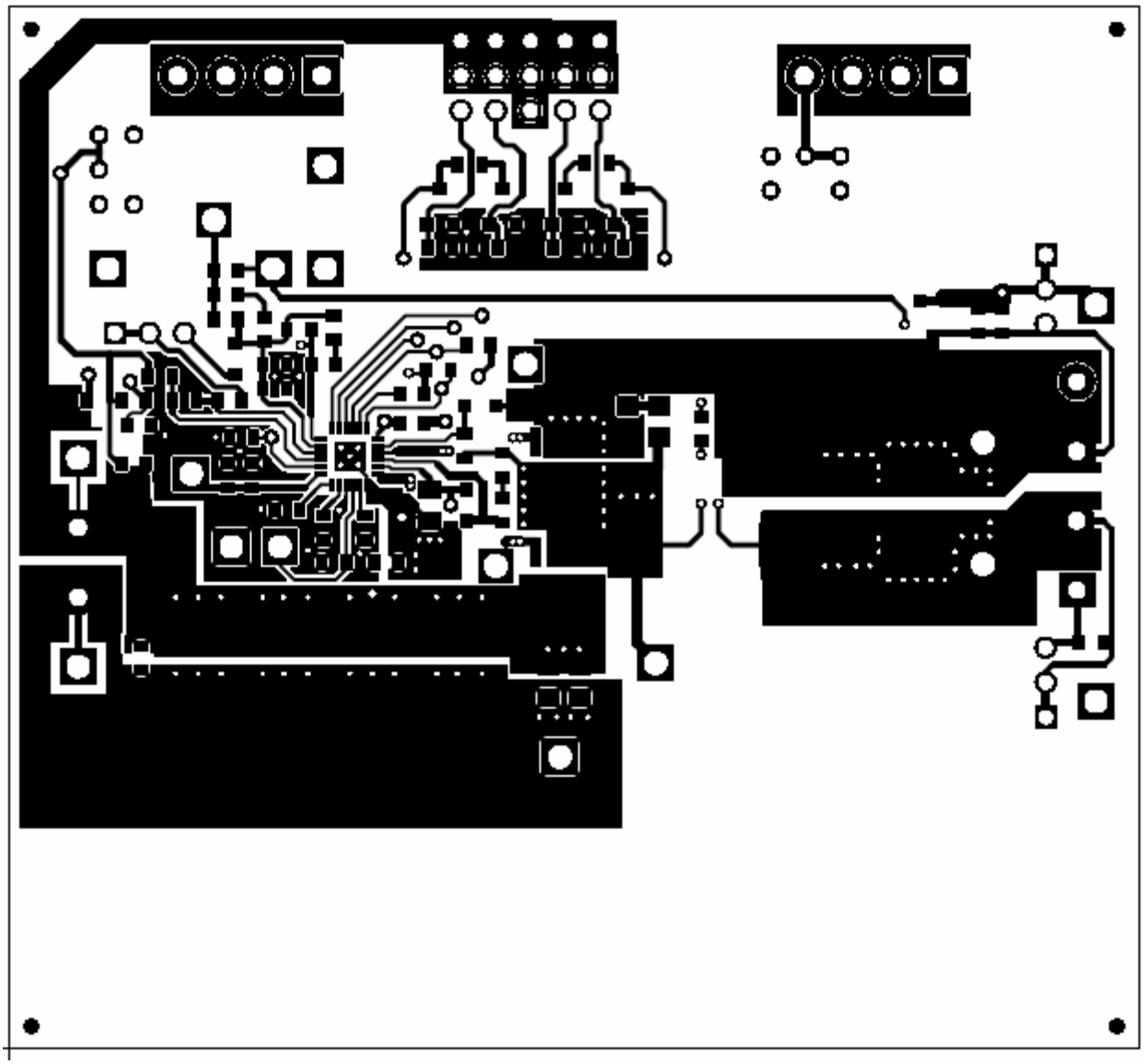

Figure 21: TPS40100EVM-001 Top Copper (Viewed from Top)

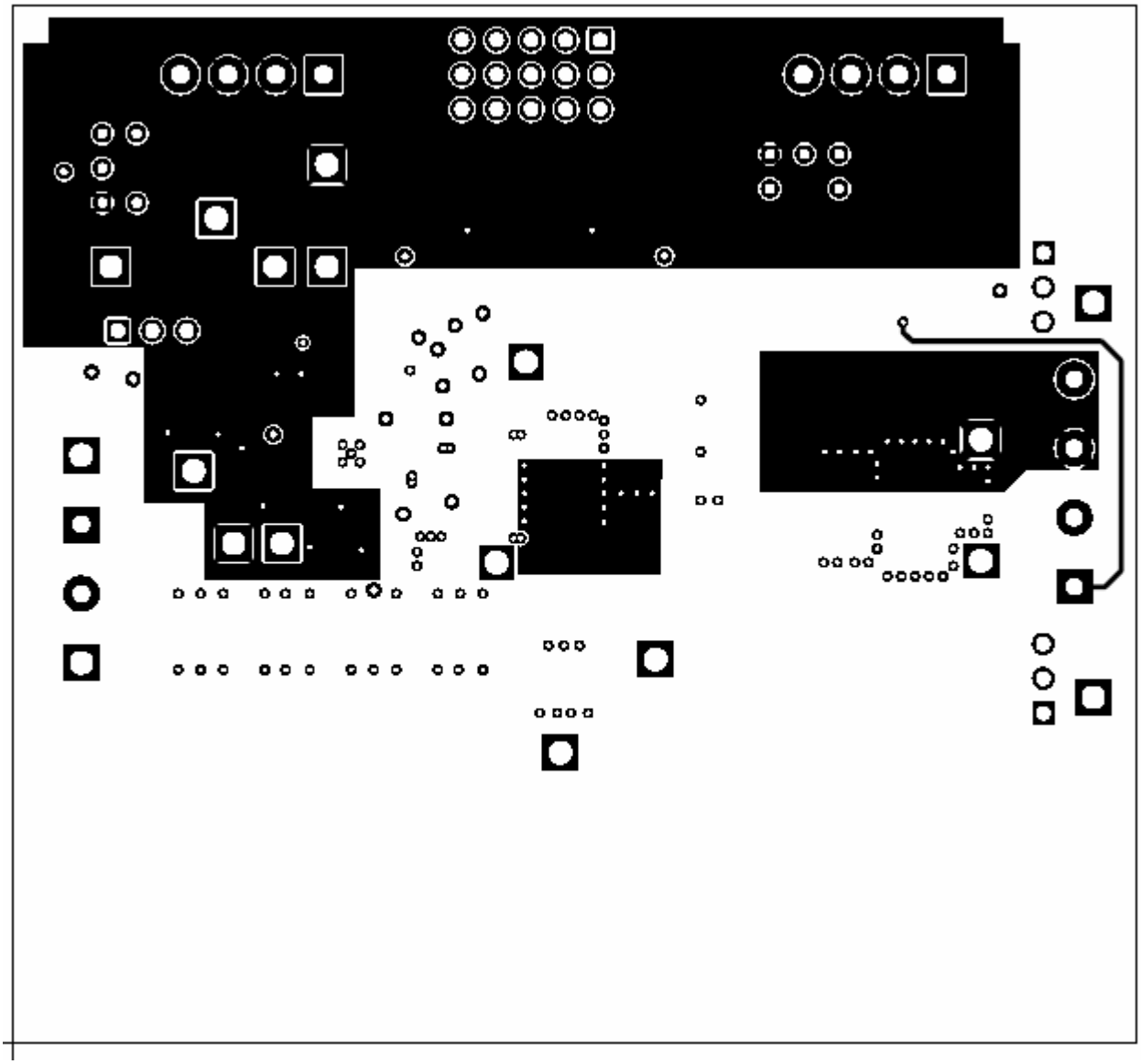

Figure 22: TPS40100EVM-001 Layer 2 (X-Ray View from Top)

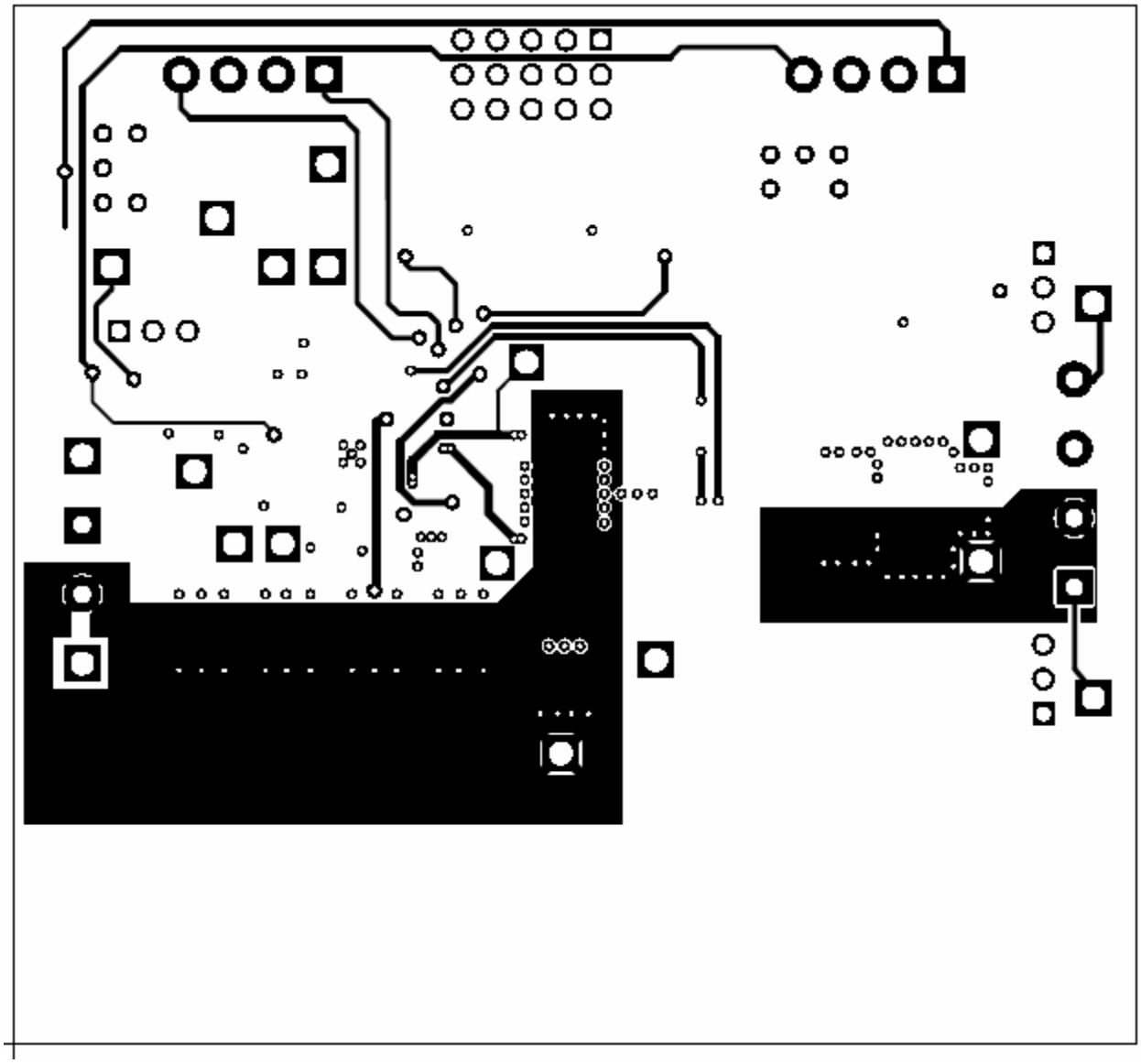

Figure 23: TPS40100EVM-001 Layer 3 (X-Ray View from Top)

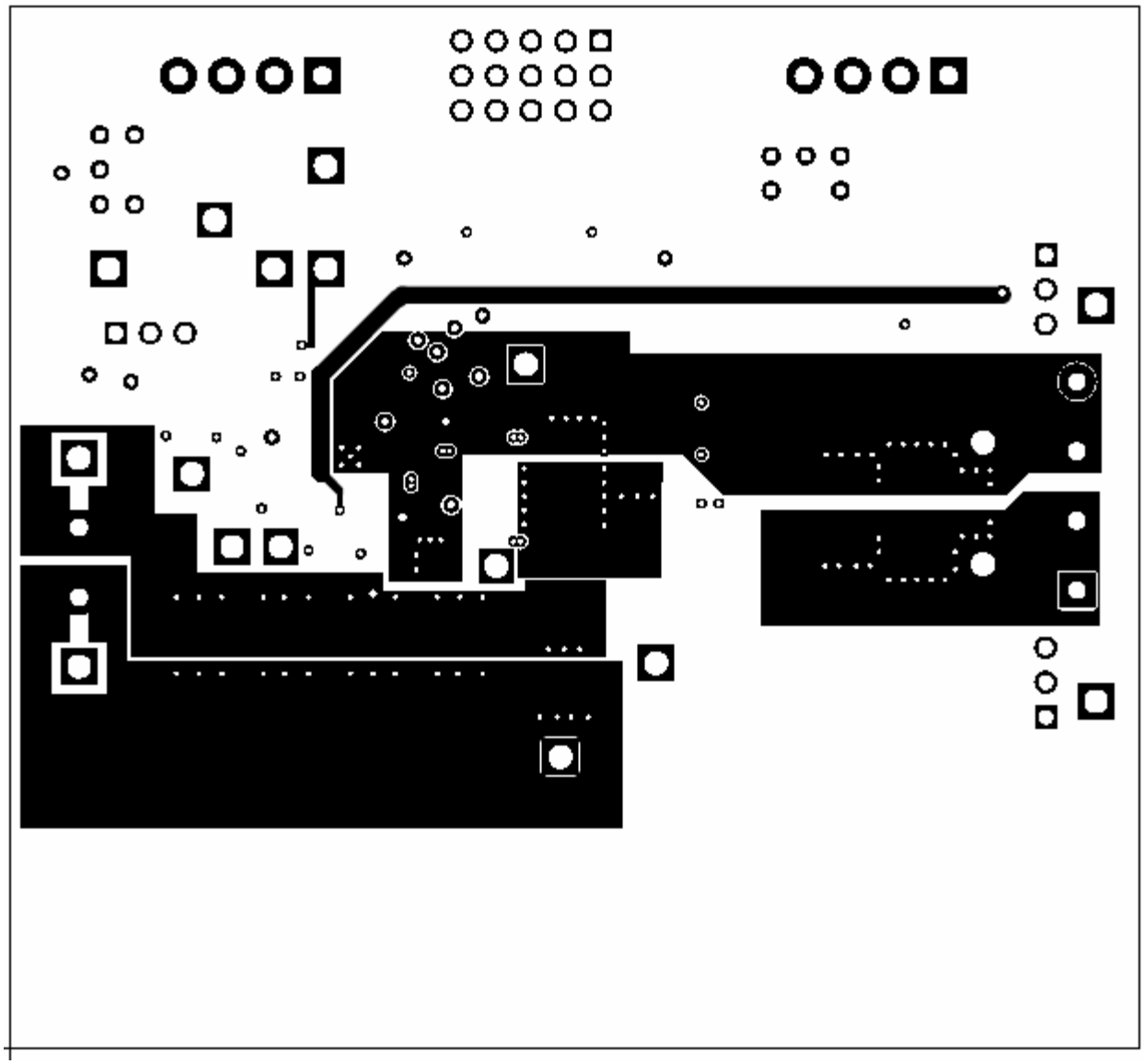

Figure 24: Bottom Copper (X-Ray View from Top)

8 LIST OF MATERIALS

Table 3 lists the EVM components as configured according to the schematic shown in Figure 1 and Figure 2.

Date: 05/03/2005

EVM BOM

COUNT	RefDes	Value	Description	Size	Part Number	MFR
5	C1, C11, C16, C18, C21	0.1uF	Capacitor, Ceramic, 0.1 uF, 50 V, X7R, 10%	0603	Std	Std
1	C10	560pF	Capacitor, Ceramic, 560 pF, 50V, X7R, 20%	0603	Std	Std
1	C12	1500pF	Capacitor, Ceramic, 1500 pF, 50 V, X7R, 10%	0603	Std	Std
1	C14	2.2uF	Capacitor, Ceramic, 2.2uF, 10V, X7R, 20%	0603	Std	Std
1	C15	2.2uF	Capacitor, Ceramic, 2.2 uF, 16 V, X7R, 20%	0805	C2012X7R1C225M	TDK
2	C17, C19	1.0uF	Capacitor, Ceramic, 1.0 uF, 25 V, X7R, 20%	0805	C2012X7R1E105M	TDK
4	C2, C3, C4, C5	22uF	Capacitor, Ceramic, 22 uF, 16V, X7R, 20%	2220	C5750X7R1C226M	TDK
1	C20	0.1uF	Capacitor, Ceramic, 0.1 uF, 6.3 V, X5R, 10%	0805	C2012X5R0J226K	TDK
1	C22	100uF	Capacitor, Ceramic, 100 uF, 6.3 V, X5R, 20%	1812	Std	Std
1	C24	1.0 uF	Capacitor, Ceramic, 1.0 uF, 50 V, X7R, 20%	0603	Std	Std
1	C25	1500pF	Capacitor, Ceramic, 1500 pF, 50 V, X7R, 10%	0805	Std	Std
1	C26	220uF	Capacitor, POSCAP, 220-uF, 10-V, 12-milliohm, 20%	7343(D)	10TPB220M	Sanyo
2	C6, C13	.068uF	Capacitor, Ceramic, 0.068 uF, 25 V, X7R, 10%	0603	Std	Std
1	C7	330pF	Capacitor, Ceramic, 330 pF, 50 V, X7R, 10%	0603	Std	Std
1	C8	10nF	Capacitor, Ceramic, 10 nF, 50V, X7R, 10%	0603	Std	Std
1	C9	270pF	Capacitor, Ceramic, 270 pF, 50V, X7R, 10%	0603	Std	Std
1	D1	1N4148SW	Diode, Switching, 75-V, 200-mA, 200-mW	SOD-323	1N4148WS-7	Diode Inc
1	D2	SDM10K45-7	Diode, Schottky, 200-mA, 45-V	SOD-	SDM10K45-7	Diodes Inc

1	D3	BAT54S	Diode, Dual Schottky, 200-mA, 30-V	SOT23	BAT54S	Zetex
1	D4	BAT54HT1	Diode, Schottky, 200-mA, 30-V	SOD323	BAT54HT1	On Semiconductor
2	J1, J3	ED1516	Terminal Block, 4-pin, 6-A, 3.5mm	0.55 x 0.25	ED1516	OST
1	J2	ED1609-ND	Terminal Block, 2-pin, 15-A, 5.1mm	0.40 x 0.35	ED1609	OST
1	J4		Header, 3x5-pin, 100mil spacing	0.100 x 5 X 3	STD	STD
1	J5		Terminal Block, 4-pin, 15-A, 5.1mm	0.80 x 0.35	ED2227	OST
3	J6, J7, J8		Header, 3-pin, 100mil spacing, (36-pin strip)	0.100 x 3	PTC36SAAN	Sullins
1	L1	1.8uH	Inductor, SMT, 1.8uH, 16A, 3.19 milliohms	0.512 x 0.550 inch	744318180/LF	Wurth Elektronik
0	**L1 (Second source only)**	**1.9uH**	**Inductor, SMT, 1.9uH, 20A, 3.00 milliohms**	**0.512 x 0.551 inch**	**PG0077.202**	**Pulse Engineering**
1	Q1	HAT2168H	Mosfet, N-Ch, Vds 30V, Rds 7.9 milliohms, Id 30A	LFPAK	HAT2168H	Hitachi
1	Q2	HAT2160H	Mosfet, N-Ch, Vds 20V, Rds 2.6 milliohms, Id 60A	LFPAK	HAT2160H	Hitachi
4	Q3, Q4, Q5, Q6	2N7002	MOSFET, N-ch, 60-V, 115-mA, 1.2-Ohms	SOT23	2N7002DICT	Vishay-Liteon
1	R1	12.4k	Resistor, Chip, 12.4kOhms, 1/16-W, 1%	0603	Std	Std
1	R10	42.2k	Resistor, Chip, 42.2k Ohms, 1/16-W, 1%	0603	Std	Std
1	R11	100	Resistor, Chip, 100ohms, 1/16-W, 1%	0603	Std	Std
1	R12	18.2k	Resistor, Chip, 18.2k Ohms, 1/16-W, 1%	0603	Std	Std
1	R13	274K	Resistor, Chip, 274k Ohms, 1/16-W, 1%	0603	Std	Std
1	R14	100k	Resistor, Chip, 100k Ohms, 1/16-W, 1%	0603	Std	Std
2	R15,R26	0	Resistor, Chip, 0 Ohms, 1/16-W, 1%	0603	Std	Std
1	R16	4.87k	Resistor, Chip, 4.87k Ohms, 1/16-W, 1%	0603	Std	Std
1	R17	49.9	Resistor, Chip, 49.9 Ohms, 1/16-W, 1%	0603	Std	Std

2	R18, R19	10	Resistor, Chip, 10.0 Ohms, 1/16-W, 1%	0603	Std	Std
1	R2	127k	Resistor, Chip, 127k Ohms, 1/16-W, 1%	0603	Std	Std
4	R20, R21, R23, R24	511k	Resistor, Chip, 511k Ohms, 1/16-W, 1%	0603	Std	Std
2	R22, R25	30.1k	Resistor, Chip, 30.1k Ohms, 1/16-W, 1%	0603	Std	Std
1	R27	2	Resistor, Chip, 2 Ohms, 1/10W, 1%	0805	Std	Std
1	R28	100	Resistor, Chip, 100-Ohms, 1/16-W, 1%	0603	Std	Std
1	R29	49.9k	Resistor, Chip, 49.9k-Ohms, 1/16-W, 1%	0603	Std	Std
1	R3	7.87k	Resistor, Chip, 7.87k Ohms, 1/16-W, 1%	0603	Std	Std
1	R4	105k	Resistor, Chip, 105k Ohms, 1/16-W, 1%	0603	Std	Std
1	R5	17.8k	Resistor, Chip, 17.8k Ohms, 1/16-W, 1%	0603	Std	Std
1	R6	1.62k	Resistor, Chip, 1.62k Ohms, 1/16-W, 1%	0603	Std	Std
1	R7	110k	Resistor, Chip, 110k Ohms, 1/16-W, 1%	0603	Std	Std
1	R8	15.0k	Resistor, Chip, 15.0k Ohms, 1/16-W, 1%	0603	Std	Std
1	R9	127k	Resistor, Chip, 127kOhms, 1/16-W, 1%	0603	Std	Std
2	S1, S2		Switch, ON-ON Mini Toggle **(Initial switch position closed shorting pins 1&2)**	0.28 x 0.18""	G12AP	NKK
5	TP1, TP2, TP4, TP12, TP14	5011	Test Point, Black, Thru Hole	0.125 x 0.125	5011	Keystone
2	TP3, TP13	5010	Test Point, Red, Thru Hole	0.125 x 0.125	5010	Keystone
1	--	(Remote Sense -)	Shunt, 100-mil, Black **(Initial Placement Across Pins 2,3 of J6)**	0.100	929950-00	3M
1	--	(Remote Sense +)	Shunt, 100-mil, Black **(Initial Placement Across Pins 2,3 of J7)**	0.100	929950-00	3M
1	--	(Tracking Enable)	Shunt, 100-mil, Black **(Initial Placement Across Pins 1,2 of J8)**	0.100	929950-01	3M

4	--	(Margin)	Shunt, 100-mil, Black **(Initial Placement Across Pins (1,2) (4,5) (7,8) (10,11) (13,14) of connector J4)**	0.100	929950-00	3M
11	TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP15, TP16, TP17, TP18	5012	Test Point, White, Thru Hole	0.125 x 0.125	5012	Keystone
1	U1	TPS40100RGE	IC, Midrange Input Synchronous Buck Controller	QFN-24	TPS40100RGE	TI
1	--		PCB, 3.25 In x 3.0 In x 0.062 In		EVM	Any

Notes:
1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

Table 3: TPS40100EVM-001 Bill of Materials