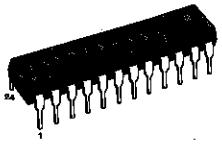
SGS-THOMSON MICROELECTRONICS

M74HCT646
M74HCT648

HCT646 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE)
HCT648 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE, INV.)

- HIGH SPEED
  f_{MAX} = 60 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.) V_{IL} = 0.8V (MAX)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS646/648



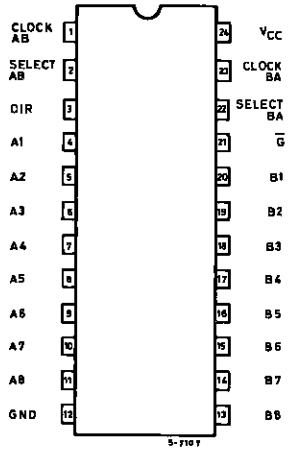
B1R
(Plastic Package)



M1R
(Micro Package)

ORDER CODES :
M74HCTXXXM1R M74HCTXXXB1R

PIN CONNECTIONS (top view)



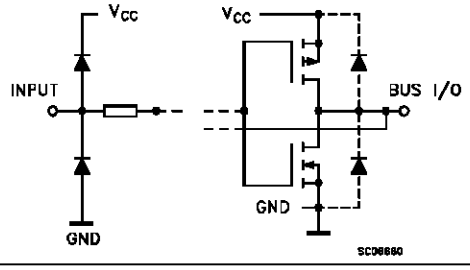
DESCRIPTION

The M74HCT646/648 are high speed CMOS OCTAL BUS TRANSCEIVERS AND REGISTERS, (3-STATE) fabricated in silicon gate C^2MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. These devices consist of bus transceiver circuits with 3-state output, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (Clock AB - or Clock BA). Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (Select AB select BA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode (enable $\overline{G}$ high), "A" data may be stored in one register and/or "B" data may be stored in the other register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. All inputs are equipped with protection circuits against static discharge and transient excess voltage.This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

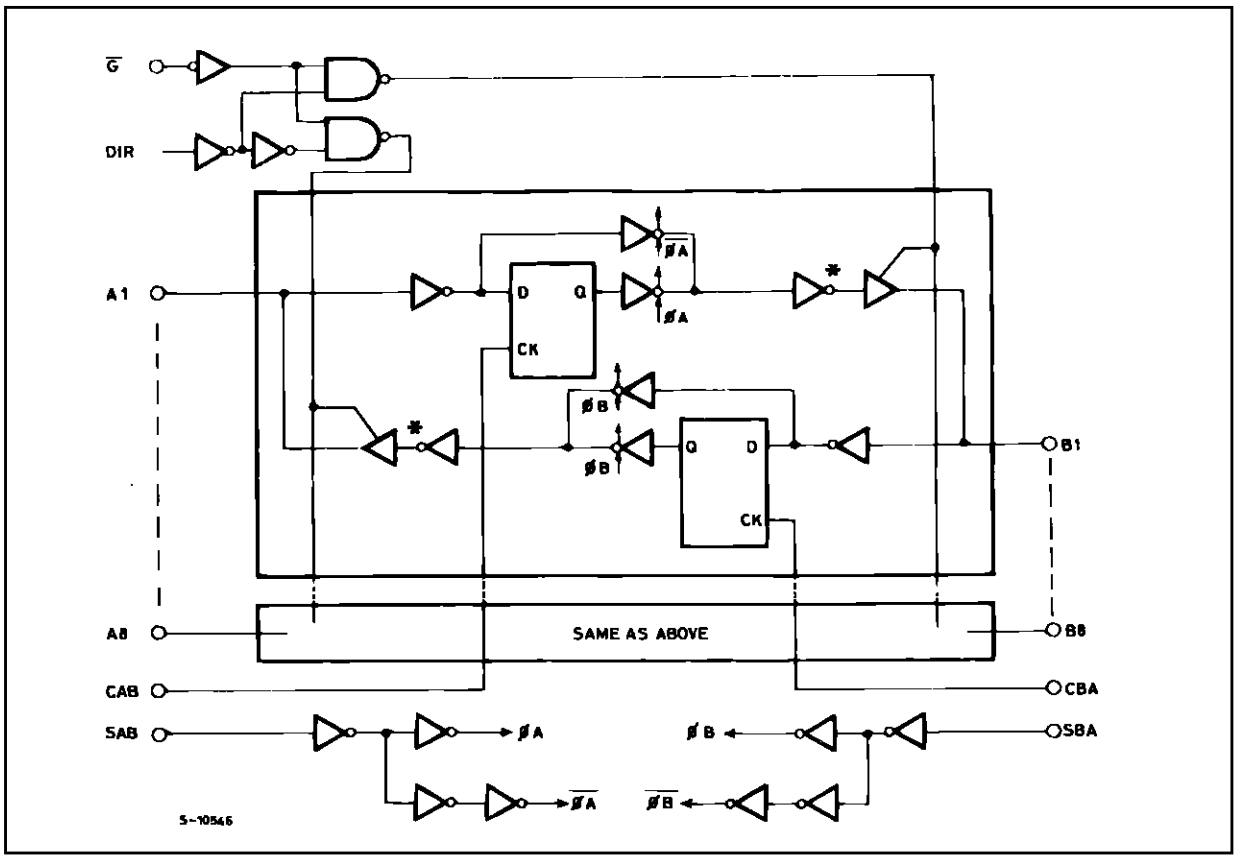
INPUT AND OUTPUT EQUIVALENT CIRCUIT

GAB, $\overline{GAB}$, CAB, SAB, SBA, CBA

A, B

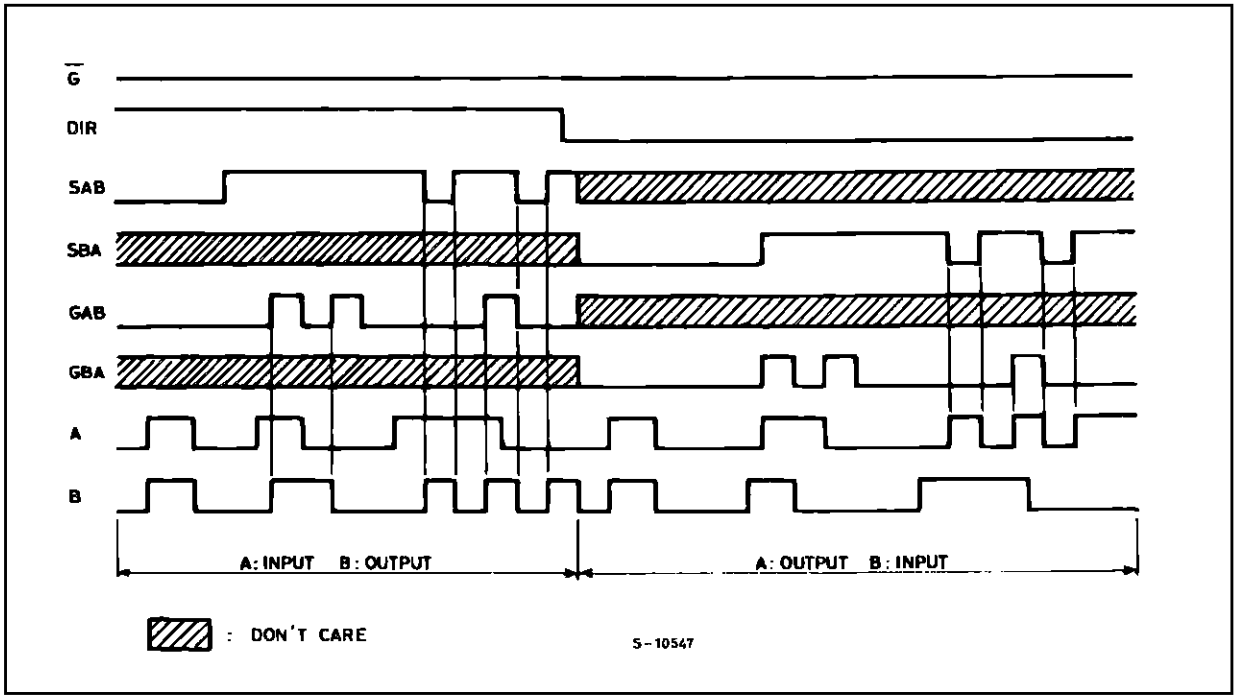


LOGIC DIAGRAM (HCT648)



Note : In case of M54/74HCT646 output inverter marked * at A bus and B bus are eliminated.

TIMING CHART



TRUTH TABLE

HCT646 (The truth table for HCT648 is the same as this, but with the outputs inverted)

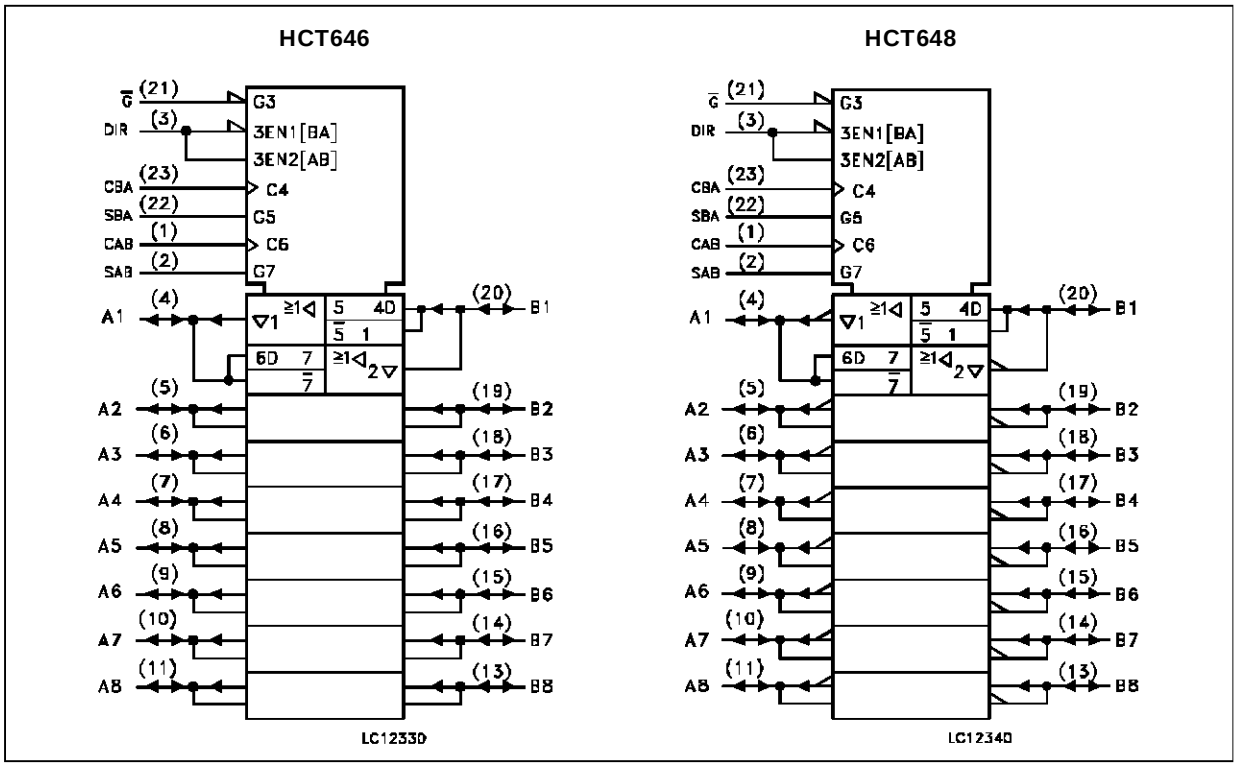
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A	B	FUNCTION
H	X					INPUTS	INPUTS	Both the A bus and the B bus are inputs
		X	X	X	X	Z	Z	The output functions of the A and B bus are disabled
		⌐	⌐	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs
L	H					iNPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs
		X	X*	L	X	L	L	The data at the A bus are displayed at the B bus
						H	H	
		⌐	X*	L	X	L	L	The data at the A bus are displayed at the B bus. The data of the A bus are stored to the internal flip-flop on low to high transition of th clock pulse.
						H	H	
		X	X*	H	X	X	Qn	The data stored to the internal flip-flop are dispayed at the B bus
		⌐	X*	H	X	L	L	The data at the A bus are stored to the internal flip-flop on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus
						H	H	
L	L					OUTPUTS	INPUTS	The A bus are outputs and the B bus are inputs
		X*	X	X	L	L	L	The data at the B bus are displayed at the A bus
						H	H	
		X*	⌐	X	L	L	L	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flop on low to high transition of the clock pulse
						H	H	
		X*	X	X	H	Qn	X	The data stored to the internal flip-flops are displayed at the B bus
		x*	⌐	X	H	L	L	the data at the B bus are stored to the internal flip-flop on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus
						H	H	

X : DON'T CARE
Z : HIGH IMPEDANCE
Qn : THE DATA STORED TO THE INTERNAL FLIP-FLOPS BY MOST RECENT LOW TO HIGH TRANSITION OF THE CLOCK INPUTS
* : THE DATA AT THE A AND B BUS WILL BE STORED TO THE INTERNAL FLIP-FLOPS ON EVERY LOW TO HIGH TRANSITION OF THE CLOCK INPUTS

PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	CLOCK AB	A to B Clock Input (LOW to HIGH, Edge-Trigged)
2	SELECT AB	Select A to B Source Input
3	DIR	Direction Control Input
4, 5, 6, 7, 8, 9, 10, 11	A1 to A8	A data Inputs/Outputs
20, 19, 18, 17, 16, 15, 14, 13	B1 to B8	B Data Inputs/Outputs
21	$\overline{G}$	Output Enable Input (Active LOW)
22	SELECT BA	Select B to A Source Input
23	CLOCK BA	B to A Clock Input (LOW to HIGH, Edge-Triggered)
12	GND	Ground (0V)
24	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-40 to +85	°C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)			T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		V
				I_O=-6.0 mA	4.18	4.31		4.13		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1	V
				I_O= 6.0 mA		0.17	0.26		0.33	
I_I	Input Leakage Current (*)	5.5	V_I = V_{CC} or GND				±0.1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40	µA
I_{OZ}	Output Off-state Current	5.5	V_O = V_{CC} or GND V_I = V_{IH} or V_{IL}				æ0.5		±5	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND I_O= 0				2.0		2.9	mA

(*): Applicable only to DIR, $\overline{G}$, CAB, CBA, SBA input.

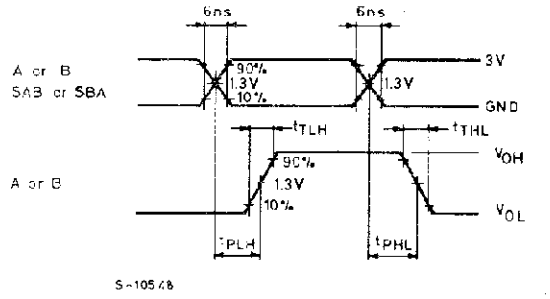
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		
					Min.	Typ.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5	50			7	12		15	ns
t_{PLH} t_{PHL}	Propagation Delay Time (BUS - BUS)	4.5	50			20	30		38	ns
		4.5	150			25	38		48	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - BUS)	4.5	50			29	44		55	ns
		4.5	150			34	52		65	ns
t_{PLH} t_{PHL}	Propagation Delay Time (SELECT - BUS)	4.5	50			24	34		43	ns
		4.5	150			29	42		53	ns
t_{PZL} t_{PZH}	3-State Output Enable Time ($\overline{G}$, DIR - BUS)	4.5	50	R_L = 1 KΩ		26	38		48	ns
		4.5	150	R_L = 1 KΩ		31	46		58	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time ($\overline{G}$, DIR - BUS)	4.5	50	R_L = 1 KΩ		26	35		44	ns
f_{MAX}	Maximum Clock Frequency	4.5	50		31	55		25		MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width	4.5	50			8	15		19	ns
t_s	Minimum Set-up Time	4.5	50			3	10		13	ns
t_h	Minimum Hold Time	4.5	50				5		5	ns
C_{IN}	Input Capacitance					5	10		10	pF
$C_{I/O}$	Bus Terminal Capacitance					13				pF
C_{PD} (*)	Power Dissipation Capacitance		for HCT646 for HCT648			40 39				pF

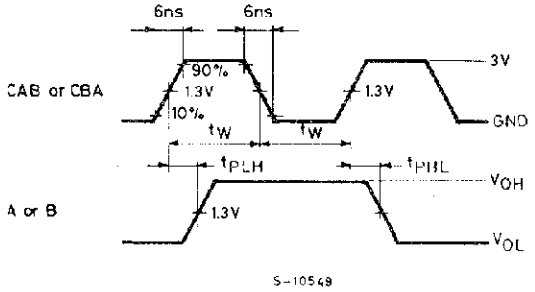
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/8$ (per bit)

SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM

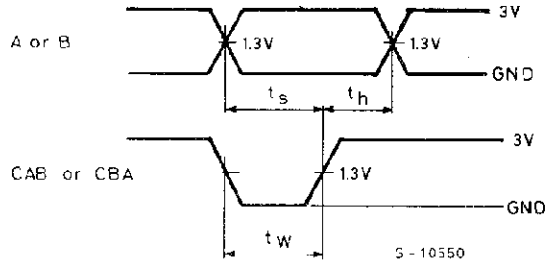
WAVEFORM 1



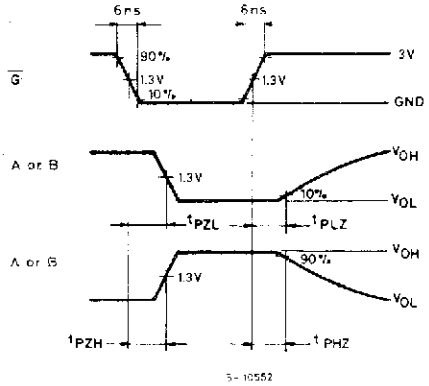
WAVEFORM 2



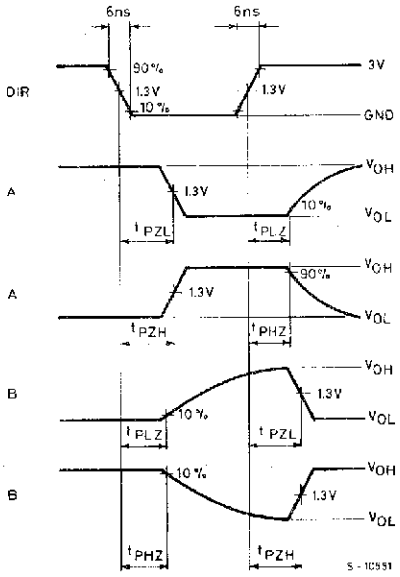
WAVEFORM 3



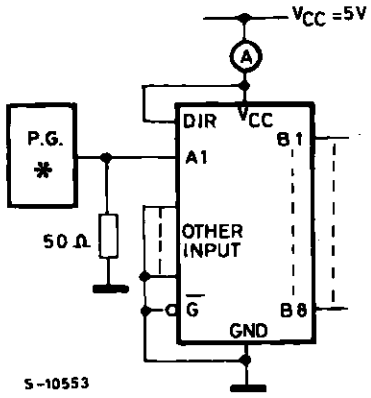
WAVEFORM 4



WAVEFORM 5



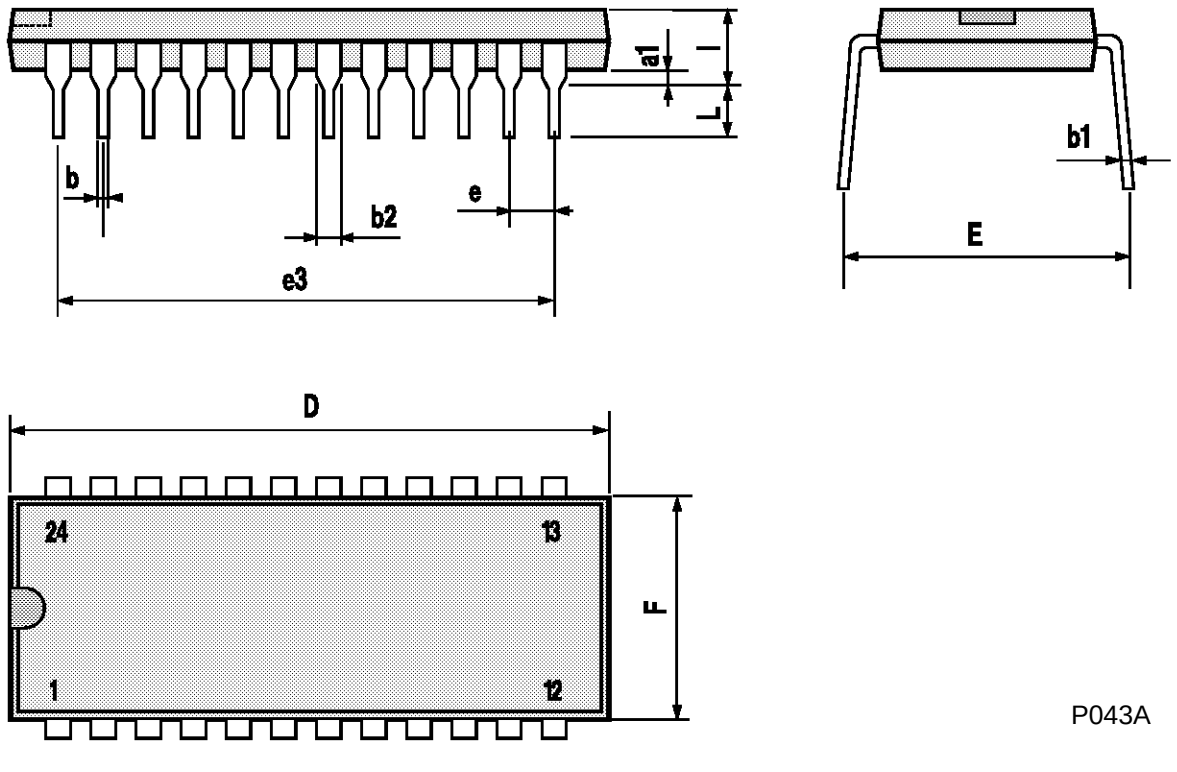
TEST WAVEFORM I_{CC} (Opr.)



* INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

Plastic DIP24 (0.25) MECHANICAL DATA

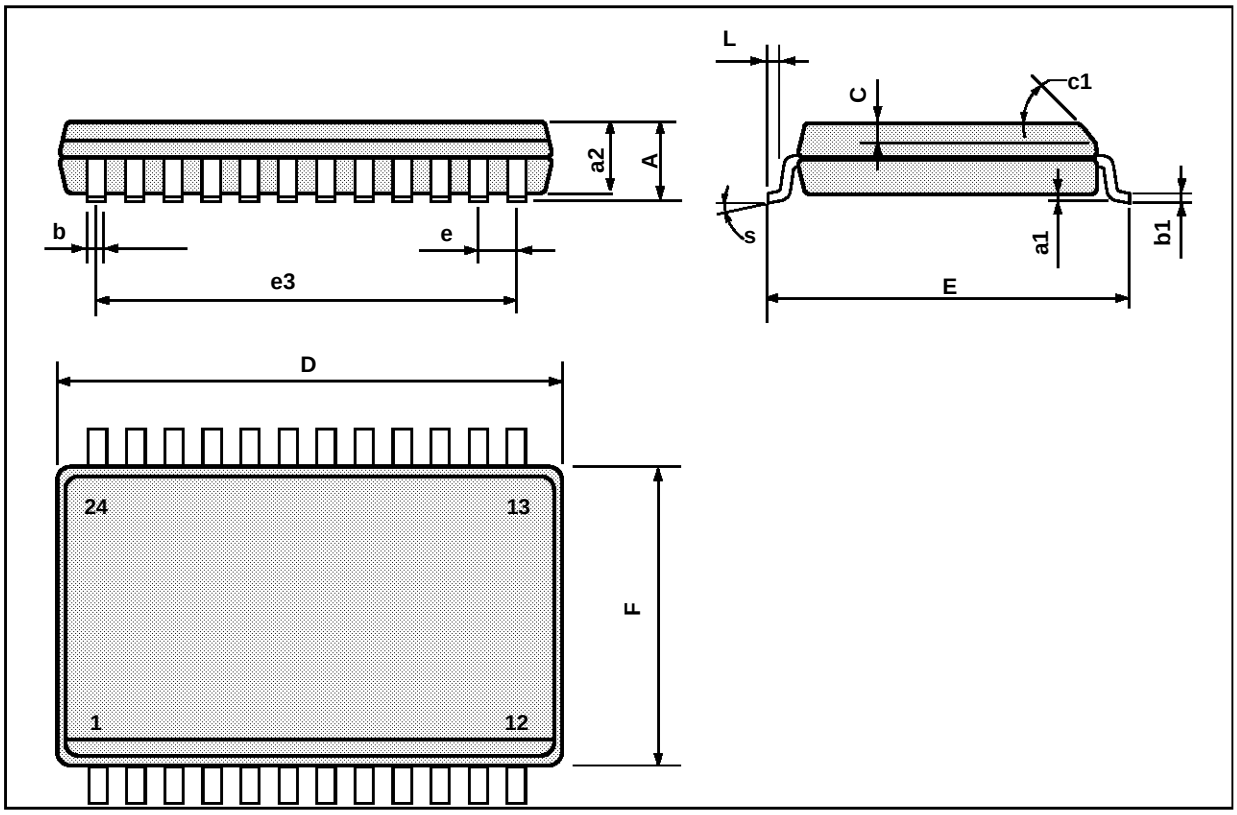
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	



P043A

SO24 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45° (typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.420
e		1.27			0.05	
e3		13.97			0.55	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
S	8° (max.)					



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