HI5702

August 1997

10-Bit, 40 MSPS A/D Converter

Features

- **Sampling Rate . . . . . 40 MSPS**
- **8.3 Bits Guaranteed at f_{IN} = 10MHz**
- **Low Power**
- **Wide Full Power Input Bandwidth 250MHz**
- **Sample and Hold Not Required**
- **Single-Ended or Differential Input**
- **Input Signal Range 1.25V**
- **Single Supply Voltage . . . . . +5V**
- **TTL Compatible Interface**

Applications

- **Professional Video Digitizing**
- **Medical Imaging**
- **Digital Communication Systems**
- **High Speed Data Acquisition**

Description

The HI5702 is a monolithic, 10-bit, analog-to-digital converter fabricated in a BiCMOS process. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 40 MSPS speed is made possible by a fully differential pipeline architecture which also eliminates the need for an external sample and hold circuit. The HI5702 has excellent dynamic performance while consuming <650mW power at 40 MSPS. Data output latches are provided which present valid data to the output bus with a latency of 7 clock cycles.

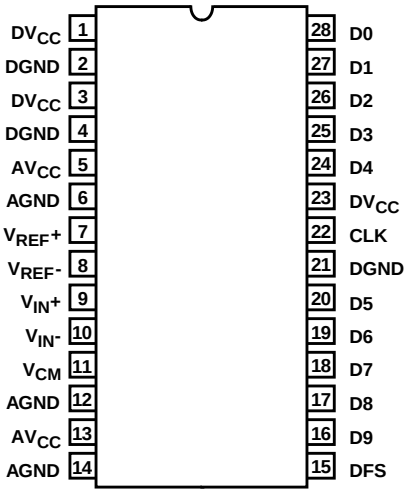
Refer to the HI5703, HI5746, or HI5767 data sheets for lower power consumption.

Ordering Information

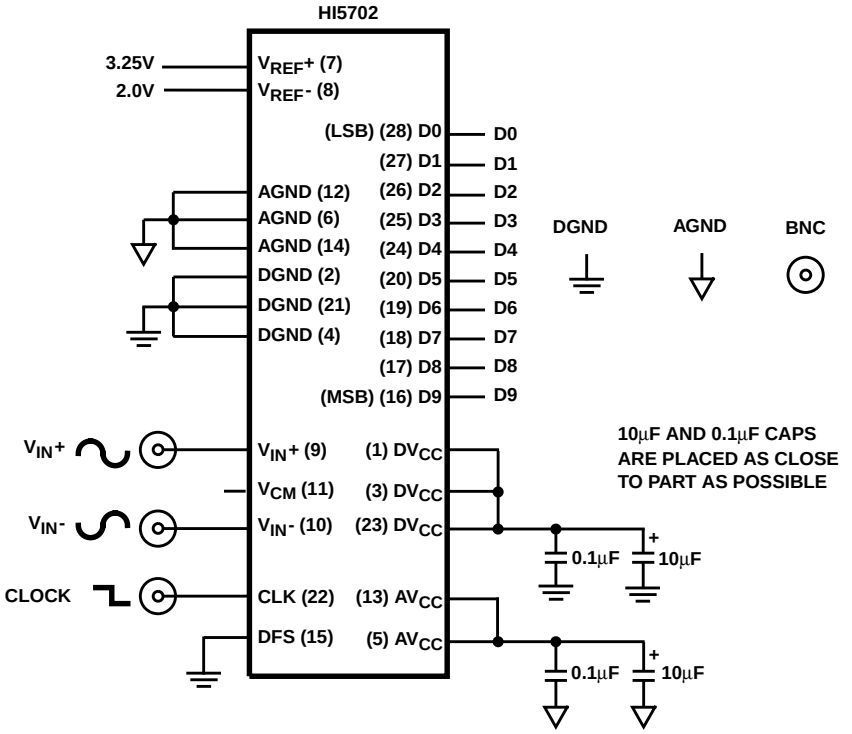
PART NUMBER	SAMPLE RATE	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI5702KCB	40 MSPS	0 to 70	28 Ld SOIC (W)	M28.3
HI5702JCB	36 MSPS	0 to 70	28 Ld SOIC (W)	M28.3
HI5702-EV2		25	Evaluation Board	

Pinout

HI5702
(SOIC)
TOP VIEW



Typical Application Schematic

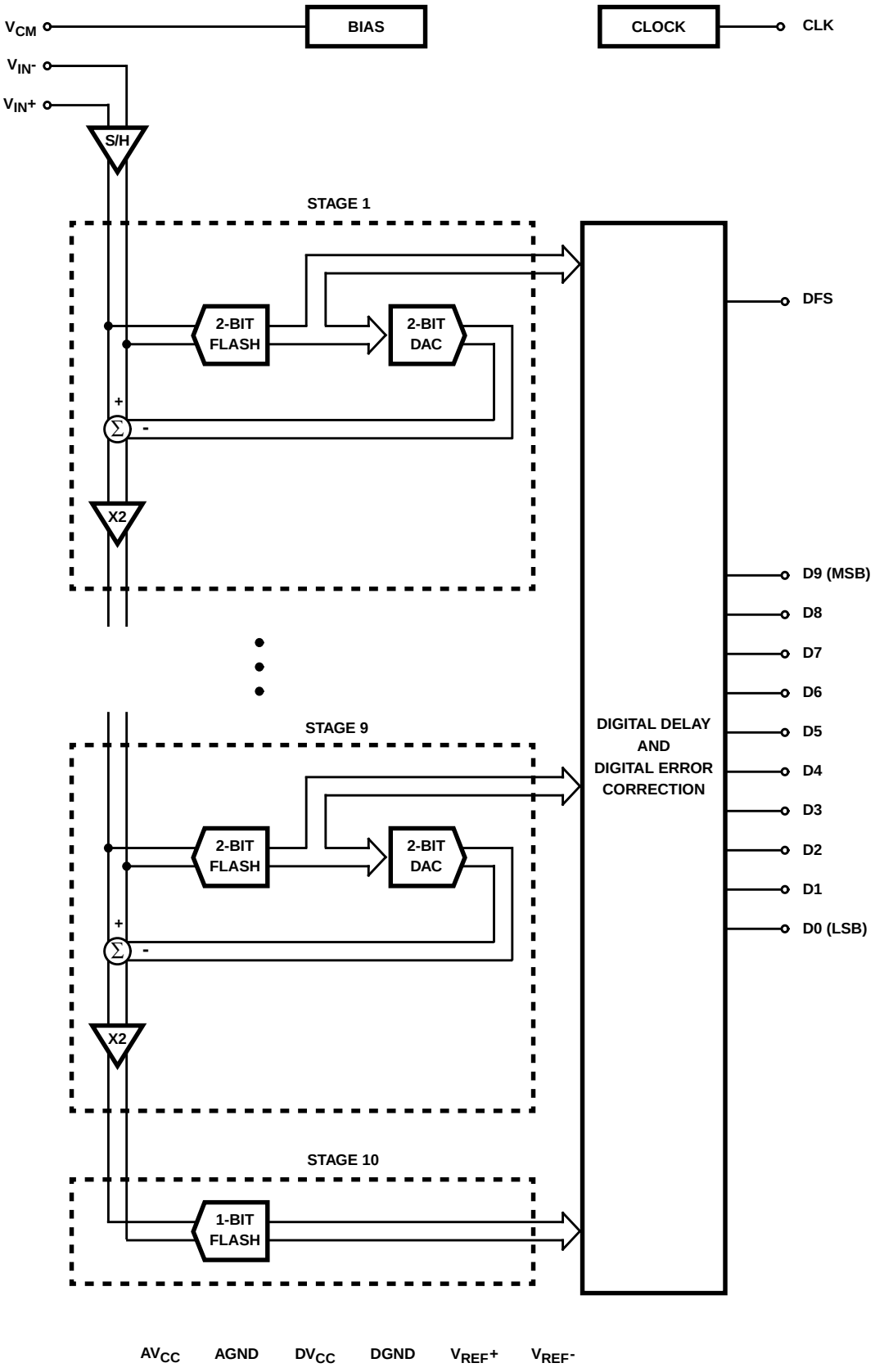


CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

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File Number **3745.4**

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage, AV_{CC} or DV_{CC} to AGND or DGND . . . . . +6V
DGND to AGND 0.3V
Digital I/O Pins . . . . . DGND to DV_{CC}
Analog I/O Pins. . . . . AGND to AV_{CC}

Operating Conditions

Temperature Range
HI5702KCB/JCB . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	70

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering, 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

9. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$AV_{CC} = DV_{CC} = +5V$; $V_{REF}+ = 3.25V$; $V_{REF}- = 2V$; f_S = Specified Clock Frequency at 50% Duty Cycle; $C_L = 20pF$; $T_A = 25^oC$; Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	f_{IN} = DC	-	±1	±2.0	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_{IN} = DC	-	±0.5	±1	LSB
Offset Error, V_{OS}	f_{IN} = DC	-	3	-	LSB
Full Scale Error, FSE	f_{IN} = DC	-	2	-	LSB
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes	-	0.5	-	MSPS
Maximum Conversion Rate	No Missing Codes HI5702KCB	40	-	-	MSPS
	HI5702JCB	36	-	-	MSPS
Effective Number of Bits, ENOB	f_{IN} = 1MHz	-	9.0	-	Bits
	f_{IN} = 5MHz	-	9.0	-	Bits
	f_{IN} = 10MHz	8.3	8.8	-	Bits
Signal to Noise and Distribution Ratio, SINAD $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_{IN} = 1MHz	-	57	-	dB
	f_{IN} = 5MHz	-	57	-	dB
	f_{IN} = 10MHz	51	56	-	dB
Signal to Noise Ratio, SNR $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_{IN} = 1MHz	-	56	-	dB
	f_{IN} = 5MHz	-	56	-	dB
	f_{IN} = 10MHz	51	55	-	dB
Total Harmonic Distortion, THD	f_{IN} = 1MHz	-	-64	-	dBc
	f_{IN} = 5MHz	-	-63	-	dBc
	f_{IN} = 10MHz	-	-60	-	dBc
2nd Harmonic Distortion	f_{IN} = 1MHz	-	-75	-	dBc
	f_{IN} = 5MHz	-	-75	-	dBc
	f_{IN} = 10MHz	-	-73	-	dBc
3rd Harmonic Distortion	f_{IN} = 1MHz	-	-66	-	dBc
	f_{IN} = 5MHz	-	-64	-	dBc
	f_{IN} = 10MHz	-	-63	-	dBc
Spurious Free Dynamic Range, SFDR	f_{IN} = 1MHz	-	66	-	dBc
	f_{IN} = 5MHz	-	64	-	dBc
	f_{IN} = 10MHz	54	63	-	dBc
Intermodulation Distortion, IMD	f_1 = 1MHz, f_2 = 1.02MHz	-	-59	-	dBc

Electrical Specifications $AV_{CC} = DV_{CC} = +5V$; $V_{REF}+ = 3.25V$; $V_{REF}- = 2V$; f_S = Specified Clock Frequency at 50% Duty Cycle; $C_L = 20pF$; $T_A = 25^oC$; Unless Otherwise Specified **(Continued)**

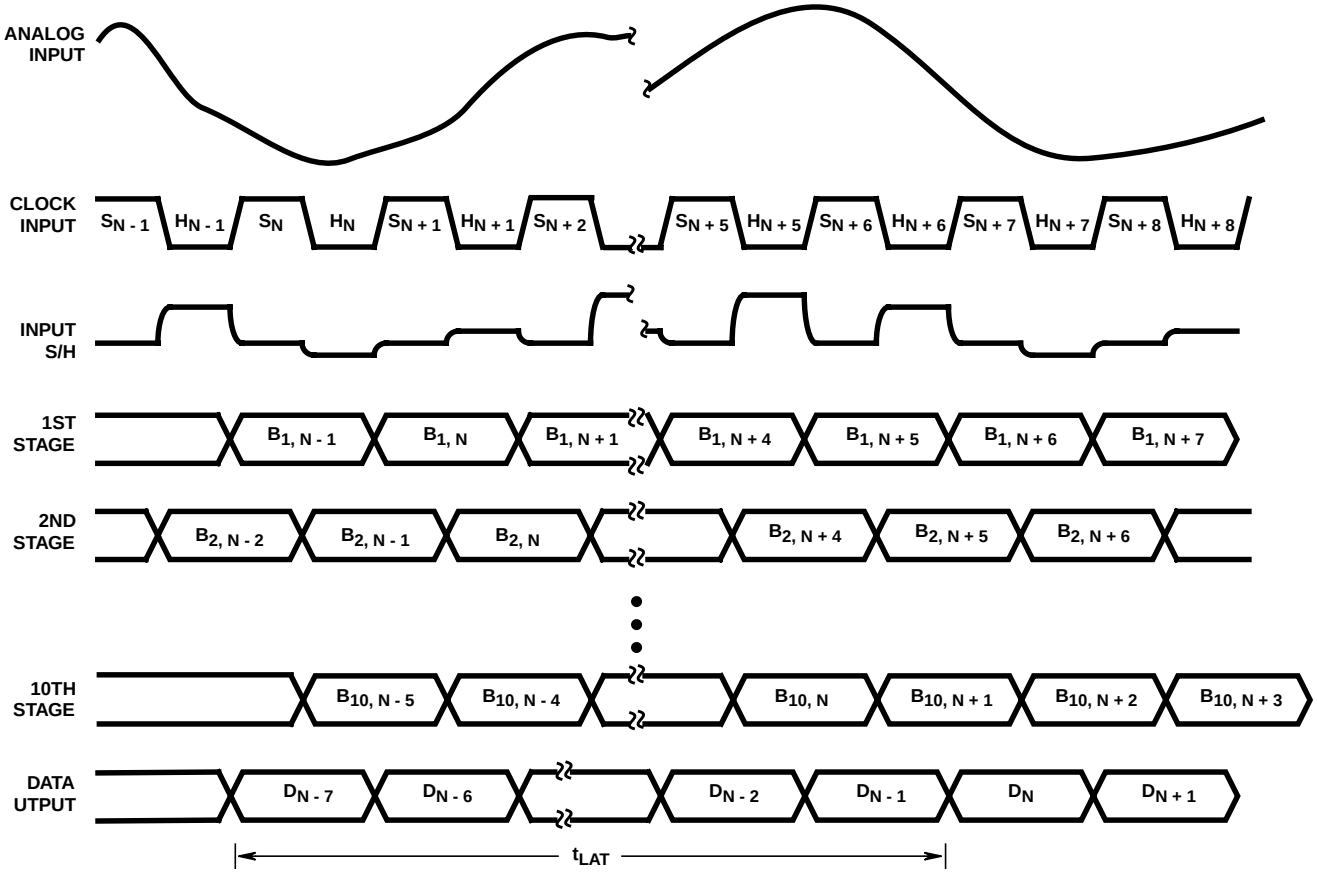
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Differential Gain Error	f_S = 17.72MHz, 6 Step, Mod Ramp	-	0.5	1	%
Differential Phase Error	f_S = 17.72MHz, 6 Step, Mod Ramp	-	0.25	0.5	Degree
Transient Response		-	1	-	Cycle
Overvoltage Recovery	0.2V Overdrive	-	1	-	Cycle
ANALOG INPUT					
Analog Input Resistance, R_{IN}	(Note 3)	-	1	-	MΩ
Analog Input Capacitance, C_{IN}		-	7	-	pF
Analog Input Bias Current, I_B	(Note 3)	-50	-	+50	µA
Full Power Input Bandwidth		-	250	-	MHz
Analog Input Common Mode Range $(V_{IN}+ + V_{IN}-) / 2$	Differential Mode (Note 2)	0.625	-	4.375	V
REFERENCE INPUT					
Total Reference Resistance, R_L		200	400	-	Ω
Reference Current		-	3	6	mA
Positive Reference Input, $V_{REF}+$	(Note 2)	-	3.25	3.3	V
Negative Reference Input, $V_{REF}-$	(Note 2)	1.95	2.0	-	V
Reference Common Mode Voltage $(V_{REF}+ + V_{REF}-) / 2$	(Note 2)	2.575	2.625	2.675	V
COMMOM MODE VOLTAGE					
Common Mode Voltage Output, V_{CM}		-	2.8	-	V
Max Output Current		-	-	1	mA
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic High Current, I_{IH}	V_{IN} = 5V	-	-	10.0	µA
Input Logic Low Current, I_{IL}	V_{IN} = 0V	-	-	10.0	µA
Input Capacitance, C_{IN}		-	7	-	pF
DIGITAL OUTPUTS					
Output Logic Sink Current, I_{OL}	V_O = 0.4V	3.2	-	-	mA
Output Logic Source Current, I_{OH}	V_O = 2.4V	-0.2	-	-	mA
Output Capacitance, C_{OUT}		-	5	-	pF
TIMING CHARACTERISTICS					
Aperture Delay, t_{AP}		-	5	-	ns
Aperture Jitter, t_{AJ}		-	5	-	ps
Data Output Delay, t_{OD}		-	6	-	ns
Data Output Hold, t_H		-	5	-	ns
Data Latency, t_{LAT}	For a Valid Sample (Note 2)	-	-	7	Cycles
Power-Up Initialization	Data Invalid Time (Note 2)	-	-	20	Cycles
POWER SUPPLY CHARACTERISTICS					
Supply Current, I_{CC}	V_{IN} = 0V	-	120	130	mA
Power Dissipation	V_{IN} = 0V	-	600	650	mW
Offset Error PSRR, ΔV_{OS}	AV_{CC} or DV_{CC} = 5V ±5%	-	0.2	-	LSB
Gain Error PSRR, ΔFSE	AV_{CC} or DV_{CC} = 5V ±5%	-	1	-	LSB

NOTES:

10. Parameter guaranteed by design or characterization and not production tested.

11. With the clock off.

Timing Waveforms



NOTES:

1. S_N: N-th sampling period.
2. H_N: N-th holding period.
3. $B_{M, N}$: M-th stage digital output corresponding to N-th sampled input.
4. D_N: Final data output corresponding to N-th sampled input.

FIGURE 8. HI5702 INTERNAL CIRCUIT TIMING

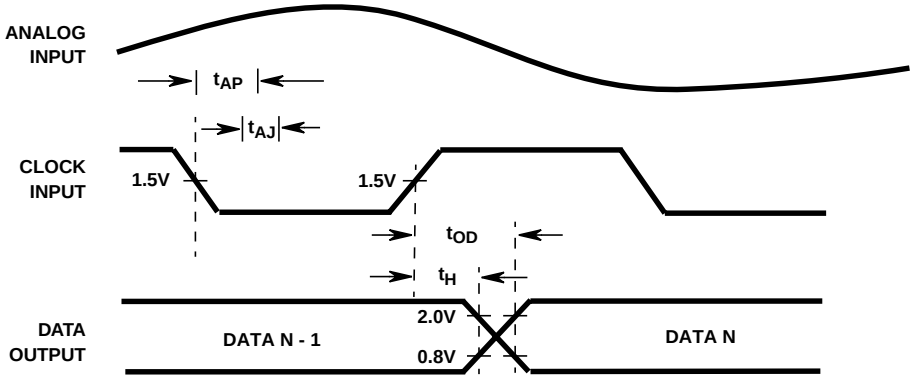


FIGURE 9. INPUT-TO-OUTPUT TIMING

Typical Performance Curves

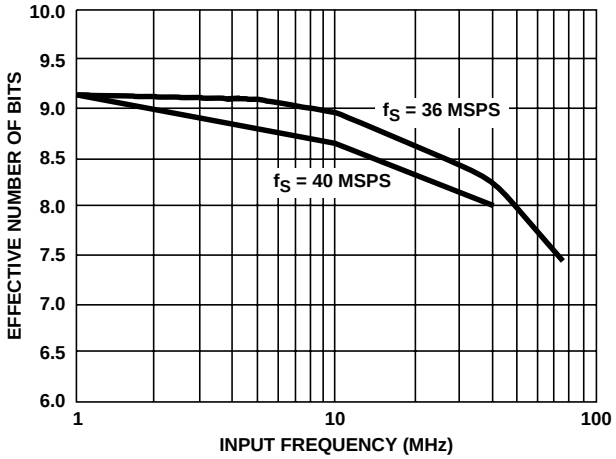


FIGURE 10. ENOB vs INPUT FREQUENCY

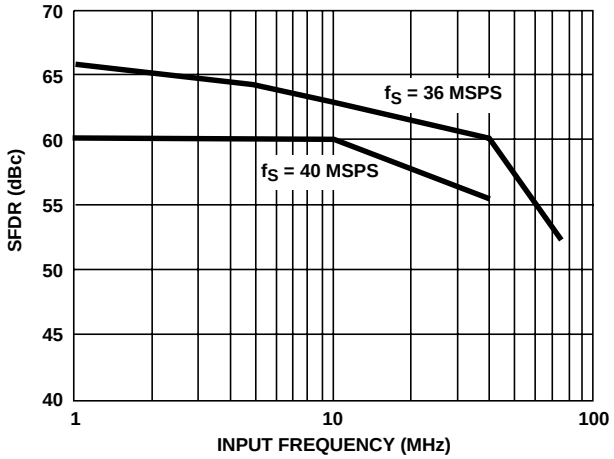


FIGURE 11. SFDR vs INPUT FREQUENCY

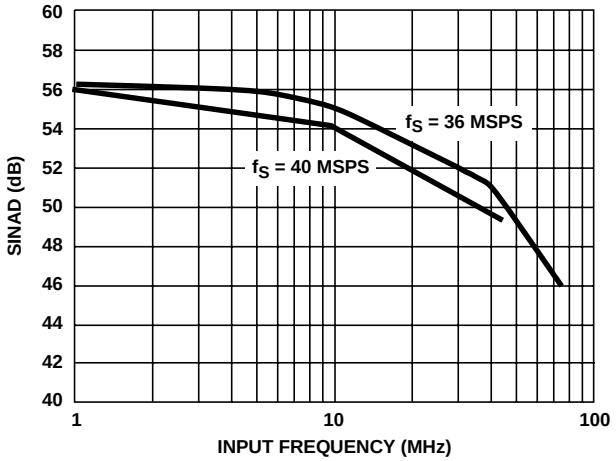


FIGURE 12. SINAD vs INPUT FREQUENCY

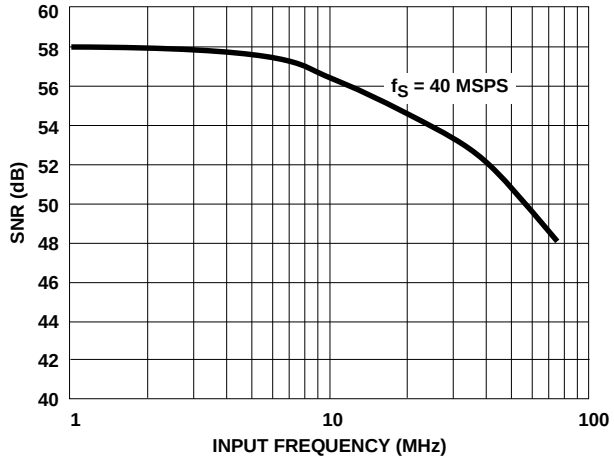


FIGURE 13. SNR vs INPUT FREQUENCY

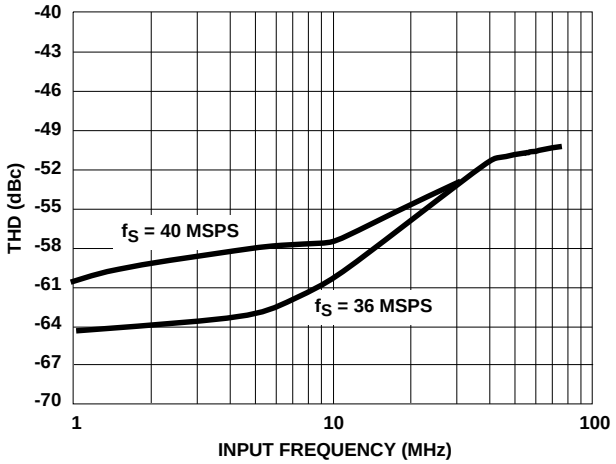


FIGURE 14. THD vs INPUT FREQUENCY

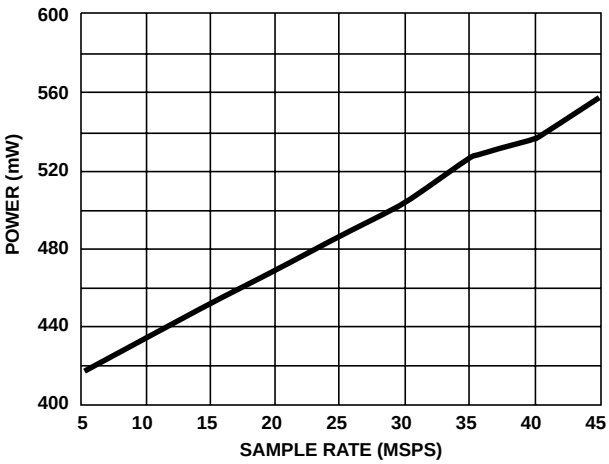


FIGURE 15. POWER DISSIPATION vs SAMPLE RATE

Typical Performance Curves (Continued)

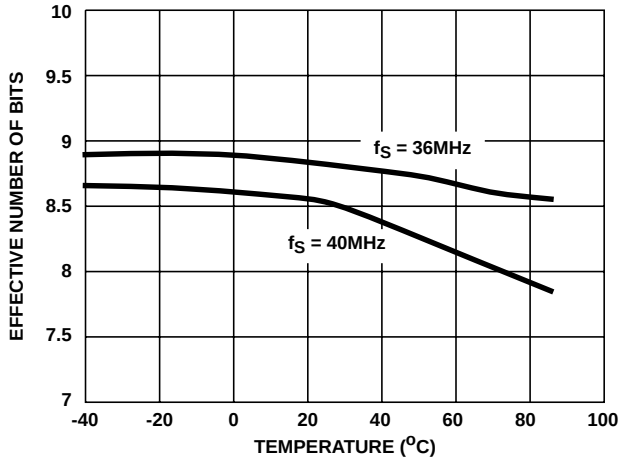


FIGURE 16. ENOB vs TEMPERATURE

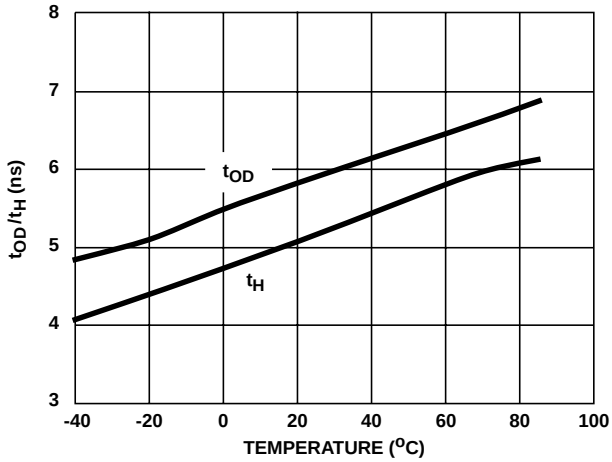


FIGURE 17. t_{OH}/t_D vs TEMPERATURE

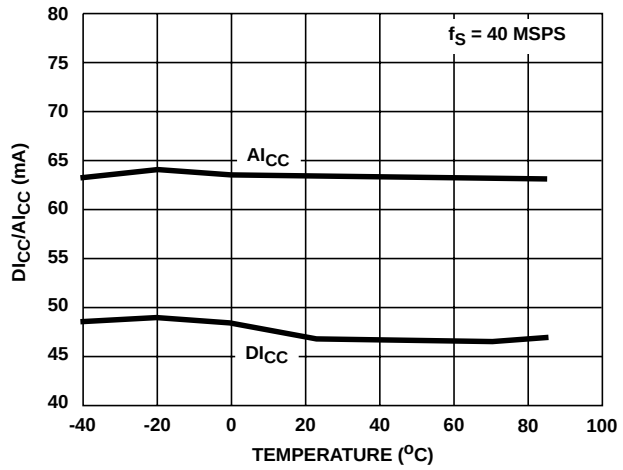


FIGURE 18. SUPPLY CURRENT vs TEMPERATURE

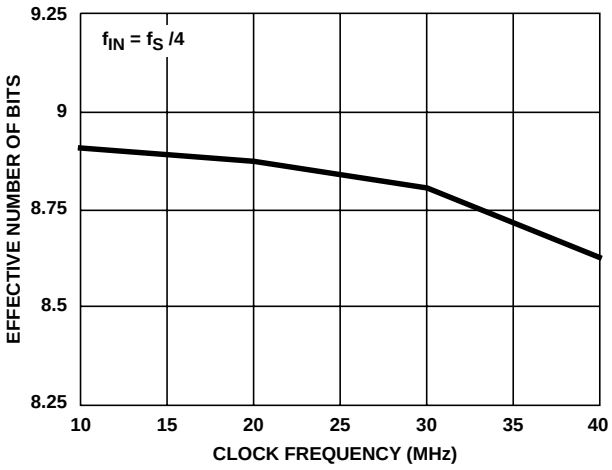


FIGURE 19. ENOB vs SAMPLE RATE WITH FIXED 12.5ns CLOCK PULSE WIDTH

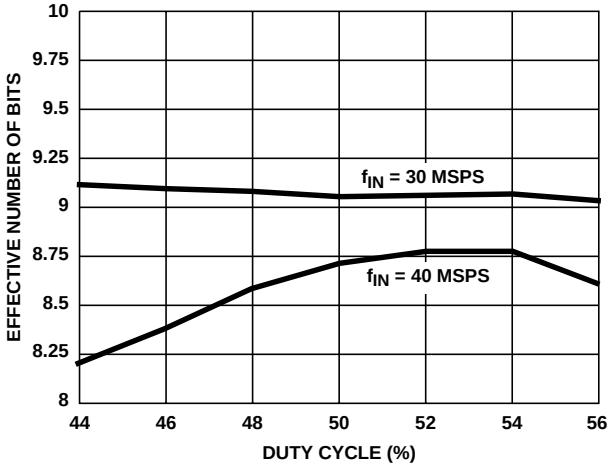


FIGURE 20. ENOB vs DUTY CYCLE

TABLE 1. PIN DESCRIPTIONS

PIN #	NAME	DESCRIPTION
1	DV_{CC}	Digital Supply.
2	DGND	Digital Ground.
3	DV_{CC}	Digital Supply.
4	DGND	Digital Ground.
5	AV_{CC}	Analog Supply.
6	AGND	Analog Ground.
7	$V_{REF}+$	Positive Reference.
8	$V_{REF}-$	Negative Reference.
9	$V_{IN}+$	Positive Analog Input.
10	$V_{IN}-$	Negative Analog Input.
11	V_{CM}	DC Output Voltage Source.
12	AGND	Analog Ground.
13	AV_{CC}	Analog Supply.
14	AGND	Analog Ground.
15	DFS	Data Format Select.
16	D9	Data Bit 9 Output (MSB).
17	D8	Data Bit 8 Output.
18	D7	Data Bit 7 Output.
19	D6	Data Bit 6 Output.
20	D5	Data Bit 5 Output.
21	DGND	Digital Ground.
22	CLK	Input Clock.
23	DV_{CC}	Digital Supply.
24	D4	Data Bit 4 Output.
25	D3	Data Bit 3 Output.
26	D2	Data Bit 2 Output.
27	D1	Data Bit 1 Output.
28	D0	Data Bit 0 Output (LSB).

Detailed Description

Theory of Operation

The HI5702 is a 10-bit fully differential sampling pipeline A/D converter with digital error correction. Figure 13 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal clock which is a non-overlapping two phase signal, ϕ_1 and ϕ_2, derived from the master clock. During the sampling phase, ϕ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of ϕ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, ϕ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op-amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of a switch and C_S. The small values of these components result in a typical full power bandwidth of 250MHz.

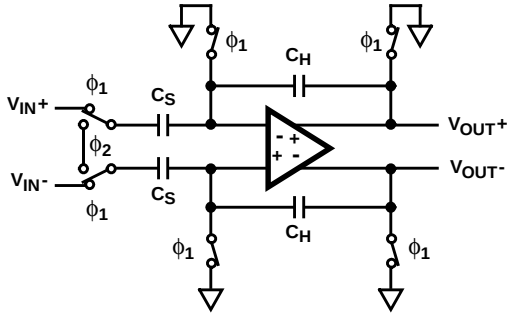


FIGURE 21. ANALOG INPUT SAMPLE-AND-HOLD

As illustrated in the Functional Block Diagram and the Timing Diagram in Figure 1, nine identical pipeline subconverter stages, each containing a two-bit flash and a two-bit multiplying digital-to-analog converter, follow the S/H circuit with the tenth stage being a one bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual sub-converter clock signal is offset by 180 degrees from the previous stage clock signal with the result that alternate stages in the pipeline will perform the same operation.

The two-bit digital output of each stage is fed to a digital delay line controlled by the internal clock. The purpose of the delay line is to align the digital output data to the corresponding sampled analog input signal. This delayed data is fed to the digital error correction circuit which corrects the error in the output data with the information contained in the redundant bits to form the final 10-bit output for the converter.

Because of the pipeline nature of this converter, the data on the bus is output at the 7th cycle of the clock after the analog sample is taken. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The output data is synchronized to the external clock by a double buffered latching technique.

The output of the digital correction circuit is available in two's complement or binary format depending on the condition of the Data Format Select (DFS) input.

Analog Input, Differential Connection

The analog input to the HI5702 is a differential input that can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (Figure 15) will give the best performance for the converter.

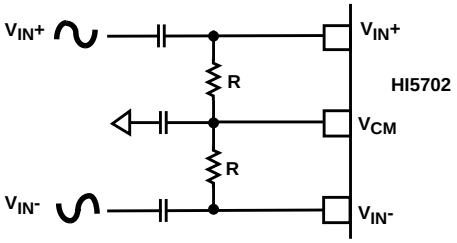


FIGURE 22. AC COUPLED DIFFERENTIAL INPUT

Since the HI5702 is powered by a single +5V analog supply, the analog input is limited to be between ground and +5V, which implies the common mode voltage can range of 0.625V to 4.375V. The performance of the ADC does not change significantly with the value of the common mode voltage.

A DC voltage source, V_{CM}, about half way between the top and bottom reference voltages, is made available to the user to help simplify circuit design when using a differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent bias source and stays within the common mode range over temperature. It has a temperature coefficient of about 200ppm.

Assume the difference between $V_{REF}+$, typically 3.25V, and $V_{REF}-$, typically 2V, is 1.25V in Figure 15. Fullscale is achieved when $V_{IN}+$ and $V_{IN}-$ inputs are $1.25V_{P-P}$, with $V_{IN}-$ being 180 degrees out of phase with $V_{IN}+$. The converter will be at positive fullscale when the $V_{IN}+$ input is at V_{CM} + 0.625V and $V_{IN}-$ is at V_{CM} - 0.625V ($V_{IN}+ - V_{IN}- = 1.25V$). Conversely, the ADC will be at negative fullscale when the $V_{IN}+$ input is equal to V_{CM} - 0.625V and $V_{IN}-$ is at V_{CM} + 0.625V ($V_{IN}+ - V_{IN}- = -1.25V$).

The analog input can be DC coupled as long as the inputs are within the common mode range, Figure 16.

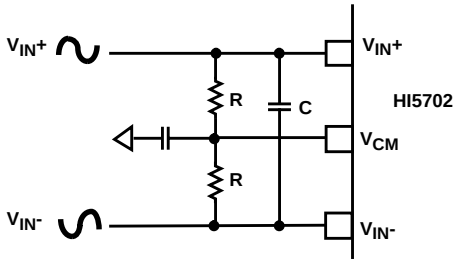


FIGURE 23. DC COUPLED DIFFERENTIAL INPUT

The resistors, R, in Figure 16 are not absolutely necessary but will improve performance. Values of 100Ω or less are typical. A capacitor, C, connected from $V_{IN}+$ to $V_{IN}-$ will help common mode any noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well.

Analog Input, Single-Ended Connection

The configuration shown in Figure 17 may be used with a single ended AC coupled input.

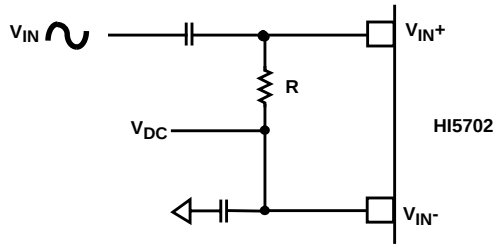


FIGURE 24. AC COUPLED SINGLE ENDED INPUT

Sufficient headroom must be provided such that the input voltage never goes above +5V or below AGND.

Again, assume the difference between $V_{REF}+$, typically 3.25V, and $V_{REF}-$, typically 2V, is 1.25V. If V_{IN} is a $2.5V_{P-P}$ sinewave riding on a positive voltage equal to V_{DC}, the converter will be at positive fullscale when $V_{IN}+$ is at V_{DC} + 1.25V and will be at negative fullscale when V_{IN} is equal to V_{DC} - 1.25V. In this case, V_{DC} could range between 1.25V and 3.75V without a significant change in ADC performance. The simplest way to produce V_{DC} is to use the V_{CM} output of the HI5702.

The analog input can be DC coupled as long as the input is within the common mode range, Figure 18.

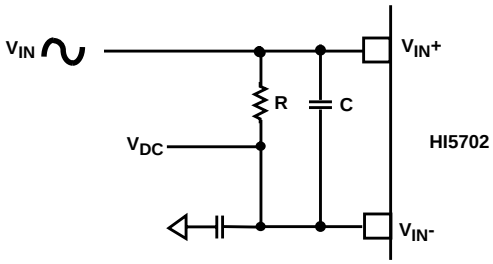


FIGURE 25. DC COUPLED SINGLE ENDED INPUT

The resistor, R, in Figure 18 is not absolutely necessary but will improve performance. Values of 100Ω or less are typical. A capacitor, C, connected from $V_{IN}+$ to $V_{IN}-$ will help common mode any noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well.

A single ended source may give better overall system performance if it is first converted to differential before driving the HI5702. Also refer to the application note AN9413, “Driving the Analog Input of the HI5702”. This application note describes several different ways of driving the analog differential inputs.

Reference Input, $V_{REF}-$ $V_{REF}+$

The converter requires two reference voltages connected to the V_{REF} pins. The voltage range of the part with a differential input will be $V_{REF}+ - V_{REF}-$. The HI5702 is tested with $V_{REF}-$ equal to 2V and $V_{REF}+$ equal to 3.25V for an input range of 1.25V. $V_{REF}+$ and $V_{REF}-$ can differ from the above voltages as long as the common mode voltage between the reference pins (($V_{REF}+ + V_{REF}-$) / 2) does not exceed 2.65V ±50mV and the limits on $V_{REF}+$ and $V_{REF}-$ are not exceeded.

In order to minimize overall converter noise it is recommended that adequate high frequency decoupling be provided at the reference input pin.

Digital Control and Clock Requirements

The HI5702 provides a standard high-speed interface to external TTL logic families.

In order to ensure rated performance of the HI5702, the duty cycle of the clock should be held at 50%. It must also have low jitter and operate at standard TTL levels.

A Data Format Select (DFS) pin is provided which will determine the format of the digital data. When at logic low the data will be output in offset binary format. When at a logic high the data will be output in a two’s complement format. Refer to Table 2 for further information.

Performance of the HI5702 will only be guaranteed at conversion rates above 1 MSPS. This ensures proper performance of the internal dynamic circuits. Similarly, when power is first applied to the converter, a maximum of 20 cycles at a sample rate above 1 MSPS will have to be performed before valid data is available.

Supply and Ground Considerations

The HI5702 has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds. For best performance, the supplies to the HI5702 should be driven by clean, linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the converter. If the part is powered off a single supply then the analog supply and ground pins should be isolated by ferrite beads from the digital supply and ground pins.

Refer to the Application Note “Using Intersil High Speed A/D Converters” (AN9214) for additional considerations when using high speed converters.

Increased Accuracy

The V_{OS} and FSE errors as reported on the data sheet can be decreased by further calibration of the ADC. It will be assumed that the converter has offset binary coding. See the A/D code table (Table 2) for the ideal code transitions.

The first step would be to center the analog input to the desired midscale voltage. This voltage would then be adjusted up or down in the circuitry driving one side of the input to the HI5702 until the 511 to 512 transition occurs on the digital output.

Next, set the analog input to the HI5702 to the desired positive fullscale voltage. Adjust one side of the reference circuit up or down until the 1022 to 1023 transition occurs on the digital output of the converter.

Static Performance Definitions

Offset Error (V_{OS})

The midscale code transition should occur at a level $^1/_4$ LSB above half-scale. Offset is defined as the deviation of the actual code transition from this point.

Full-Scale Error (FSE)

The last code transition should occur for a analog input that is $1^3/_4$ LSBs below positive full-scale with the offset error removed. Full-scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Rejection Ratio (PSRR)

Each of the power supplies are moved plus and minus 5% and the shift in the offset and gain error (in LSBs) is noted.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5702. A low distortion sine wave is applied to the input, it is coherently sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with an FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full-scale for all these tests.

SNR and SINAD are quoted in dB. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

TABLE 2. A/D CODE TABLE

CODE DESCRIPTION	(NOTE 1) DIFFERENTIAL INPUT VOLTAGE $V_{REF}+ = 3.25V$ $V_{REF}- = 2.0V$ (V)	OFFSET BINARY OUTPUT CODE (DFS LOW)										TWO'S COMPLEMENT OUTPUT CODE (DFS HIGH)									
		MSB									LSB	MSB									LSB
		D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Full Scale (FS)	1.25V	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
FS - $1^3/_4$ LSB	1.2479V	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0
$^1/_2$ FS + $^1/_4$ LSB	0.3mV	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$^1/_2$ FS - $^3/_4$ LSB	2.1mV	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$1^1/_4$ LSB	-1.2485V	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1
Zero	-1.25V	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

NOTE:

1. The voltages listed above represent the ideal transition of each output code shown as a function of the reference voltage.

Signal-to-Noise Ratio (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number of Bits (ENOB)

The effective number of bits (ENOB) is calculated from the SINAD data by

$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02$

where: $V_{CORR} = 0.5dB$

V_{CORR} adjusts the ENOB for the amount the input is below fullscale.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the fundamental input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the applicable harmonic component to the RMS value of the fundamental input signal.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f_1 and f_2, are present on the inputs. The ratio of the measured signal to the distortion terms is calculated. The terms included in the calculation are $(f_1 + f_2)$, $(f_1 - f_2)$, $(2f_1)$, $(2f_2)$, $(2f_1 + f_2)$, $(2f_1 - f_2)$, $(f_1 + 2f_2)$, $(f_1 - 2f_2)$. The ADC is tested with each tone 6dB below full scale.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component in the spectrum below $f_S/2$.

Transient Response

Transient response is measured by providing a full scale transition to the analog input of the ADC and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Overvoltage Recovery

Overvoltage Recovery is measured by providing a full scale transition to the analog input of the ADC which overdrives the input by 200mV, and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Full Power Input Bandwidth (FPBW)

Full power bandwidth is the frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Video Definitions

Differential gain and Differential Phase are two commonly found video specifications for characterizing the distortion of a chrominance (3.58MHz) signal as it is offset through the input voltage range of an ADC.

Differential Gain (DG)

Differential Gain is the peak difference in chrominance amplitude (in percent) at two different DC levels.

Differential Phase (DP)

Differential Phase is the peak difference in chrominance phase (in degrees) at two different DC levels.

Timing Definitions

Refer to Figure 1 and Figure 2 for these definitions.

Aperture Delay (t_{AD})

Aperture delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

This is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Hold Time (t_H)

Data hold time is the time to where the previous data (N - 1) is no longer valid.

Data Output Delay Time (t_{OD})

Data output delay time is the time to where the new data (N) is valid.

Data Latency (t_{LAT})

After the analog sample is taken, the data on the bus is output at 7th cycle of the clock. This is due to the pipeline nature of the converter where the data has to ripple through the stages. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The digital data lags the analog input by 7 cycles.

Power-Up Initialization

This time is defined as the maximum number of clock cycles that are required to initialize the converter at power-up. The requirement arises from the need to initialize the dynamic circuits within the converter.



HFA1135	HI5702	HSP9501	HI5780	HA5020
HFA1245	HI5703	HSP48410	HI1171	HA2842
	HI5746	HSP48908		HFA1115
	HI5767	HSP48212		
		HSP43891		
		HSP43168		
		HSP43216		

HFA1135: 350MHz Op Amp with Output Limiting
HFA1245: Dual 350MHz Op Amp with Disable/Enable
HI5702: 10-Bit, 40 MSPS, A/D Converter
HI5703: Low Power, 10-Bit, 40 MSPS, A/D Converter
HI5746: Low Power, CMOS, 10-Bit, 40 MSPS A/D Converter
HI5767: Low Power, CMOS, 10-Bit, 40 MSPS A/D Converter, with Voltage Reference
HSP9501: Programmable Data Buffer
HSP48410: Histogrammer/Accumulating Buffer, 10-Bit Pixel Resolution
HSP48908: 2-D Convolver, 3 x 3 Kernal Convolution, 8-Bit
HSP48212: Digital Video Mixer
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HI5780: 10-Bit, 80MHz, Video D/A Converter
HI1171: 8-Bit, 40MHz, Video D/A Converter
HFA5020: 100MHz Video Op Amp
HA2842: High Output Current, Video Op Amp
HFA1115: 350MHz Programmable Gain Buffer with Output Limiting

CMOS Logic Available in HC, HCT, AC, ACT, and FCT.

FIGURE 26. 10-BIT VIDEO IMAGING COMPONENTS



HFA3600	HI5702	HSP43168	HI5721	HFA1115
HFA3102	HI5703	HSP43216	HI5780	
HFA3101	HI5746	HSP43891	HI20201	
HFA1100	HI5767	HSP50016	HI20203	
		HSP50110		
		HSP50210		

HFA3600: Low Noise Amplifier/Mixer
HFA3102: Dual Long-Tailed Pair Transistor Array
HFA3101: Gilbert Cell Transistor Array
HFA1100: 850MHz Op Amp
HI5702: 10-Bit, 40 MSPS, A/D Converter
HI5703: Low Power, 10-Bit, 40 MSPS, A/D Converter
HI5746: Low Power, CMOS, 10-Bit, 40 MSPS A/D Converter
HI5767: Low Power, CMOS, 10-Bit, 40 MSPS A/D Converter, with Voltage Reference
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP50016: Digital Down Converter
HSP50110: Digital Quadrature Tuner
HSP50210: Digital Costas Loop
HI5721: 10-Bit, 125MHz, Communications D/A Converter
HI5780: 10-Bit, 80MHz, D/A Converter
HI20201: 10-Bit, 160MHz, High Speed D/A Converter
HFA1115: 350MHz Programmable Gain Buffer with Output Limiting

CMOS Logic Available in HC, HCT, AC, ACT, and FCT.

FIGURE 27. 10-BIT COMMUNICATIONS COMPONENTS

Die Characteristics

DIE DIMENSIONS:

159.4 mils x 175.2 mils x 19 mils ±1 mil

METALLIZATION:

Type: AlSiCu
Thickness: 11kÅ ±1kÅ

SUBSTRATE POTENTIAL (Powered Up):

GND (0.0V)

PASSIVATION:

Type: Sandwich Passivation
Nitride + Undoped Silicon Glass (USG)
Thickness: Nitride 4.2kÅ, USG 8kÅ
Total 12.2kÅ ±2kÅ

WORST CASE CURRENT DENSITY:

1.6×10^4 A/cm^2

TRANSISTOR COUNT:

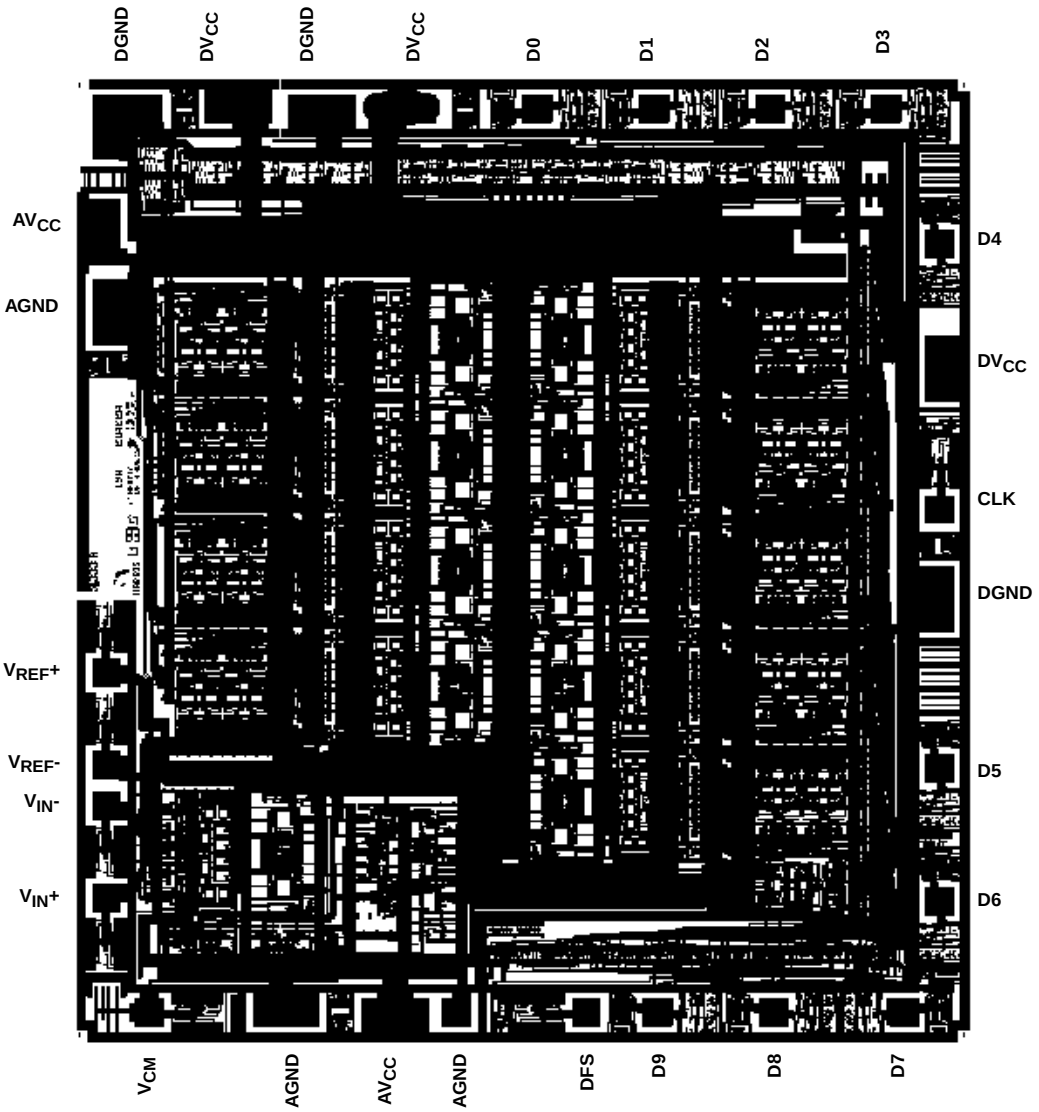
4514

DIE DIMENSIONS:

Silver Filled Epoxy

Metallization Mask Layout

HI5702



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