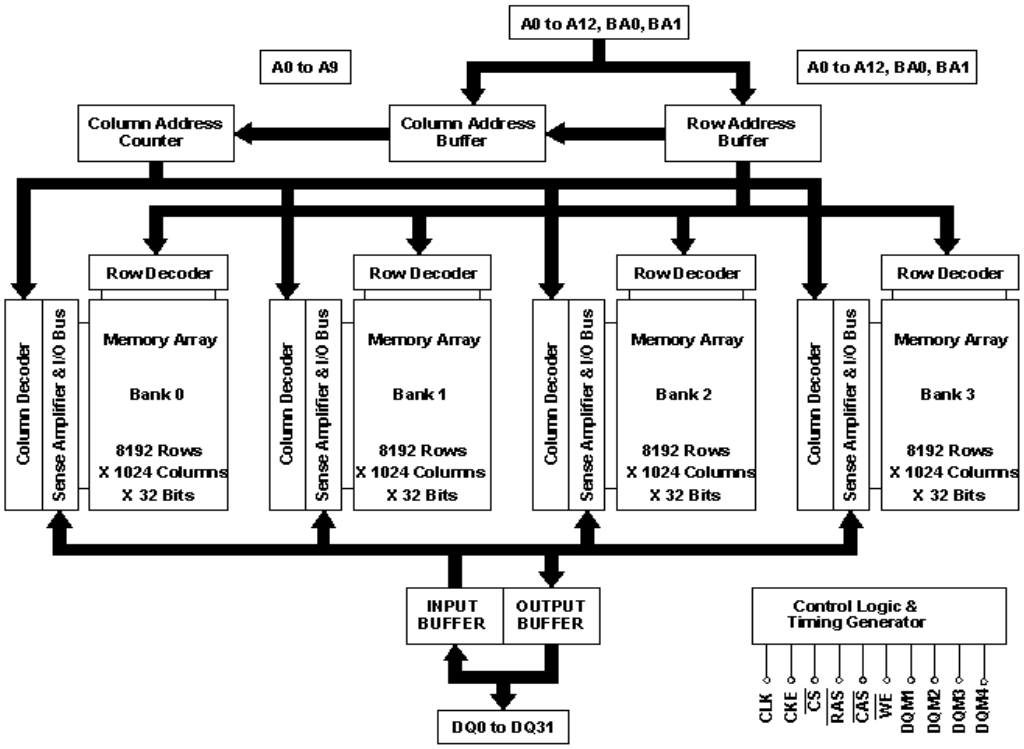
72SD3232B
1 Gbit SDRAM
8-Meg X 32-Bit X 4-Banks



FEATURES:

- 1 Gigabit (8-Meg X 32-Bit X 4-Banks)
- RAD-PAK® radiation-hardened against natural space radiation
- Total Dose Hardness:
  >100 krad (Si), depending upon space mission
- Excellent Single Event Effects:
  SEL_{TH} > 85 MeV/mg/cm^2 @ 25°C
- JEDEC Standard 3.3V Power Supply
- Clock Frequency: 100 MHz Operation
- Operating tremperature: -55 to +125°C
- Auto Refresh
- Single pulsed RAS
- 2 Burst Sequence variations
  Sequential (BL =1/2/4/8)
  Interleave (BL = 1/2/4/8)
- Programmable CAS latency: 2/3
- Power Down and Clock Suspend Modes
- LVTTL Compatible Inputs and Outputs
- Package: 72-Pin Flat Package

DESCRIPTION:

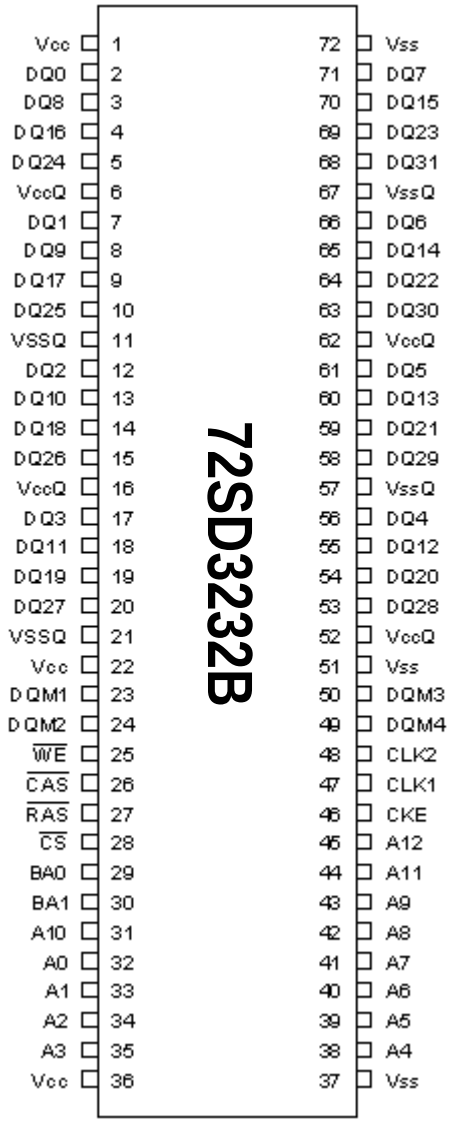
Maxwell Technologies' Synchronous Dynamic Random Access Memory (SDRAM) is ideally suited for space applications requiring high performance computing and high density memory storage. As microprocessors increase in speed and demand for higher density memory escalates, SDRAM has proven to be the ultimate solution by providing bit-counts up to 1 Gigabits and speeds up to 100 Megahertz. SDRAMs represent a significant advantage in memory technology over traditional SRAMs including the ability to burst data synchronously at high rates with automatic column-address generation, the ability to interleave between banks masking precharge time, and the ability to randomly change column address during each clock cycle.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding for a lifetime in orbit or space mission. In a typical GEO orbit, RAD-PAK® provides greater than 100 krads(Si) radiation dose tolerance. This product is available with screening up to Maxwell technologies self-defined screening flow.

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Pinout Description



Pin Descriptions

Pin Name	Function
A0 to A12	Address Input
BA0, BA1	Row Address A0 to A12
	Column Address A0 to A9
	Bank Select Address BA0/BA1 (BS)
DQ0 to DQ7	Data-Input/Output - Layer 1
DQ8 to DQ15	Data-Input/Output - Layer 2
DQ16 to DQ23	Data-Input/Output - Layer 3
DQ24 to DQ32	Data-Input/Output - Layer 4
CS\	Chip Select
RAS\	Row Address Strobe
CAS\	Column Address Strobe
WE\	Write Enable
DQM 1	Input/Output Mask - Layer 1
DQM 2	Input/Output Mask - Layer 2
DQM 3	Input/Output Mask - Layer 3
DQM 4	Input/Output Mask - Layer 4
CLK1	Clock Input - Layer 1 & 3
CLK2	Clock Input - Layer 2 & 4
CKE	Clock Enable
Vcc	Power for internal circuits
Vss	Ground for internal circuits
VccQ	Power for DQ circuits
VssQ	Ground for DQ circuits
NC	No Connection

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TABLE 1. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MAX	UNIT
Voltage on any pin relative to V_{SS}	V_{IN} V_{OUT}	-0.5 to VCC + 0.5 (< 4.6(max))	V
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Short circuit output current	I_{OUT}	50	mA
Power Dissipation	P_D	1.0	W
Operating Temperature	T_{OPR}	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

TABLE 2. RECOMMENDED OPERATING CONDITIONS

(V_{CC} = 3.3V ± 0.3V, $V_{CC}Q$ = 3.3V ± 0.3V, T_A = -55 TO 125°C, UNLESS OTHERWISE SPECIFIED)

CC

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{CC}, V_{CCQ}[1,2]	3.0	3.6	V
	V_{SS}, V_{SSQ}[3]	0	0	V
Input High Voltage	V_{IH}[1,4]	2.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}[1,5]	-0.3	.8	V

1. All voltage referred to VSS
2. The supply voltage with all V_{CC} and V_{CCQ} pins must be on the same level
3. The supply voltage with all V_{SS} and V_{SSQ} pins must be on the same level
4. V_{IH} (max) = V_{CC}+2.0V for pulse width <3ns at V_{CC}
5. V_{IL} (min) = V_{SS}-2.0V for pulse width <3ns at V_{SS}

TABLE 3. DELTA LIMITS

PARAMETER	DESCRIPTION	VARIATION[1]
I_{CC1}	Operating Current	± 10%
I_{CC2P} I_{CC2PS} I_{CC2N} I_{CC2NS}	Standby Current in Power Down	± 10%
I_{CC3P} I_{CC3PS} I_{CC3N} I_{CC3NS}	Active Standby Current	± 10%

1. ±10% of value specified in Table 4

TABLE 4. DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ± 0.3V, $V_{CC}Q$ = 3.3V ± 0.3V, T_A = -55 TO 125°C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS		SUBGROUPS	MIN	MAX	UNITS
Operating Current[1,2,3]	I_{CC1}	Burst length = 1 t_{RC} = min	$\overline{CAS}$ Latency = 2	1, 2, 3		460	mA
			$\overline{CAS}$ Latency = 3			460	
Standby Current in Power Down[4]	I_{CC2P}	CKE = V_{IL} t_{CK} = 12 ns		1, 2, 3		12	mA

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TABLE 4. DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ± 0.3V, $V_{CC}Q$ = 3.3V ± 0.3V, T_A = -55 TO 125°C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	SUBGROUPS	MIN	MAX	UNITS
Standby Current in Power Down (input signal stable)[5]	I_{CC2PS}	CKE = V_{IL} t_{CK} = 0	1, 2, 3		8	mA
Standby Current in non power down[6]	I_{CC2N}	CKE, CS = V_{IH} t_{CK} = 12 ns	1, 2, 3		80	mA
Standby Current in non power down (Input signal stable)[7]	I_{CC2NS}	CKE = V_{IH} t_{CK} = 0	1, 2, 3		36	mA
Active standby current in power down[1,2,4]	I_{CC3P}	CKE = V_{IL} t_{CK} = 12 ns	1, 2, 3		16	mA
Active standby current in power down (input signal stable)[2,5]	I_{CC3PS}	CKE = V_{IL} t_{CK} = 0	1, 2, 3		12	mA
Active standby power in non power down[1,2,6]	I_{CC3N}	CKE, CS = V_{IN} t_{CK} = 12 ns	1, 2, 3		120	mA
Active standby current in non power down (input signal stable)[2,7]	I_{CC3NS}	CKE = V_{IH} t_{CK} = 0	1, 2, 3		60	mA
Burst Operating Current[1,2,8] CAS Latency = 2 CAS Latency = 3	I_{CC4}	t_{CK} = min BL = 4	1, 2, 3		 440 580	mA
Refresh Current[3]	I_{CC5}	t_{RC} = min	1, 2, 3		880	mA
Self Refresh current[9]	I_{CC6}	$V_{IH} \geq V_{CC}$ - 0.2V $V_{IL} \leq$ 0.2 V	1, 2, 3		12	mA
Input Leakage Current - CLK 1 & 2	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$	1, 2, 3	-2	4	uA
Input Leakage Current - All Other	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$	1, 2, 3	-4	4	uA
Output Leakage Current	I_{LO}	$0 \leq VOUT \leq V_{CC}$	1, 2, 3	-1.5	1.5	uA
Output high voltage	V_{OH}	I_{OH} = -4mA	1, 2, 3	2.4		V
Output low voltage	V_{OL}	I_{OL} = 4 mA	1, 2, 3		0.4	V

1. ICC1 depends on output load conditions when the device is selected. ICC(max) is specified with the output open.
2. One Bank operation.
3. Input signals are changed once per one clock.
4. After power down mode, CLK operating current.
5. Afer power down mode, no CLK operating current.
6. Input signals are changed once per two clocks.
7. Input signals are VIH or VIL fixed.
8. Input signals are changed once per four clocks.
9. After self refresh mode set, self refresh current. Use self reset only at temperatures below 70°C

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TABLE 5. AC Electrical Characteristics

(V_{DD} =3.3V ± 0.3V, $V_{DD}Q$ = 3.3V ± 0.3V, T_A = -55 TO 125°C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	TYP	MAX	UNIT
System clock cycle time[1] (CAS latency = 2) (CAS latency = 3)	t_{CK}	9, 10, 11	 10 7.5			ns
CLK high pulse width[1,7]	t_{CKH}	9, 10, 11	2.5			ns
CLK low pulse width[1,7]	t_{CKL}	9, 10, 11	2.5			ns
Access time from CLK[1,2] (CAS latency = 2) (CAS latency = 3)	t_{AC}	9, 10, 11			 6 6	ns
Data-out hold time[1,2]	t_{OH}	9, 10, 11	2.7			ns
CLK to Data-out low impedance[1,2,3,7]	t_{LZ}	9, 10, 11	2			ns
CLK to Data-out high impedance[1,4,7] (CAS latency = 2, 3)	t_{HZ}	9, 10, 11			5.4	ns
Input setup time [1,5,6]	t_{AS}, t_{CS}, t_{DS}, t_{CES}	9, 10, 11	1.5			ns
CKE setup time for power down exit[1]	t_{CESP}	9, 10, 11	1.5			ns
Input hold time[1,6]	t_{AH}, t_{CH}, t_{DH} t_{CEH}	9, 10, 11	1.5			ns
Ref/Active to Ref/Active command period[1]	t_{RC}	9, 10, 11	70			ns
Active to Precharge command period[1]	t_{RAS}	9, 10, 11	50		120000	ns
Active command to column command (same bank)[1]	t_{RCD}	9, 10, 11	20			ns
Precharge to Active command period[1]	t_{RP}	9, 10, 11	20			ns
Write recovery or data-in to precharge lead time[1]	t_{DPL}	9, 10, 11	20			ns
Active(a) to Active (b) command period	t_{RRD}	9, 10, 11	20			ns
Transition time(rise and fall)[7]	t_T	9, 10, 11	1		5	ns
Refresh Period	t_{REF}	9, 10, 11		16	6.4	ms
		105°C		32	16[8]	
		85°C		64		
		70°C		128		

1. AC measurement assumes t_T=1ns. Reference level for timing of input signals is 1.5V
2. Access time is measured at 1.5V.
3. t_{LZ}(min) defines the time at which the outputs achieve the low impedance state.
4. t_{HZ}(min) defines the time at which the outputs achieve the high impedance state.
5. tCES defines CKE setup time to CLK rising edge except for the power down exit command.
6. t_{AS}/t_{AH}: Address, tC/tCH: /$\overline{CS}$, /$\overline{RAS}$, /CAS, /WE, DQM
7. Guarenteed by design. (Not Tested)
8. Guarenteed by Device Characterization. (Not 100% Tested)

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TABLE 6. CAPACITANCE[1]

(T_A=25°C, V_{CC}/V_{CCQ}=3.3 ±0.3V

PARAMETER	SYMBOL	MAX	UNIT
Input Capacitance (CLK)	C_{I1}	14	pF
Input Capacitance(all other Inputs)	C_{I2}	15.2	pF
Output Capacitance	C_O	4	pF

1. Guarenteed by design.

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Pin Functions:

CLK (INPUT PIN): CLK are the master clock inputs to this pin. The other input signals are referred at CLK rising edge.

$\overline{\text{CS}}$ (INPUT PIN): When $\overline{\text{CS}}$ is Low, the command input cycle becomes valid. When $\overline{\text{CS}}$ is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ AND $\overline{\text{WE}}$ (INPUT PINS): Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operations section.

A0 TO A12 (INPUT PINS): Row address (AX0 to AX12) is determined by A0 to A12 level at the bank active command cycle CLK rising edge. Column address (AY0 to AY9) is determined by A0 to A9 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, all banks are pre-charged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0/BA1 (BS) is pre charged. For details refer to the command operation section.

BA0/BA1 (INPUT PINS): BA0/BA1 are bank select signals (BS). The memory array of the 72SD3232B is divided into bank 0, bank 1, bank 2 and bank 3. The 72SD3232B contains 8192-row X 1024-column X 32-bit. If BA0 and BA1 is Low, bank 0 is selected. If BA0 is Low and BA1 is High, bank 1 is selected. If BA0 is High and BA1 is Low, bank 2 is selected. If BAO is High and BA1 is High, bank 3 is selected.

CKE (INPUT PIN): This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for ***power-down mode***, ***clock suspend mode*** and ***self refresh mode***[1].

DQM1 - DQM4 (INPUT PIN): DQM1 - DQM4 control input/output buffers

Read operation: If DQM1 - DQM4 are High, the output buffers becomes High-Z. If the DQM1- DQM4 are Low, the output buffers becomes Low-Z. (The latency of DQM1 - DQM4 during reading is 2 clock cycles.)

Write operation: If DQM1 - DQM4 are High, the previous data is held (the new data is not written). If the DQM1 - DQM4 are Low, the data is written. (The latency of DQM1 - DQM4 during writing is 0 clock cycles.)

DQ0 TO DQ31 (DQ PINS): Data is input to and output from these pins (DQ0 to DQ31).

V_{CC} AND $V_{CC}Q$ (POWER SUPPLY PINS): 3.3V is applied. (V_{CC} is for the internal circuit and $V_{CC}Q$ is for the output buffer.)

V_{SS} AND $V_{SS}Q$ (POWER SUPPLY PINS): Ground is connected. (V_{SS} is for the internal circuit and $V_{SS}Q$ is for the output buffer.)

1. Use self refresh at temperatures below 70°C only.

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Command Operation

Command Truth Table

The SDRAM recognizes the following commands specified by the $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address pins:

COMMAND	SYMBOL	N-1	N	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0/ BA1	A10	A0 TO A12
Ignore command	DESL	H	x	H	x	x	x	x	x	x
No Operation	NOP	H	x	L	H	H	H	x	x	x
Column Address and Read command	READ	H	x	L	H	L	H	V	L	V
Read with auto-pre-charge	READ A	H	x	L	H	L	H	V	H	V
Column Address and write command	WRIT	H	x	L	H	L	L	V	L	V
Write with auto-pre-charge	WRIT A	H	x	L	H	L	L	V	H	V
Row address strobe and bank active	ACTV	H	x	L	L	H	H	V	V	V
Precharge select bank	PRE	H	x	L	L	H	L	V	L	x
Precharge all banks	PALL	H	x	L	L	H	L	x	H	x
Refresh	REF/ SELF	H	L	L	L	L	H	x	x	x
Mode register set	MRS	H	x	L	L	L	L	V	V	V

Note: H: V_{IH} L: V_{IL} x V_{IH} or V_{IL} V: Valid address input

Ignore command (DESL): When this command is set ($\overline{CS}$ = High), the SDRAM ignores command input at the clock. However, the internal status is held.

No Operation (NOP): This command is not an execution command. However, the internal operations continue.

Column address strobe and read command (READ): This command starts a read operation. In addition, the start address of a burst read is determined by the column address (AY0 to AY9) and the bank select address (BS). After the read operation, the output buffer becomes High-Z.

Read with auto-precharge (READ A): This command automatically performs a precharge operation after a burst read with a burst length of 1, 2, 4, or 8.

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Column address strobe and write command (WRIT): This command starts a write operation. When the burst write mode is selected, the column address (AY0 to AY9) and the bank select address (BA0/BA1) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address (AY0 to AY9) and bank select address(BA0/BA1).

Write with auto-precharge (WRIT A): This command automatically performs a precharge operation after a burst write with a length of 1, 2, 4, or 8, or after a single write operation.

Row address strobe and bank activate (ACTV): This command activates the bank that is selected by BA0/BA1 (BS) and determines the row address (AX0 to AX12). When BA0 and BA1 are Low, bank 0 is activated. When BA0 is Low, and BA1 is High, bank 1 is activated. When BA0 is High and BA1 is Low, bank 2 is activated. When BA0 and BA1 are High, bank 3 is activated.

Precharge select bank (PRE): This command starts precharge operation for the bank selected by BA0/BA1. If BA0 and BA1 are Low, bank 0 is selected. If BA0 is Low and BA1 is High, bank 1 is selected. If BA0 is High and BA1 is Low, bank 2 is selected. If BA0 and BA1 are High, bank 3 is selected.

Precharge all banks (PALL): This command starts a precharge operation for all banks.

Refresh (REF/SELF)[1]: This command starts the refresh operation. There are two types of refresh operations; one is auto-refresh, and the other is self-refresh. For details, refer to the CKE truth table section.

Mode register set (MRS): The SDRAM has a mode register that defines how it operates. The mode register is specified by the address pins (A0 to A12, BA0 andBA1) at the mode register set cycle. For details, refer to the mode register configuration. After power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

1. Use self refresh for temperatures below 70 °C.

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DQM1 - DQM4 Truth Table

COMMAND	SYMBOL	CKE = N-1	CKE = N	DQM4	DQM3	DQM2	DQM1
(DQ248 to DQ31) write enable/output enable	ENB4	H	x	H	x	x	x
(DQ248 to DQ31) write inhibit/output disable	MASK4	H	x	L	x	x	x
(DQ16 to DQ24) write enable/output enable	ENB3	H	x	x	H	x	x
(DQ16 to DQ24) write inhibit/output disable	MASK3	H	x	x	L	x	x
(DQ8 to DQ15) write enable/output enable	ENB2	H	x	x	x	H	x
(DQ8 to DQ15) write inhibit/output disable	MASK2	H	x	x	x	L	x
(DQ0 to DQ7) write enable/output enable	ENB1	H	x	x	x	x	H
(DQ0 to DQ7) write inhibit/output disable	MASK1	H	x	x	x	x	L

Note: H: V_{IH} L: V_{IL} x V_{IH} or V_{IL}
Write: I_{DID} is Needed
Read: I_{DOD} is Needed

The SDRAM can mask input/output data by means of DQM1- DQM4.

During reading, the output buffer is set to Low-Z by setting DQM1 - DQM4 to Low, enabling data output. On the other hand, when DQM1 - DQM4 are set High, the output buffer becomes High-Z, disabling data output.

During writing, data is written by setting DQM1 - DQM4 to Low. When DQM1 - DQM4 is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQM1 - DQM4. For more details, refer to the DQM1 - DQM4 control section of the SDRAM operating instructions.

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CKE Truth Table

CURRENT STATE	COMMAND	n-1	n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESS
Active	Clock suspended mode entry	H	L	x	x	x	x	x
Any	Clock Suspend	L	L	x	x	x	x	x
Clock Suspend	Clock Suspend mode exit	L	H	x	x	x	x	x
Idle	Auto-refresh command (REF)	H	H	L	L	L	H	x
Idle	Self-refresh entry (SELF)	H	L	L	L	L	H	x
Idle Power down entry		H	L	L	H	H	H	x
		H	L	HL	x	x	x	x
Self Refresh	Self Refresh exit (SELFX)	L	H	L	H	H	H	x
Power down Power down exit		L	H	L	H	H	H	x
		L	H	H	x	x	x	x

Note: H:V_{IH} L:V_{IL} x V_{IH} or V_{IL}

Clock suspend mode entry: The SDRAM enters clock suspend mode from active mode by setting CKE to Low. If a command is input in the clock suspend mode entry cycle, the command is valid. The clock suspend mode change depending on the current status (1 clock before) as described below.

ACTIVE clock suspend: This suspend mode ignores inputs after the next clock by internally maintaining the bank active status.

READ suspend and READ with Auto-precharge suspend: The data being output is held (and continues to be output).

WRITE suspend and WRIT with Auto-precharge suspended: In this mode, external signals are not accepted. However, the internal state is held.

Clock suspend: During clock suspend mode, keep the CKE to Low.

Clock suspend mode exit: The SDRAM exits from clock suspend mode by setting CKE to High during the clock suspend state.

IDLE: In this state, all banks are not selected, and have completed precharge operation.

Auto-refresh command (REF): When this command is input from the IDLE state, the SDRAM starts auto-refresh operation. (The auto-refresh is the same as the CBR refresh of conventional DRAMs.) During the auto-refresh operation, refresh address and bank select address are generated inside the SDRAM. For every auto-refresh cycle, the internal address counter is updated. Accordingly, 8192 cycles are required to refresh the entire memory contents. Before executing the auto-refresh command, all the banks must be in

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the IDLE state. In addition, since the precharge for all banks is automatically performed after auto-refresh, no precharge command is required after auto-refresh.

Self Refresh entry (SELF)[1]: When this command is input during the IDLE state, the SDRAM starts self-refresh operation. After the execution of this command, self-refresh continues while CKE is Low. Since self-refresh is performed internally and automatically, external refresh operations are unnecessary.

Power down mode entry: When this command is executed during the IDLE state, the SDRAM enters power down mode. In power down mode, power consumption is suppresses by cutting off the initial input circuit.

Self-refresh exit: When this command is executed during self-refresh mode, the SDRAM can exit from self-refresh mode. After exiting from self-refresh mode, the SDRAM enters the IDLE state.

Power down exit: When this command is executed at power down mode, the SDRAM can exit from power down mode. After exiting from power down mode, the SDRAM enters the IDLE state.

1. Use self refresh for temperatures below 70 °C

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Function Truth Table

The following function table shows the operations that are performed when each command is issued in each mode of the SDRAM.

The following table assumes that CKE is High.

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESS	COMMAND	OPERATION
Precharge	H	x	x	x	x	DESL	Enter IDLE after t_{RP}
	L	H	H	H	x	NOP	Enter IDLE after t_{RP}
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL[1]
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL[1]
	L	L	H	H	BA, RA	ACTV	ILLEGAL[1]
	L	L	H	L	BA, A10	PRE, PALL	NOP[2]
	L	L	L	H	x	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Idle	H	x	x	x	x	DESL	NOP
	L	H	H	H	x	NOP	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL[3]
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL[3]
	L	L	H	H	BA, RA	ACTV	Bank and row active
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	x	REF, SELF	Refresh
	L	L	L	L	MODE	MRS	Mode register set
Row active	H	x	x	x	x	DESL	NOP
	L	H	H	H	x	NOP	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	Begin read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Begin write
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank[4]
	L	L	H	L	BA, A10	PRE, PALL	Precharge
	L	L	L	H	x	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

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CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESS	COMMAND	OPERATION
READ	H	x	x	x	x	DESL	Continue burst to end
	L	H	H	H	x	NOP	Continue burst to end
	L	H	L	H	BA, CA, A10	READ/READ A	Continue burst read to $\overline{CAS}$ latency and new read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst read/start write
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank[4]
	L	L	H	L	BA, A10	PRE, PALL	Term burst read and Precharge
	L	L	L	H	x	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read with auto-precharge	H	x	x	x	x	DESL	Continue burst to end and pre-charge
	L	H	H	H	x	NOP	Continue burst to end and pre-charge
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL[1]
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL[1]
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank[4]
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL[1]
	L	L	L	H	x	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Write	H	x	x	x	x	DESL	Continue burst to end
	L	H	H	H	x	NOP	Continue burst to end
	L	H	L	H	BA, CA, A10	READ/READ A	Term burst and new read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst and new write
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank[4]
	L	L	H	L	BA, A10	PRE, PALL	Term burst write and precharge[5]
	L	L	L	H	x	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

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CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESS	COMMAND	OPERATION
Write with auto-precharge	H	x	x	x	x	DESL	Continue burst to end and pre-charge
	L	H	H	H	x	NOP	Continue burst to end and pre-charge
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL[1]
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL[1]
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank[4]
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL[1]
	L	L	L	H	x	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Refresh (auto-refresh)	H	x	x	x	x	DESL	Enter IDLE after t_{RC}
	L	H	H	H	x	NOP	Enter IDLE after t_{RC}
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL[3]
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL[3]
	L	L	H	H	BA, RA	ACTV	ILLEGAL[3]
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL[3]
	L	L	L	H	x	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

1. Illegal for same bank, except for another bank
2. NOP for same bank, except for another bank
3. Illegal for all banks
4. If t_{RRD} is not satisfied, this operation is illegal
5. An interval of t_{DPL} is required between the final valid data input and the precharge command

From PRECHARGE state, command operation

To [DESL], [NOP]: When these commands are executed, the SDRAM enters the IDLE state after t_{RP} has elapsed from the completion of precharge.

From IDLE state, command operation

To [DESL], [NOP], [PRE], or [PALL]: These commands result in no operation.

To [ACTV]: The bank specified by the address pins and the ROW address is activated.

To [REF], [SELF]: The SDRAM enters refresh mode (auto-refresh or self-refresh).

To [MRS]: The synchronous DRAM enters the mode register set cycle.

From ROW ACTIVE state, command operation

To [DESL], [NOP]: These commands result in no operation.

To [READ], [READ A]: A read operation starts. (However, an interval of t_{RCD} is required.)

To [WRIT], [WRIT A]: A write operation starts. (However, an interval of t_{RCD} is required.)

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To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands set the SDRAM to precharge mode. (However, an interval of t_{RAS} is required.)

From READ state, command operation

To [DESL], [NOP]: These commands continue read operations until the operation is completed.

To [READ], [READ A]: Data output by the previous read command continues to be output. After $\overline{CAS}$ latency, the data output resulting from the next command will start.

To [WRIT], [WRIT A]: These commands stop a burst read, and start a write cycle.

To [ACTV]: This command makes other banks bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop a burst read, and the SDRAM enters precharge mode.

From READ with AUTO-PRECHARGE state, command operation

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed, and the SDRAM then enters precharge mode.

To [ACTV]: This command makes other banks active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

From WRITE state, command operation

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed.

To [READ], [READ A]: These commands stop a burst and start a read cycle.

To [WRIT], [WRIT A]: These commands stop a burst and start the next write cycle.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop burst write and the SDRAM then enters precharge mode.

From WRITE with AUTO-PRECHARGE state, command operation

To [DESL], [NOP]: These commands continue write operations until the burst is completed, and the synchronous DRAM enters precharge mode.

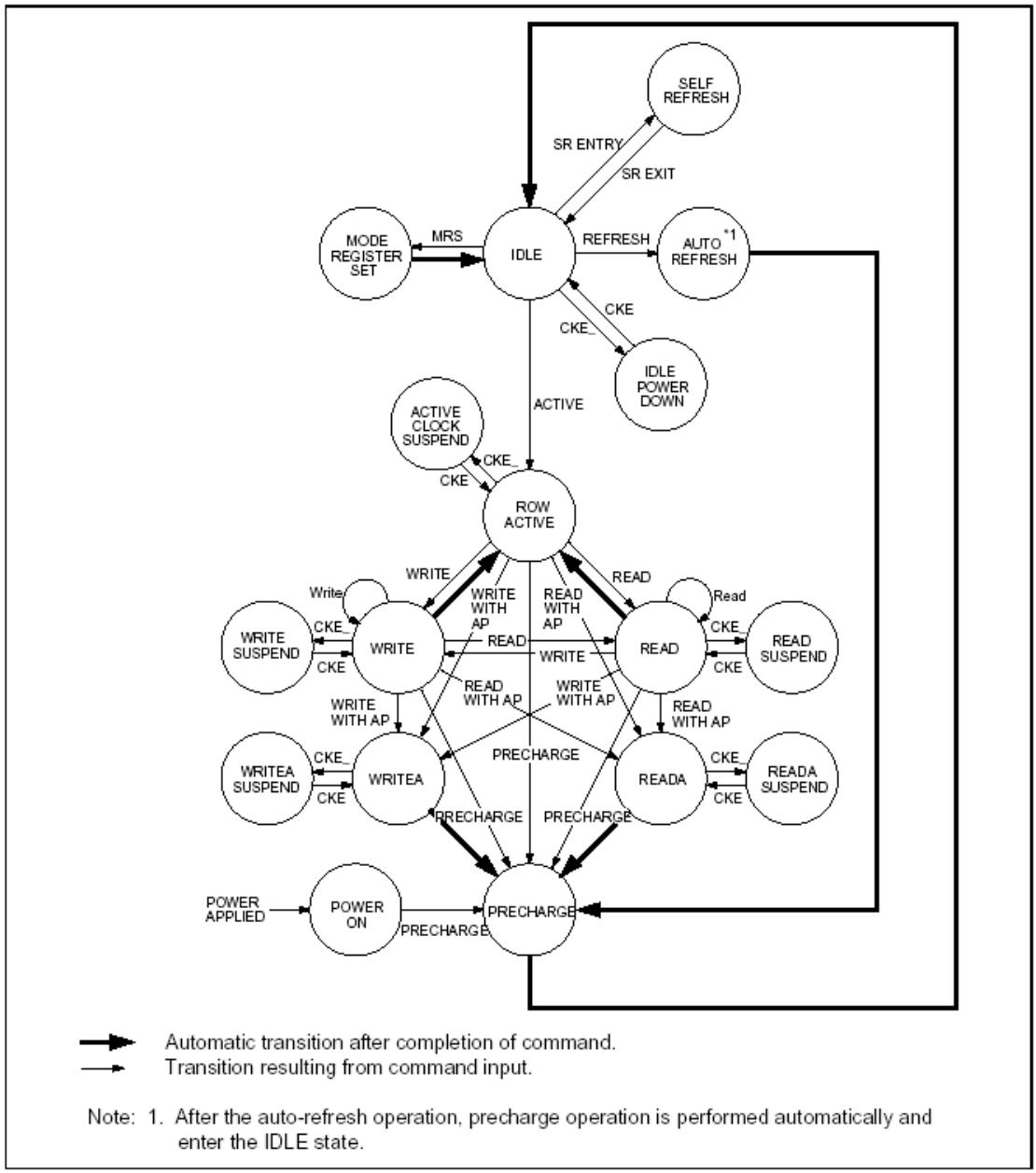
To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active result in an illegal command.

From REFRESH state, command operation

To [DESL], [NOP]: After an auto-refresh cycle (after t_{RC}) the SDRAM automatically enters the IDLE state.

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Simplified State Diagram



Note: 1. After the auto-refresh operation, precharge operation is performed automatically and enter the IDLE state.

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Mode Register Configuration

The mode register is set by the input to the address pins (A0 to A12, BA0 and BA1) during mode register set cycles. The mode register consists of five sections, each of which is assigned to address pins.

BA0, BA1, A11, A10, A12, A9, A8: (OPCODE): The SDRAM has two types of write modes. One is the *burst write mode*, and the other is the *single write mode*. These bits specify write mode.

Burst read and burst write: Burst write is performed for the specified burst length starting from the column address specified in the write cycle.

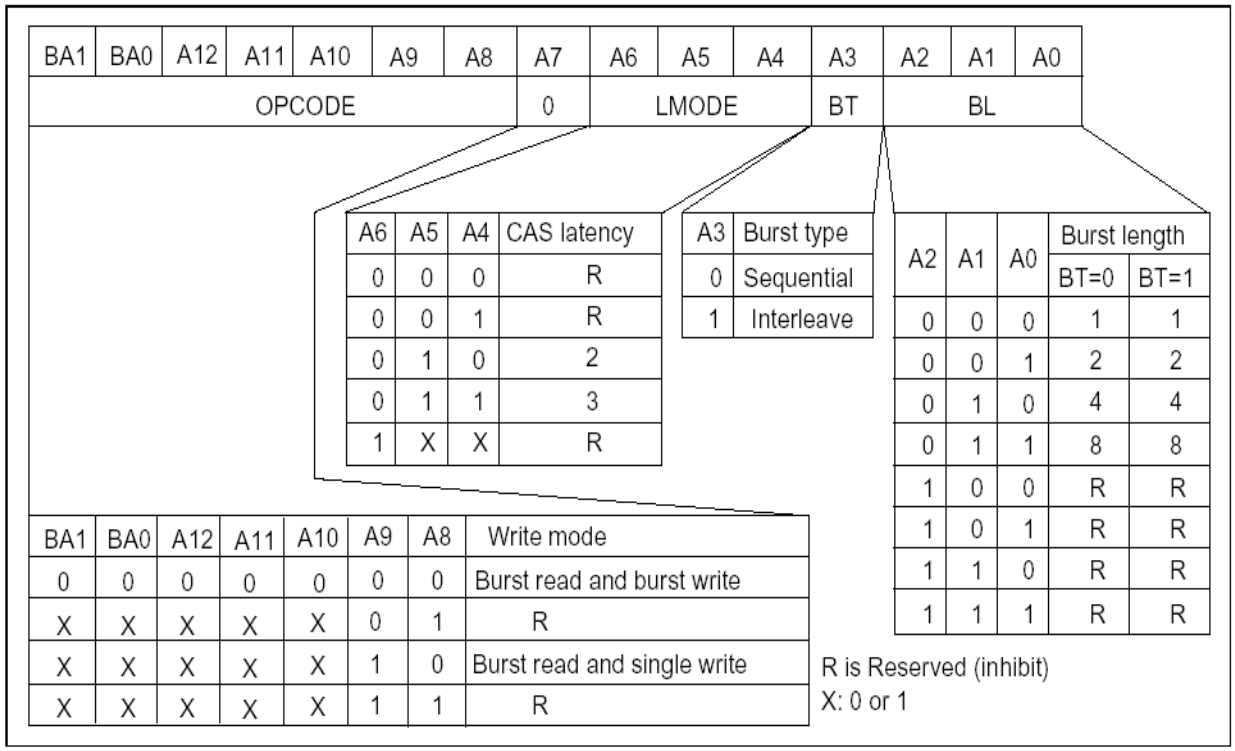
Burst read and single write: Data is only written to the column address specified during the write cycle, regardless of the burst length.

A7: Keep this bit Low at the mode register set cycle. If this pin is high, the vender test mode is set.

A6, A5, A4: (LMODE): These pins specify the $\overline{\text{CAS}}$ latency.

A3: (BT): A burst type is specified.

A2, A1, A0: (BL): These pins specify the burst length.



BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
OPCODE							0	LMODE			BT	BL		

A6	A5	A4	CAS latency
0	0	0	R
0	0	1	R
0	1	0	2
0	1	1	3
1	X	X	R

A3	Burst type
0	Sequential
1	Interleave

A2	A1	A0	Burst length BT=0	Burst length BT=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	R	R
1	0	1	R	R
1	1	0	R	R
1	1	1	R	R

BA1	BA0	A12	A11	A10	A9	A8	Write mode
0	0	0	0	0	0	0	Burst read and burst write
X	X	X	X	X	0	1	R
X	X	X	X	X	1	0	Burst read and single write
X	X	X	X	X	1	1	R

R is Reserved (inhibit)
X: 0 or 1

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Burst Sequence

Burst length = 2

Starting Ad.	Addressing(decimal)	
A0	Sequential	Interleave
0	0, 1,	0, 1,
1	1, 0,	1, 0,

Burst length = 4

Starting Ad.		Addressing(decimal)	
A1	A0	Sequential	Interleave
0	0	0, 1, 2, 3,	0, 1, 2, 3,
0	1	1, 2, 3, 0,	1, 0, 3, 2,
1	0	2, 3, 0, 1,	2, 3, 0, 1,
1	1	3, 0, 1, 2,	3, 2, 1, 0,

Burst length = 8

Starting Ad.			Addressing(decimal)	
A2	A1	A0	Sequential	Interleave
0	0	0	0, 1, 2, 3, 4, 5, 6, 7,	0, 1, 2, 3, 4, 5, 6, 7,
0	0	1	1, 2, 3, 4, 5, 6, 7, 0,	1, 0, 3, 2, 5, 4, 7, 6,
0	1	0	2, 3, 4, 5, 6, 7, 0, 1,	2, 3, 0, 1, 6, 7, 4, 5,
0	1	1	3, 4, 5, 6, 7, 0, 1, 2,	3, 2, 1, 0, 7, 6, 5, 4,
1	0	0	4, 5, 6, 7, 0, 1, 2, 3,	4, 5, 6, 7, 0, 1, 2, 3,
1	0	1	5, 6, 7, 0, 1, 2, 3, 4,	5, 4, 7, 6, 1, 0, 3, 2,
1	1	0	6, 7, 0, 1, 2, 3, 4, 5,	6, 7, 4, 5, 2, 3, 0, 1,
1	1	1	7, 0, 1, 2, 3, 4, 5, 6,	7, 6, 5, 4, 3, 2, 1, 0,

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Operation of the SDRAM

The following section shows operation examples of 72SD3232.

Note: The SDRAM should be used according to the product capability (See Pin Description and AC Characteristics.)

Read/Write Operations:

Bank Active: Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACTV) command. An interval of t_{RCD} is required between the bank active command input and the following read/write command input.

Read operation: A read operation starts when a read command is input. The output buffer becomes Low-Z in the ($\overline{CAS}$ latency - 1) cycle after read command set. The SDRAM can perform a burst read operation.

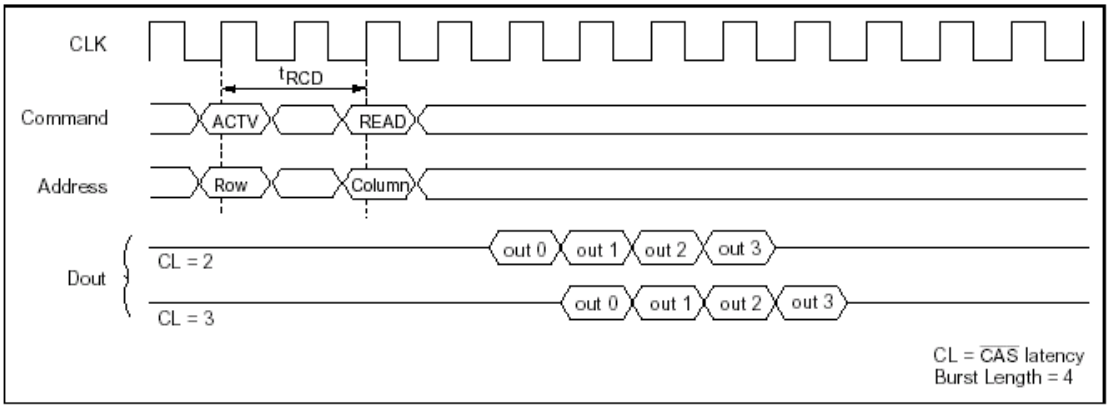
The burst length can be set to 1, 2, 4, or 8. The start address for a burst read is specified by the column address and the bank select address (BA0/BA1) at the read command set cycle. In a read operation, data output starts after the number of clocks specified by the $\overline{CAS}$ latency. The $\overline{CAS}$ latency can be set to 2 or 3.

When the burst length is 1, 2, 4, or 8, the D_{OUT} buffer automatically becomes High-Z at the next clock after the successive burst-length data has been output.

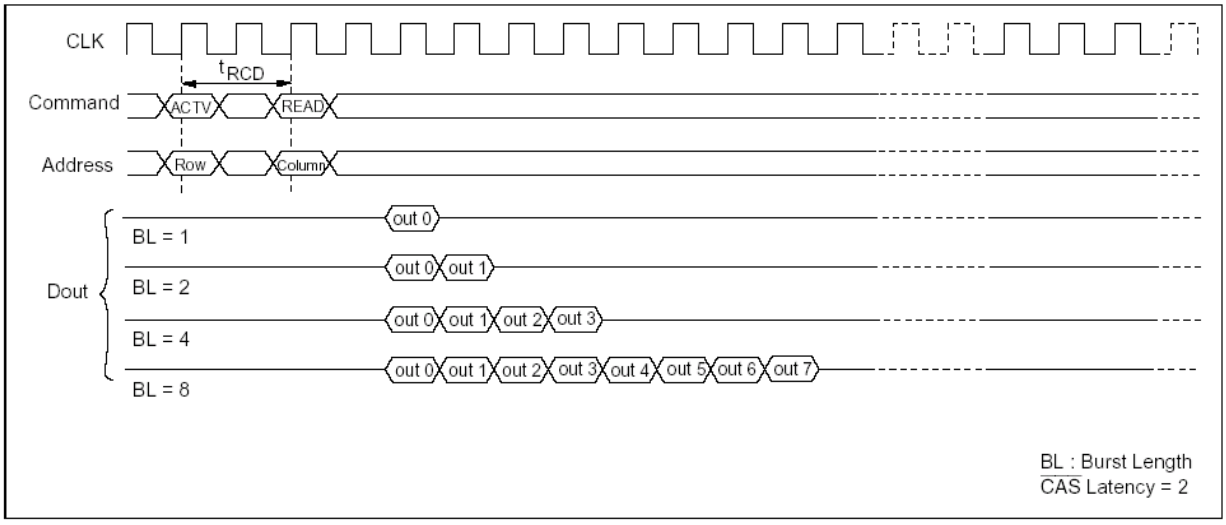
The $\overline{CAS}$ latency and burst length must be specified at the mode register.

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$\overline{\text{CAS}}$ Latency



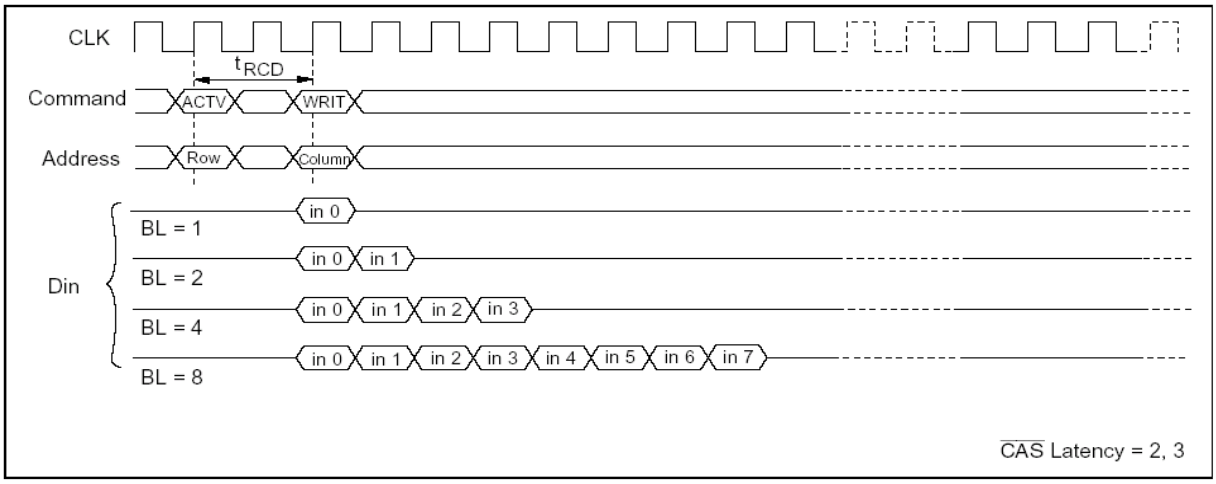
Burst Length



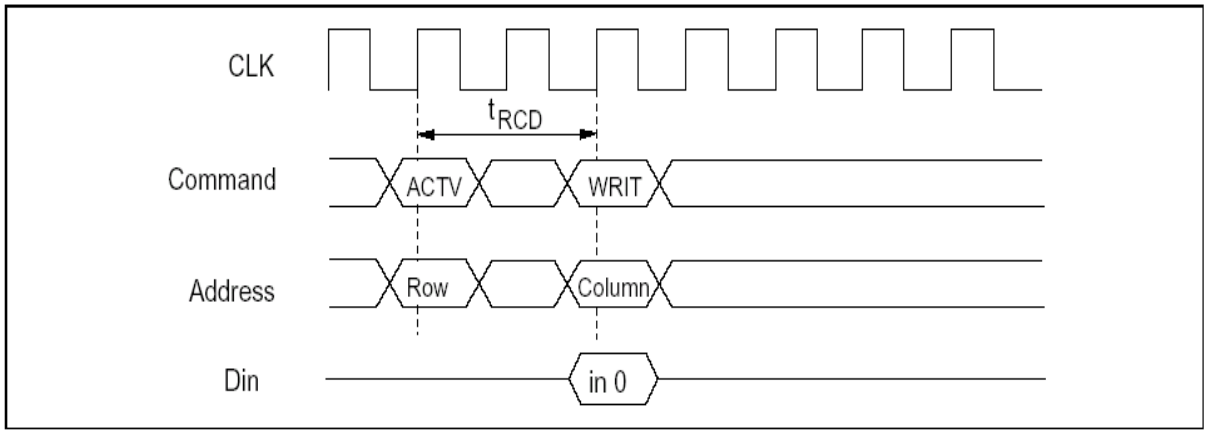
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Write Operation: Burst write or single write mode is selected by the OPCODE (BA1, BA0, A12, A11, A10, A9, A8) of the mode register.

1. Burst write: A burst write operation is enabled by setting OPCODE (A9, A8) to (0, 0). A burst write starts in the same clock as a write command set. (The latency of data input is 0 clock.) The burst length can be set to 1, 2, 4, or 8, like burst read operations. The write start address is specified by the column address and the bank select address (BA0/BA1) at the write command set cycle.



2. Single write: A single write operation is enabled by setting OPCODE (A9, A8) to (1, 0). In a single write operation, data is only written to the column address and the bank select address (BA0/BA1) specified by the write command set cycle without regard to the burst length setting. (The latency of data input is 0 clock.)



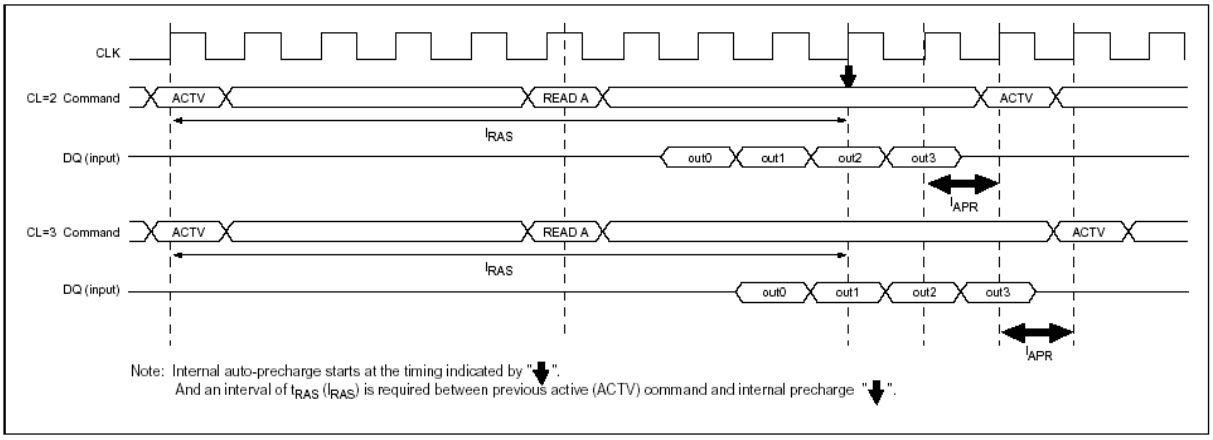
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Auto Precharge

Read with auto-precharge: In this operation, since precharge is automatically performed after completing a read operation, a precharge command need not be executed after each read operation. The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval defined by I_{ARP} is required before execution of the next command.

$\overline{CAS}$ latency	Precharge start cycle
3	2 cycles before the final data is output
2	1 cycle before the final data is output

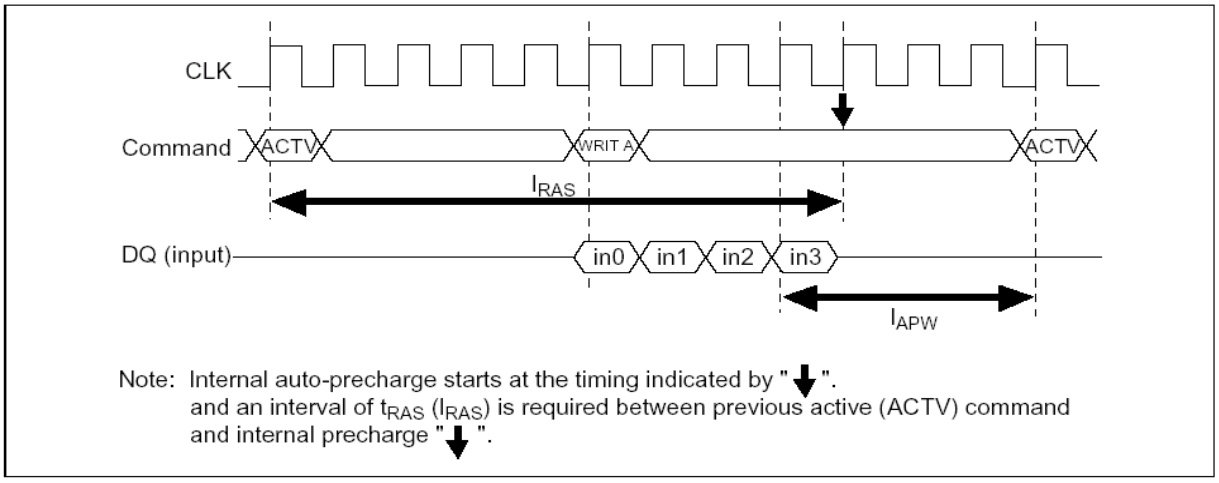
Burst Read (Burst Length = 4)



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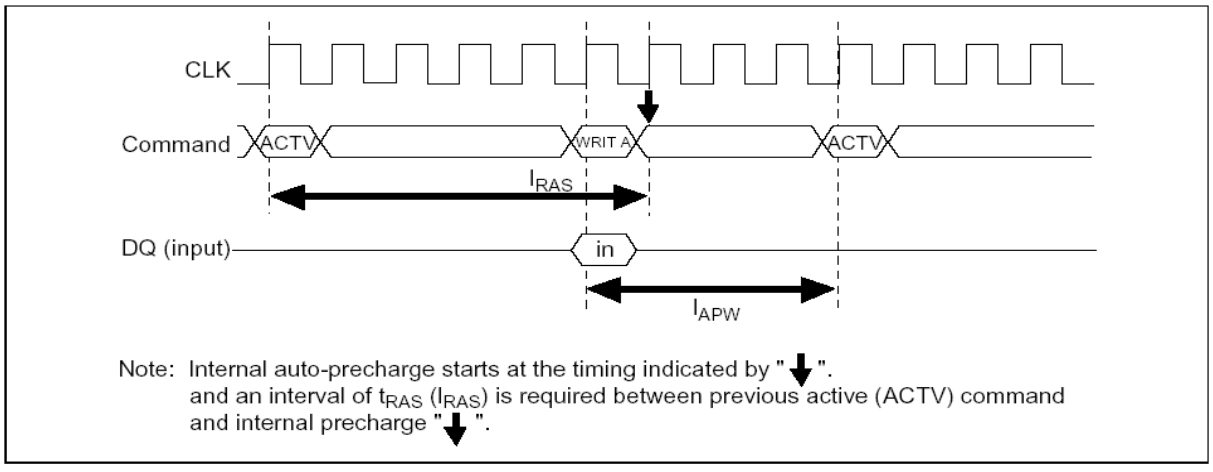
Write with auto-precharge: In this operation, since precharge is automatically preformed after completing a burst write or single write operation, a precharge command need not be executed after each write operation. The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval of I_{APW} is required between the final valid data input and input of next command.

Burst Write (Burst Length = 4)



Note: Internal auto-precharge starts at the timing indicated by "↓".
and an interval of t_{RAS} (I_{RAS}) is required between previous active (ACTV) command and internal precharge "↓".

Single Write



Note: Internal auto-precharge starts at the timing indicated by "↓".
and an interval of t_{RAS} (I_{RAS}) is required between previous active (ACTV) command and internal precharge "↓".

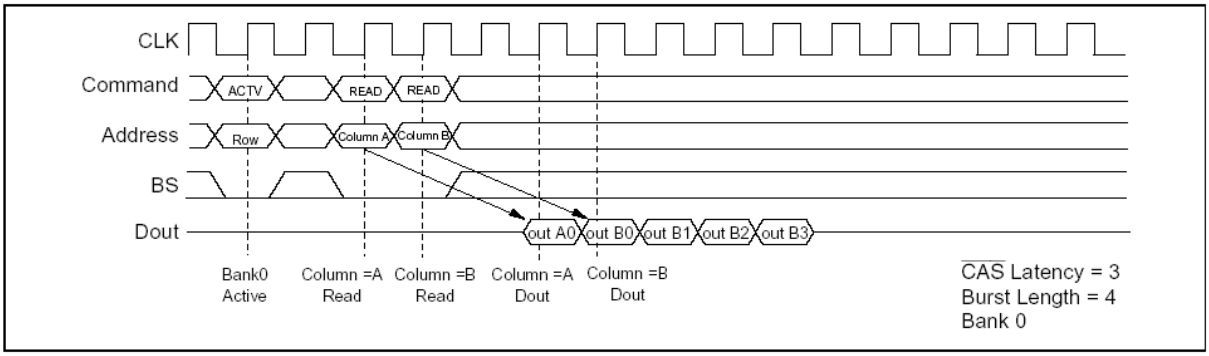
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Command Intervals

READ command to READ command interval

1. Same bank, same ROW address: When another read command is executed at the same ROW address of the same bank as the preceding read command execution, the second read can be performed after an interval of no less than 1 clock. Even when the first command is a burst read that is not yet finished, the data read by second command will be valid.

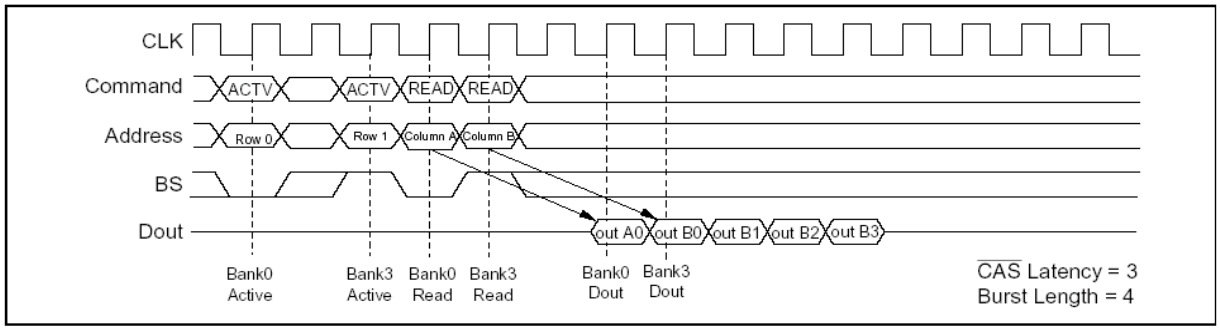
READ to READ Command Interval (Same ROW address in same bank)



2. Same bank, different ROW address: When the ROW address changes on the same bank, consecutive read commands cannot be executed; it is necessary to separate the two read commands with a precharge command and a bank-active command.

3. Different bank: When the bank changes, the second read can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank-active state. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

READ to READ Command Interval (Different Bank)

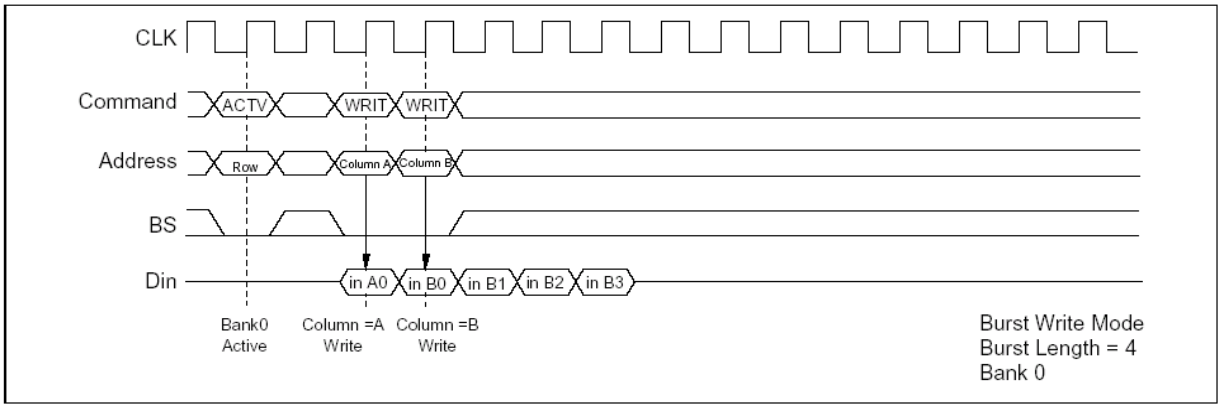


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Write command to Write command interval:

1. Same bank, same ROW address: When another write command is executed at the same ROW address of the same bank as the preceding write command, the second write can be performed after as interval of no less than 1 clock. In the case of burst writes, the second write command has priority.

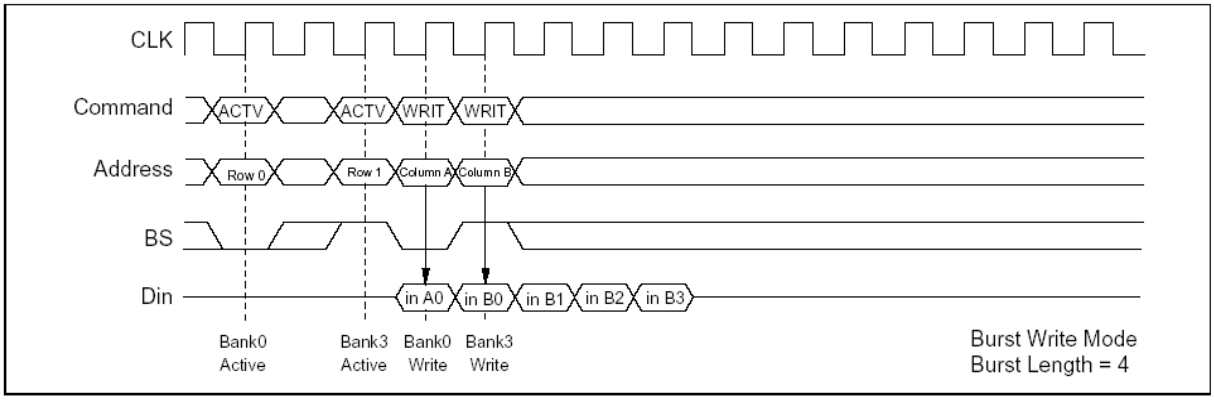
Write to Write Command Interval (Same ROW address in same bank)



2. Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank-active command.

3. Different bank: When the bank changes, the second write can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank-active state. In the case of burst write, the second write command has priority.

WRITE to WRITE Command Interval (Different bank)

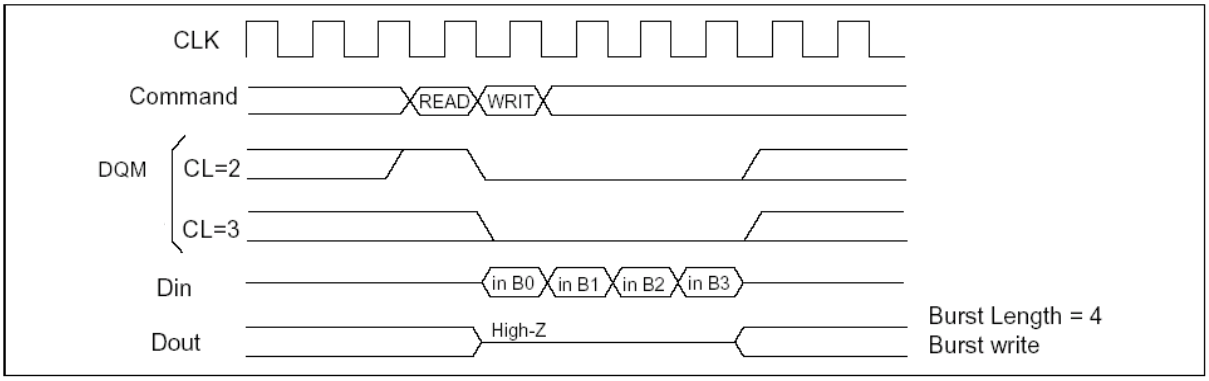


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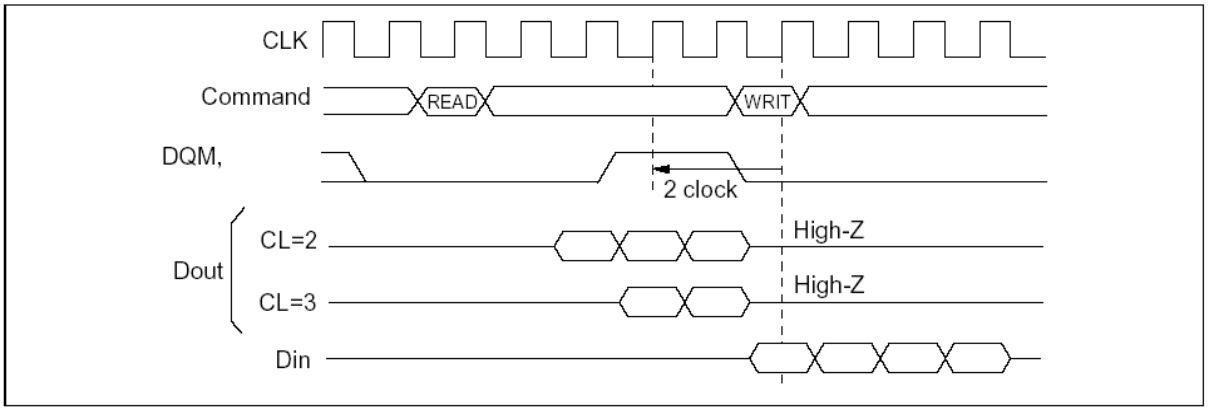
Read command to Write command Interval:

1. Same bank, same ROW address: When the write command is executed at the same ROW address of the same bank as the preceding read command, the write command can be performed after an interval of no less than 1 clock. However, DQM1 - DQM4 must be set High so the output buffer becomes High-Z before data input.

READ to WRITE Command Interval (1)



READ to WRITE Command Interval (2)



2. Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank-active command.

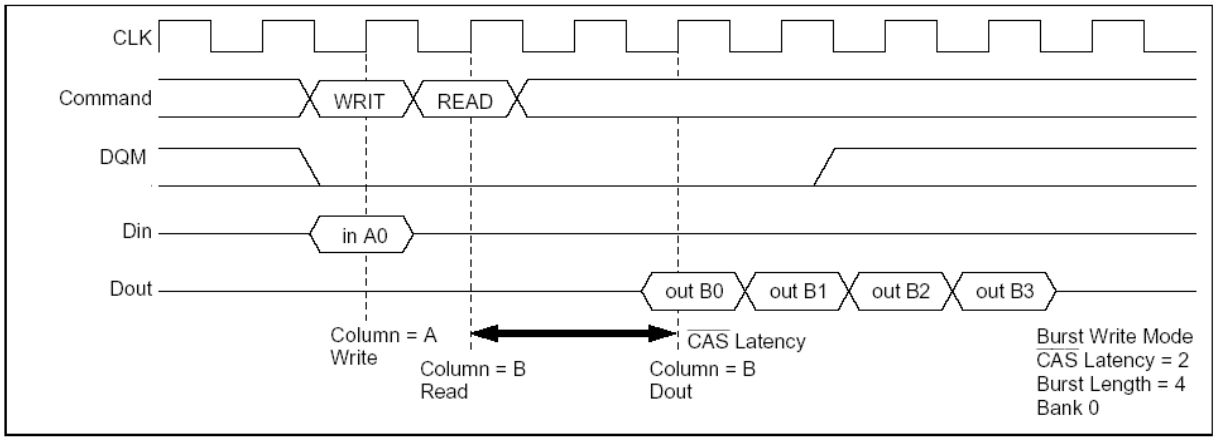
3. Different bank: When the bank changes, the write command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. However, DQM must be set High so that the output buffer becomes High-Z before data input.

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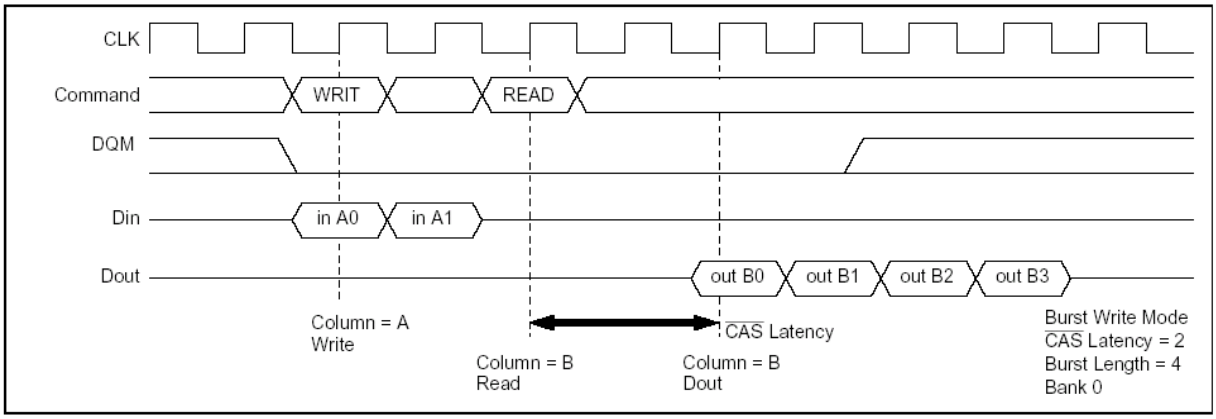
Write command to READ command interval:

1. Same bank, same ROW address: When the read command is executed at the same ROW address of the same bank as the preceding write command, the read command can be performed after an interval of no less than 1 clock. However, in the case of a burst write, data will continue to be written until one clock before the read command is executed.

WRITE to READ Command Interval (1)



Write to READ Command Interval (2)



2. Same bank, different ROW address: When the ROW address changes, consecutive read commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank-active command.

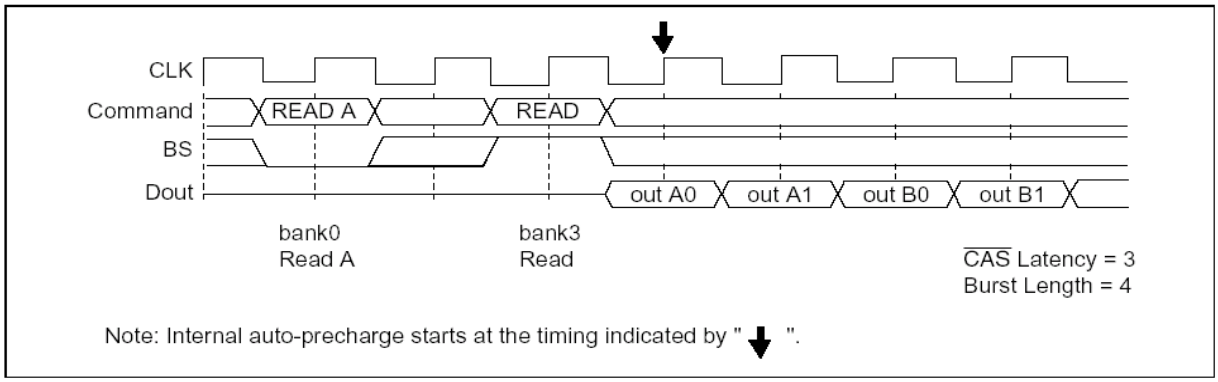
3. Different bank: When the bank changes, the read command can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank-active state. However, in the case of a burst write, data will continue to be written until one clock before the read command is executed (as in the case of the same bank and the same address).

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Read with Auto Precharge to READ command interval

1. Different bank: When some banks are in the active state, the second read command (another bank) is executed. Even when the first read with auto-precharge is a burst read that is not yet finished, the data read by the second command is valid. The interval auto-precharge of one bank starts at the next clock of the second command.

Read with Auto Precharge to Read Command Interval (Different Bank)

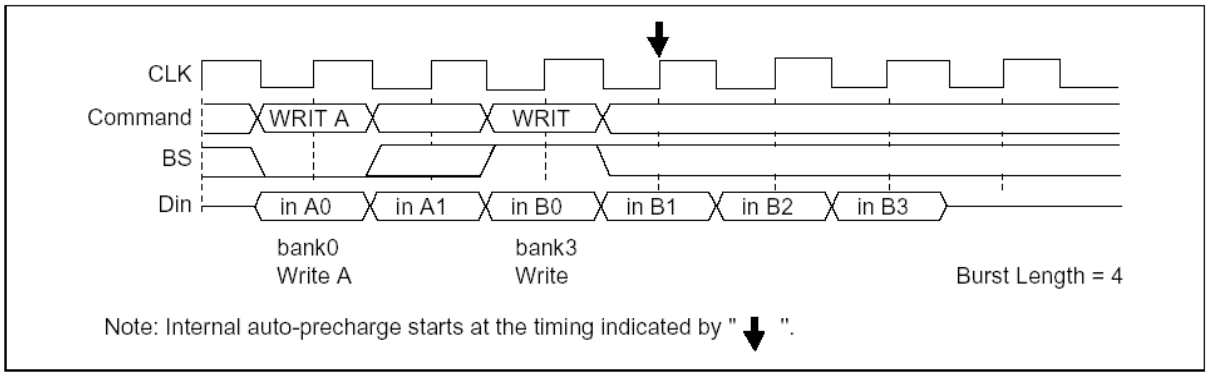


2. Same Bank: The consecutive read command (the same bank) is illegal.

Write with Auto Precharge to Write command interval

1. Different bank: When some banks are in the active state, the second write command (another bank) is executed. In the case of burst writes, the second write command has priority. The internal auto-precharge of one bank starts at the next clock of the second command.

Write with Auto Precharge to Write Command Interval (Different bank)



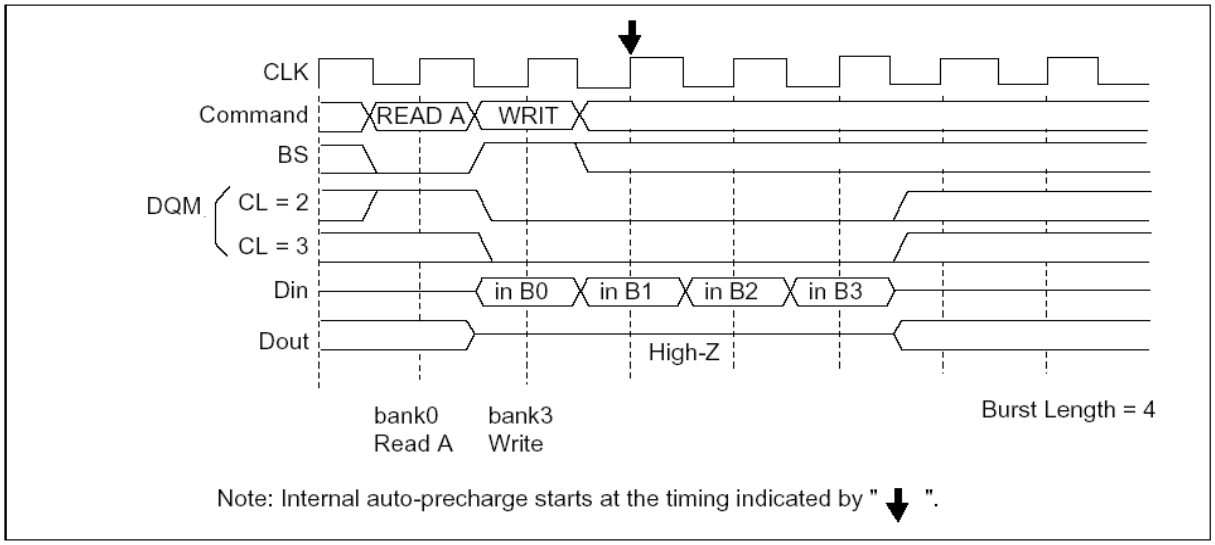
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2. Same bank: The consecutive write command (the same bank) is illegal.

Read with Auto Precharge to Write command interval

1. Different bank: When some banks are in the active state, the second write command (another bank) is executed. However, DQM1 - DQM4 must be set High so that the output buffer becomes High-Z before data input. The internal auto-precharge of one bank starts at the next clock of the second command.

Read with Auto Precharge to Write Command Interval (Different bank)



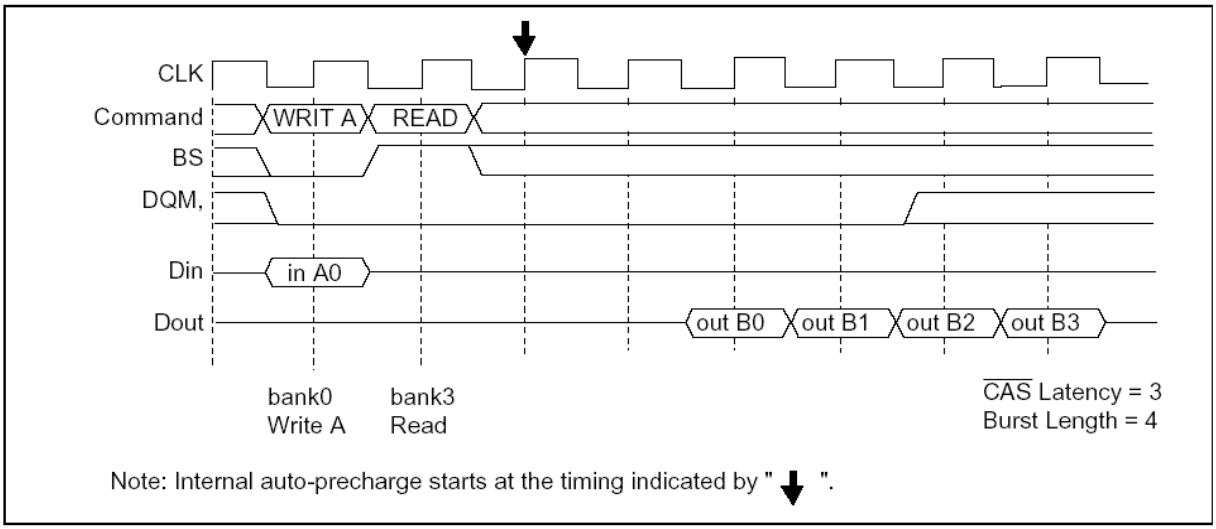
2. Same bank: The consecutive write command from read with auto precharge (the same bank) is illegal. It is necessary to separate the two commands with a bank active command.

Write with Auto Precharege to Read command interval

1. Different bank: When some banks are in the active state, the second read command (another bank) is executed. However, in the case of a burst write, data will continue to be written until one clock before the read command is executed. The internal auto precharge of one bank starts at the next clock of the second command.

Write with Auto Precharge to Read command Interval (Different bank)

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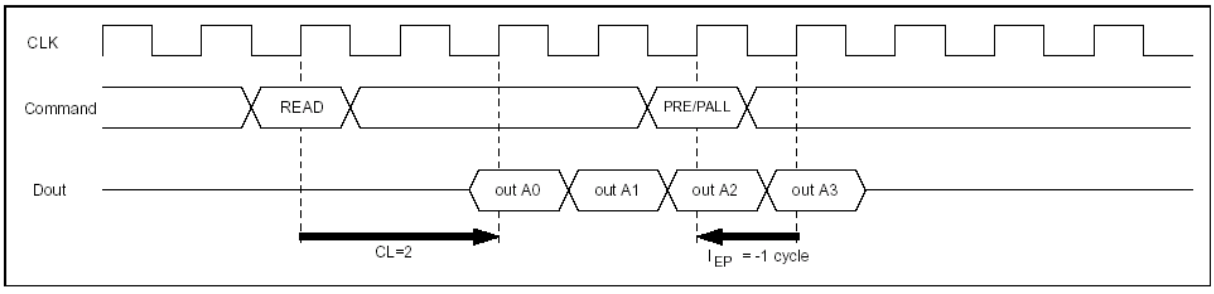
2. Same Bank: The consecutive read command from write with auto precharge (the same bank) is illegal. It is necessary to separate the two commands with a bank active command.

Read command to Precharge command Interval (same bank)

When the precharge command is executed for the same bank as the read command that preceded it, the minimum interval between the two commands is one clock. However, since the output buffer than becomes High-Z after the clock defined by I_{HZP} , there is a case of interruption to burst read data. Output will be interrupted if the precharge command is input during burst read. To read all data by burst read, the clocks defined by I_{EP} must be assured as an interval from the final data output to precharge command execution.

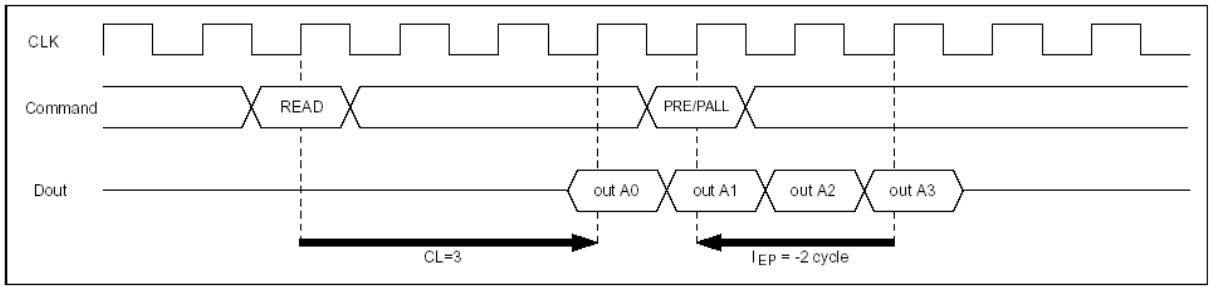
READ to PRECHARGE command Interval (same bank: To output all data)

$\overline{\text{CAS}}$ Latency = 2, Burst Length = 4



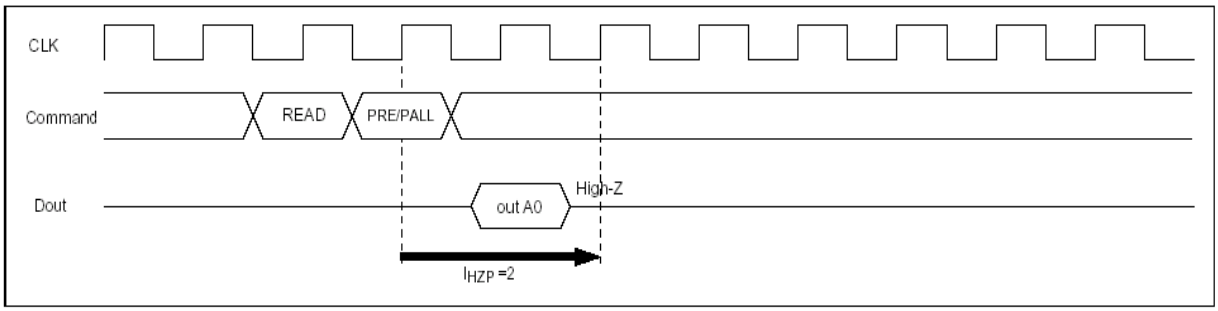
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$\overline{\text{CAS}}$ Latency = 3, Burst Length = 4

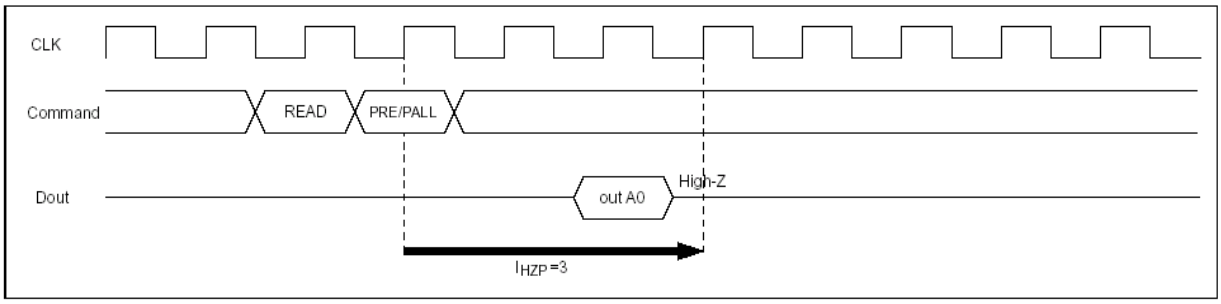


Recharge command Interval (same bank): To stop output data

$\overline{\text{CAS}}$ Latency = 2, Burst Length = 1, 2, 4, 8



$\overline{\text{CAS}}$ Latency = 3, Burst Length = 1, 2, 4, 8

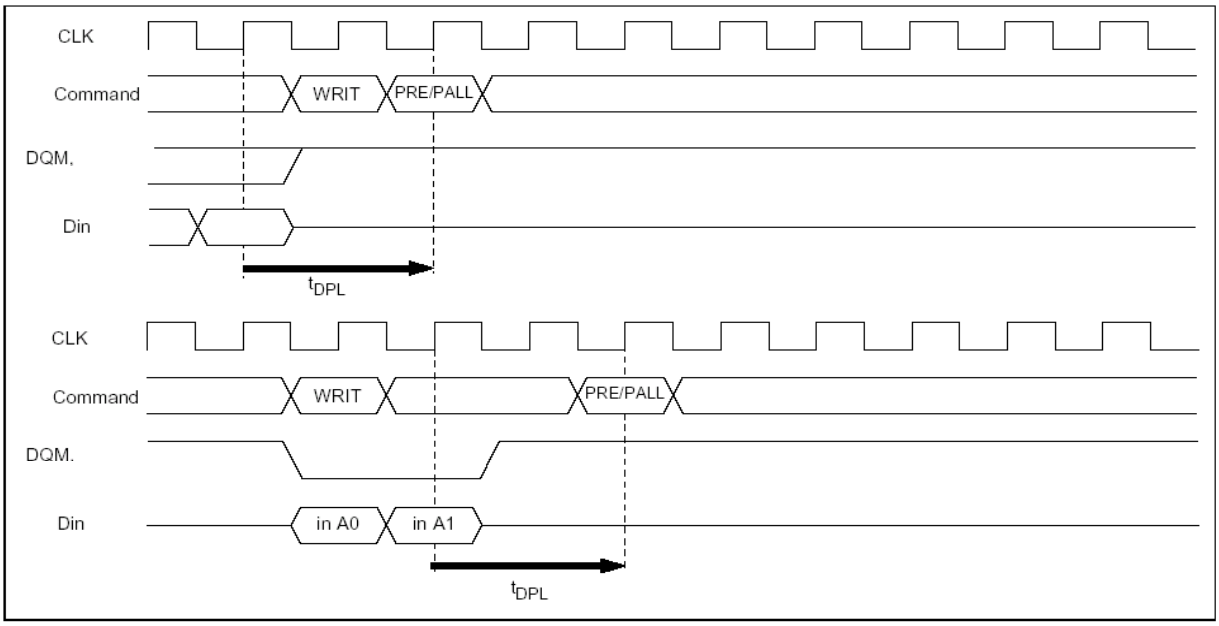


d to Precharge command interval (same bank): When the precharge command is executed for the same bank as the write command that preceded it, the minimum interval between the two commands is 1 clock. However, if the burst write operation is unfinished, the data must be masked by means of DQM1 - DQM4 for assurance of the clock defined by t_{DPL}.

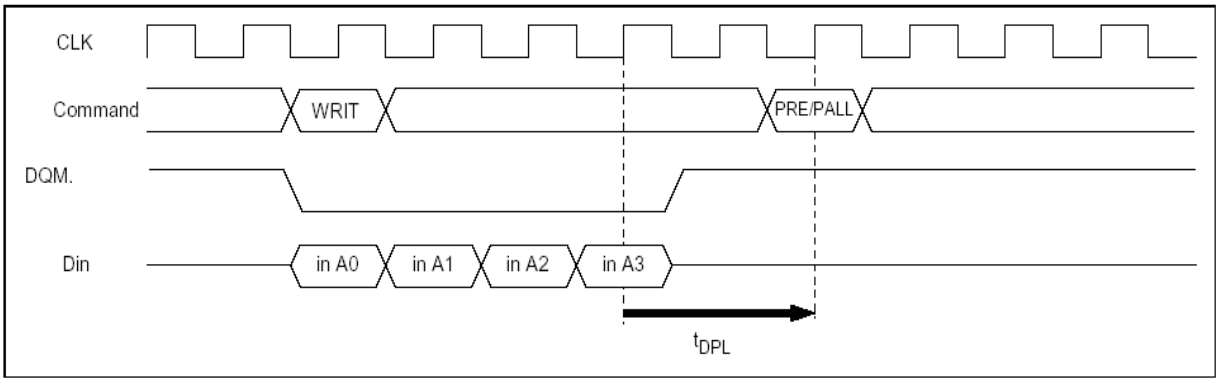
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WRITE to PRECHARGE Command Interval (same bank)

Burst Length = 4 (To stop write operation)



Burst Length = 4 (To write to all data)



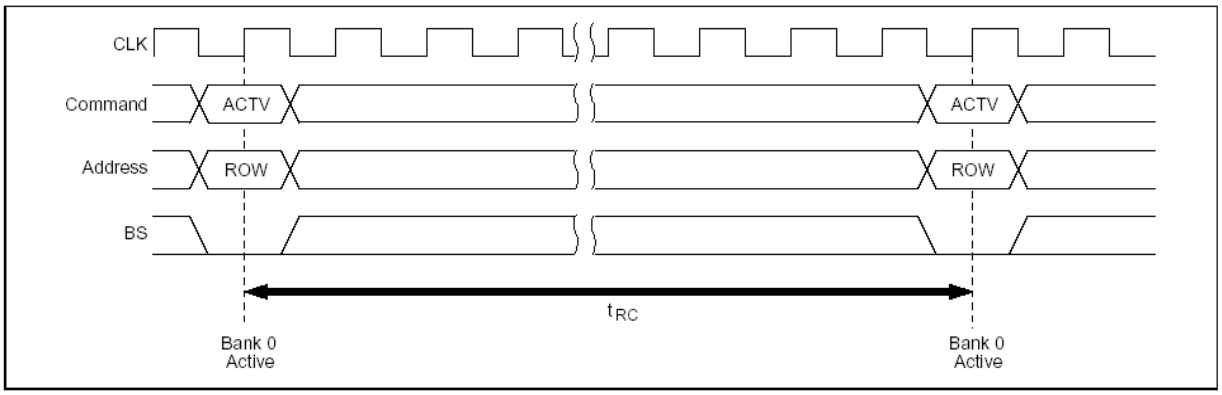
Bank active command interval:

1. Same bank: The interval between the two bank-active commands must be no less than t_{RC}.

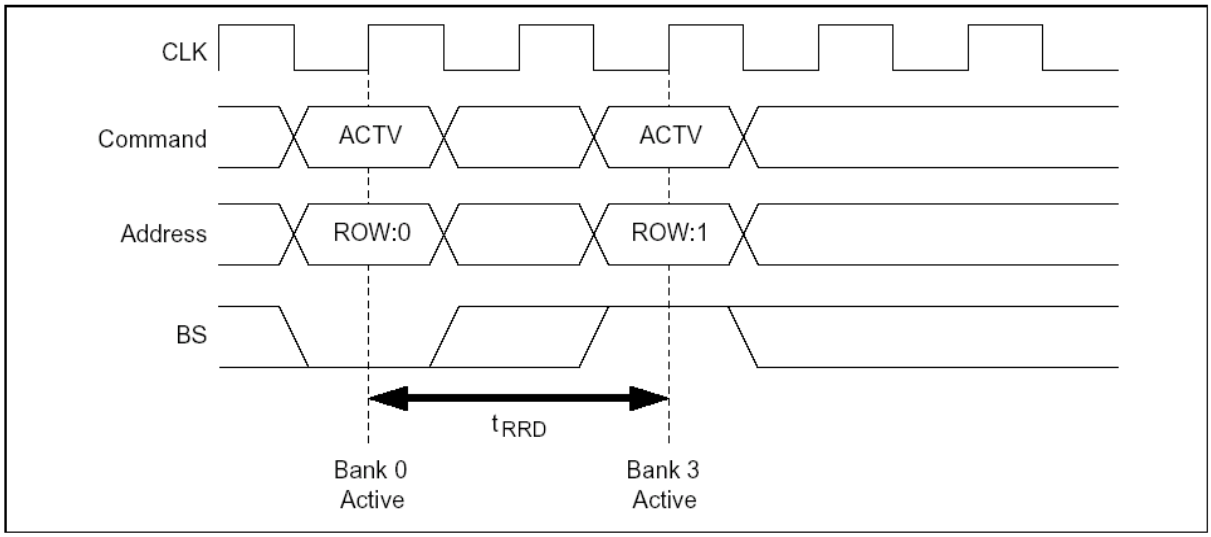
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2. In the case of different bank-active commands: The interval between the two bank-active commands must be no less than t_{RRD}.

Bank Active to Bank Active for Same Bank

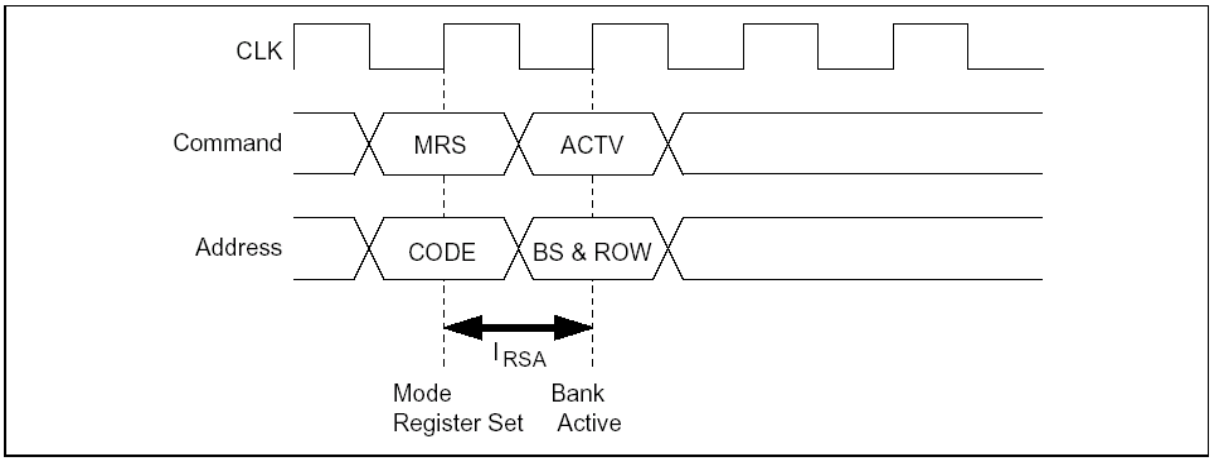


Bank Active to Bank Active for Different Bank



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Mode register set to Bank-active interval: The interval between setting the mode register and executing a bank-active command must be no less than I_{RSA}.



DQM Control

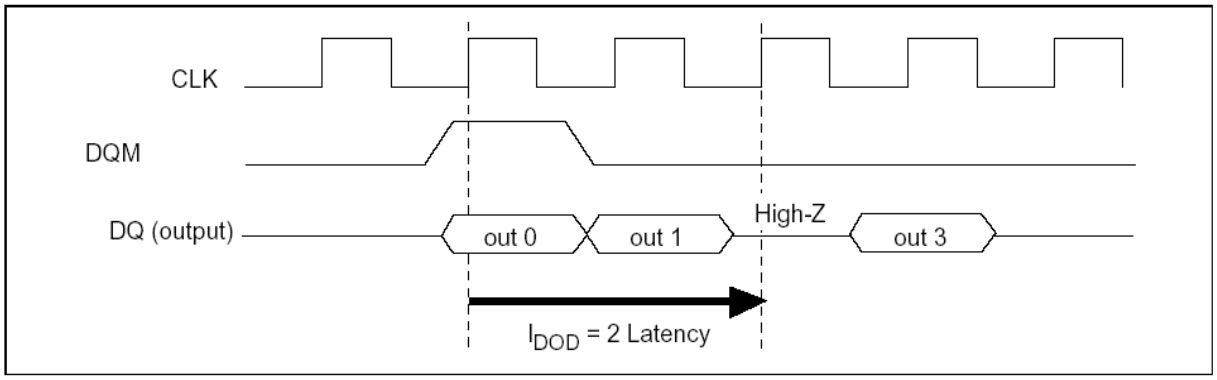
The DQM1 - DQM4 mask the bytes of the DQ data. The timing of DQM1 - DQM4 is different during reading and writing.

Reading: When data is read, the output buffer can be controlled by DQM1 - DQM4. By setting DQM1 - DQM4 to Low, the output buffer becomes Low-Z, enabling data output. By setting DQM1 - DQM4 to High, the output buffer becomes High-Z and the corresponding data is not output. However, internal reading operations continue. The latency of DQM1 - DQM4 during reading is 2 clocks.

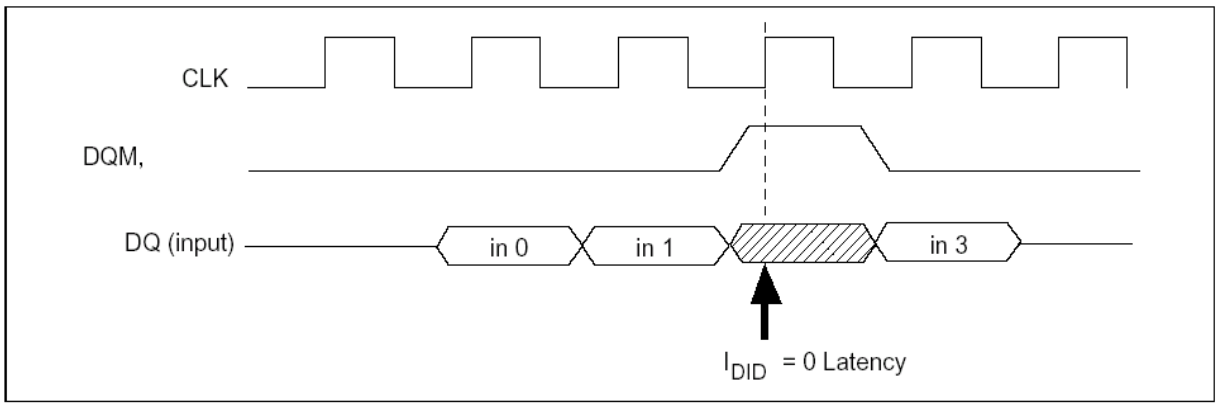
Writing: Input data can be masked by DQM1 - DQM4. By setting DQM1 - DQM4 to Low, data can be written. In addition, when DQM1 - DQM4 is set to High, the corresponding data is not written, and previous data is held. The latency of DQM1 - DQM4 during writing is 0 clock.

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Reading



Writing



Refresh

Auto-Refresh: All the banks must be precharged before executing an auto-refresh command. Since the auto-refresh command updates the internal counter every time it is executed and determines the banks and the ROW addresses to be refreshed, external address specification is not required. The refresh cycle is 8192 cycles / 6.4 ms. (8192 cycles are requires to refresh all the ROW addresses.) The output buffer becomes High-Z after auto-refresh start. In addition, since a precharge has been completed by an internal operation after the auto-refresh, an additional precharge operation by the precharge command is not required.

Self-refresh[1]: After executing a self-refresh command, the self-refresh operation continues while CKE is held Low. During self-refresh operation, all ROW addresses are refreshed by the internal refresh timer. A self-refresh is terminated by a self-refresh exit command. Before and after self-refresh mode, execute auto-refresh to all refresh addresses in or within 6.4 ms period on the condition (1) and (2) below.

1. Use self refresh at temperatures below 70°C only.

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(1) Enter self-refresh mode within 7.8 us after either burst refresh or distributed refresh at equal interval until all refresh addresses are completed.

(2) Start burst refresh or distributed refresh at equal interval to all refresh addreses within 7.8 us after exiting from self-refresh mode.

Others

Power-down mode: The SDRAM enters power-down mode when CKE goes Low in the IDLE state. In power-down mode, power consumption is suppressed by deactivating the input initial circuit. Power-down mode continues while CKE is held Low. In addition, by setting CKE to High, the SDRAM exits from the power-down mode, and command input is enabled from the next clock. In this mode, internal refresh is not performed.

Clock suspend mode: By driving CKE to Low during a bank-active or read/write operation, the SDRAM enters clock suspend mode. During clock suspend mode, external input signals are ignored and the internal state is maintained. When CKE is driven High, the SDRAM terminates clock suspend mode, and command input is enabled from the next clock. For more details, refer to the “CKE Truth Table”.

Power-up sequence: The SDRAM should use the following sequence during power-up:

The CLK, CKE, $\overline{CS}$, DQM1 - DQM4 and DQ pins stay low until power stabilizes.

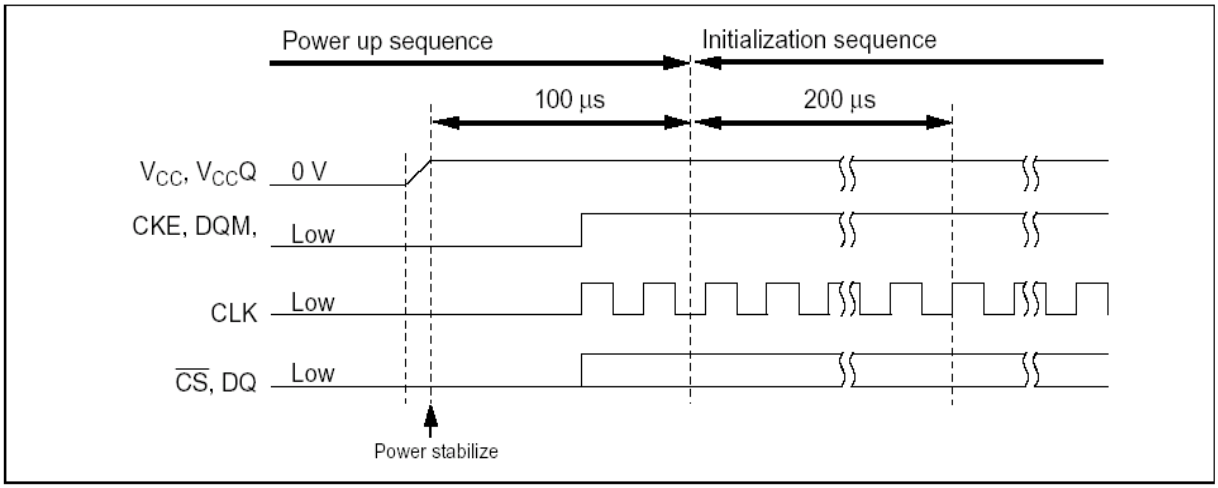
The CLK pin is stable within 100ms after power stabilizes before the following initialization sequence.

The CKE and DQM1 - DQM4 aredriven high between when power stabilizes and the initialization sequence.

This SDRAM has V_{CC} clamp diodes for CLK, CKE, $\overline{CS}$, DQM1 - DQM4 and DQ pins. If these pins go high before power up, the large current flows from these pins to V_{CC} through the diodes.

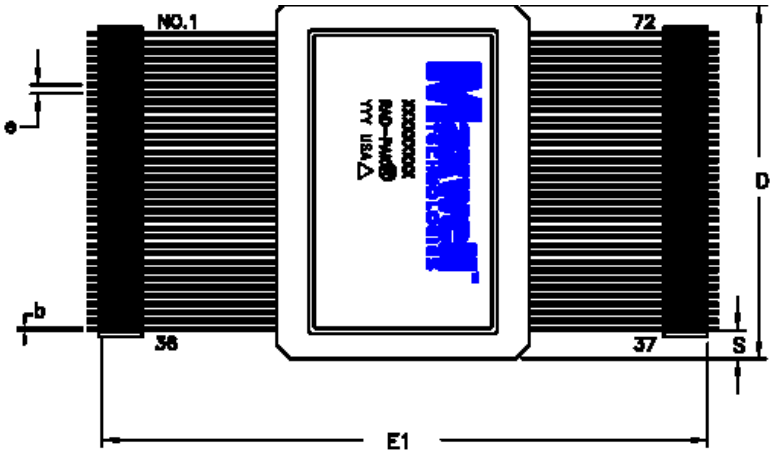
Initialization sequence: When 200ms or more has past after the power up sequence, all banks must be precharged using the precharge command (PALL). After t_{RP} delay, set 8 or more auto refresh commands (REF). Set the mode register set command (MRS) to initialize the mode register. It is recommended that by keeping DQM1 - DQM4 and CKE High, the output buffer becomes High-Z during initialization sequence, to avoid DQ bus contention on a memory system formed with a number of devices.

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Note: All dimensions in inches.





72-PIN RAD-PAC PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	.269	.292	.315
b	.006	.008	.010
c	.006	.008	.010
D	1.142	1.154	1.166
E	.881	.890	.899
E1	--	1.950	--
e		.025	
F1	.030	.035	.040
F2	.125	.130	.135
L		.390	
Q	.070	.074	.079
S	.005	.237	--

Note: All Dimensions in inches.

Important Notice:

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These data sheets are created using the chip manufacturer's published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

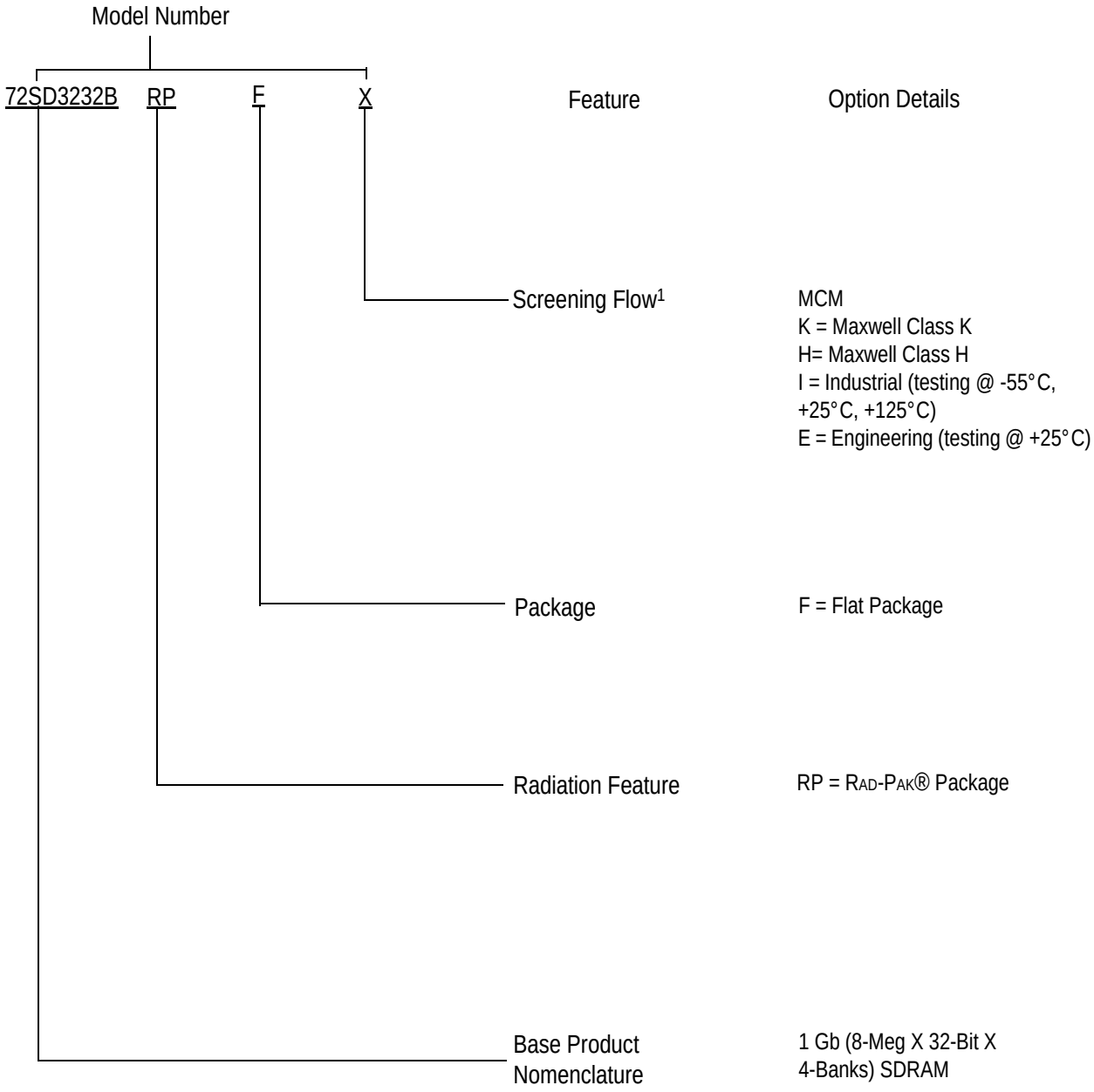
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1) Note: Products are manufactured and screened up to Maxwell Technologies self-defined Class K flow.

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