MXED202
128-Channel OLED Row Driver

Features

- CMOS High Voltage Process: 9V-30V Display Panel Supply Compatible
- 128 Output Channels, Cascadable; Configurable 120-Output Mode
- 150mA Maximum Current Capability per channel (two channels maximum active simultaneously)
- 20 Ohm Maximum Row Switch “On” Resistance
- Token-Based Control: Bidirectional data transfer; Single and Dual-Token Mode
- Current Source Magnitude User Control: 4 µA to 1 mA
- 6-Bit Monochromatic/Color Gray-Scale User Control
- Monochromatic Voltage Precharge Options
- 3.3 V to 5 V logic supply
- Up to 100kHz clock frequency
- Gold-Bumped Die @ ~ 60 micron Output Pitch
- TCP packaging
- Companion to MXED102 240-Channel OLED Column Driver

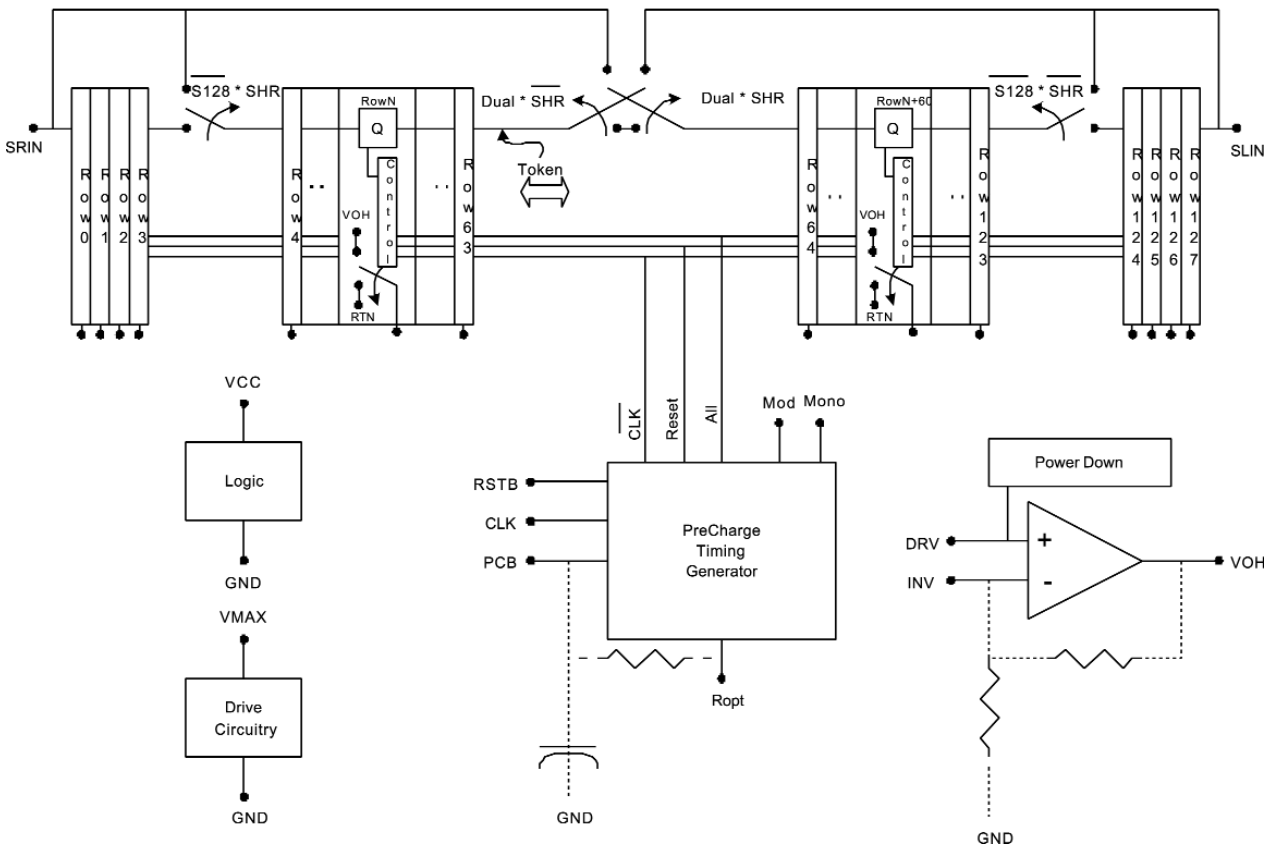
Description

The MXED202 Row Driver supports up to 128-row OLED panel displays. The MXED202 has low "on" switch resistance, and support of voltage precharge options, ensures uniform luminance at rapid row scan rates. This is the first ASSP production row driver for OLED display OEM's, enabling the development and manufacture of this new standard in flat-panel display technology.

For All Passive-Matrix Organic-Light-Emitting-Diode Displays

- Monochrome and Color
- Small-Molecule and Polymer
- Common-Cathode Row Switching

Functional Block Diagram



Preliminary

PRELIMINARY ELECTRICAL DATA SHEET

The MXED202 is a row-multiplexed display driver, for Passive Matrix Organic Light Emitting Diode (OLED) and Polymer Light Emitting Diode arrays (PLED, PolyLED, LEP, . . .), with anodes connected to current-sourcing column data drivers. The common cathode rows (channels) of the display matrix are activated by sequentially switching them to a low impedance voltage source (ground/0V, typically) in synchronism with the digital data column current drive. The MXED202 supports precharging options to improve luminance control. It is manufactured in a high voltage (30 V) CMOS process and provided in bumped die and TCP (Tape Carrier Package) form.

Overview

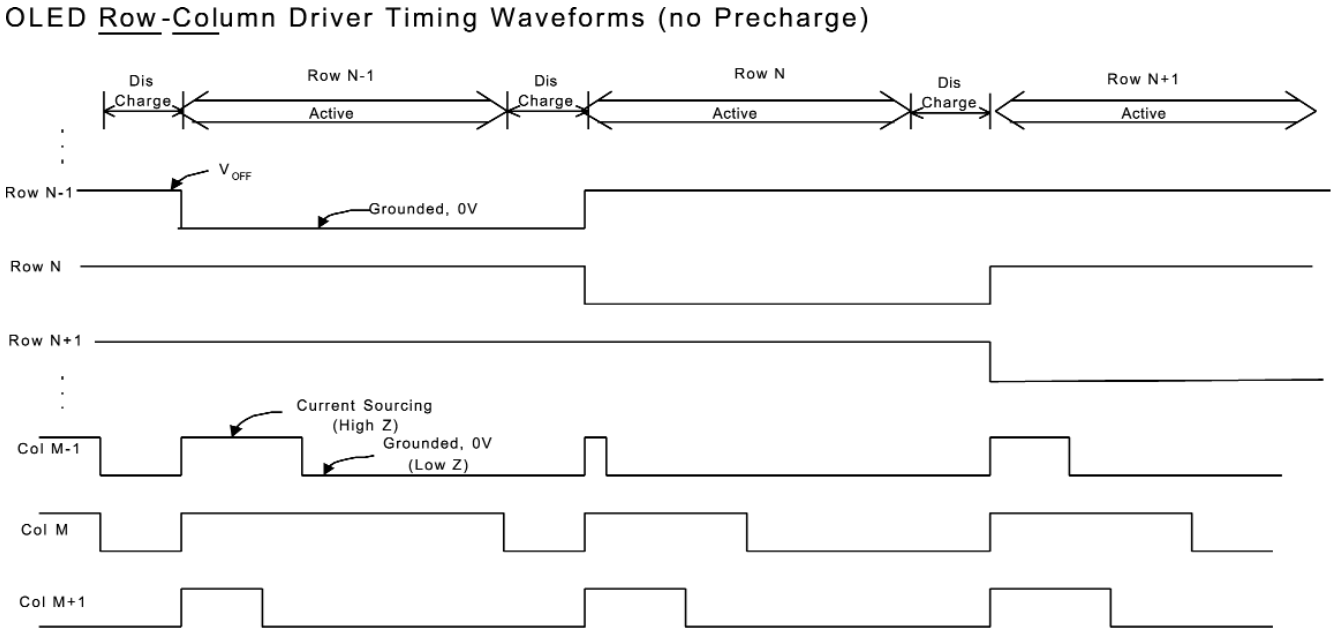
A row-scan token bit is passed along the length of MXED202 shift register to successively activate the row switches. The OLED cathodes of the active row(s) are switched to RTN, a low impedance return, ground or 0V typically, while the companion column drivers source data-driven currents through each OLED to be illuminated. Inactive rows are connected to a programmable "Off" (or Precharge) voltage to ensure the OLED's are not forward-biased. A programmable precharge interval and programmable precharge voltage are available to set initial conditions for the next active row(s).

In normal, or single token mode, the token may be entered at either end of the MXED202 row shift register (SRIN or SLIN), depending on the shift direction selection Shift Right (SHR). The token is shifted one row (one channel) per clock cycle, CLK. One row maximum is active at a time. In dual mode (DUAL), the token is entered at one end and automatically in the center, and again the tokens may be selectively shifted left or right at the CLK rate; two rows maximum are active at a time. The MXED202 has options for 128- and 120-row display panels. When the Select 128 (S128) pin is tied low, the token is also automatically entered at the fifth cell from the entry direction end; only the 120 middle outputs, Rows 4 through 123, should be used. Note that a lesser number of rows may be used by resetting the MXED202 (RSTB) at any time, truncating the shift cycle.

Overview of Operation

A row-scan token bit is passed along the length of MXED202 shift register to successively activate the row switches. The OLED cathodes of the active row(s) are switched to RTN, a low impedance return, ground or 0V typically, while the companion column drivers source data-driven currents through each OLED to be illuminated. Three successive row activations, N-1, N, N+1, are depicted in the simplified timing diagram below. Inactive rows are connected to a programmable "Off" (or Precharge) voltage to ensure the OLED's are not forward-biased. A programmable precharge interval and programmable precharge voltage are available to set initial conditions for the next active row(s). Precharge is described on page 9.

Simplified Timing Diagram



Token:

The row-scan token(s) activate row switches. Token entry positions, 0 to 127, are defined in the table below:

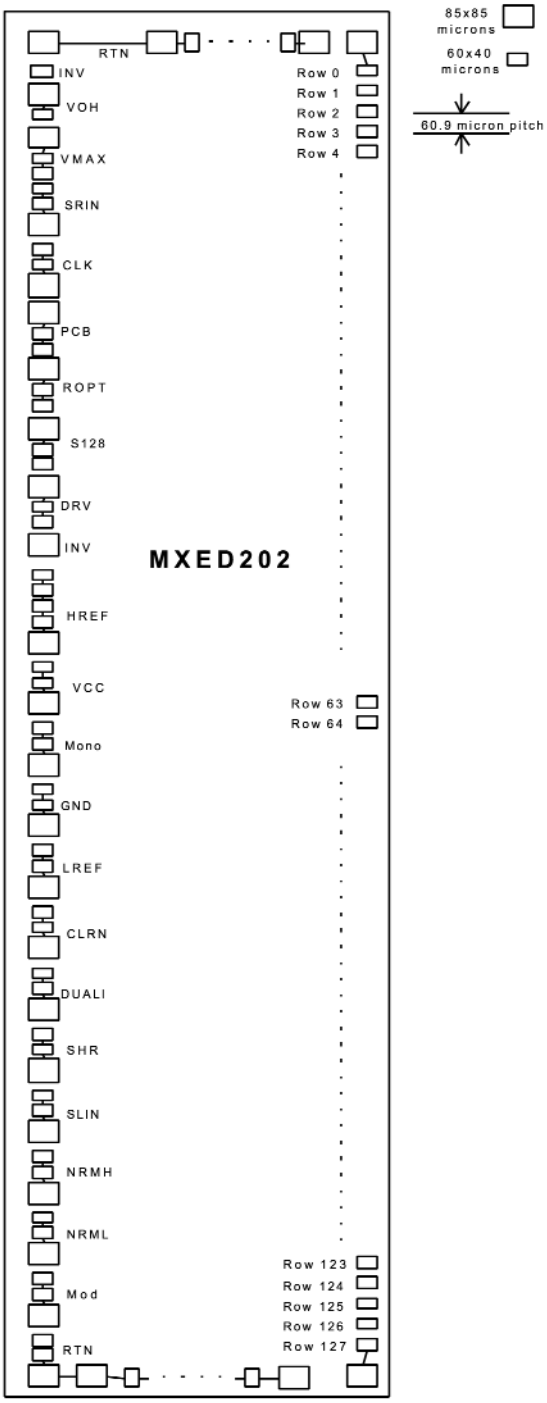
S128	DUAL • SHR				Outputs Used
	00	01	10	11	
0	127,123	0,4	127,123,63	0,4,64	Rows 4-123 (Rows 0-3, 124-127 N/C)
1	127	0	127,63	0,64	Rows 0-127

PACKAGE AND PINOUT

This drawing illustrates the pin ordering and relative locations of the bond pads, only. See the MXED202 Semiconductor Die specification(2) for exact coordinates.

Top View:

---- Not To Scale ----



PIN LIST

Name	I/O/A	Description
RTN	I	ReTurN for all display current. (Low impedance ground connection, typically)
GND	I	GrouND, the negative return for all chip current and the digital logic "zero" refer ence level.
VCC	I	The logic voltage positive supply. MXED202 logic operates between VCC and VSS. Digital inputs should not exceed VCC, VSS
VMAX	I	This Voltage MAXimum is the highest positive power supply voltage present on the chip, and supplies the display panel precharge current either directly or at derived voltage VOH. Inputs to the chip should not exceed VMAX to avoid for ward biasing substrate diodes.
VOH [Page 12]	I/O/A	Row Voltage Output High supply. This pin is normally connected to an external power supply pin VMAX with bypass capacitor, and to pin DRV. Alternatively, an internal amplifier can generate VOH from an input voltage DRV.
INV [Page 12]	I	INVerting input to Voltage Regulator Op Amp, to which an input Resistor RI and feedback Resistor RF may be connected to develop VOH from VDRV; see DRV pin.
DRV [Page 12]	I	When not connected to VOH and VMAX, a Drive Reference Voltage >1V can be connected to the DRV pin.Note: If VDRV <0.3V, all row circuitry is powered down.
SHR	I	Active high static SHift Right control input: When SHR=1, the token bit travels from R0 to R127, with SRIN being the token input, SLIN the token output. When SHR=0, the token bit travels from R127 to R0, with SLIN being the token input, SRIN the token output. SHR should always be driven to the desired logic level.
SRIN	I/O	Shift Right INput. This bi-directional pin is the token input when SHR is high, and the token output (for synchronization or cascading) when SHR is low. When con figured as an input, this pin should always be driven. Normally low, SRIN should be driven high once per frame to enter the token into the shift register.
SLIN	I/O	Shift Left INput. This bi-directional pin is the token input when SHR is low, and the token output (for synchron- ization or cascading) when SHR is high. When configured as an input, this pin should always be driven. Normally low, SLIN should be driven high once per frame to enter the token into the shift register.
DUAL	I	DUAL tokens are seeded into the first and middle shift register cells from SRIN or SLIN when DUAL is static active high. When low, a single token is active.
CLK	I	The rising edge of the CLocK input shifts the token along the internal shift regis ter to activate successive rows. The display Row Scan Rate is the CLK frequen cy times the number of tokens.
PCB [Pages 9-11]	I	If the PreCharge Bar input is low on the rising edge of CLK, all row outputs will be switched to the same voltage (see MONO) to enable display panel precharg ing until PCB returns high. Holding PCB high disables MXED202 precharge.
MONO [Pages 9-11]	I	Enables MXED202 row driver precharge of MONOchromatic displays, if PCB=0. The MONO input has no effect if PCB=1.
MOD [Pages 9-11]	I	This input MODifies precharge timing
S128	I	Select 128 row driver output mode when static active high. When low, 120 row driver output mode is selected.

Pin List (Continued)

ROPT [Pages 10-11]	I/O/A	Resistor OPTion pin, normally N/C for digitally controlled precharge timing (PCB), or when precharge is disabled. When a resistor R is connected between ROPT and PCB, and a capacitor C is connected between PCB and VSS, the precharge time will be RC/1.65 when measured from the rising edge of CLK to the falling edge of ROPT. The timing components should be selected such that RC/1.65 not exceed 10% of the row active time.
RSTB	I	ReSeT Bar, static, active low reset input, clears all the shift register cells, elimi nating token content.
R(n)	O	Row driver outputs. R(0)-R(127) are used in 128 output mode, S128=1. Only R(4)-R(123) should be connected when S128=0.
HREF	O	High voltage REFerence is an internally generated PFET switch drive voltage (approximately five-volts less than VOH), which should be bypassed to VOH with a 2200pF external capacitor.
LREF	O	Low voltage REFerence is an internally generated NFET switch drive voltage (approximately five-volts above GND), which should be bypassed to GND with a 2200pF external capacitor.
NRMH	O	Test Pin, N/C
NRML	O	Test Pin, N/C

ELECTRICAL SPECIFICATION

Note: positive currents flow into the part, negative currents flow out of the part.

Absolute Maximum Ratings:

Parameter	Operating Condition	Min	Typ	Max	Units
Ambient temp	-	-65		155	°C
Low voltage supply	-	-0.3		7.0	V
High voltage supply	-	-0.3		35.0	V

Operating Conditions:

Unless otherwise stated, all parameters are specified for the following operating conditions.

Parameter	Sym	Operating Condition	Min	Typ	Max	Units
Ambient temp	TA	-	0	-	70	°C
Low voltage supply	VCC	-	3.0	-	5.5	V
High voltage supplies	VMAX	-	5.0	-	30	V
Clock Frequency	CLK	-	-	-	100	kHz

Chip Supply Currents - Exclusive of Load

Parameter	Sym	Operating Condition	Min	Typ	Max	Units
Logic Supply, Operating	IVCC	V_{DRV}>1V, f_{CLK}<100kHz 3V<VCC<5.5V	-	140	210	µA
Logic Supply, Powerdown	IVCC	V_{DRV}<0.3V, 3V<VCC<5.5V	-	15	25	µA
High Voltage Supply, Operating	IVMAX	V_{DRV}>1V, f_{CLK}<100kHz 9V<MAX<30V	-	445	700	µA
High Voltage Supply, Powerdown	IVMAX	V_{DRV}<0.3V, 9V<MAX<30V	-	-	20	µA

Digital Inputs: SHR, SRIN, SLIN, DUAL, CLK, PCB, MONO, S128, RSTB

Parameter	Sym	Operating Condition	Min	Typ	Max	Units
Input low voltage	VIL	-	-	-	0.4	V
Input high voltage	VIH	-	VCC-0.4	-	-	V
Input current	II	-	-10	-	10	µA
Clock Rise Time	CLK_{RT}	-	-	-	5	nS
Clock Fall Time	CLK_{FT}	-		-	5	nS
Clock Duty Cycle	$CLK_{\%}$	-	20	-	80	%
Setup Time	T_{Set}	Time in advance of 10% rising edge of CLK that inputs SHR, SRIN, SLIN, DUAL, PCB, MONO, S128, CLRB must be at valid input logic levels to take effect on next clock cycle.	50	-	-	nS
Hold Time	T_{Hold}	Time subsequent to 90% rising edge of CLK that inputs SHR, SRIN, SLIN, DUAL, PCB, MONO, S128, CLRB must be valid to take effect on next rising edge of the clock (CLK).	50	-	-	nS

Digital Outputs: SRIN, SLIN, ROPT

Parameter	Sym	Operating Condition	Min	Typ	Max	Units
Output low voltage	VOL	Iout = 200 µA	-	-	0.4	V
Output high voltage	VOH	Iout = -200 µA	VCC-0.4	-	-	V
Output rise/fall time	TRF	10 to 90 %, Cload = 5 pF	-	-	5	nS
Precharge Timing Resistor connected to pin ROPT	R_{ROPT}	Pages 9-11	50	-	200	kΩ

Analog Inputs: DRV, INV

Parameter	Sym	Operating Condition	Min	Typ	Max	Units
DRV Pin Input Resistance	DRV_{Rin}	-	10	-	-	kΩ
DRV Pin Input Capacitance	DRV_{Cin}	-	-	-	10	pF
Voltage Range of DRV Input	V_{DRV}	-	1.0	-	VMAX-1.5	V
Feedback Resistor from VOH to INV	R_F	-	10	-	100	kΩ
Input Resistor from INV to GND	R_I	-	10	-	100	kΩ
Gain Ratio	R_F / R_I	-	0.1	-	10	-

Analog Outputs: VOH, HREF, LREF, R(n)

Bypass capacitors to GND: CVOH=10µF; CHREF, CLREF =2nF

Parameter	Sym	Operating Condition	Min	Typ	Max	Units
Precharge Voltage	VOH	$Iout_{avg}$= 100 µA, CLOAD=1000pF	5	-	30	V
Precharge Ripple	VOH_{ac}	Voltage Regulator Active, $Iout_{avg}$= 100 µA	-	-	100	mV p-p
Row 0-127 Output Pulldown Resistance	Row_{ON}	VROW < 5V (to enable OLED turn-on)	-	-	20	Ω
Row 0-127 Output Pullup Resistance	Row_{OFF}	VROW > (VOH-2V) (to disable OLED turn-on)	-	-	300	Ω
Row 0-127 Chip Output Capacitance	C_{Row}	Per output	-	-	20	pF

PRECHARGE:

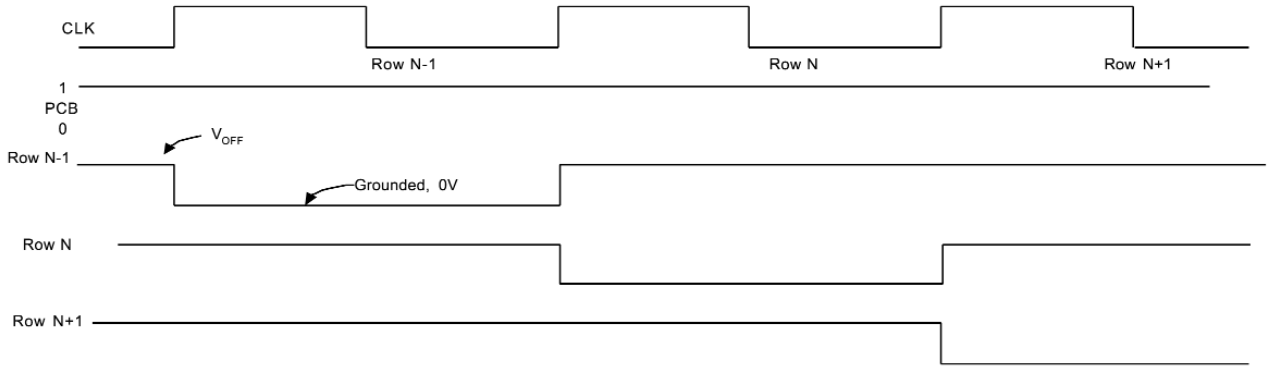
(Organic) Light-Emitting Diodes are current controlled devices, their photonic output (luminance) being proportional to the time-average charge passed through them. To pass charge, the forward voltage must first reach the diode "on" threshold. In passive-matrix panel displays, OLED's are connected in n-row x m-column matrix fashion. In the row multiplex scheme, where a single row of OLED's is activated at a time, the parasitic capacitance of the n-1 "off" rows of OLED's appears connected to the columns - this capacitance must be charged to the "on" threshold before current flows through the selected "on" row diodes. If the column drive current alone were to charge this capacitance, much of the allotted row time would be consumed in just reaching the "on" threshold. Therefore, to improve the efficiency of the display, and to make luminance directly proportional to column current-magnitude and current-duty cycle, the MXED102 and MXED202 Display drivers support optional voltage precharge. In all precharge options, a predetermined voltage is impressed upon the diodes. For instance, the user may configure the precharge voltage to be near the OLED "on threshold," to bias the diodes to the onset of conduction.

The Timing Diagrams, Pages 10-11, illustrate the Prechage Options:

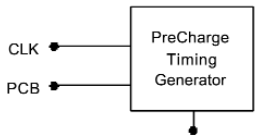
Condition	Precharge
PCB=1	No Precharge
MONO=1	A Monochromatic Precharge voltage may be applied via the MXED202 Row Driver, as a function of CLK, PCB, MOD. During the Discharge interval, all Row and Column driver outputs are grounded, discharging all pixels. At the beginning of the Active interval, a selected Precharge Voltage is applied to all but the next active row, and the column drivers source data-driven currents.
MONO=0	Color/Monochrome Precharge by the MXED102 Column Driver, as function of CLK, PCB.

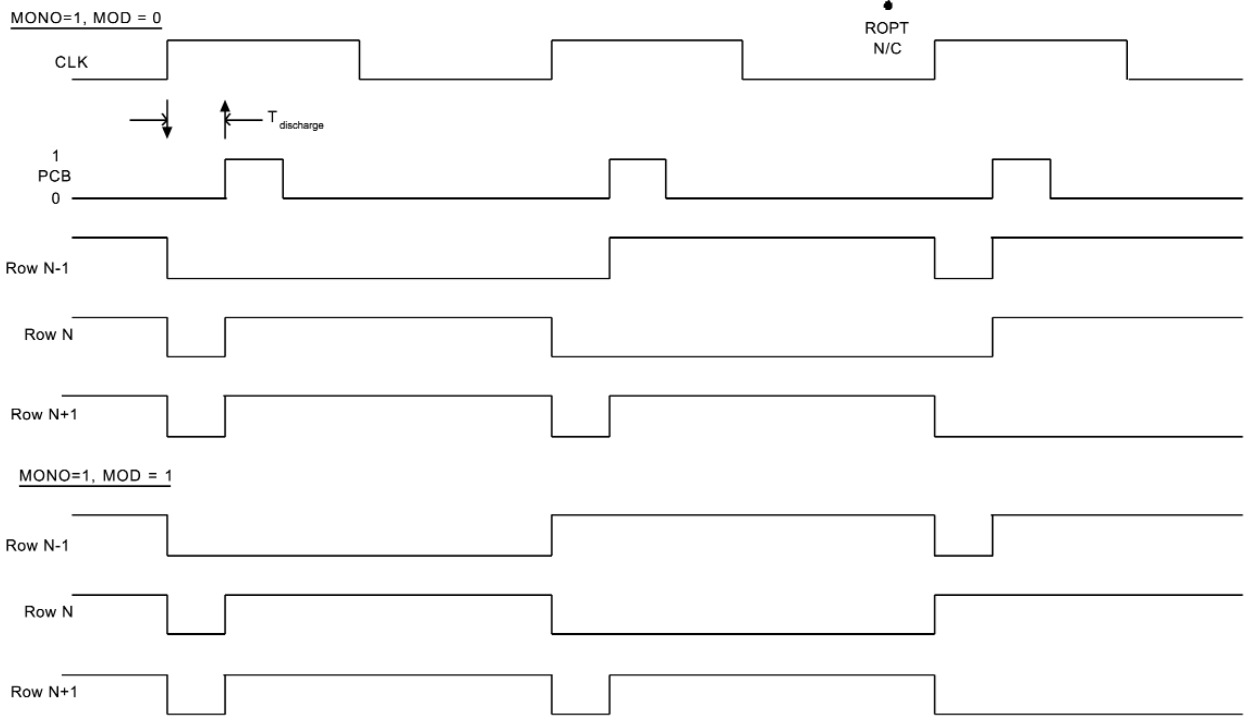
TIMING DIAGRAMS

No Precharge

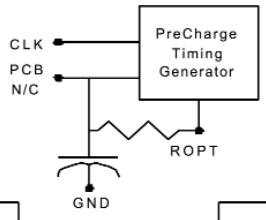


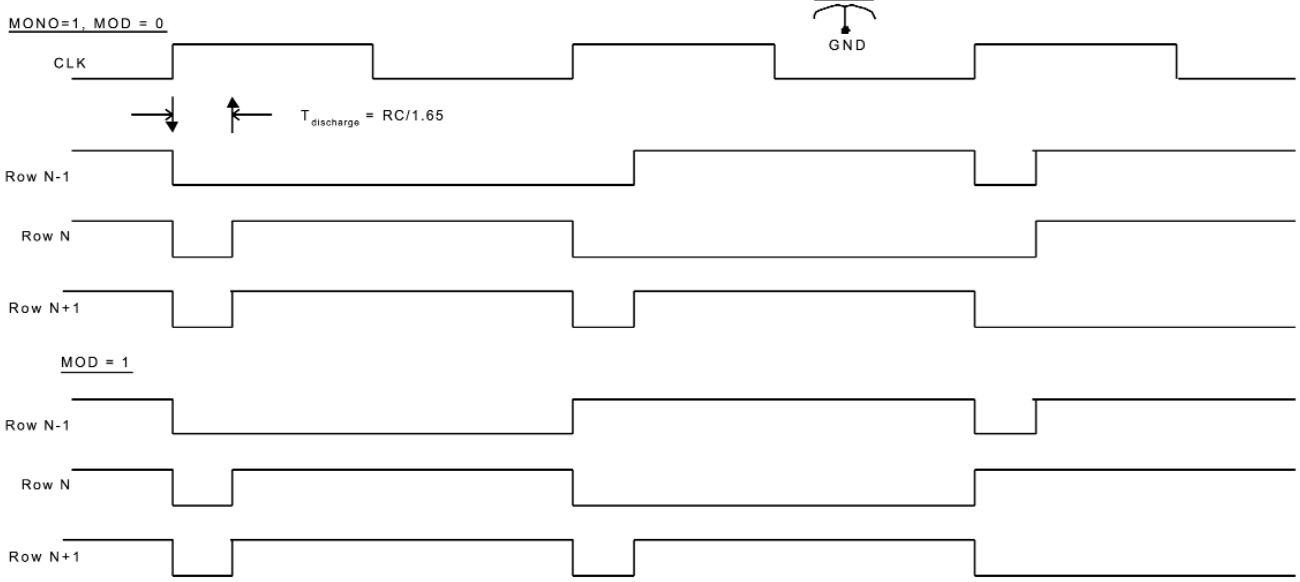
PCB-Driven Precharge; Discharge Time is from rising edge of CLK to rising edge of PCB



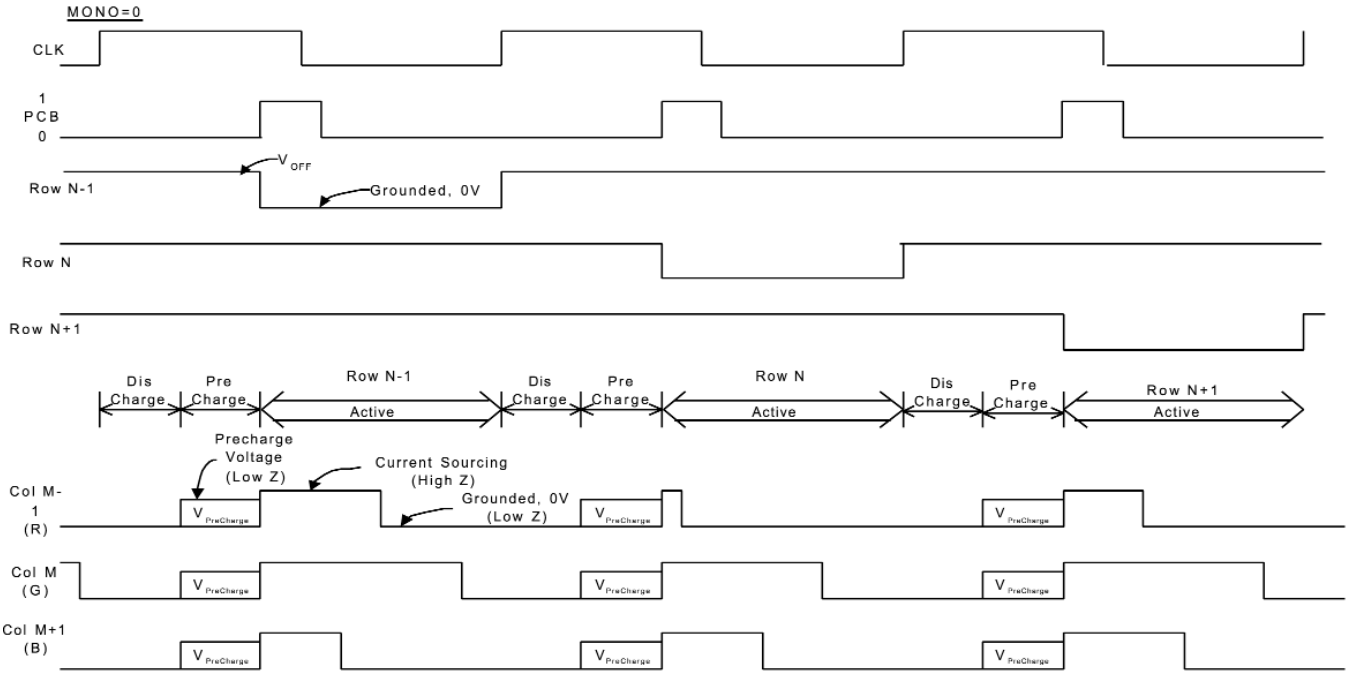


Monostable-Timed Precharge; Discharge Time is from rising edge of CLK to 0.6 RC time constants



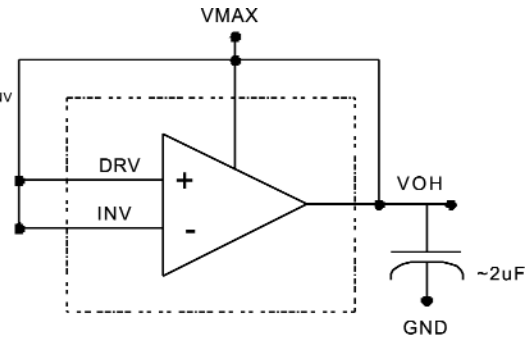


Optional MXED102 Column Driver Discharge and Precharge

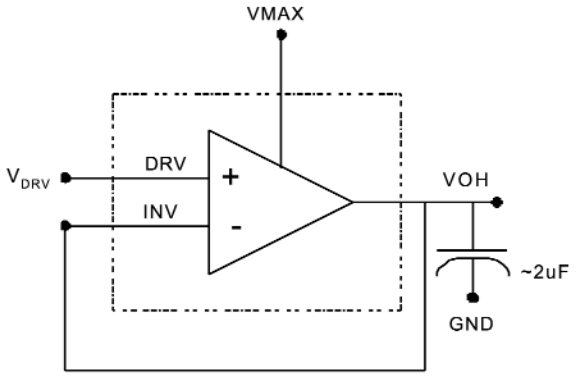


VOH OPTIONS

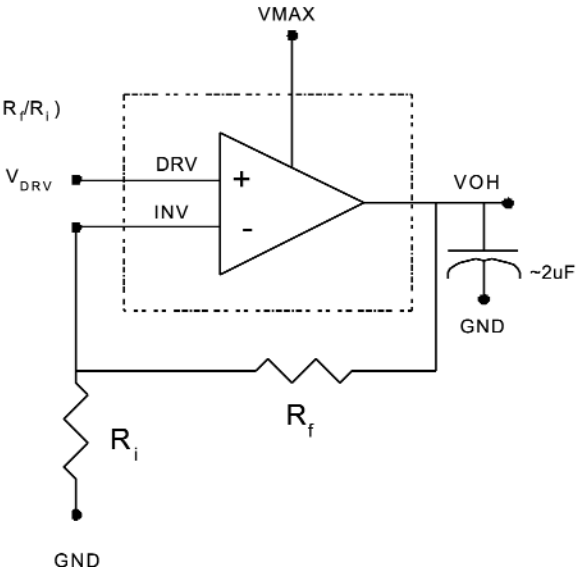
(a) VOH = VMAX , V_{DRV}, V_{INV}



(b) VOH = V_{DRV}



(c) VOH = $V_{DRV}(1 + R_f/R_i)$



SEMICONDUCTOR DIE DATA SHEET

The MXED202 is a common cathode (row) driver for Passive Matrix Organic Light Emitting Diode (OLED) and Polymer Light Emitting Diode (PLED, PolyLED, LEP,…etc.) displays, with anodes connected to the columns. This document specificies the physical and mechanical properties of MXED202 semiconductor die, as provided in wafer form.

DIMENSIONS

Die Size

"X Dimensions" Center Scribe to Center Scribe: 8270 µm

"Y Dimensions" Scribe to Center Scribe: 2300 µm

Die Thickness

Unthinned (Non Back Lapped Wafer) Thickness: 25 mil

BONDING PADS

Locations and Sizes -Driver Outputs

MXED202 PAD LOCATIONS

COORDINATES REFERENCE LOWER LEFT EDGE

	RECT(60X BY 40Y)			RECT(60X BY 40Y)	
Name	X	Y	Name	X	Y
R0	1,882.7	7856.8	R64	1,882.7	3959.2
R1	1,882.7	7795.9	R65	1,882.7	3898.3
R2	1,882.7	7735.0	R66	1,882.7	3837.4
R3	1,882.7	7674.1	R67	1,882.7	3776.5
R4	1,882.7	7613.2	R68	1,882.7	3715.6
R5	1,882.7	7552.3	R69	1,882.7	3654.7
R6	1,882.7	7491.4	R70	1,882.7	3593.8
R7	1,882.7	7430.5	R71	1,882.7	3532.9
R8	1,882.7	7369.6	R72	1,882.7	3472.0
R9	1,882.7	7308.7	R73	1,882.7	3411.1
R10	1,882.7	7247.8	R74	1,882.7	3350.2
R11	1,882.7	7186.9	R75	1,882.7	3289.3
R12	1,882.7	7126.0	R76	1,882.7	3228.4
R13	1,882.7	7065.1	R77	1,882.7	3167.5
R14	1,882.7	7004.2	R78	1,882.7	3106.6
R15	1,882.7	6943.3	R79	1,882.7	3045.7
R16	1,882.7	6882.4	R80	1,882.7	2984.8
R17	1,882.7	6821.5	R81	1,882.7	2923.9
R18	1,882.7	6760.6	R82	1,882.7	2863.0
R19	1,882.7	6699.7	R83	1,882.7	2802.1
R20	1,882.7	6638.8	R84	1,882.7	2741.2
R21	1,882.7	6577.9	R85	1,882.7	2680.3
R22	1,882.7	6517.0	R86	1,882.7	2619.4
R23	1,882.7	6456.1	R87	1,882.7	2558.5
R24	1,882.7	6395.2	R88	1,882.7	2497.6
R25	1,882.7	6334.3	R89	1,882.7	2436.7
R26	1,882.7	6273.4	R90	1,882.7	2375.8
R27	1,882.7	6212.5	R91	1,882.7	2314.9
R28	1,882.7	6151.6	R92	1,882.7	2254.0
R29	1,882.7	6090.7	R93	1,882.7	2193.1
R30	1,882.7	6029.8	R94	1,882.7	2132.2
R31	1,882.7	5968.9	R95	1,882.7	2071.3
R32	1,882.7	5908.0	R96	1,882.7	2010.4
R33	1,882.7	5847.1	R97	1,882.7	1949.5
R34	1,882.7	5786.2	R98	1,882.7	1888.6
R35	1,882.7	5725.3	R99	1,882.7	1827.7
R36	1,882.7	5664.4	R100	1,882.7	1766.8
R37	1,882.7	5603.5	R101	1,882.7	1705.9
R38	1,882.7	5542.6	R102	1,882.7	1645.0
R39	1,882.7	5481.7	R103	1,882.7	1584.1
R40	1,882.7	5420.8	R104	1,882.7	1523.2
R41	1,882.7	5359.9	R105	1,882.7	1462.3
R42	1,882.7	5299.0	R106	1,882.7	1401.4
R43	1,882.7	5238.1	R107	1,882.7	1340.5
R44	1,882.7	5177.2	R108	1,882.7	1279.6
R45	1,882.7	5116.3	R109	1,882.7	1218.7
R46	1,882.7	5055.4	R110	1,882.7	1157.8
R47	1,882.7	4994.5	R111	1,882.7	1096.9
R48	1,882.7	4933.6	R112	1,882.7	1036.0
R49	1,882.7	4872.7	R113	1,882.7	975.1
R50	1,882.7	4811.8	R114	1,882.7	914.2
R51	1,882.7	4750.9	R115	1,882.7	853.3
R52	1,882.7	4690.0	R116	1,882.7	792.4
R53	1,882.7	4629.1	R117	1,882.7	731.5
R54	1,882.7	4568.2	R118	1,882.7	670.6
R55	1,882.7	4507.3	R119	1,882.7	609.7
R56	1,882.7	4446.4	R120	1,882.7	548.8
R57	1,882.7	4385.5	R121	1,882.7	487.9
R58	1,882.7	4324.6	R122	1,882.7	427.0
R59	1,882.7	4263.7	R123	1,882.7	366.1
R60	1,882.7	4202.8	R124	1,882.7	305.2
R61	1,882.7	4141.9	R125	1,882.7	244.3
R62	1,882.7	4081.0	R126	1,882.7	183.4
R63	1,882.7	4020.1	R127	1,882.7	122.5

The information contained on this page is preliminary. Although the order of the bond pad will remain the same, the XY dimensions in the final document may vary slightly. Please take this possibility into consideration when doing any chip on board layouts.

Interface Input/Output

	RECT(60X BY 40Y)			SQ(85X BY 85Y)	
Name	X	Y		X	Y
RTN	0	110.0		0	0.0
	0	170.0			
MOD	0	391.0		0	282.9
	0	451.0			
NRML	0	621.9		0	513.9
	0	681.8			
NRMH	0	852.9		0	744.9
	0	912.8			
SLIN	0	1135.6		0	1027.6
	0	1195.6			
SHR	0	1417.3		0	1309.2
	0	1477.3			
DUAL	0	1699.4		0	1591.3
	0	1759.4			
RSTB	0	1981.4		0	1873.4
	0	2041.4			
LREF	0	2278.0		0	2170.0
	0	2338.0			
GND	0	2518.0		0	2410.0
	0	2578.0			
MONO	0	2800.7		0	2692.6
	0	2860.7			
VPLS	0	3031.6		0	2923.6
	0	3091.5			
HREF	0	3328.3		0	3220.2
	0	3388.3			
	0	3448.3			
	0	3508.3			
INV	NA	NA		0	3571.2
DRV	0	3755.2		0	3878.1
	0	3815.2			
S128	0	4060.7		0	4183.7
	0	4120.7			
ROPT	0	4343.4		0	4466.3
	0	4403.4			
PCB	0	4625.7		0	4748.9
	0	4685.7			
CLK	0	5281.1		0	5173.1
	0	5341.1			
SRIN	0	5563.0		0	5455.2
	0	5623.0			
VMAX	0	6563.2		0	6685.9
	0	6623.2			
VOH	0	7540.6		0	7605.6
INV	0	7778.9		NA	NA
RTN				0	7928.7
R0				1857.7	7946.0
R127				1857.7	-25.0

RECTANGULAR PAD ORIENTATION

	RECT(40X BY 60Y)		SQ(85X BY 85Y)	
Name	X	Y	X	Y
RTN			1557.7	-25
RTN	1497.7	-25		
RTN	1437.7	-25		
RTN	1377.7	-25		
RTN	1317.7	-25		
RTN	1257.7	-25		
RTN	1197.7	-25		
RTN	1137.7	-25		
RTN	1077.7	-25		
RTN	1017.7	-25		
RTN	957.7	-25		
RTN	897.7	-25		
RTN	837.7	-25		
RTN	777.7	-25		
RTN	717.7	-25		
RTN	657.7	-25		
RTN	597.7	-25		
RTN	537.7	-25		
RTN	477.7	-25		
RTN	417.7	-25		
RTN			312.7	-25
RTN			1557.7	7946
RTN	1497.7	7971		
RTN	1437.7	7971		
RTN	1377.7	7971		
RTN	1317.7	7971		
RTN	1257.7	7971		
RTN	1197.7	7971		
RTN			1092.7	7946

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