

4M × 72-Bit Dynamic RAM Module (ECC - Module)

**HYM 724000GS-50/-60
HYM 724010GS-50/-60**

Preliminary Information

- 4 194 304 words by 72-bit ECC - mode organization
- Fast access and cycle time
 - 50 ns access time
 - 90 ns cycle time (-50 version)
 - 60 ns access time
 - 110 ns cycle time (-60 version)
- Fast page mode capability with
 - 35 ns cycle time (-50 version)
 - 40 ns cycle time (-60 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
 - max. 9900 mW active (-50 version)
 - max. 8910 mW active (-60 version)
- CMOS – 165 mW standby
- TTL – 275 mW standby
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only-refresh
- 18 decoupling capacitors mounted on substrate
- All inputs, outputs and clock fully TTL compatible
- 4 Byte interleave enabled, Dual Address inputs (A0/B0)
- Buffered inputs excepts $\overline{\text{RAS}}$ and DQ
- 168 pin, dual read-out, Single in-Line Memory Module
- Utilizes eighteen 4M × 4 -DRAMs in TSOPII-packages and four BiCMOS 8-bit buffers/line drivers 74ABT244
- Two versions : HYM 724000GS with TSOPII-components (4.06 mm thickness)
HYM 724010GS with SOJ-components (8.89 mm thickness)
- 4096 refresh cycles / 64 ms with 12 / 10 addressing
- Gold contact pad
- double sided module with 25.35 mm (1000 mil) height

The HYM 724000/10GS-60/-70 is a 32 MByte DRAM module organized as 4 194 430 words by 72-bit in a 168-pin, dual read-out, single-in-line package comprising eighteen HYB 5116400BT/BJ 4M x 4 DRAMs in 300 mil wide TSOPII or SOJ- packages mounted together with eighteen 0.2 μ F ceramic decoupling capacitors on a PC board. All inputs except RAS and DQ are buffered by using four BiCMOS 8-bit buffers/line drivers.

Each HYB 5116400BT/BJ is described in the data sheet and is fully electrically tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The density and speed of the module can be detected by the use of presence detect pins.

Ordering Information

Type	Ordering Code	Package	Descriptions
HYM 724000GS-50		L-DIM-168-6	50ns DRAM module
HYM 724000GS-60	Q67100-Q2075	L-DIM-168-6	60ns DRAM module
HYM 724010GS-50		L-DIM-168-6	50ns DRAM module
HYM 724010GS-60	Q67100-Q2076	L-DIM-168-6	60ns DRAM module

Pin Names

A0-A11,B0	Address Input
DQ0 - DQ71	Data Input/Output
RAS0, RAS2	Row Address Strobe
CAS0, CAS2	Column Address Strobe
WE0, WE2	Read / Write Input
OE0, OE2	Output Enable
Vcc	Power (+5 Volt)
Vss	Ground
PD1 - PD8	Presence Detect Pins
PDE	Presence Detect Enable
ID0, ID1	ID identification bit
N.C.	No Connection

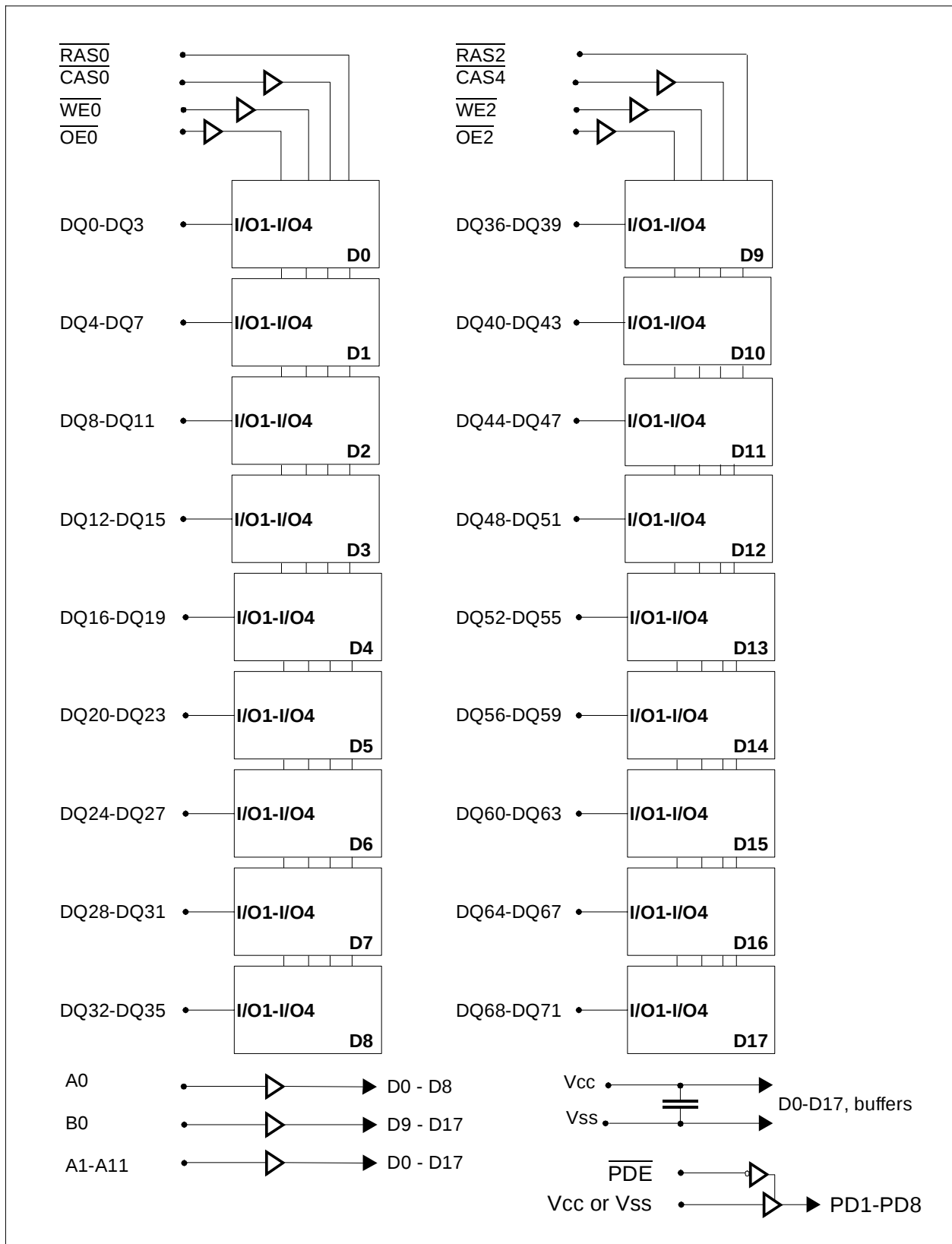
Presence-Detect and ID-pin Truth Table:

Module	ID0	ID1	PD1	PD2	PD3	PD4	PD5	PD6	PD7	PD8
HYM 724000GS-50	Vss	Vss	1	1	0	1	0	0	0	0
HYM 724000GS-60	Vss	Vss	1	1	0	1	0	1	1	0

Note: 1 = High Level (Driver Output) , 0 = Low Level (Driver Output) for $\overline{\text{PDE}}$ active (ground) . For $\overline{\text{PDE}}$ at a high level all PD terminal are in tri-state.

Pin Configuration

PIN #	Symbol	PIN #	Symbol	PIN #	Symbol	PIN #	Symbol
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	OE2	86	DQ36	128	NC
3	DQ1	45	RAS2	87	DQ37	129	NC
4	DQ2	46	CAS4	88	DQ38	130	NC
5	DQ3	47	NC	89	DQ39	131	NC
6	VCC	48	WE2	90	VCC	132	PDE
7	DQ4	49	VCC	91	DQ40	133	VCC
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	VCC	101	DQ49	143	VCC
18	VCC	60	DQ24	102	VCC	144	DQ60
19	DQ14	61	NC	103	DQ50	145	NC
20	DQ15	62	NC	104	DQ51	146	NC
21	DQ16	63	NC	105	DQ52	147	NC
22	DQ17	64	NC	106	DQ53	148	NC
23	VSS	65	DQ25	107	VSS	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	VCC	68	VSS	110	VCC	152	VSS
27	WE0	69	DQ28	111	NC	153	DQ64
28	CAS0	70	DQ29	112	NC	154	DQ65
29	NC	71	DQ30	113	NC	155	DQ66
30	RAS0	72	DQ31	114	NC	156	DQ67
31	OE0	73	VCC	115	NC	157	VCC
32	VSS	74	DQ32	116	VSS	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	A11	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	VCC	82	PD7	124	VCC	166	PD8
41	NC	83	ID0 (VSS)	125	NC	167	ID1 (VSS)
42	NC	84	VCC	126	B0	168	VCC



Block Diagram

Absolute Maximum Ratings

Operating temperature range 0 to + 70 °C
 Storage temperature range..... – 55 to + 125 °C
 Input/output voltage -0.5 to min (V_{CC}+0.5, 7.0) V
 Power supply voltage..... – 1 to + 7 V
 Power dissipation..... 12,60 W
 Data out current (short circuit) 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V _{IH}	2.4	5.5	V	1)
Input low voltage	V _{IL}	– 1.0	0.8	V	1)
Output high voltage (I _{OUT} = – 5 mA)	V _{OH}	2.4	–	V	1)
Output low voltage (I _{OUT} = 4.2 mA)	V _{OL}	–	0.4	V	1)
Input leakage current (0 V < V _{IN} < 6.5 V, all other pins = 0 V)	I _{I(L)}	– 10	10	μA	1)
Output leakage current (DO is disabled, 0 V < V _{OUT} < 5.5 V)	I _{O(L)}	– 10	10	μA	1)
Average V _{CC} supply current: –50 version –60 version ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, address cycling, t _{RC} = t _{RC} min.)	I _{CC1}	– –	1800 1620	mA mA	2) 3) 4)
Standby V _{CC} supply current ($\overline{\text{RAS}}$ = $\overline{\text{CAS}}$ = V _{IH})	I _{CC2}	–	50	mA	–
Average V _{CC} supply current during $\overline{\text{RAS}}$ only refresh cycles: –50 version –60 version ($\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ = V _{IH} , t _{RC} = t _{RC} min.)	I _{CC3}	– –	1800 16	mA mA	2) 4)

DC Characteristics (cont'd) ¹⁾

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during fast page mode: -50 version -60 version ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, address cycling $t_{PC} = t_{PC \text{ min.}}$)	I_{CC4}	— — —	720 630	mA mA	2) 3) 4)
Standby V_{CC} supply current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2 \text{ V}$)	I_{CC5}	—	30	mA	—
Average V_{CC} supply current during CAS-before-RAS refresh mode: -50 version -60 version ($\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC \text{ min.}}$)	I_{CC6}	— —	1800 1620	mA mA	2) 4)

Capacitance

$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$; $V_{CC} = 5 \text{ V} \pm 10 \%$; $f = 1 \text{ MHz}$

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11, B0)	C_{I1}	—	10	pF
Input capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I2}	—	50	pF
Input capacitance ($\overline{CAS0}$ - $\overline{CAS7}$)	C_{I3}	—	15	pF
Input capacitance ($\overline{WE0}$, $\overline{WE2}$, $\overline{OE0}$, $\overline{OE2}$)	C_{I4}	—	15	pF
I/O capacitance (DQ0-DQ71)	C_{IO1}	—	15	pF

AC Characteristics (note: 5,6,7,8)

$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$, $V_{CC} = 5.0 \pm 10 \%$

Parameter	Symbol	-50		-60		Unit	Note
		min.	max.	min.	max.		

common parameters

Random read or write cycle time	t_{RC}	90	—	110	—	ns	
RAS precharge time	t_{RP}	30	—	40	—	ns	
RAS pulse width	t_{RAS}	50	100k	60	100k	ns	
CAS pulse width	t_{CAS}	13	100k	15	100k	ns	
Row address setup time	t_{ASR}	5	—	5	—	ns	9
Row address hold time	t_{RAH}	8	—	8	—	ns	10
Column address setup time	t_{ASC}	2	—	2	—	ns	11
Column address hold time	t_{CAH}	15	—	15	—	ns	9
RAS to CAS delay time	t_{RCD}	16	32	18	40		12
RAS to column address delay time	t_{RAD}	11	20	13	25	ns	12
RAS hold time	t_{RSH}	18	—	20	—	ns	9
CAS hold time	t_{CSH}	48	—	58	—	ns	10
CAS to RAS precharge time	t_{CRP}	10	—	10	—	ns	9
Transition time (rise and fall)	t_T	3	30	3	30	ns	7
Refresh period	t_{REF}	—	64	—	64	ms	

Read Cycle

Access time from RAS	t_{RAC}	—	50	—	60	ns	13,14
Access time from CAS	t_{CAC}	—	18	—	20	ns	9,13,14
Access time from column address	t_{AA}	—	30	—	35	ns	9,13, 15
OE access time	t_{OEA}	—	18	—	20	ns	9,13
Column address to RAS lead time	t_{RAL}	30	—	35	—	ns	9
Read command setup time	t_{RCS}	2	—	2	—	ns	11
Read command hold time	t_{RCH}	2	—	2	—	ns	11,16
Read command hold time referenced to RAS	t_{RRH}	0	—	0	—	ns	16
CAS to output in low-Z	t_{CLZ}	2	—	2	—	ns	11,13
Output buffer turn-off delay	t_{OFF}	—	18	—	20	ns	9,17
Output buffer turn-off delay from OE	t_{OEZ}	—	18	—	20	ns	9,17

AC Characteristics (cont'd)(note: 5,6,7,8)

$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$, $V_{CC} = 5.0 \pm 10 \%$

Parameter	Symbol	-50		-60		Unit	Note
		min.	max.	min.	max.		
CAS delay time from Din	t_{DZC}	0	—	0	—	ns	18
Data to $\overline{OE}$ low delay	t_{DZO}	0	—	0	—	ns	18
$\overline{CAS}$ high to data delay	t_{CDD}	18	—	20	—	ns	9,19
$\overline{OE}$ high to data delay	t_{ODD}	18	—	20	—	ns	9,19

Write Cycle

Write command hold time	t_{WCH}	13	—	15	—	ns	9
Write command pulse width	t_{WP}	8	—	10	—	ns	
Write command setup time	t_{WCS}	2	—	2	—	ns	11,20
Write command to $\overline{RAS}$ lead time	t_{RWL}	18	—	20	—	ns	9
Write command to $\overline{CAS}$ lead time	t_{CWL}	13	—	15	—	ns	
Data setup time	t_{DS}	-2	—	-2	—	ns	10,21
Data hold time	t_{DH}	15	—	15	—	ns	9,21

Read-Modify-Write Cycle

Read-write cycle time	t_{RWC}	131	—	155	—	ns	9
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	70	—	82	—	ns	11,21
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	33	—	37	—	ns	11,21
Column address to $\overline{WE}$ delay time	t_{AWD}	45	—	52	—	ns	11,21
$\overline{OE}$ command hold time	t_{OEH}	11	—	13	—	ns	10

Fast Page Mode Cycle

Fast page mode cycle time	t_{PC}	35	—	40	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	35	—	40	ns	9,13
$\overline{RAS}$ pulse width	t_{RAS}	50	200k	60	200k	ns	
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHCP}	35	—	40	—	ns	9

AC Characteristics (cont'd)(note: 5,6,7,8)

$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$, $V_{CC} = 5.0 \pm 10 \%$

Parameter	Symbol	-50		-60		Unit	Note
		min.	max.	min.	max.		

Fast Page Mode Read-Modify-Write Cycle

Fast page mode read-write cycle time	t_{PRWC}	73	—	82	—	ns	11
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$	t_{CPWD}	50	—	57	—	ns	11,21

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle

$\overline{\text{CAS}}$ setup time	t_{CSR}	7	—	7	—	ns	11
$\overline{\text{CAS}}$ hold time	t_{CHR}	8	—	8	—	ns	10
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t_{RPC}	5	—	5	—	ns	
Write to $\overline{\text{RAS}}$ precharge time	t_{WRP}	12	—	12	—	ns	11
Write hold time referenced to $\overline{\text{RAS}}$	t_{WRH}	8	—	8	—	ns	10

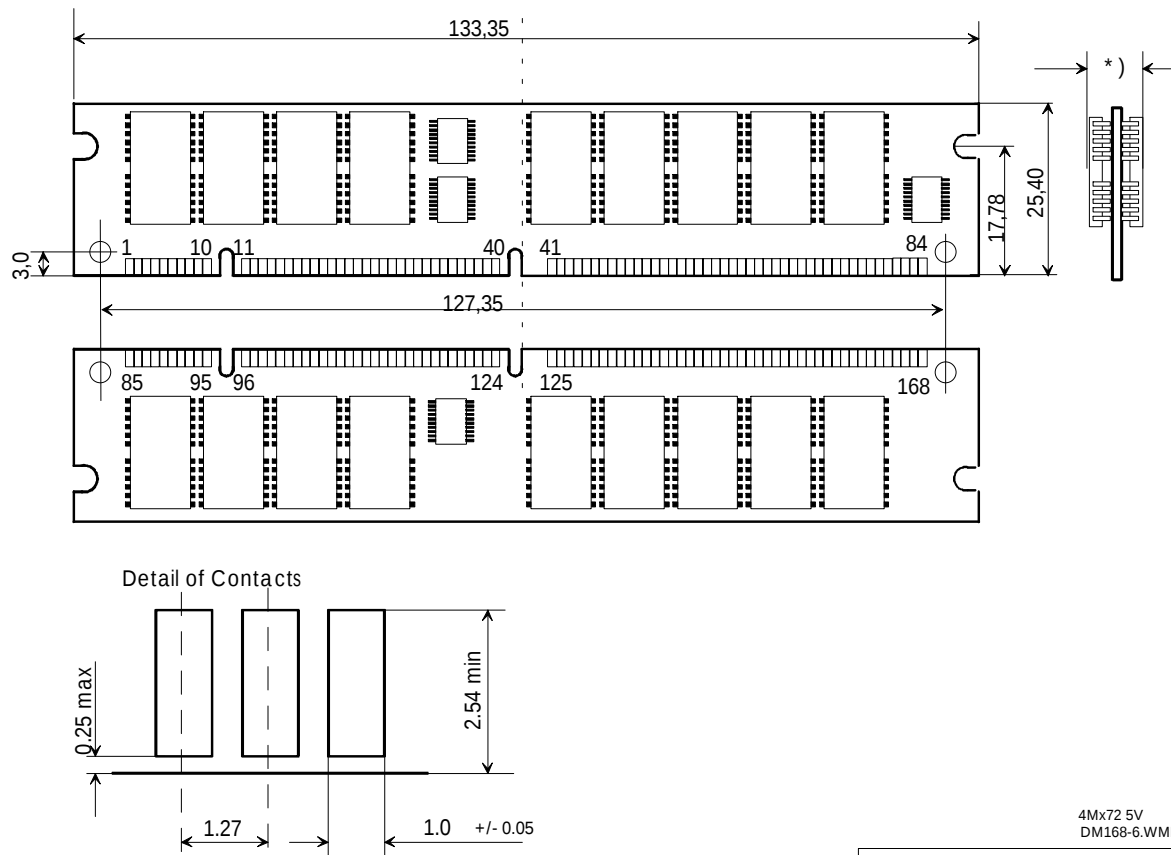
Presence Detect Read Cycle

$\overline{\text{PDE}}$ to valid presence detect data	t_{PD}	—	10	—	10	ns	
$\overline{\text{PDE}}$ inactive to presence detects inactive	$t_{PD OFF}$	0	10	0	10	ns	

Notes:

- 1) All voltages are referenced to VSS.
- 2) ICC1, ICC3, ICC4 and ICC6 and ICC7 depend on cycle rate.
- 3) ICC1 and ICC4 depend on output loading. Specified values are measured with the output open.
- 4) Address can be changed once or less while $\overline{\text{RAS}} = \text{Vil}$. In the case of ICC4 it can be changed once or less during a fast page mode cycle (tpc).
- 5) An initial pause of 100 μs is required after power-up followed by 8 RAS-only-refresh cycles, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.
- 6) AC measurements assume $t_T = 5 \text{ ns}$.
- 7) VIH (min.) and VIL (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between VIH and VIL .
- 8) The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns ($\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$, addresses) maximum delay, no pulse shrinkage to the DRAM device timings. The data and RAS signals are not buffered, which preserves the DRAMs access specification of 50ns and 60ns.
- 9) A +5ns timing skew from the DRAM to the module resulted from the addition of line drivers.
- 10) A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
- 11) A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
- 12) A -2ns (min.) and a -5ns (max.) timing skew from the DRAM to the module resulted from the addition of line drivers.
- 13) Measured with the specified current load and 100 pF at $\text{Voh} = 2.4 \text{ V}$ and $\text{Vol} = 0.4 \text{ V}$.
- 14) Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC} .
- 15) Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA} .
- 16) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- 17) t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
- 18) Either t_{DZC} or t_{DZO} must be satisfied.
- 19) Either t_{CDD} or t_{ODD} must be satisfied.
- 20) t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} > t_{\text{WCS}} (\text{min.})$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{\text{RWD}} > t_{\text{RWD}} (\text{min.})$, $t_{\text{CWD}} > t_{\text{CWD}} (\text{min.})$, $t_{\text{AWD}} > t_{\text{AWD}} (\text{min.})$ and $t_{\text{CPWD}} > t_{\text{CPWD}} (\text{min.})$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
- 21) These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in Read-Modify-Write cycles.

L-DIM-168-6
Module package
(dual read-out, single in-line memory module)



preliminary drawing

*) 9 mm thickness for modules assembled with SOJ-devices
4mm thickness for modules assembled with TSOPII-devices