Data Sheet | October 1999 | File Number 1490.2

-6A, -80V and -100V, 0.600 Ohm, P-Channel Power MOSFETs

These are P-Channel enhancement mode silicon gate power field effect transistors designed for high speed applications such as switching regulators, switching convertors, relay drivers, and drivers for high power bipolar switching transistors.

Formerly developmental type TA09046.

Ordering Information

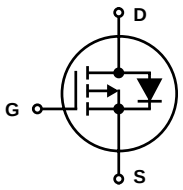
PART NUMBER	PACKAGE	BRAND
RFP6P08	TO-220AB	RFP6P08
RFP6P10	TO-220AB	RFP6P10

NOTE: When ordering, include the entire part number.

Features

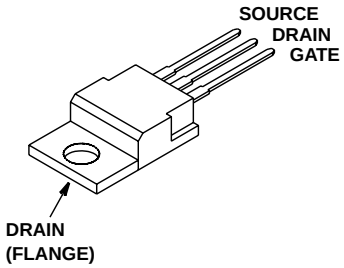
- -6A, -80V and -100V
- $r_{DS(ON)} = 0.600\Omega$
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

JEDEC TO-220AB



CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD Handling Procedures.
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Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFP6P08	RFP6P10	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	80	100	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	80	100	V
Continuous Drain Current				
RMS Continuous	I_D	6	6	A
Pulsed Drain Current (Note 3)	I_{DM}	20	20	A
Gate to Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation	P_D	60	60	W
Linear Derating Factor		0.48	0.48	$W/^oC$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 150	-55 to 150	^oC
Maximum Temperature for Soldering				
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	300	^oC
Package Body for 10s, See Techbrief 334 (for TO-220AB)	T_{pkg}	260	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V				
RFP6P08			-80	-	-	V
RFP6P10			-100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250µA (Figure 7)	-2	-	-4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}	-	-	1	µA
		V_{DS} = 0.8 x Rated BV_{DSS} ($T_C = 125^oC$)	-	-	25	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 6A, V_{GS} = -10V (Figures 5, 6)	-	-	0.6	Ω
Drain to Source On Voltage (Note 2)	$V_{DS(ON)}$	I_D = 6A, V_{GS} = -10V	-	-	-3.6	V
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, $I_D \approx$ 6A R_G = 50Ω, R_L = 16Ω V_{GS} = -10V (Figures 13, 14)	-	11	60	ns
Rise Time	t_r		-	48	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	102	150	ns
Fall Time	t_f		-	70	100	ns
Input Capacitance	C_{ISS}	V_{DS} = 25V V_{GS} = 0V f = 1MHz (Figure 8)	-	-	800	pF
Output Capacitance	C_{OSS}		-	-	350	pF
Reverse-Transfer Capacitance	C_{RSS}		-	-	150	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	RFP6P08, RFP6P10	-	-	2.083	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = -3A	-	-	-1.4	V
Reverse Recovery Time	t_{rr}	I_{SD} = 4A, dI_{SD}/dt = 50A/µs	-	150	-	ns

NOTES:

2. Pulse Test: Pulse Duration ≤ 300µs max, Duty Cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves

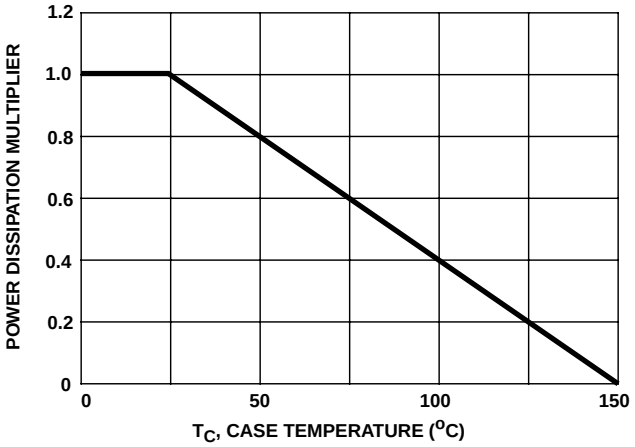


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

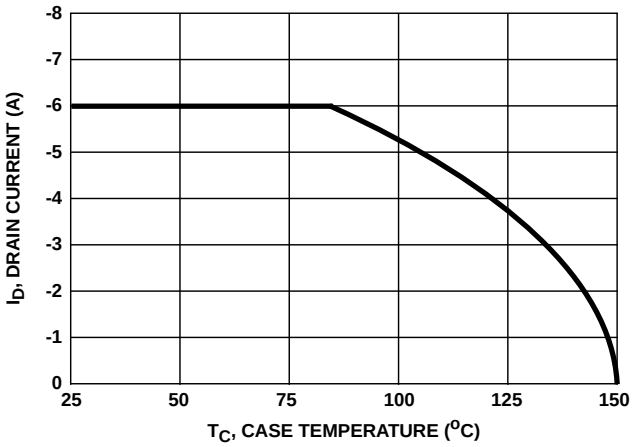


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

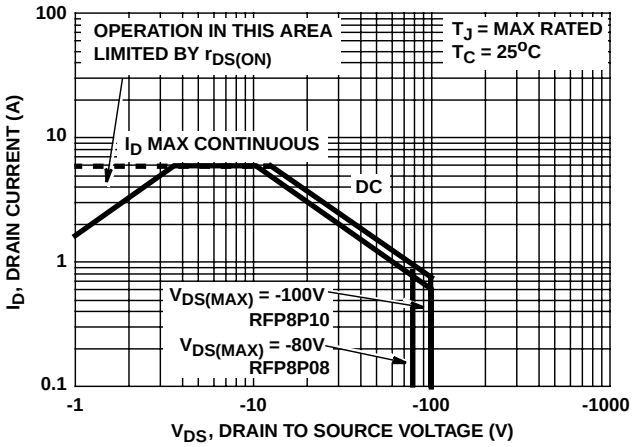


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

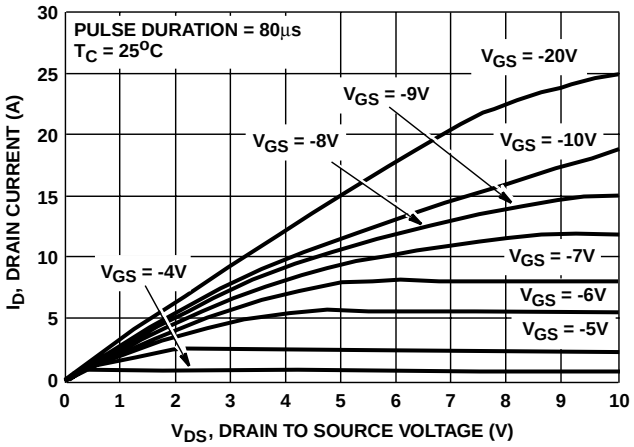


FIGURE 4. SATURATION CHARACTERISTICS

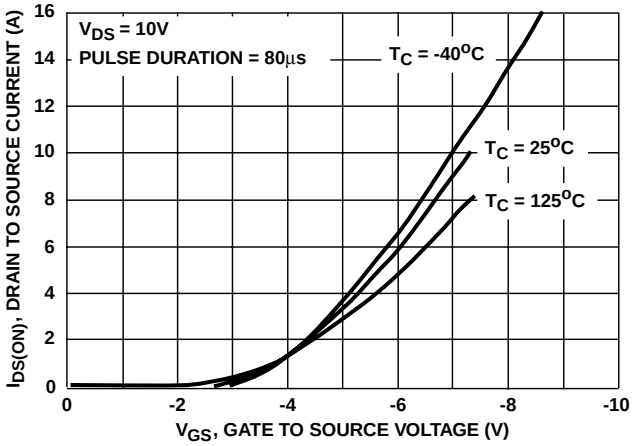


FIGURE 5. TRANSFER CHARACTERISTICS

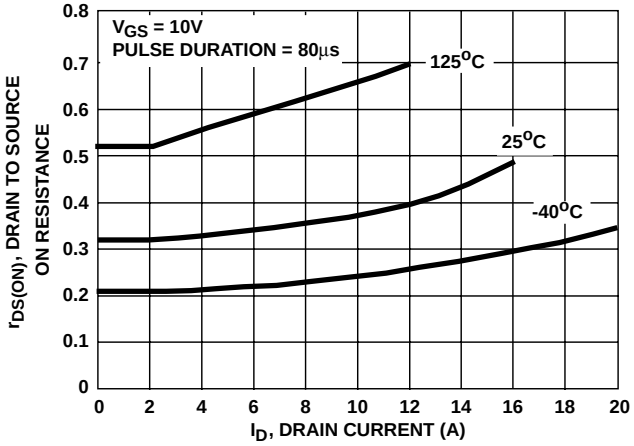


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

Typical Performance Curves (Continued)

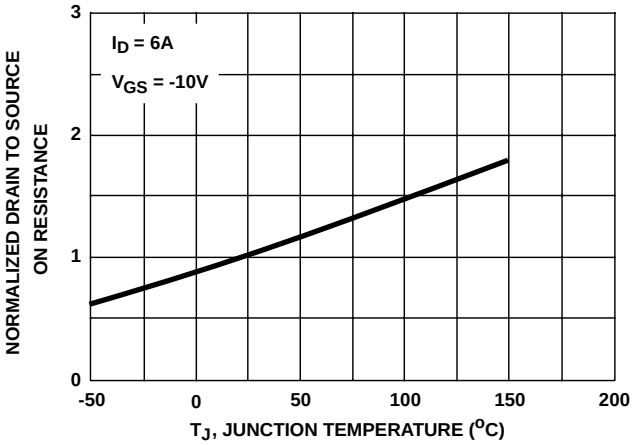


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

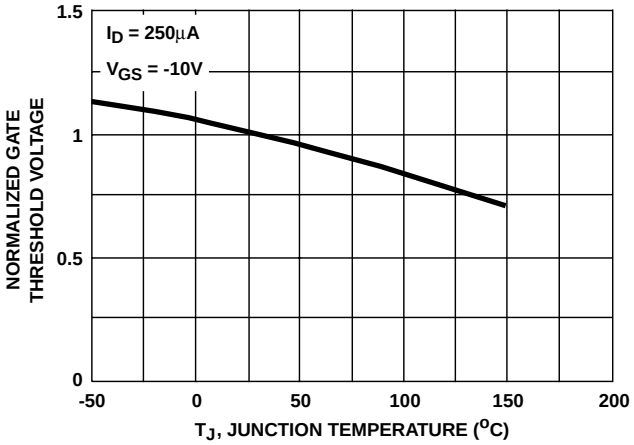


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

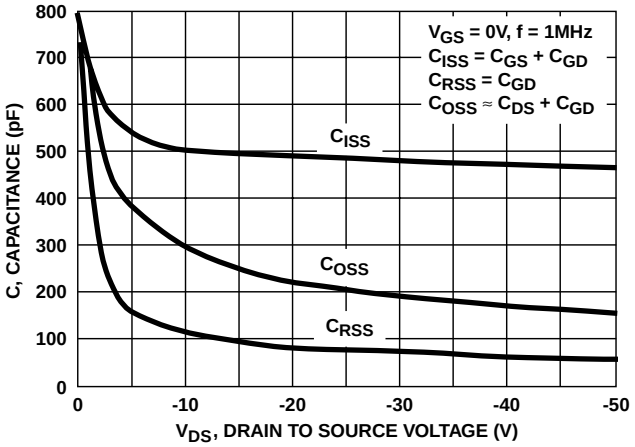
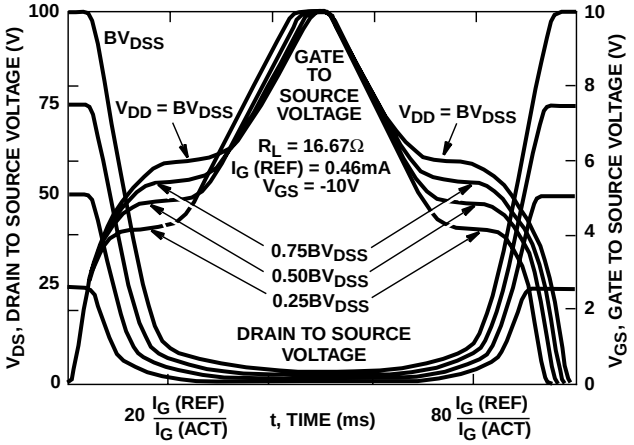


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Applications Notes AN7254 and AN7260.

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

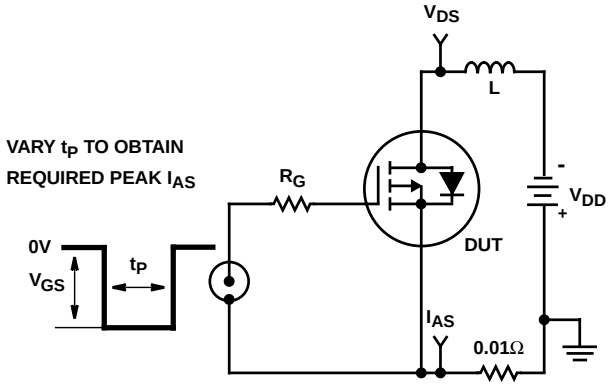


FIGURE 11. UNCLAMPED ENERGY TEST CIRCUIT

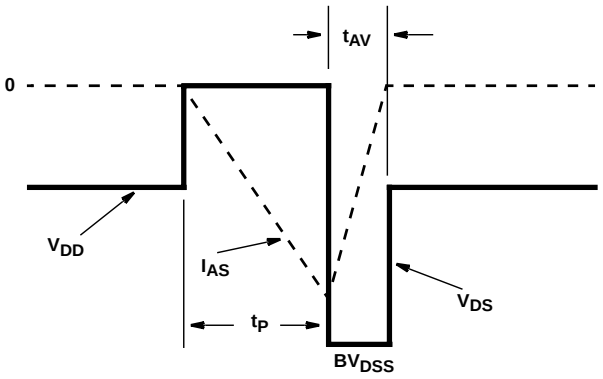


FIGURE 12. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

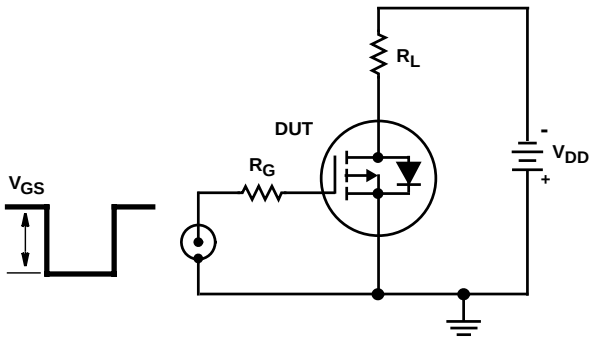


FIGURE 13. SWITCHING TIME TEST CIRCUIT

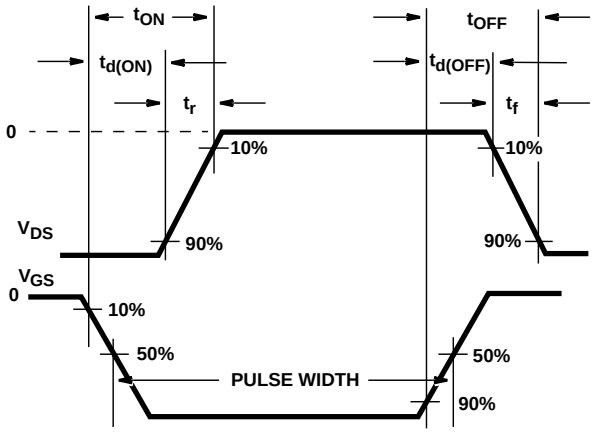


FIGURE 14. RESISTIVE SWITCHING WAVEFORMS

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