# AX8052F100

# Ultra-Low Power Microcontroller

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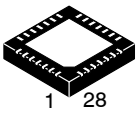


**QFN28 5x5, 0.5P**
**CASE 485EH**

## ORDERING INFORMATION

| Device | Type | Qty |
|---|---|---|
| AX8052F100−2−TA05 | Tape & Reel | 500 |
| AX8052F100−2−TW30 | Tape & Reel | 3,000 |

## OVERVIEW

The AX8052F100 is a single chip ultra−lowpower microcontroller primarily for use in radio applications. The AX8052F100 contains a high speed microcontroller compatible to the industry standard 8052 instruction set. It contains 64 kBytes of FLASH and 8.25 kBytes of internal SRAM. The AX8052F100 features 3 16−bit general purpose timers with ΣΔ capability, 2 output compare units for generating PWM signals, 2 input compare units to record timings of external signals, 2 16−bit wakeup timers, a watchdog timer, 2 UARTs, a Master/Slave SPI controller, a 10−bit 500 kSample/s A/D converter, 2 analog comparators, a temperature sensor, a 2 channel DMA controller, and a dedicated AES crypto controller. Debugging is aided by a dedicated hardware debug interface controller that connects using a 3−wire protocol (1 dedicated wire, 2 shared with GPIO) to the PC hosting the debug software.

### Features

Ultra−low Power Microcontroller

- QFN28 Package
- Supply Range 1.8 V − 3.6 V
- −40°C to 85°C
- Ultra−low Power Consumption:
  - CPU Active Mode 150 μA/MHz
  - Sleep Mode with 256 Byte RAM Retention and Wake−up Timer running 850 nA
  - Sleep Mode 4 kByte RAM Retention and Wake−up Timer running 1.5 μA
  - Sleep Mode 8 kByte RAM Retention and Wake−up Timer running 2.2 μA

AX8052 Core

- Industry Standard 8052 Instruction Set
- High Performance Core, most Instructions Require only 1 Clock per Instruction Byte
- 20 MIPS
- Dual DPTR for High Speed Memory Chips
- 22 Interrupt Vectors

Debugger

- Three−wire (1 dedicated, 2 shared with GPIO Pins) Debugger Interface
- True Hardware Debugger with Breakpoints and Single Stepping Support
- User Programmable 64−bit Key to restrict Debugging to Authorized Personnel
- DebugLink Interface allows “printf” Style Debugging without utilizing a UART or GPIO Pins

Memory

- 64 kByte FLASH
  100,000 Erase Cycles
  10 Year Data Retention
- 8.25 kByte RAM
- High Performance Memory Crossbar

Clocking

- Four Clock Sources
  - On−chip 20 MHz RC−oscillator
  - 10 kHz/640 Hz Ultra−low−power RC−oscillator
  - Fast Crystal Oscillator
  - Low Power Tuning Fork Crystal Oscillator
- Fully Automatic Calibration of On−chip RC Oscillators to a Reference Clock
- Clock Monitor can Detect Failures of the Main Clock and Switch to the On−chip Fast RC Oscillator
- Watchdog

Power Modes

- Standby, Sleep and Deep Sleep Power Modes for Very Low Idle Power Consumption
- On−chip Power−on−Reset and Brown−out Detection
- Unrestricted Operation from 1.8 V − 3.6 V VDD_IO

16−bit Wakeup Timer

- Two Counting Registers
- Four Event Registers Allow Flexible Wakeup and Software Schedules

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GPIO
- 24 GPIO Pins
- PB0−PB7, PC0−PC3 and PR0−PR5 5 V Tolerant Inputs
- All GPIO Pins Support Individually Programmable Pull−ups and Interrupt on Change
- Flexible Allocation of GPIO Pins to Peripherals

16−bit General Purpose Timer (3x)
- Saw Tooth and Triangle Modes
- Sigma−Delta Mode Converts Timer into a DAC
- Optional Double Buffering of the PERIOD Register allows Controlled Frequency Changes
- Optional High−byte Buffering allows Atomic 16−bit Accesses
- Flexible Clocking Options, can use any Internal or an External Clock Source
- Pre−scaler Included

16−bit Output Compare Unit (2x)
- Used together with a General Purpose Timer to create PWM Waveforms
- Optional Double Buffering

16−bit Input Capture Unit (2x)
- Used together with a General Purpose Timer to time Events on an External or Internal Signal

UART (2x)
- 5−9 bit Word Length, 1−2 Stop Bits
- Uses One of the General Purpose Timers as Baud Rate Generator

Dedicated Radio Master SPI Interface
- Compatible to AX RF and other Peripherals
- Efficient CPU Access
- Easy Access to Transceiver Registers by Mapping Transceiver Registers into X Address Space
- Transceiver Crystal may clock MCU

Master/Slave SPI
- Supports 3 and 4 Wire Variants

ADC
- 10−bit 500 kSamples/s ADC
- Up to 8 Channels
- Single Ended and Differential Sampling
- x0.1, x1 and x10 Gain Amplifier
- Internal 1 V Reference
- Flexibly Programmable Conversion Schedule
- Built−in Temperature Sensor

Analog Comparators
- Internal and External Reference
- Output Signal may be Routed to GPIO, Read by Software, or Used as Input Capture Trigger

DMA Controller
- 2 Independent DMA Channels
- Moves Data between X−RAM and most On−chip Peripherals
- Cycle−steal and Round−robin Memory Arbitration ensure Minimal Impact on AX8052 Core
- Chained Buffer Descriptors allow Arbitrarily Elaborate Buffering Schemes and Flexible Interrupt Generation

AES
- Dedicated AES Crypto Controller
- Dedicated DMA Engine to fetch Input Data and Key Stream from X−RAM and Strobe Output Data into X−RAM
- Multi Megabit/s Data Rates
- Supports AES−128, AES−192 and AES−256 International Standards
- Programmable Round Number and Software Key Schedule Generation allow Longer Key Lengths for Higher Security Applications
- ECB, CFB and OFB Chaining Modes

NOTE: The AES engine requires software enabling and support.

True Random Number Generator (RNG)
- Cryptographic Random Numbers

NOTE: The random number generator requires software enabling and support.

### Applications
- Ultra−low Power Microcontroller Applications, especially in Conjunction with AXRadio IC
- Sensor Applications
- Home Automation
- Automatic Meter Reading
- Remote Keyless Entry
- Active RFID
- Wireless Audio

## BLOCK DIAGRAM

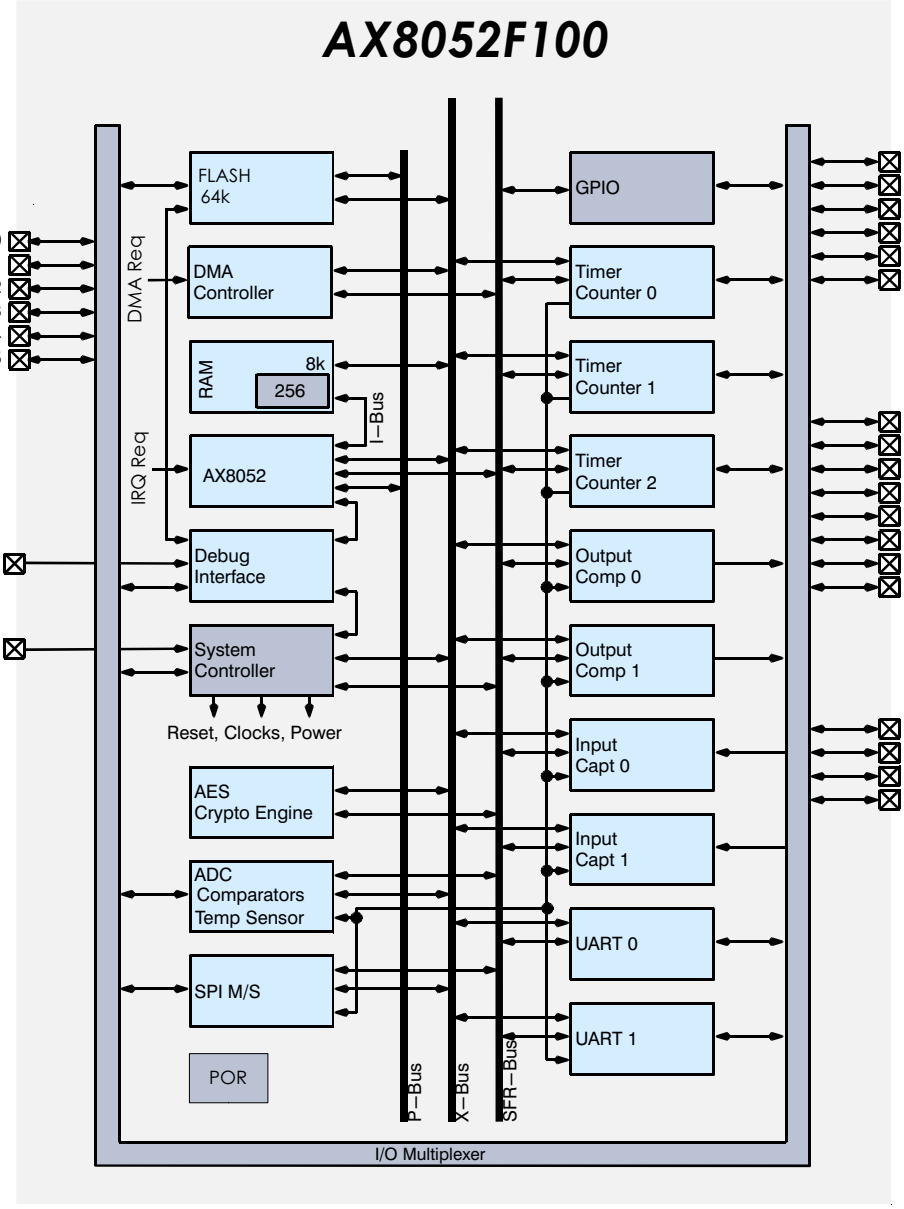



**Figure 1. Functional Block Diagram of the AX8052F100**

**Table 1. PIN FUNCTION DESCRIPTIONS**

| Symbol | Pin(s) | Type | Description |
|---|---|---|---|
| PR5 | 1 | I/O/PU | General Purpose I/O |
| VDD_CORE | 2 | P | Regulated output voltage |
| PR4 | 3 | I/O/PU | General Purpose I/O |
| PR3 | 4 | I/O/PU | General Purpose I/O |
| PR2 | 5 | I/O/PU | General Purpose I/O |
| PR1 | 6 | I/O/PU | General Purpose I/O |
| PR0 | 7 | I/O/PU | General Purpose I/O |
| PC3 | 8 | I/O/PU | General Purpose I/O |
| PC2 | 9 | I/O/PU | General Purpose I/O |
| PC1 | 10 | I/O/PU | General Purpose I/O |
| PC0 | 11 | I/O/PU | General Purpose I/O |
| PB0 | 12 | I/O/PU | General Purpose I/O |
| PB1 | 13 | I/O/PU | General Purpose I/O |
| PB2 | 14 | I/O/PU | General Purpose I/O |
| PB3 | 15 | I/O/PU | General Purpose I/O |
| PB4 | 16 | I/O/PU | General Purpose I/O |
| PB5 | 17 | I/O/PU | General Purpose I/O |
| PB6, DBG_DATA | 18 | I/O/PU | General Purpose I/O, debugger data line |
| PB7, DBG_CLK | 19 | I/O/PU | General Purpose I/O, debugger clock line |
| DBG_EN | 20 | I/PD | In−Circuit Debugger Enable |
| RESET_N | 21 | I/PU | Optional reset pin. If this pin is not used it must be connected to VDD_IO |
| VDD_IO | 22 | P | Unregulated power supply |
| PA0 | 23 | I/O/PU | General Purpose I/O |
| PA1 | 24 | I/O/PU | General Purpose I/O |
| PA2 | 25 | I/O/PU | General Purpose I/O |
| PA3 | 26 | I/O/PU | General Purpose I/O |
| PA4 | 27 | I/O/PU | General Purpose I/O |
| PA5 | 28 | I/O/PU | General Purpose I/O |
| GND | Center pad | P | Ground on center pad of QFN, must be connected |

A = analog input
I = digital input signal
O = digital output signal
PU = pull−up
I/O = digital input/output signal
N = not to be connected
P = power or ground
PD = pull−down

All digital inputs are Schmitt trigger inputs, digital input and output levels are LVCMOS/LVTTL compatible. Port A Pins (PA0 − PA7) must not be driven above VDD_IO, all other digital inputs are 5 V tolerant. Pull−ups are programmable for all GPIO pins.

### Alternate Pin Functions

GPIO Pins are shared with dedicated Input/Output signals of on−chip peripherals. The following table lists the available functions on each GPIO pin.

**Table 2. ALTERNATE PIN FUNCTIONS**

| GPIO | Alternate Functions | | | |
|---|---|---|---|---|
| PA0 | T0OUT | IC1 | ADC0 | XTALP |
| PA1 | T0CLK | OC1 | ADC1 | XTALN |
| PA2 | OC0 | U1RX | ADC2 | COMPI00 |
| PA3 | T1OUT | | ADC3 | LPXTALP |
| PA4 | T1CLK | COMPO0 | ADC4 | LPXTALN |
| PA5 | IC0 | U1TX | ADC5 | COMPI10 |
| PB0 | U1TX | IC1 | EXTIRQ0 | |
| PB1 | U1RX | OC1 | | |
| PB2 | IC0 | T2OUT | | |
| PB3 | OC0 | T2CLK | EXTIRQ1 | DSWAKE |
| PB4 | U0TX | T1CLK | | |
| PB5 | U0RX | T1OUT | | |
| PB6 | DBG_DATA | | | |
| PB7 | DBG_CLK | | | |
| PC0 | SSEL | T0OUT | EXTIRQ0 | |
| PC1 | SSCK | T0CLK | COMPO1 | |
| PC2 | SMOSI | U0TX | | |
| PC3 | SMISO | U0RX | COMPO0 | |
| PR0 | RSEL | | | |
| PR1 | RSYSCLK | | | |
| PR2 | RCLK | | | |
| PR3 | RMISO | | | |
| PR4 | RMOSI | | | |
| PR5 | RIRQ | | | |

**Pinout Drawing**

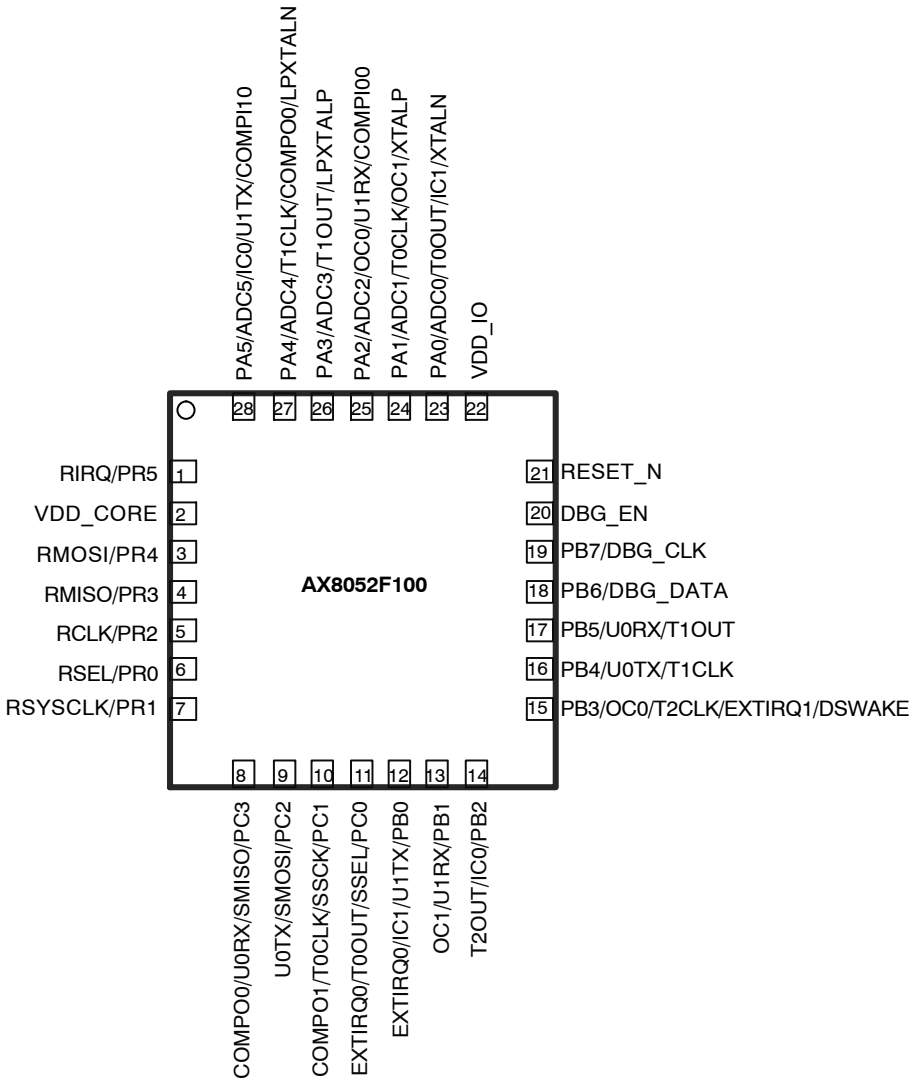



**Figure 2. Pinout Drawing (Top View)**

## SPECIFICATIONS

### Table 3. ABSOLUTE MAXIMUM RATINGS

| Symbol | Description | Condition | Min | Max | Units |
|---|---|---|---|---|---|
| VDD_IO | Supply voltage | | −0.5 | 5.5 | V |
| IDD | Supply current | | | 100 | mA |
| $P_{tot}$ | Total power consumption | | | 800 | mW |
| $I_{I1}$ | DC current into any pin | | −10 | 10 | mA |
| $I_{I2}$ | DC current into pins | | −100 | 100 | mA |
| $I_O$ | Output Current | | | 40 | mA |
| $V_{ia}$ | Input voltage digital pins | | −0.5 | 5.5 | V |
| $V_{es}$ | Electrostatic handling | HBM | −2000 | 2000 | V |
| $T_{amb}$ | Operating temperature | | −40 | 85 | °C |
| $T_{stg}$ | Storage temperature | | −65 | 150 | °C |
| $T_j$ | Junction Temperature | | | 150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### DC Characteristics

### Table 4. SUPPLIES

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{AMB}$ | Operational ambient temperature | | −40 | 27 | 85 | °C |
| VDD_IO | I/O and voltage regulator supply voltage | | 1.8 | 3.0 | 3.6 | V |
| $VDD_{IO_R1}$ | I/O voltage ramp for reset activation; Note 1 | Ramp starts at VDD_IO ≤ 0.1 V | 0.1 | | | V/ms |
| $VDD_{IO_R2}$ | I/O voltage ramp for reset activation; Note 1 | Ramp starts at 0.1V < VDD_IO < 0.7 V | 3.3 | | | V/ms |
| $V_{BOUT}$ | Brown−out Threshold | Note 2 | | 1.3 | | V |
| $I_{DEEPSLEEP}$ | Deep Sleep current | | | 50 | | nA |
| $I_{SLEEP256PIN}$ | Sleep current, 256 Bytes RAM retained | Wakeup from dedicated pin | | 450 | | nA |
| $I_{SLEEP256}$ | Sleep current, 256 Bytes RAM retained | Wakeup Timer running at 640 Hz | | 850 | | nA |
| $I_{SLEEP4K}$ | Sleep current, 4.25 kBytes RAM retained | Wakeup Timer running at 640 Hz | | 1.5 | | μA |
| $I_{SLEEP8K}$ | Sleep current, 8.25 kBytes RAM retained | Wakeup Timer running at 640 Hz | | 2.2 | | μA |
| $I_{MCU}$ | Micro−controller Running Power consumption | All peripherals disabled | | 150 | | μA/ MHz |
| $I_{VSUP}$ | Voltage Supervisor | Run and Standby mode | | 85 | | μA |
| $I_{XTALOSC}$ | Crystal oscillator current | 20 MHz | | 160 | | μA |
| $I_{LFXTALOSC}$ | Low Frequency Crystal Oscillator current | 32 kHz | | 700 | | nA |
| $I_{RCOSC}$ | Internal Oscillator current | 20 MHz | | 210 | | μA |
| $I_{LPOSC}$ | Internal Low Power Oscillator current | 10 kHz | | 650 | | nA |
| | | 640 Hz | | 210 | | nA |
| $I_{ADC}$ | ADC current | 311 kSample/s, DMA 5 MHz | | 1.1 | | mA |

1. If VDD_IO ramps cannot be guaranteed, an external reset circuit is recommended, see the AX8052 Application Note: Power On Reset
2. Digital circuitry is functional down to typically 1 V.

**Table 5. LOGIC**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Digital Inputs** | | | | | | |
| $V_{T+}$ | Schmitt trigger low to high threshold point | VDD_IO = 3.3 V | | 1.55 | | V |
| $V_{T-}$ | Schmitt trigger high to low threshold point | | | 1.25 | | V |
| $V_{IL}$ | Input voltage, low | | | | 0.8 | V |
| $V_{IH}$ | Input voltage, high | | 2.0 | | | V |
| $V_{IPA}$ | Input voltage range, Port A | | −0.5 | | VDD_IO | V |
| $V_{IPBC}$ | Input voltage range, Ports B, C | | −0.5 | | 5.5 | V |
| $I_L$ | Input leakage current | | −10 | | 10 | μA |
| $R_{PU}$ | Programmable Pull−Up Resistance | | | 65 | | kΩ |
| **Digital Outputs** | | | | | | |
| $I_{OH}$ | P[ABC]x Output Current, high | $V_{OH}$ = 2.4 V | 8 | | | mA |
| $I_{OL}$ | P[ABC]x Output Current, low | $V_{OL}$ = 0.4 V | 8 | | | mA |
| $I_{PROH}$ | PRx Output Current, high | $V_{OH}$ = 2.4 V | 2 | | | mA |
| $I_{PROL}$ | PRx Output Current, low | $V_{OL}$ = 0.4 V | 2 | | | mA |
| $I_{OZ}$ | Tri−state output leakage current | | −10 | | 10 | μA |

## AC Characteristics

**Table 6. CRYSTAL OSCILLATOR**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{XTAL}$ | Crystal frequency | | 8 | | 20 | MHz |
| $gm_{xosc}$ | Transconductance oscillator<br>Note 1 | XTALOSCGM = 0001 | | 0.5 | | mS |
| | | XTALOSCGM = 0010 | | 1.0 | | |
| | | XTALOSCGM = 1110 | | 4.5 | | |
| | | XTALOSCGM = 1111 | | 11.0 | | |
| $RIN_{xosc}$ | Input DC impedance | | 10 | | | kΩ |

1. During normal operation the oscillator transconductance is automatically adjusted for lowest power consumption

**Table 7. LOW FREQUENCY CRYSTAL OSCILLATOR**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{LPXTAL}$ | Crystal frequency | | | 32 | 150 | kHz |
| $gm_{lpxosc}$ | Transconductance oscillator | LPXOSCGM = 00110 | | 3.5 | | μs |
| | | LPXOSCGM = 01000 | | 4.6 | | |
| | | LPXOSCGM = 01100 | | 6.9 | | |
| | | LPXOSCGM = 10000 | | 9.1 | | |
| $RIN_{lpxosc}$ | Input DC impedance | | 10 | | | MΩ |

**Table 8. INTERNAL LOW POWER OSCILLATOR**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{LPOSC}$ | Oscillation Frequency | LPOSCFAST = 0<br>Factory calibration applied. Over the full temperature and voltage range | 630 | 640 | 650 | Hz |
| | | LPOSCFAST = 1<br>Factory calibration applied. Over the full temperature and voltage range | 10.08 | 10.24 | 10.39 | kHz |

**Table 9. INTERNAL RC OSCILLATOR**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{LFRPCOSC}$ | Oscillation Frequency | Factory calibration applied. Over the full temperature and voltage range | 19.8 | 20 | 20.2 | MHz |

**Table 10. MICROCONTROLLER**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{SYSCLKL}$ | SYSCLK Low | | 27 | | | ns |
| $T_{SYSCLKH}$ | SYSCLK High | | 21 | | | ns |
| $T_{SYSCLKP}$ | SYSCLK Period | | 47 | | | ns |
| $T_{FLWR}$ | FLASH Write Time | 2 Bytes | | 20 | | μs |
| $T_{FLPE}$ | FLASH Page Erase | 1 kBytes | | 2 | | ms |
| $T_{FLE}$ | FLASH Secure Erase | 64 kBytes | | 10 | | ms |
| $T_{FLEND}$ | FLASH Endurance: Erase Cycles | | 10 000 | 100 000 | | Cycles |
| $T_{FLRETroom}$ | FLASH Data Retention | 25°C<br>See Figure 3 for the lower limit set by the memory qualification | 100 | | | Years |
| $T_{FLREThot}$ | | 85°C<br>See Figure 3 for the lower limit set by the memory qualification | 10 | | | |

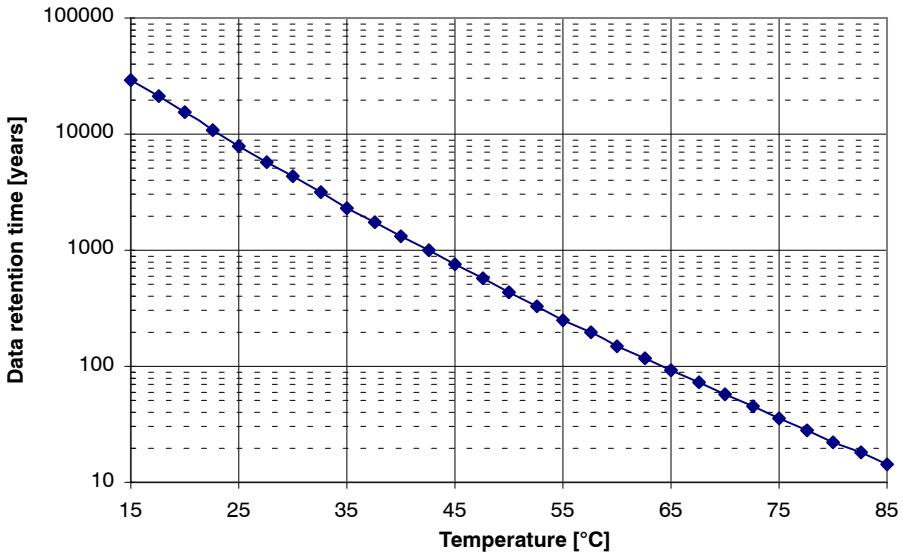



**Figure 3. FLASH Memory Qualification Limit for Data Retention after 10k Erase Cycles**

**Table 11. ADC / COMPARATOR / TEMPERATURE SENSOR**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| ADCSR | ADC sampling rate GPADC mode | | 30 | | 500 | kHz |
| ADCSR_T | ADC sampling rate temperature sensor mode | | 10 | 15.6 | 30 | kHz |
| ADCRES | ADC resolution | | | 10 | | Bits |
| $V_{ADCREF}$ | ADC reference voltage & comparator internal reference voltage | | 0.95 | 1 | 1.05 | V |
| $Z_{ADC00}$ | Input capacitance | | | | 2.5 | pF |
| DNL | Differential nonlinearity | | | | ± 1 | LSB |
| INL | Integral nonlinearity | | | ± 1 | | LSB |
| OFF | Offset | | | 3 | | LSB |
| GAIN_ERR | Gain error | | | 0.8 | | % |
| **ADC in Differential Mode** | | | | | | |
| $V_{ABS_DIFF}$ | Absolute voltages & common mode voltage in differential mode at each input | | 0 | | VDD_IO | V |
| $V_{FS_DIFF01}$ | Full swing input for differential signals | Gain x1 | −500 | | 500 | mV |
| $V_{FS_DIFF10}$ | | Gain x10 | −50 | | 50 | mV |
| **ADC in Single Ended Mode** | | | | | | |
| $V_{MID_SE}$ | Mid code input voltage in single ended mode | | | 0.5 | | V |
| $V_{IN_SE00}$ | Input voltage in single ended mode | | 0 | | VDD_IO | V |
| $V_{FS_SE01}$ | Full swing input for single ended signals | Gain x1 | 0 | | 1 | V |
| $V_{FS_SE10}$ | | Gain x10 | 0.45 | | 0.55 | V |
| **Comparators** | | | | | | |
| $V_{COMP_ABS}$ | Comparator absolute input voltage | | 0 | | VDD_IO | V |
| $V_{COMP_COM}$ | Comparator input common mode | | 0 | | VDD_IO − 0.8 | V |
| $V_{COMPOFF}$ | Comparator input offset voltage | | | | 20 | mV |
| **Temperature Sensor** | | | | | | |
| $T_{RNG}$ | Temperature range | | −40 | | 85 | °C |
| $T_{RES}$ | Temperature resolution | | | 0.1607 | | °C/LSB |
| $T_{ERR_CAL}$ | Temperature error | Factory calibration applied | −2 | | 2 | °C |

## CIRCUIT DESCRIPTION

The AX8052F100 is a single chip ultra−lowpower microcontroller primarily for use in radio applications. The AX8052F100 contains a high speed microcontroller compatible to the industry standard 8052 instruction set. It contains 64 kBytes of FLASH and 8.25 kBytes of internal SRAM. The AX8052F100 features 3 16−bit general purpose timers with ΣΔ capability, 2 output compare units for generating PWM signals, 2 input compare units to record timings of external signals, 2 16−bit wakeup timers, a watchdog timer, 2 UARTs, a Master/Slave SPI controller, a 10−bit 500 kSample/s A/D converter, 2 analog comparators, a temperature sensor, a 2 channel DMA controller, and a dedicated AES crypto controller. Debugging is aided by a dedicated hardware debug interface controller that connects using a 3−wire protocol (1 dedicated wire, 2 shared with GPIO) to the PC hosting the debug software.

The system clock that clocks the microcontroller, as well as peripheral clocks, can be selected from one of the following clock sources: the crystal oscillator, an internal high speed 20 MHz oscillator, an internal low speed 640 Hz/10 kHz oscillator, or the low frequency crystal oscillator. Pre−scalers offer additional flexibility with their programmable divide by a power of two capability. To improve the accuracy of the internal oscillators, both oscillators may be slaved to the crystal oscillator.

AX8052F100 can be operated from a 1.8 V to 3.6 V power supply over a temperature range of −40°C to 85°C. The AX8052F100 features make it an ideal interface for integration into various battery powered SRD solutions such as ticketing or as transceiver for telemetric applications e.g. in sensors.

### Microcontroller

The AX8052F100 microcontroller core executes the industry standard 8052 instruction set. Unlike the original 8052, many instructions are executed in a single cycle. The system clock and thus the instruction rate can be programmed freely from DC to 20 MHz.

*Memory Architecture*

The AX8052F100 Microcontroller features the highest bandwidth memory architecture of its class. Figure 4 shows the memory architecture. Three bus masters may initiate bus cycles:

- The AX8052 Microcontroller Core
- The Direct Memory Access (DMA) Engine
- The Advanced Encryption Standard (AES) Engine

Bus targets include:

- Two individual 4 kBytes RAM blocks located in X address space, which can be simultaneously accessed and individually shut down or retained during sleep mode
- A 256 Byte RAM located in internal address space, which is always retained during sleep mode
- A 64 kBytes FLASH memory located in code space.
- Special Function Registers (SFR) located in internal address space accessible using direct address mode instructions
- Additional Registers located in X address space (X Registers)

The upper half of the FLASH memory may also be accessed through the X address space. This simplifies and makes the software more efficient by reducing the need for generic pointers.

NOTE: Generic pointers include, in addition to the address, an address space tag.

SFR Registers are also accessible through X address space, enabling indirect access to SFR registers. This allows driver code for multiple identical peripherals (such as UARTs or Timers) to be shared.

The 4 word × 16 bit fully associative cache and a pre−fetch controller hide the latency of the FLASH.

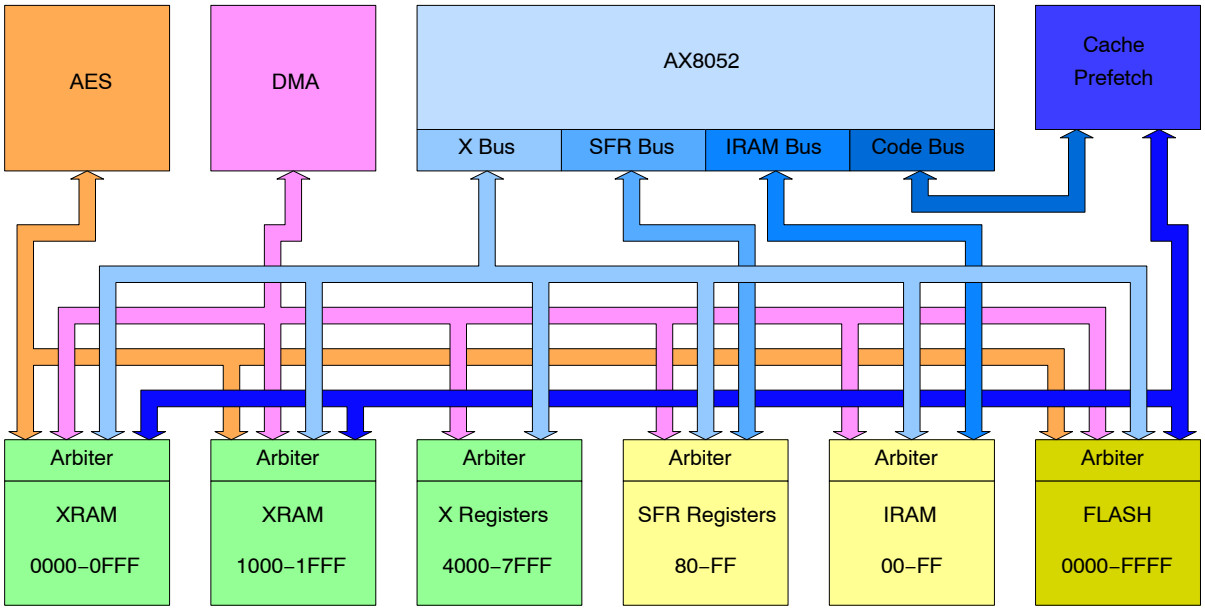



**Figure 4. AX8052 Memory Architecture**

The AX8052 Memory Architecture is fully parallel. All bus masters may simultaneously access different bus targets during each system clock cycle. Each bus target includes an arbiter that resolves access conflicts. Each arbiter ensures that no bus master can be starved.

Both 4 kBytes RAM blocks may be individually retained or switched off during sleep mode. The 256 Byte RAM is always retained during sleep mode.

The AES engine accesses memory 16 bits at a time. It is therefore slightly faster to align its buffers on even addresses.

*Memory Map*

The AX8052, like the other industry standard 8052 compatible microcontrollers, uses a Harvard architecture. Multiple address spaces are used to access code and data. Figure 5 shows the AX8052 memory map.

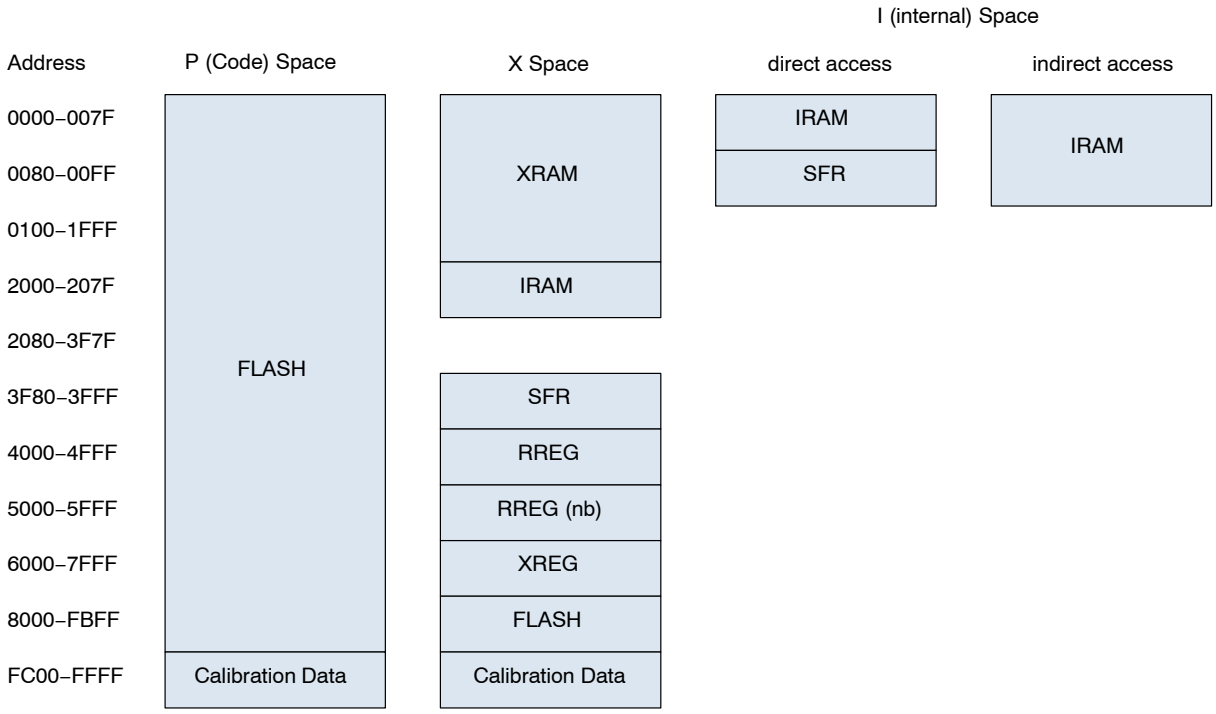



**Figure 5. AX8052 Memory Map**

The AX8052 uses P or Code Space to access its program. Code space may also be read using the MOVC instruction.

Smaller amounts of data can be placed in the Internal (see Note) or Data Space. A distinction is made in the upper half of the Data Space between direct accesses (MOV reg,addr; MOV addr,reg) and indirect accesses (MOV reg,@Ri; MOV @Ri,reg; PUSH; POP); Direct accesses are routed to the Special Function Registers, while indirect accesses are routed to the internal RAM.

NOTE: The origin of Internal versus External (X) Space is historical. External Space used to be outside of the chip on the original 8052 Microcontrollers.

Large amounts of data can be placed in the External or X Space. It can be accessed using the MOVX instructions. Special Function Registers, as well as additional Microcontroller Registers (XREG) and the Radio Registers (RREG) are also mapped into the X Space.

Detailed documentation of the Special Function Registers (SFR) and additional Microcontroller Registers can be found in the AX8052 Programming Manual.

The Radio Registers are documented in the Programming Manual of the connected Radio chip. Register Addresses given in the Radio chip's Programming Manual are relative to the beginning of RREG, i.e. 0x4000 must be added to these addresses. If an AXRadio chip is connected, the appropriate provided ax8052f1xx.h header file should be used.

Normally, accessing Radio Registers through the RREG address range is adequate. Since Radio Register accesses have a higher latency than other AX8052 registers, the AX8052 provides a method for non−blocking access to the Radio Registers. Accessing the RREG (nb) address range initiates a Radio Register access, but does not wait for its completion. The details of mechanism is documented in the Radio Interface section of the AX8052 Programming Manual.

The FLASH memory is organized as 64 pages of 1 kBytes each. Each page can be individually erased. The write word size is 16 Bits. The last 1 kByte page is dedicated to factory calibration data and should not be overwritten.

*Power Management*

The microcontroller supports the following power modes:

**Table 12. POWER MANAGEMENT**

| PCON register | Name | Description |
|---|---|---|
| 00 | RUNNING | The microcontroller and all peripherals are running. Current consumption depends on the system clock frequency and the enabled peripherals and their clock frequency. |
| 01 | STANDBY | The microcontroller is stopped. All register and memory contents are retained. All peripherals continue to function normally. Current consumption is determined by the enabled peripherals. STANDBY is exited when any of the enabled interrupts become active. |
| 10 | SLEEP | The microcontroller and its peripherals, except GPIO and the system controller, are shut down. Their register settings are lost. The internal RAM is retained. The external RAM is split into two 4 kByte blocks. Software can determine individually for both blocks whether contents of that block are to be retained or lost. SLEEP can be exited by any of the enabled GPIO or system controller interrupts. For most applications this will be a GPIO or wakeup timer interrupt. |
| 11 | DEEPSLEEP | The microcontroller, all peripherals and the transceiver are shut down. Only 4 bytes of scratch RAM are retained. DEEPSLEEP can only be exited by tying the PB3 pin low. |

*Clocking*

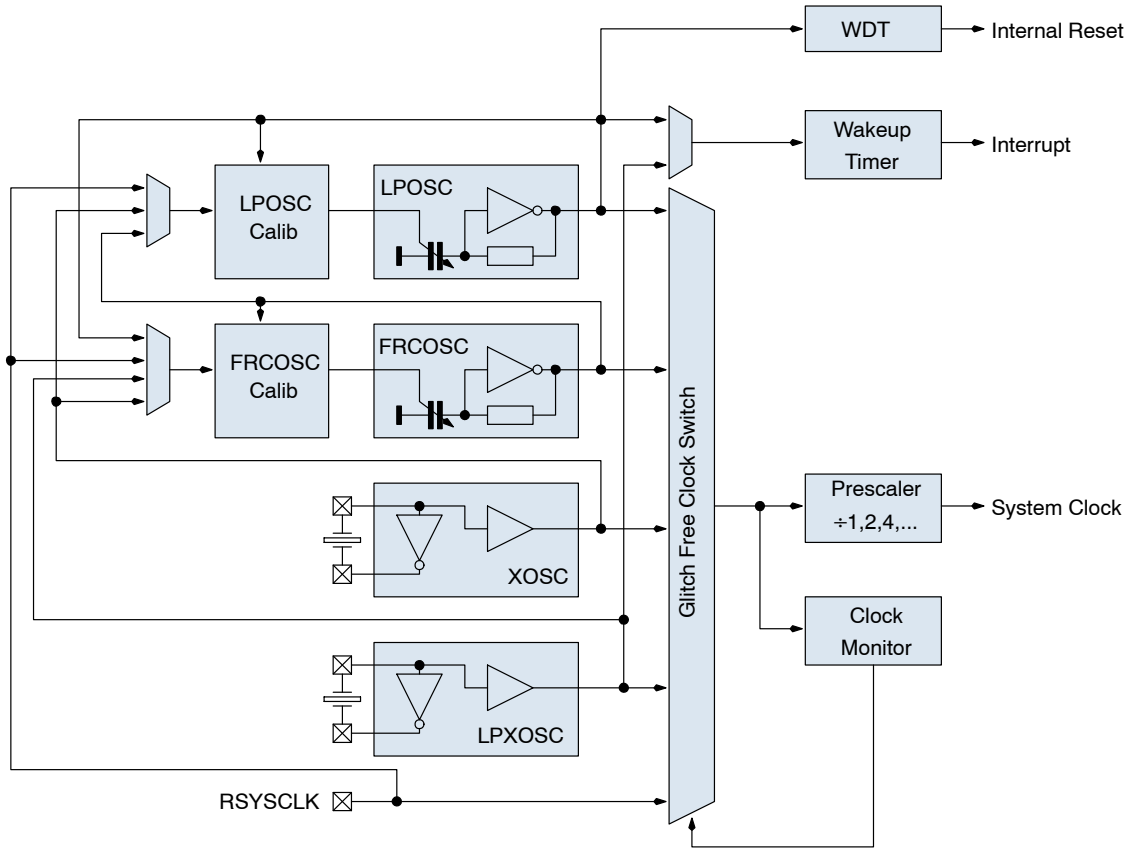



**Figure 6. Clock System Diagram**

The system clock can be derived from any of the following clock sources:

- The crystal oscillator
- The low speed crystal oscillator
- The internal high speed RC (20 MHz) oscillator
- The internal low power (640 Hz/10 kHz) oscillator

An additional pre−scaler allows the selected oscillator to be divided by a power of two. After reset, the microcontroller starts with the internal high speed RC oscillator selected and divided by two. I.e. at start−up, the microcontroller runs with 10 MHz ± 10%. Clocks may be switched any time by writing to the CLKCON register. In order to prevent clock glitches, the switching takes approximately $2\cdot(T_1+T_2)$, where $T_1$ and $T_2$ are the periods of the old and the new clock. Switching may take longer if the new oscillator first has to start up. Internal oscillators start up instantaneously, but crystal oscillators may take a considerable amount of time to start the oscillation. CLKSTAT can be read to determine the clock switching status.

A programmable clock monitor resets the CLKCON register when no system clock transitions are found during a programmable time interval, thus reverts to the internal RC oscillator.

Both internal oscillators can be slaved to one of the crystal oscillators to increase the accuracy of the oscillation frequency. While the reference oscillator runs, the internal oscillator is slaved to the reference frequency by a digital frequency locked loop. When the reference oscillator is switched off, the internal oscillator continues to run unslaved with the last frequency setting.

*Reset and Interrupts*

After reset, the microcontroller starts executing at address 0x0000. All registers except SCRATCH0...SCRATCH3 are set to default values. RAM is either retained (SLEEP mode) or undefined.

Several events can lead to resetting the microcontroller core:

- POR or hardware RESET_N pin activated and released
- Leaving SLEEP or DEEPSLEEP mode
- Watchdog Reset
- Software Reset

The reset cause can be determined by reading the PCON register.

After POR or reset all registers are set to their default values.

AX8052F100 has an integrated power−on−reset block which is edge sensitive to VDD_IO. For many common

application cases no external reset circuitry is required. However, if VDD_IO ramps cannot be guaranteed, an external reset circuit is recommended. For detailed recommendations and requirements see the AX8052 Application Note: Power On Reset.

The RESET_N pin contains a weak pull−up. However, it is strongly recommended to connect the RESET_N pin to VDD_IO if not used, for additional robustness.

The microcontroller supports 22 interrupt sources. Each interrupt can be individually enabled and can be programmed to have one of two possible priorities. The interrupt vectors are located at 0x0003, 0x000B,…, 0x00AB.

*Debugging*

A hardware debug unit considerably eases debugging compared to other 8052 microcontrollers. It allows to reliably stop the micro−controller at breakpoints even if the stack is smashed. The debug unit communicates with the host PC running the debugger using a 3 wire interface. One wire is dedicated (DBG_EN), while two wires are shared with GPIO pins (PB6, PB7). When DBG_EN is driven high, PB6 and PB7 convert to debug interface pins and the GPIO functionality is no longer available. A pin emulation feature however allows bits PINB[7:6] to be set and PORTB[7:6] and DIRB[7:6] to be read by the debugger software. This allows for example switches or LEDs connected to the PB6, PB7 pins to be emulated in the debugger software whenever the debugger is active.

In order to protect the intellectual property of the firmware developer, the debug interface can be locked using a developer−selectable 64−bit key. The debug interface is then disabled and can only be enabled with the knowledge of this 64−bit key. Therefore, unauthorized persons cannot read the firmware through the debug interface, but debugging is still possible for authorized persons. Secure erase can be initiated without key knowledge; secure erase ensures that the main FLASH array is completely erased before erasing the key, reverting the chip into factory state.

The DebugLink peripheral looks like an UART to the microcontroller, and allows exchange of data between the microcontroller and the host PC without disrupting program execution.

### Timer, Output Compare and Input Capture

The AX8052F100 features three general purpose 16−bit timers. Each timer can be clocked by the system clock, any of the available oscillators, or a dedicated input pin. The timers also feature a programmable clock inversion, a programmable prescaler that can divide by powers of two, and an optional clock synchronization logic that synchronizes the clock to the system clock. All three counters are identical and feature four different counting modes, as well as a ΣΔ mode that can be used to output an analog value on a dedicated digital pin only employing a simple RC lowpass filter.

Two output compare units work in conjunction with one of the timers to generate PWM signals.

Two input capture units work in conjunction with one of the timers to measure transitions on an input signal.

For software timekeeping, two additional 16−bit wakeup timers with 4 16−bit event registers are provided, generating an interrupt on match events.

### UART

The AX8052F100 features two universal asynchronous receiver transmitters. They use one of the timers as baud rate generator. Word length can be programmed from 5 to 9 bits.

### Dedicated Radio SPI Master Controller

The AX8052F100 features a dedicated Radio master SPI controller. It is compatible with AX RF chips as well as some third party SPI slave devices. It features efficient access by the CPU. RF IC registers are mapped into the CPU X address space.

### SPI Master/Slave Controller

The AX8052F100 features a master/slave SPI controller. Both 3 and 4 wire SPI variants are supported. In master mode, any of the on−chip oscillators or the system clock may be selected as clock source. An additional pre−scaler with divide by two capability provides additional clocking flexibility. Shift direction, as well as clock phase and inversion, are programmable.

### ADC, Analog Comparators and Temperature Sensor

The AX8052F100 features a 10−bit, 500 kSample/s Analog to Digital converter. Figure 7 shows the block diagram of the ADC. The ADC supports both single ended and differential measurements. It uses an internal reference of 1 V. ×1, ×10 and ×0.1 gain modes are provided. The ADC may digitize signals on PA0…PA7, as well as VDD_IO and an internal temperature sensor. The user can define four channels which are then converted sequentially and stored in four separate result registers. Each channel configuration consists of the multiplexer and the gain setting.

The AX8052F100 contains an on−chip temperature sensor. Built−in calibration logic allows the temperature sensor to be calibrated in °C, °F or any other user defined temperature scale.

The AX8052F100 also features two analog comparators. Each comparator can either compare two voltages on dedicated PA pins, or one voltage against the internal 1 V reference. The comparator output can be routed to a dedicated digital output pin or can be read by software. The comparators are clocked with the system clock.

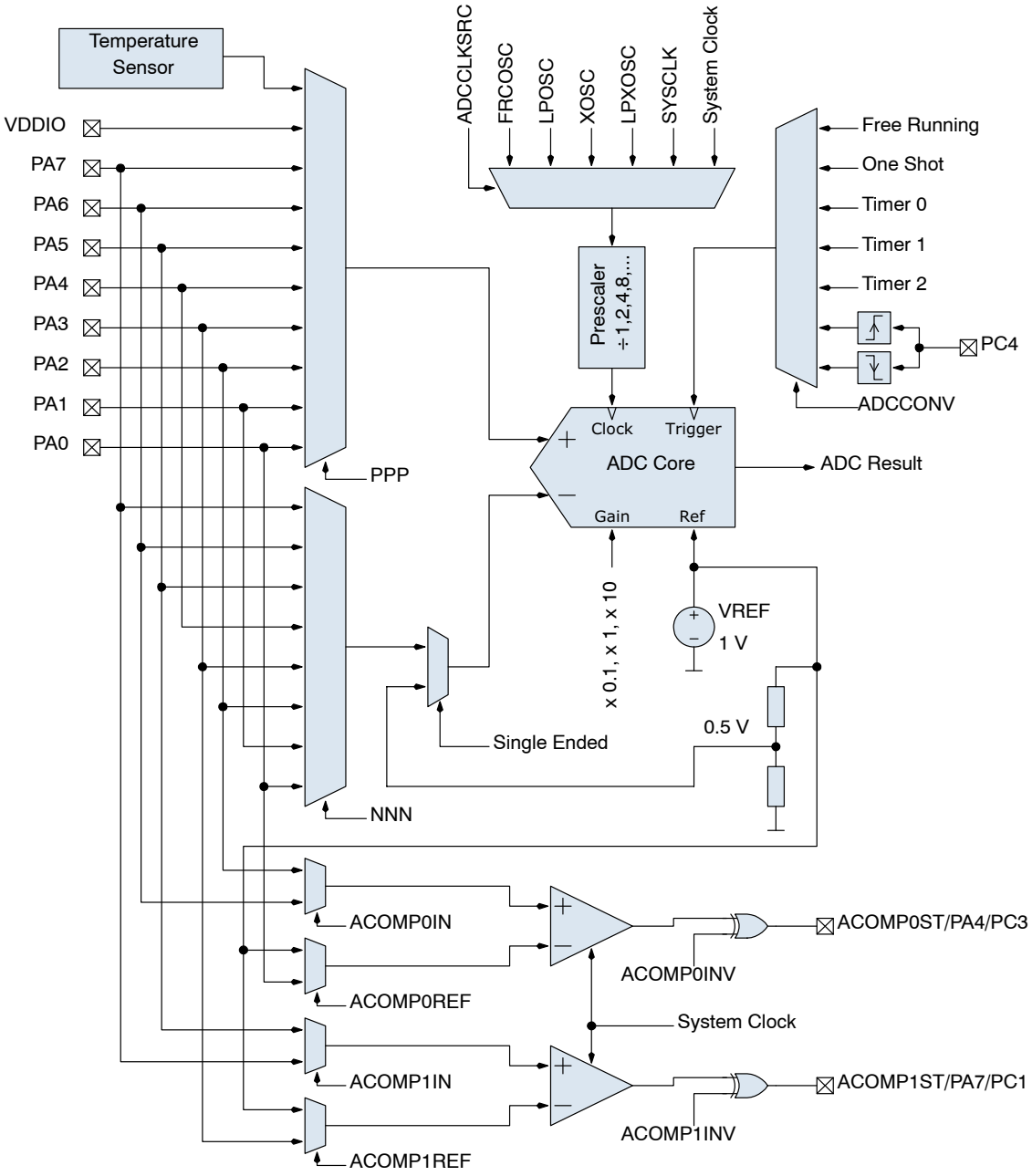



**Figure 7. ADC Block Diagram**

### DMA Controller

The AX8052F100 features a dual channel DMA engine. Each DMA channel can either transfer data from XRAM to almost any peripheral on chip, or from almost any peripheral to XRAM. Both channels may also be cross−linked for memory−memory transfers. The DMA channels use buffer descriptors to find the buffers where data is to be retrieved or placed, thus enabling very flexible buffering strategies.

The DMA channels access XRAM in a cycle steal fashion. They access XRAM whenever XRAM is not used by the microcontroller. Their priority is lower than the microcontroller, thus interfering very little with the microcontroller. Additional logic prevents starvation of the DMA controller.

### AES Engine

The AX8052F100 contains a dedicated engine for the government mandated Advanced Encryption Standard (AES). It features a dedicated DMA engine and reads input data as well as key stream data from the XRAM, and writes output data into a programmable buffer in the XRAM. The round number is programmable; the chip therefore supports AES−128, AES−192, and AES−256, as well as higher security proprietary variants. Key stream (key expansion) is

performed in software, adding to the flexibility of the AES engine. ECB (electronic codebook), CFB (cipher feedback) and OFB (output feedback) modes are directly supported without software intervention. In conjunction with the true random number generator a high degree of security can be achieved.

### Crystal Oscillator

The on−chip crystal oscillator allows the use of an inexpensive quartz crystal as timing reference. Normally, the oscillator operates fully automatically. It is powered on whenever the system clock or any peripheral clock is programmed to be derived from the crystal clock. To hide crystal startup latencies, the oscillator may also be forced on using the OSCFORCERUN register.

The transconductance of the oscillator is automatically controlled to ensure fast startup and low steady state current consumption. For lowest phase noise applications, transconductance may be programmed manually using the XTALOSC register.

### Ports

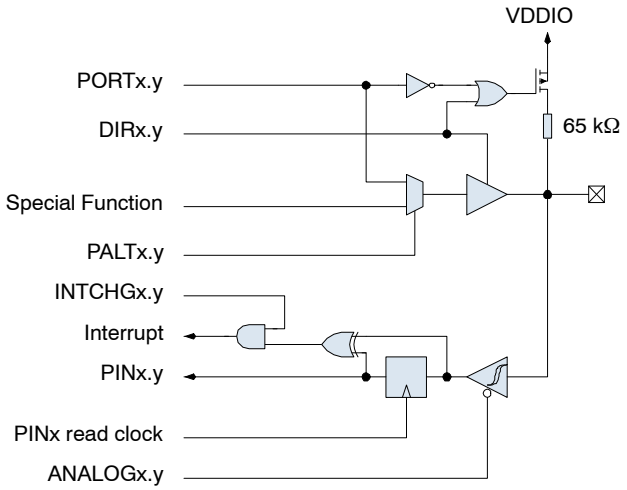



**Figure 8. Port Pin Schematic**

Figure 8 shows the GPIO logic. The DIR register bit determines whether the port pin acts as an output (1) or an input (0).

If configured as an output, the PALT register bit determines whether the port pin is connected to a peripheral output (1), or used as a GPIO pin (0). In the latter case, the PORT register bit determines the port pin drive value.

If configured as an input, the PORT register bit determines whether a pull−up resistor is enabled (1) or disabled (0). Inputs have chmitt−trigger characteristic. Port A inputs may be disabled by setting the ANALOGA register bit; this prevents additional current consumption if the voltage level of the port pin is mid−way between logic low and logic high, when the pin is used as an analog input.

Port A, B and C pins may interrupt the microcontroller if their level changes. The INTCHG register bit enables the interrupt. The PIN register bit reflects the value of the port pin. Reading the PIN register also resets the interrupt if interrupt on change is enabled.

## APPLICATION INFORMATION

### Typical Application Diagrams

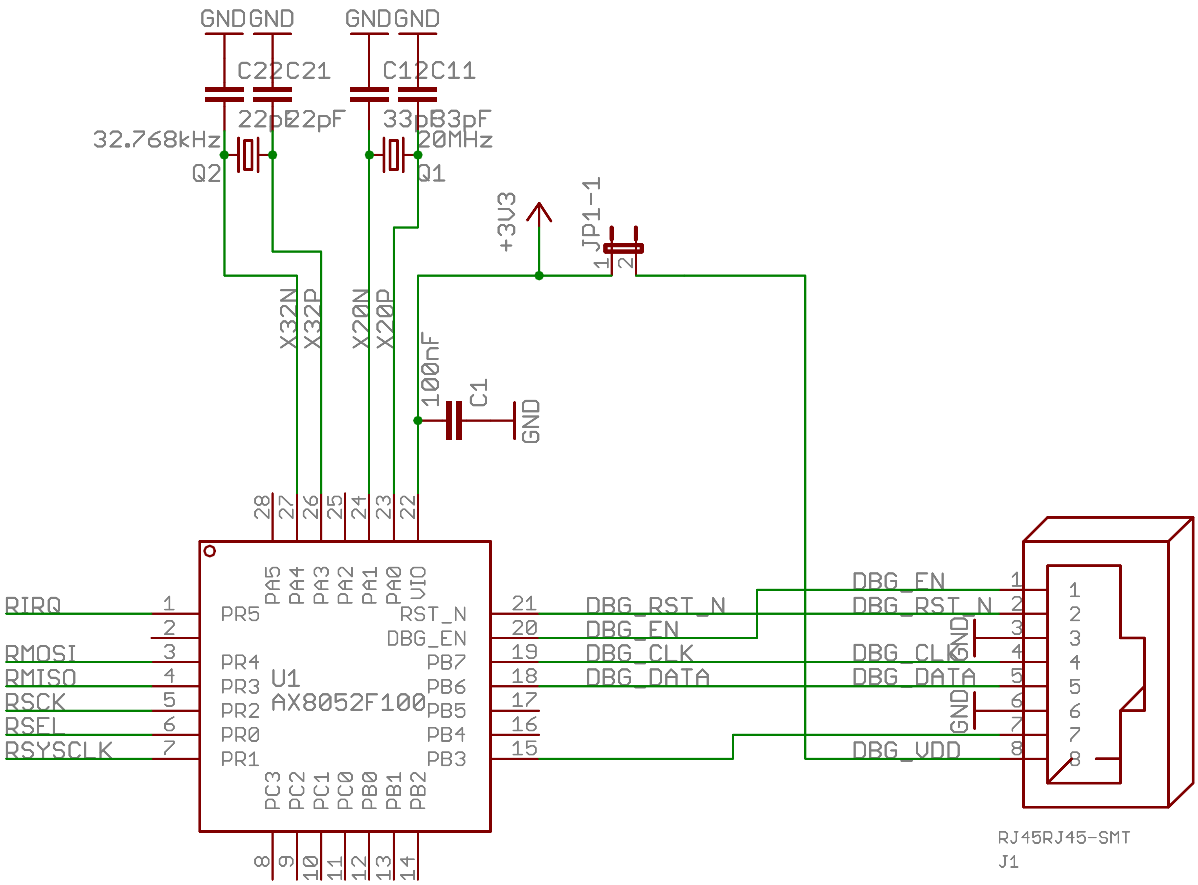



**Figure 9. Typical Application Diagram**

Figure 9 shows a typical application schematic.

Short Jumper JP1−1 if it is desired to supply the target board from the Debug Adapter (50 mA max). Connect the bottom exposed pad of the AX8052F100 to ground.

If the debugger is not running, PB6 and PB7 are not driven by the Debug Adapter. If the debugger is running, the PB6 and PB7 values that the software reads may be set using the Pin Emulation feature of the debugger.

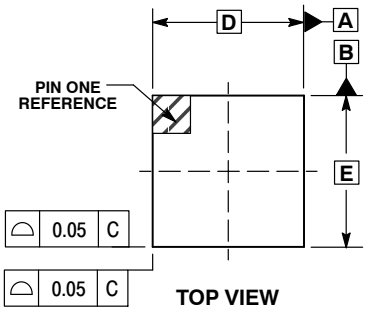
PB3 is driven by the debugger only to bring the AX8052F100 out of Deep Sleep. It is high impedance otherwise.

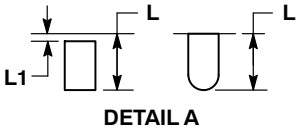
Port Pins PR0−PR5 may be used to connect an AXRadio Chip, or as General Purpose I/O.

Crystals are optional. Crystal Load Capacitances should be chosen according to the Crystal Datasheet.

## QFN28 PACKAGE INFORMATION

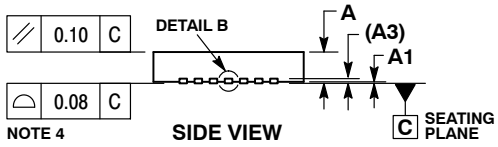
**QFN28 5x5, 0.5P**
CASE 485EH
ISSUE A

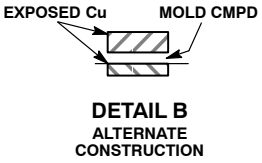


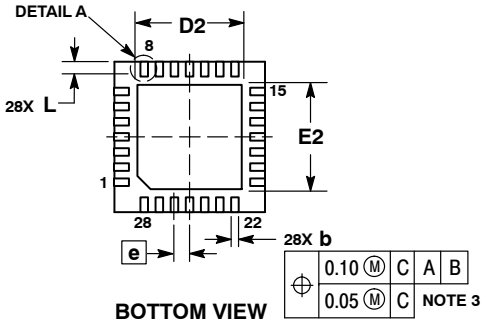




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

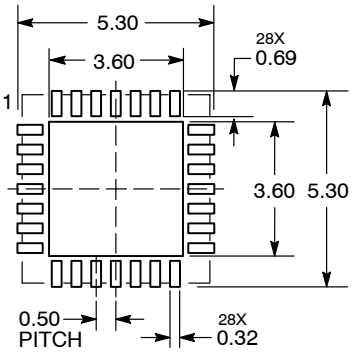
| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 5.00 BSC | |
| D2 | 3.40 | 3.50 |
| E | 5.00 BSC | |
| E2 | 3.40 | 3.50 |
| e | 0.50 BSC | |
| L | 0.44 | 0.54 |
| L1 | --- | 0.15 |




**RECOMMENDED SOLDERING FOOTPRINT***




DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### QFN28 Soldering Profile

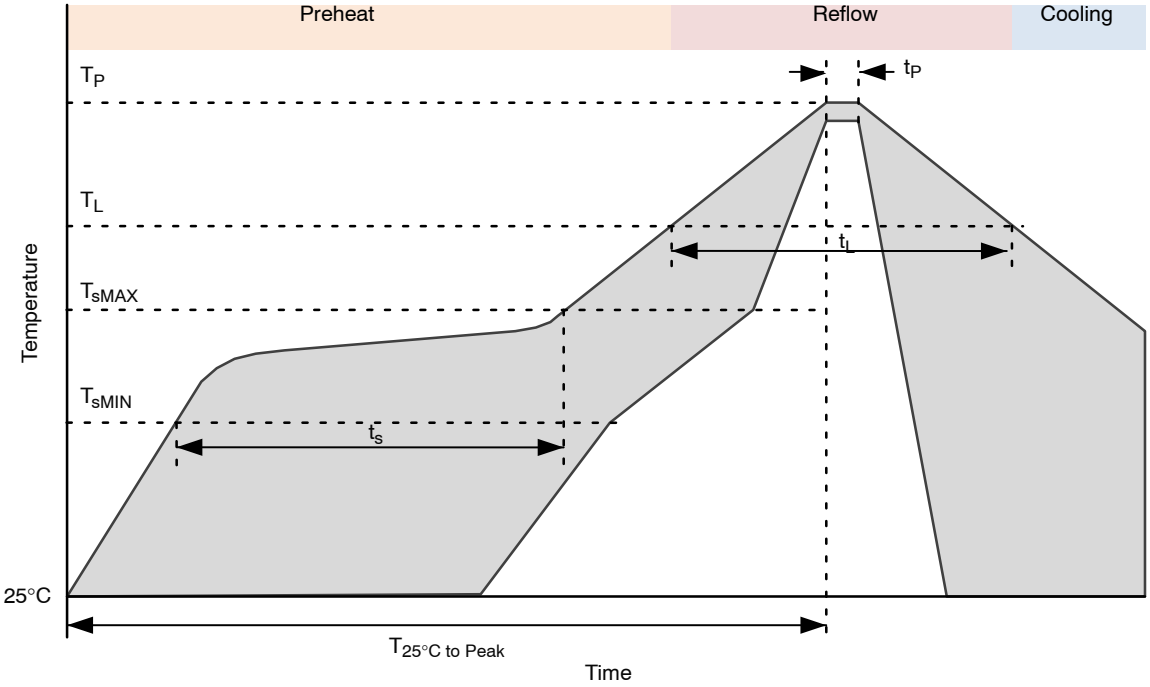



**Figure 10. QFN28 Soldering Profile**

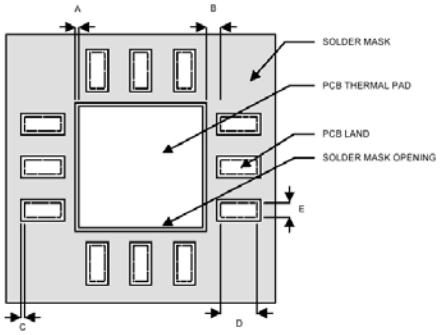
**Table 13.**

| Profile Feature | | Pb−Free Process |
|---|---|---|
| Average Ramp−Up Rate | | 3°C/s max. |
| Preheat Preheat | | |
| Temperature Min | $T_{sMIN}$ | 150°C |
| Temperature Max | $T_{sMAX}$ | 200°C |
| Time ($T_{sMIN}$ to $T_{sMAX}$) | $t_s$ | 60 − 180 sec |
| Time 25°C to Peak Temperature | $T_{25°C\ to\ Peak}$ | 8 min max. |
| Reflow Phase | | |
| Liquidus Temperature | $T_L$ | 217°C |
| Time over Liquidus Temperature | $t_L$ | 60 − 150 s |
| Peak Temperature | $t_p$ | 260°C |
| Time within 5°C of actual Peak Temperature | $T_p$ | 20 − 40 s |
| Cooling Phase | | |
| Ramp−down rate | | 6°C/s max. |

1. All temperatures refer to the top side of the package, measured on the package body surface.

### QFN28 Recommended Pad Layout

1. PCB land and solder masking recommendations are shown in Figure 11.




A = Clearance from PCB thermal pad to solder mask opening, 0.0635 mm minimum
B = Clearance from edge of PCB thermal pad to PCB land, 0.2 mm minimum
C = Clearance from PCB land edge to solder mask opening to be as tight as possible to ensure that some solder mask remains between PCB pads.
D = PCB land length = QFN solder pad length + 0.1 mm
E = PCB land width = QFN solder pad width + 0.1 mm

**Figure 11. PCB Land and Solder Mask Recommendations**

2. Thermal vias should be used on the PCB thermal pad (middle ground pad) to improve thermal conductivity from the device to a copper ground plane area on the reverse side of the printed circuit board. The number of vias depends on the package thermal requirements, as determined by thermal simulation or actual testing.
3. Increasing the number of vias through the printed circuit board will improve the thermal conductivity to the reverse side ground plane and external heat sink. In general, adding more metal through the PC board under the IC will improve operational heat transfer, but will require careful attention to uniform heating of the board during assembly.

### Assembly Process

*Stencil Design & Solder Paste Application*

1. Stainless steel stencils are recommended for solder paste application.
2. A stencil thickness of 0.125 – 0.150 mm (5 – 6 mils) is recommended for screening.
3. For the PCB thermal pad, solder paste should be printed on the PCB by designing a stencil with an array of smaller openings that sum to 50% of the QFN exposed pad area. Solder paste should be applied through an array of squares (or circles) as shown in Figure 12.
4. The aperture opening for the signal pads should be between 50−80% of the QFN pad area as shown in Figure 13.
5. Optionally, for better solder paste release, the aperture walls should be trapezoidal and the corners rounded.
6. The fine pitch of the IC leads requires accurate alignment of the stencil and the printed circuit board. The stencil and printed circuit assembly should be aligned to within + 1 mil prior to application of the solder paste.
7. No−clean flux is recommended since flux from underneath the thermal pad will be difficult to clean if water−soluble flux is used.

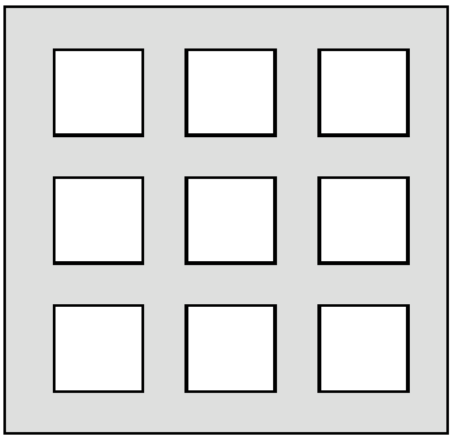


**Figure 12. Solder Paste Application on Exposed Pad**

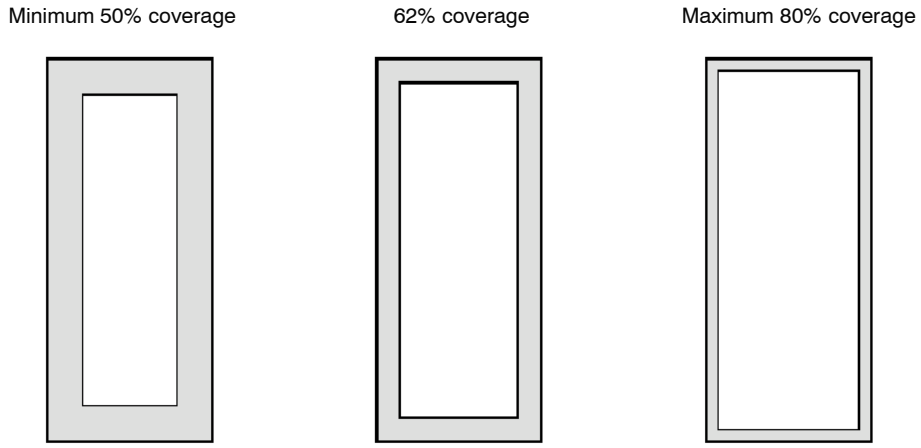



**Figure 13. Solder Paste Application on Pins**

## REFERENCES

[1] ON Semiconductor AX8052 Programming Manual, see http://www.onsemi.com
[2] ON Semiconductor AX8052 Silicon Errata, see http://www.onsemi.com

## DEVICE VERSIONS

The revision of the AX8052 silicon can be determined by the device marking or by reading the SILICONREV register. [2] documents the differences between silicon revisions.

**Table 14. DEVICE VERSIONS**

| Device Marking | AX8052 Version | SILICONREV |
|---|---|---|
| AX8052F100−1 | 1 | 0x8E (10001110) |
| AX8052F100−2 | 1C | 0x8F (10001111) |

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