PD-91866B

International
IOR Rectifier

SMPS MOSFET

IRFBA22N50A

HEXFET® Power MOSFET

Applications
- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

V_{DSS}	$R_{DS(on)}$ max	I_D
500V	**0.23Ω**	**24A**

Benefits
- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective Coss Specified (See AN1001)



Super-220™
(TO-273AA)

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	24	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	15	
I_{DM}	Pulsed Drain Current ①	96	
P_D @T_C = 25°C	Power Dissipation	340	W
	Linear Derating Factor	2.7	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	3.4	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Recommended clip force	20	N

Applicable Off Line SMPS Topologies:

- Full Bridge Converters
- Power Factor Correction Boost

Notes ① through ⑤ are on page 8

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	V_{GS} = 0V, I_D = 250µA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.23	Ω	V_{GS} = 10V, I_D = 13.8A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 500V, V_{GS} = 0V
		—	—	250		V_{DS} = 400V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	12	—	—	S	V_{DS} = 50V, I_D = 13.8A
Q_g	Total Gate Charge	—	—	114	nC	I_D = 23A
Q_{gs}	Gate-to-Source Charge	—	—	28		V_{DS} = 400V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	47		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	20	—	ns	V_{DD} = 250V
t_r	Rise Time	—	66	—		I_D = 23A
$t_{d(off)}$	Turn-Off Delay Time	—	46	—		R_G = 4.3Ω
t_f	Fall Time	—	44	—		R_D = 10.6Ω,See Fig. 10 ④
C_{iss}	Input Capacitance	—	3397	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	505	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	17	—		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	—	4884	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	134	—		V_{GS} = 0V, V_{DS} = 400V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	—	154	—		V_{GS} = 0V, V_{DS} = 0V to 400V ⑤

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	1180	mJ
I_{AR}	Avalanche Current①	—	24	A
E_{AR}	Repetitive Avalanche Energy①	—	34	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.37	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	58	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	23	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	92		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	T_J = 25°C, I_S = 23A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	490	735	ns	T_J = 25°C, I_F = 23A
Q_{rr}	Reverse RecoveryCharge	—	6.4	9.6	µC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

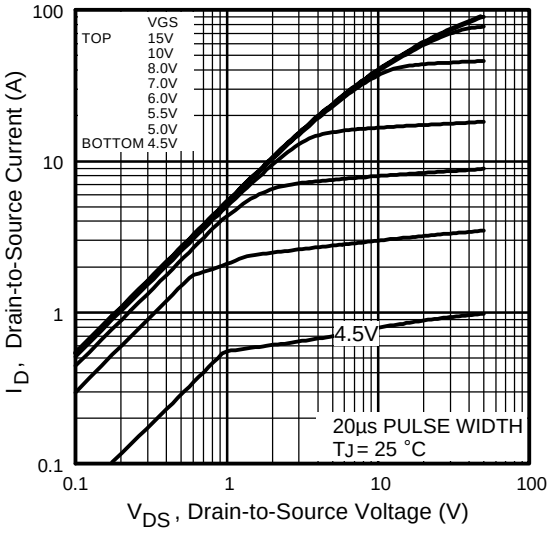


Fig 1. Typical Output Characteristics

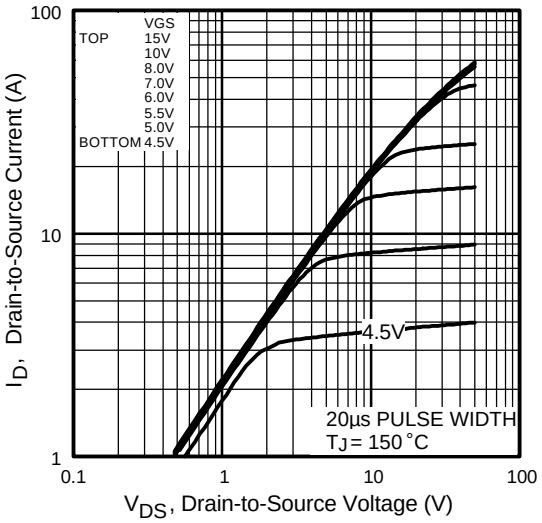


Fig 2. Typical Output Characteristics

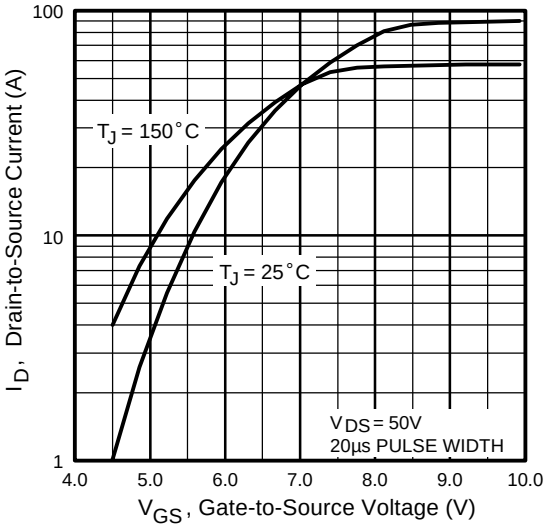


Fig 3. Typical Transfer Characteristics

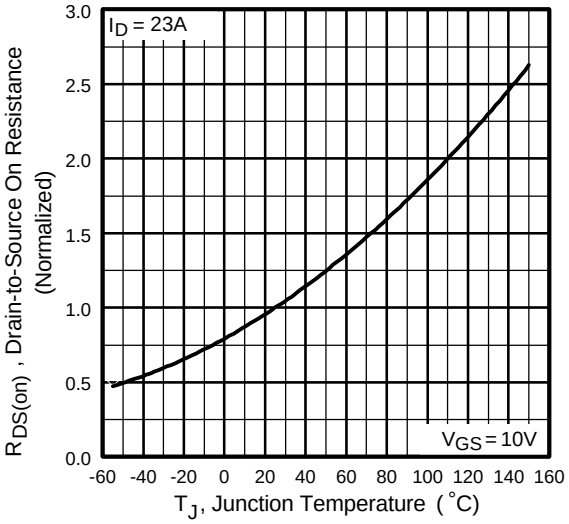


Fig 4. Normalized On-Resistance Vs. Temperature

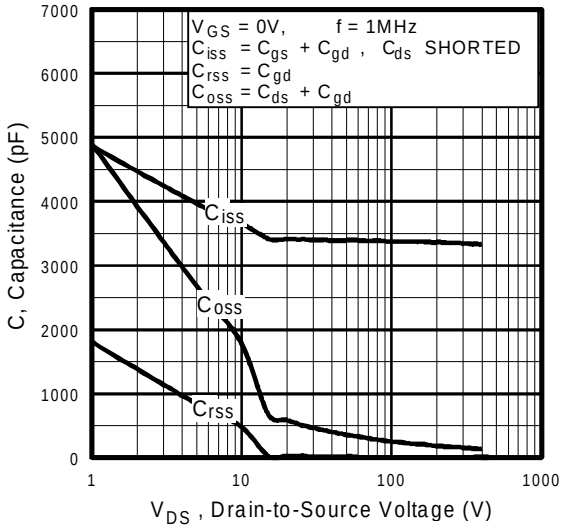


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

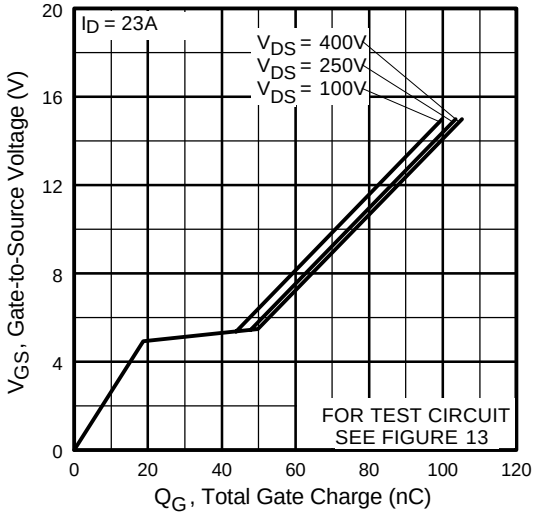


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

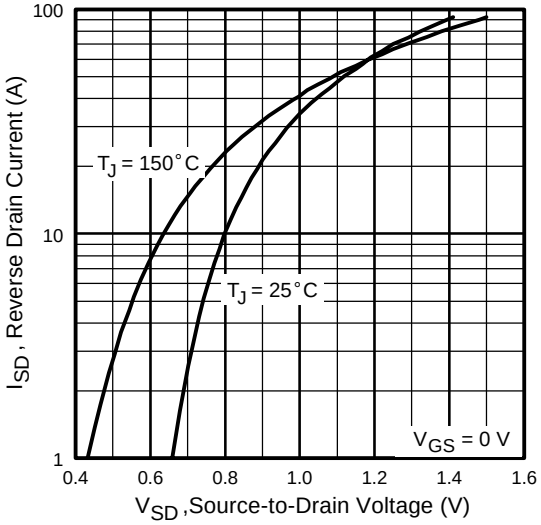


Fig 7. Typical Source-Drain Diode Forward Voltage

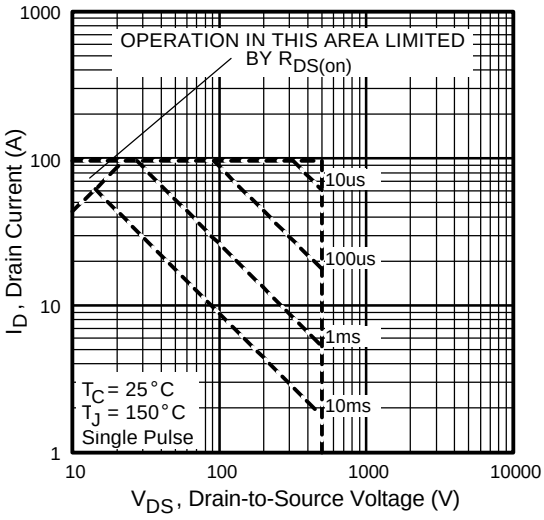


Fig 8. Maximum Safe Operating Area

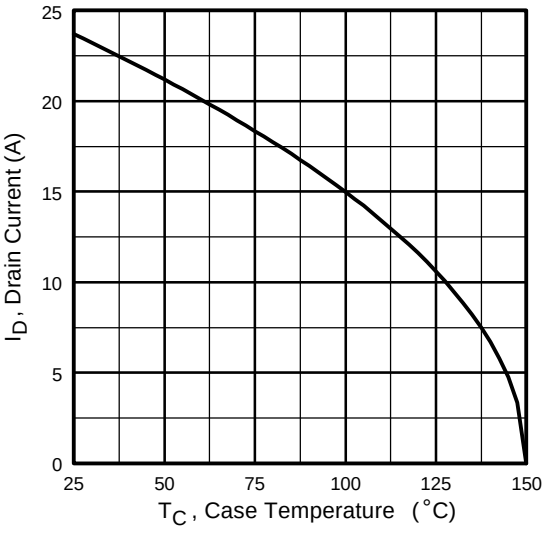


Fig 9. Maximum Drain Current Vs. Case Temperature

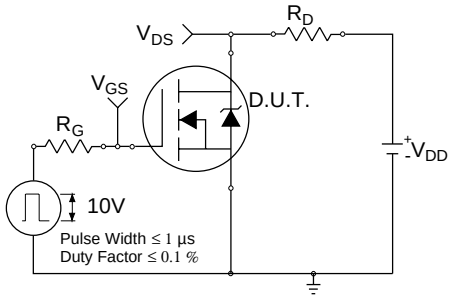


Fig 10a. Switching Time Test Circuit

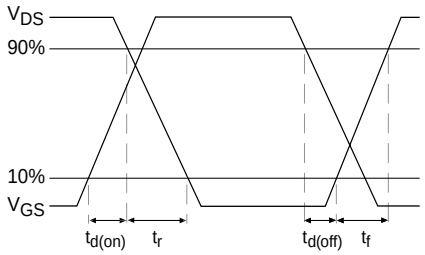


Fig 10b. Switching Time Waveforms

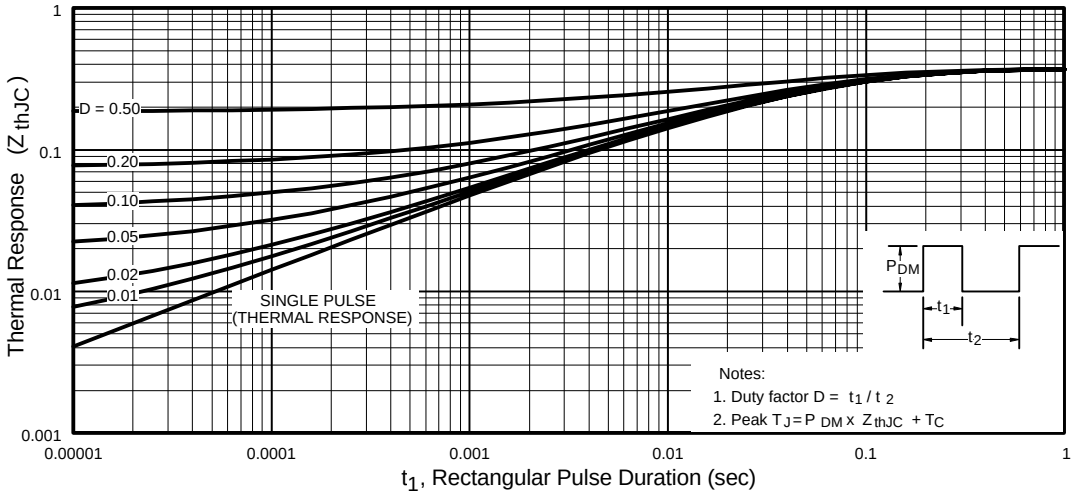


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

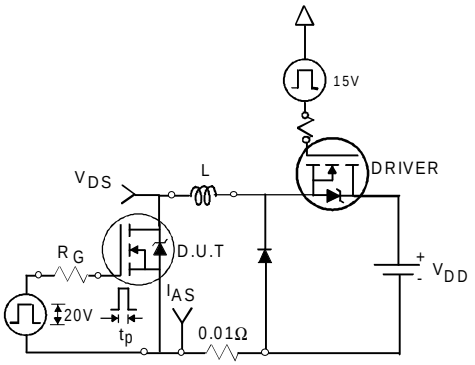


Fig 12a. Unclamped Inductive Test Circuit

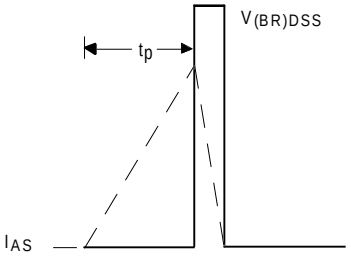


Fig 12b. Unclamped Inductive Waveforms

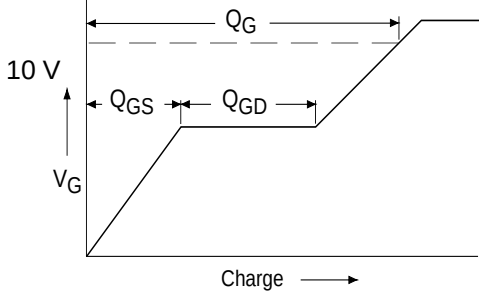


Fig 13a. Basic Gate Charge Waveform

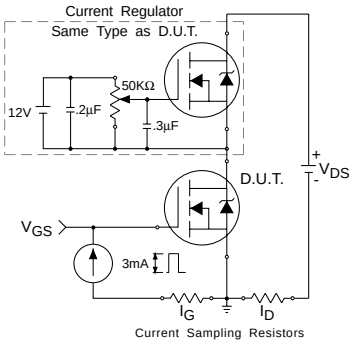


Fig 13b. Gate Charge Test Circuit

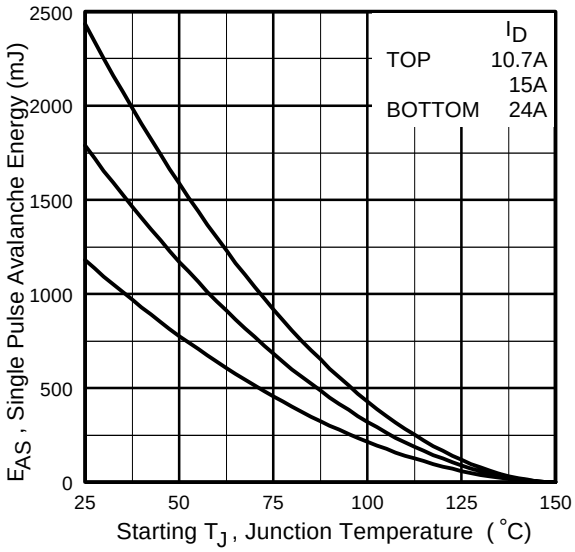


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

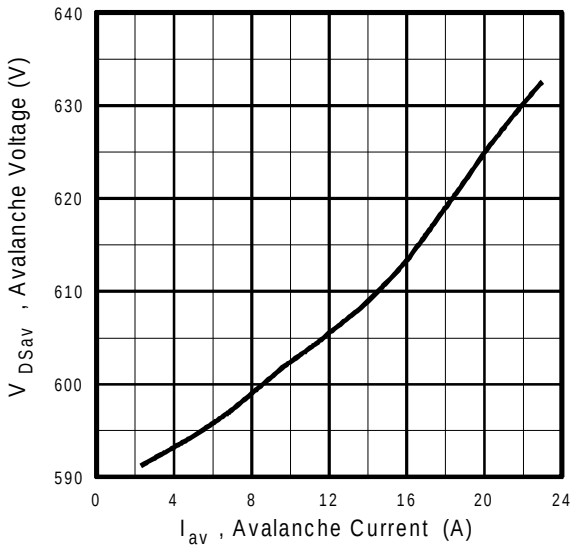
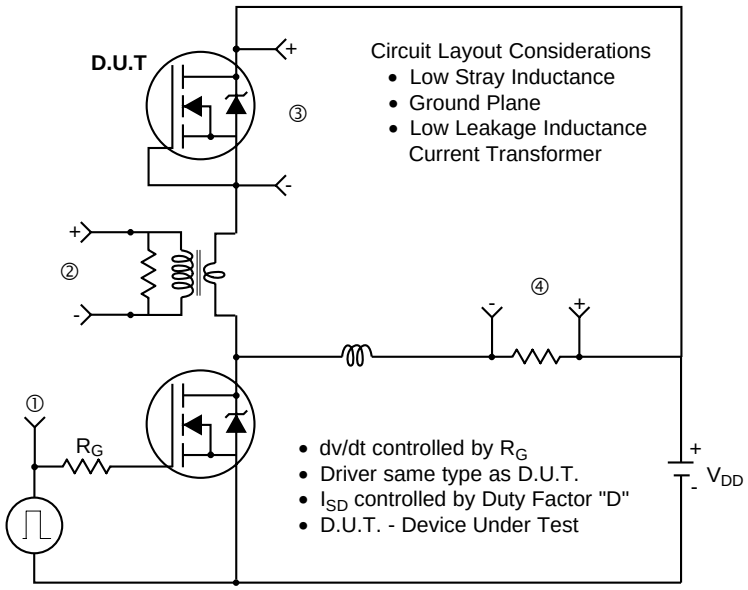
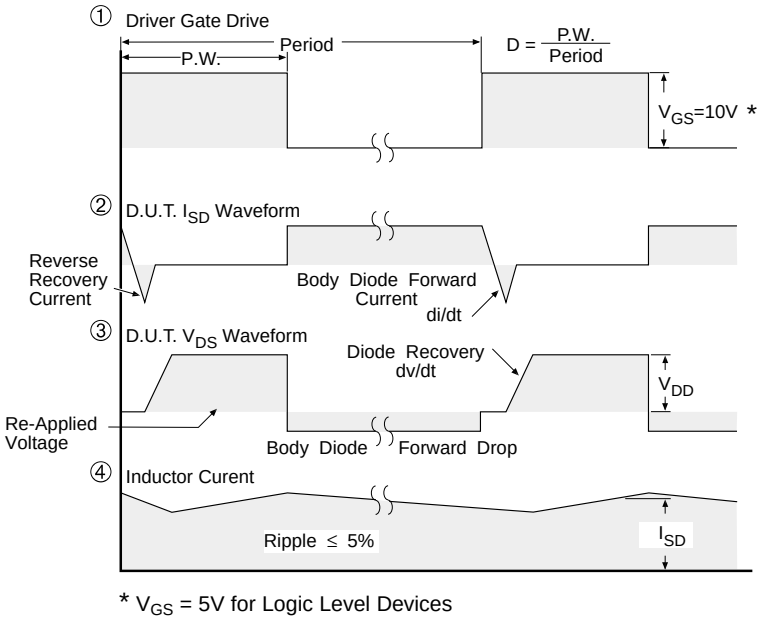


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

Peak Diode Recovery dv/dt Test Circuit





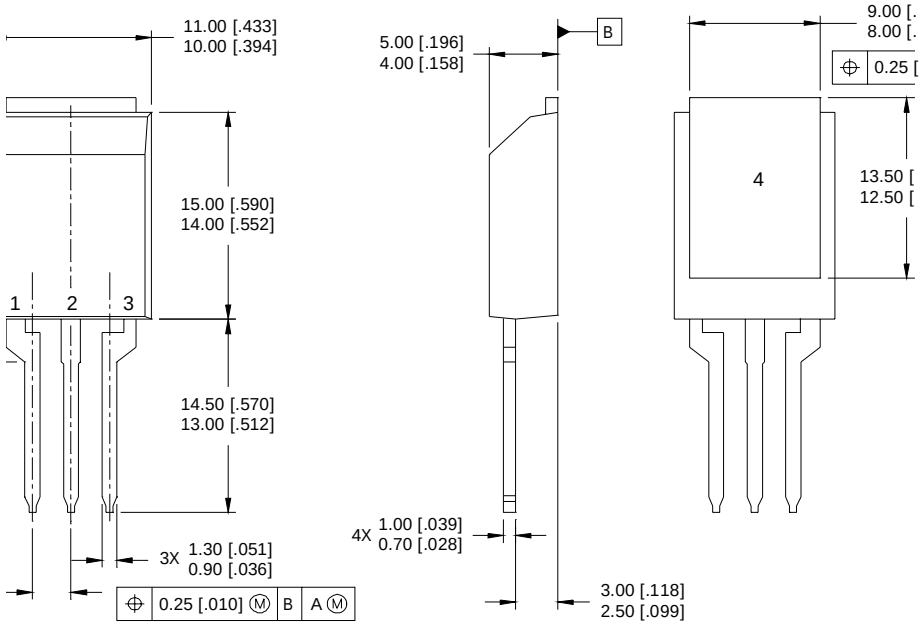
* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFET

IRFBA22N50A

International
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Super-220™ (TO-273AA) Package Outline



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO–273AA.

LEAD ASSIGNMENTS

MOSFET	IGBT
1 – GATE	1 – GATE
2 – DRAIN	2 – COLLECTOR
3 – SOURCE	3 – EMITTER
4 – DRAIN	4 – COLLECTOR

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 3.4mH R_G = 25Ω, I_{AS} = 24A. (See Figure 12)

③ $I_{SD} \leq$ 23A, di/dt ≤ 123A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 150°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

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