National Semiconductor

PRELIMINARY
May 2006

ADC14155
14-Bit, 155 MSPS, 1.1 GHz Bandwidth A/D Converter

General Description

The ADC14155 is a high-performance CMOS analog-to-digital converter capable of converting analog input signals into 14-bit digital words at rates up to 155 Mega Samples Per Second (MSPS). This converter uses a differential, pipelined architecture with digital error correction and an on-chip sample-and-hold circuit to minimize power consumption and the external component count, while providing excellent dynamic performance. A unique sample-and-hold stage yields a full-power bandwidth of 1.1 GHz. The ADC14155 operates from dual +3.3V and +1.8V power supplies and consumes 974 mW of power at 155 MSPS.

The separate +1.8V supply for the digital output interface allows lower power operation with reduced noise. A power-down feature reduces the power consumption to 5 mW with the clock input disabled, while still allowing fast wake-up time to full operation.

The differential inputs provide a full scale differential input swing equal to 2 times the reference voltage. A stable 1.0V internal voltage reference is provided, or the ADC14155 can be operated with an external reference.

For optimum performance, it is recommended to operate the ADC14155 with a differential clock input, which doubles the clock amplitude compared with single-ended clock operation. Clock mode (differential versus single-ended) and output data format (offset binary versus 2's complement) are pin-selectable. A duty cycle stabilizer maintains performance over a wide range of clock duty cycles.

The ADC14155 is available in a 48-lead LLP package and operates over the industrial temperature range of –40˚C to +85˚C.

Features

- 1.1 GHz Full Power Bandwidth
- Internal sample-and-hold circuit
- Low power consumption
- Internal precision 1.0V reference
- Single-ended or Differential clock modes
- Data Ready output clock
- Clock Duty Cycle Stabilizer
- Dual +3.3V and +1.8V supply operation (+/- 10%)
- Power-down mode
- Offset binary or 2's complement output data format
- 48-pin LLP package, (7x7x0.8mm, 0.5mm pin-pitch)

Key Specifications

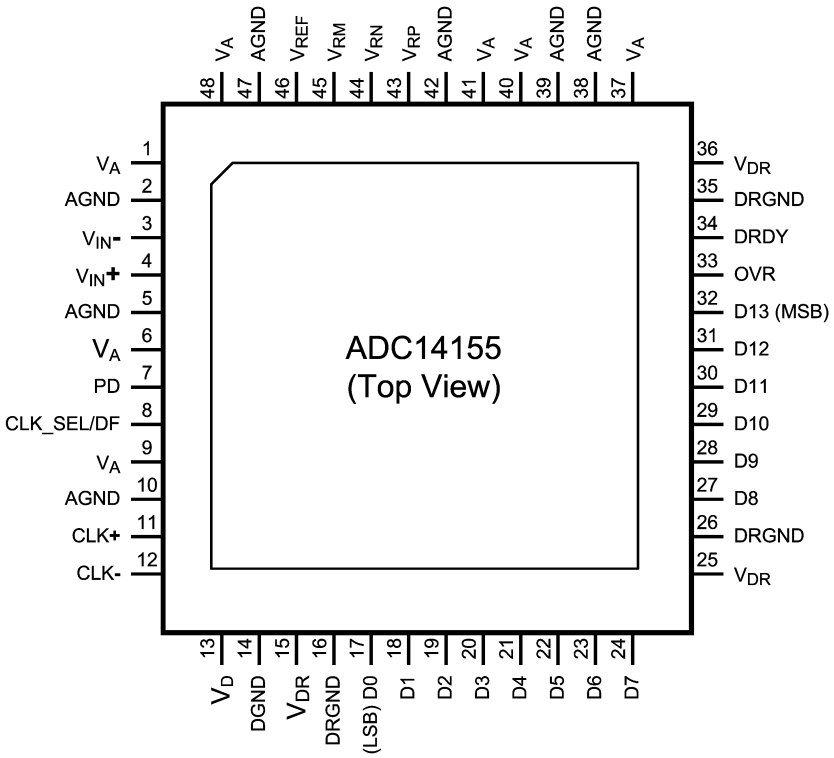
Resolution	14 Bits
Conversion Rate	155 MSPS
SNR (f_{IN} = 70 MHz)	71.4 dBFS (typ)
SFDR (f_{IN} = 70 MHz)	85.3 dBFS (typ)
ENOB (f_{IN} = 70 MHz)	11.5 bits (typ)
Full Power Bandwidth	1.1 GHz (typ)
Power Consumption	974 mW (typ)

Applications

- High IF Sampling Receivers
- Wireless Base Station Receivers
- Power Amplifier Linearization
- Multi-carrier, Multi-mode Receivers
- Test and Measurement Equipment
- Communications Instrumentation
- Radar Systems

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Connection Diagram

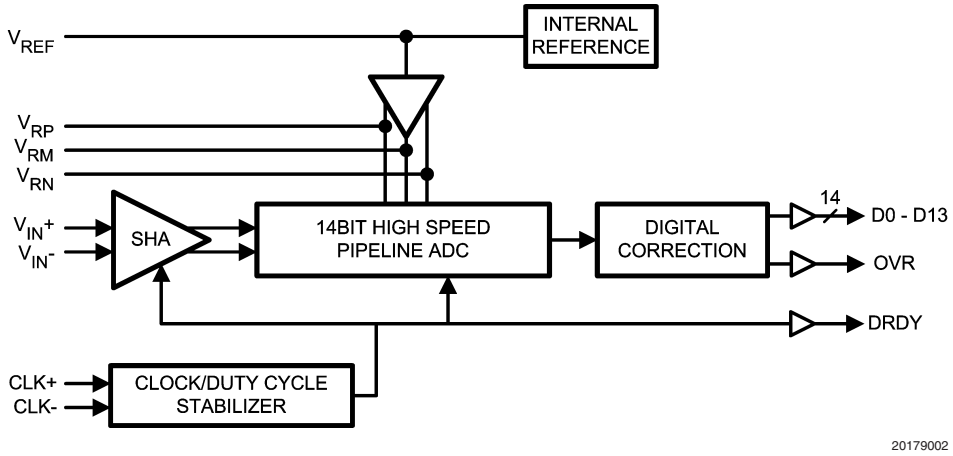


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Ordering Information

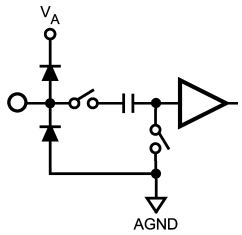
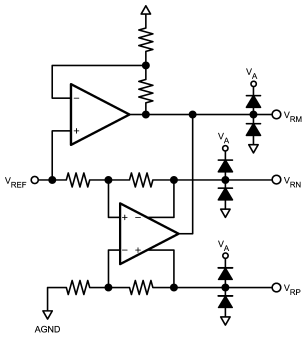
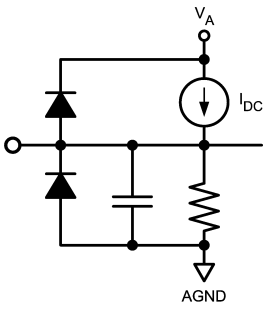
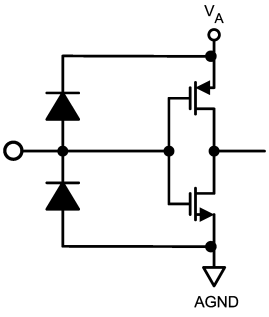
Industrial (–40˚C ≤ T_A ≤ +85˚C)	Package
ADC14155CISQ	48 Pin LLP
ADC14155EB	Evaluation Board

Block Diagram

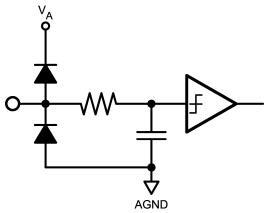
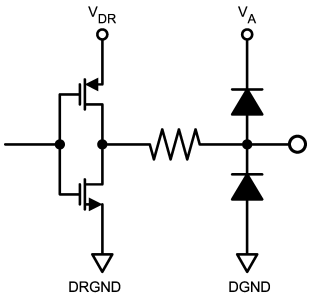


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Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
3	$V_{IN}-$		Differential analog input pins. The differential full-scale input signal level is two times the reference voltage with each input pin signal centered on a common mode voltage, V_{CM}.
4	$V_{IN}+$		
43	V_{RP}		These pins should each be bypassed to AGND with a low ESL (equivalent series inductance) 0.1 µF capacitor placed very close to the pin to minimize stray inductance. A 0.1 µF capacitor should be placed between V_{RP} and V_{RN} as close to the pins as possible, and a 10 µF capacitor should be placed in parallel. V_{RP} and V_{RN} should not be loaded. V_{RM} may be loaded to 1mA for use as a temperature stable 1.5V reference. It is recommended to use V_{RM} to provide the common mode voltage, V_{CM}, for the differential analog inputs, $V_{IN}+$ and $V_{IN}-$.
45	V_{RM}		
44	V_{RN}		
46	V_{REF}		This pin can be used as either the +1.0V internal reference voltage output (internal reference operation) or as the external reference voltage input (external reference operation). To use the internal reference, V_{REF} should be decoupled to AGND with a 0.1 µF, low equivalent series inductance (ESL) capacitor. In this mode, V_{REF} defaults as the output for the internal 1.0V reference. To use an external reference, overdrive this pin with a low noise external reference voltage. The output impedance of the internal reference at this pin is 9kΩ. Therefore, to overdrive this pin, the impedance of the external reference source should be << 9kΩ. This pin should not be used to source or sink current. The full scale differential input voltage range is 2 * V_{REF}.
DIGITAL I/O			
11	CLK+		The clock input pins can be configured to accept either a single-ended or a differential clock input signal. When the single-ended clock mode is selected through CLK_SEL/DF (pin 8), connect the clock input signal to the CLK+ pin and connect the CLK– pin to AGND. When the differential clock mode is selected through CLK_SEL/DF (pin 8), connect the positive and negative clock inputs to the CLK+ and CLK– pins, respectively. The analog input is sampled on the falling edge of the clock input.
12	CLK–		

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
8	CLK_SEL/DF		This is a four-state pin controlling the input clock mode and output data format. CLK_SEL/DF = V_A, CLK+ and CLK– are configured as a differential clock input. The output data format is 2's complement. CLK_SEL/DF = (2/3)*V_A, CLK+ and CLK– are configured as a differential clock input. The output data format is offset binary. CLK_SEL/DF = (1/3)*V_A, CLK+ is configured as a single-ended clock input and CLK– should be tied to AGND. The output data format is 2's complement. CLK_SEL/DF = AGND, CLK+ is configured as a single-ended clock input and CLK– should be tied to AGND. The output data format is offset binary.
7	PD		This is a two-state input controlling Power Down. PD = V_A, Power Down is enabled. In the Power Down state only the reference voltage circuitry remains active and power dissipation is reduced. PD = AGND, Normal operation.
17-24, 27-32	D0–D13		Digital data output pins that make up the 14-bit conversion result. D0 (pin 17) is the LSB, while D13 (pin 32) is the MSB of the output word. Output levels are CMOS compatible.
33	OVR		Over-Range Indicator. This output is set HIGH when a sample amplitude exceeds the 14-bit conversion range (0 to 16383).
34	DRDY		Data Ready Strobe. This pin is used to clock the output data. It has the same frequency as the sampling clock. One word of data is output in each cycle of this signal. The rising edge of this signal should be used to capture the output data.
ANALOG POWER			
1, 6, 9, 37, 40, 41, 48	V_A		Positive analog supply pins. These pins should be connected to a quiet +3.3V source and be bypassed to AGND with 100 pF and 0.1 µF capacitors located close to the power pins.
2, 5, 10, 38, 39, 42, 47	AGND		The ground return for the analog supply.
DIGITAL POWER			
13	V_D		Positive digital supply pin. This pin should be connected to a quiet +3.3V source and be bypassed to DGND with a 100 pF and 0.1 µF capacitor located close to the power pin.
14	DGND		The ground return for the digital supply.
15, 25, 36	V_{DR}		Positive driver supply pin for the ADC14155's output drivers. This pin should be connected to a quiet voltage source of +1.8V and be bypassed to DRGND with 100 pF and 0.1 µF capacitors located close to the power pins.
16, 26, 35	DRGND		The ground return for the digital output driver supply. These pins should be connected to the system digital ground, but not be connected in close proximity to the ADC's DGND or AGND pins. See Section 6.0 (Layout and Grounding) for more details.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_A, V_D)	−0.3V to 4.2V
Supply Voltage (V_{DR})	−0.3V to 2.4V
$\lvert V_A - V_D \rvert$	≤ 100 mV
Voltage on Any Input Pin	−0.3V to (V_A +0.3V)
Voltage on Any Output Pin	-0.3V to (V_{DR} +0.2V)
Input Current at Any Pin other than Supply Pins (Note 3)	±5 mA
Package Input Current (Note 3)	±TBD mA
Max Junction Temp (T_J)	+150˚C
Thermal Resistance (θ_{JA})	24˚C/W
Package Dissipation at T_A = 25˚C (Note 4)	5.2W
ESD Rating	
Human Body Model (1.5kΩ, 100pF)	2500V
Machine Model (0Ω, 200pF)	250V
Storage Temperature	−65˚C to +150˚C
Soldering process must comply with National Semiconductor's Reflow Temperature Profile specifications. Refer to www.national.com/packaging. (Note 5)	

Operating Ratings (Notes 1, 2)

Operating Temperature	−40˚C ≤ T_A ≤ +85˚C
Supply Voltage (V_A, V_D)	+3.0V to +3.6V
Output Driver Supply (V_{DR})	+1.6V to +2.0V
CLK	−0.05V to (V_A + 0.05V)
Clock Duty Cycle	30/70 %
Analog Input Pins	0V to 2.6V
V_{CM}	1.4V to 1.6V
|AGND-DGND|	≤100mV

Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DGND = DRGND = 0V, V_A = V_D = +3.3V, V_{DR} = +1.8V, Internal V_{REF} = +1.0V, f_{CLK} = 155 MHz, V_{CM} = V_{RM}, t_r = t_f = TBD ns, C_L = 5 pF/pin, Differential Clock Mode, Offset Binary Format. Typical values are for T_A = 25˚C. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25˚C (Notes 6, 7, 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 9)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**14**	Bits (min)
INL	Integral Non Linearity (Note 10)		±1.5	**TBD**	LSB (max)
DNL	Differential Non Linearity		±0.5	**TBD**	LSB (max)
PGE	Positive Gain Error		+0.3	**TBD**	%FS (max)
NGE	Negative Gain Error		+0.03	**TBD**	%FS (max)
TC GE	Gain Error Tempco	−40˚C ≤ T_A ≤ +85˚C	TBD		ppm/˚C
V_{OFF}	Offset Error (V_{IN}+ = V_{IN}−)		−0.1	**TBD**	%FS (max)
TC V_{OFF}	Offset Error Tempco	−40˚C ≤ T_A ≤ +85˚C	TBD		ppm/˚C
	Under Range Output Code		0	**0**	
	Over Range Output Code		16383	**16383**	
REFERENCE AND ANALOG INPUT CHARACTERISTICS					
V_{CM}	Common Mode Input Voltage		1.5	**1.5±0.1**	V
V_{RM}	Reference Ladder Midpoint Output Voltage	Output load = 1 mA	1.5	**TBD**	V

Converter Electrical Characteristics (Continued)

Unless otherwise specified, the following specifications apply: AGND = DGND = DRGND = 0V, $V_A = V_D = +3.3V$, $V_{DR} = +1.8V$, Internal $V_{REF} = +1.0V$, $f_{CLK} = 155$ MHz, $V_{CM} = V_{RM}$, $t_r = t_f =$ TBD ns, $C_L = 5$ pF/pin, Differential Clock Mode, Offset Binary Format. Typical values are for $T_A = 25^\circ C$. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for $T_A = 25^\circ C$ (Notes 6, 7, 8)

Symbol	Parameter	Conditions		Typical (Note 9)	Limits (Note 9)	Units (Limits)
C_{IN}	V_{IN} Input Capacitance (each pin to GND) (Note 11)	V_{IN} = 1.5 Vdc ± 0.5 V	(CLK LOW)	9		pF
			(CLK HIGH)	6		pF
V_{REF}	Reference Voltage (Note 12)			1.00	**0.9** **1.1**	V (min) V (max)
	Reference Input Resistance			TBD		MΩ (min)

Dynamic Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DGND = DRGND = 0V, $V_A = V_D = +3.3V$, $V_{DR} = +1.8V$, Internal $V_{REF} = +1.0V$, $f_{CLK} = 155$ MHz, $V_{CM} = V_{RM}$, $t_r = t_f =$ TBD ns, $C_L = 5$ pF/pin, Differential Clock Mode, Offset Binary Format. Typical values are for $T_A = 25^\circ C$. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for $T_A = 25^\circ C$ (Note 6) (Notes 7, 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 9)	Units (Limits)
DYNAMIC CONVERTER CHARACTERISTICS, A_{IN} = -1dBFS					
FPBW	Full Power Bandwidth	-1 dBFS Input, –3 dB Corner	1.1		GHz
SNR	Signal-to-Noise Ratio	f_{IN} = 10 MHz	72.3		dBFS
		f_{IN} = 70 MHz	71.4	**TBD**	dBFS
		f_{IN} = 169 MHz	71.0		dBFS
		f_{IN} = 238 MHz	70.4		dBFS
		f_{IN} = 398 MHz	TBD		dBFS
SFDR	Spurious Free Dynamic Range	f_{IN} = 10 MHz	87.0		dBFS
		f_{IN} = 70 MHz	85.3	**TBD**	dBFS
		f_{IN} = 169 MHz	80.0		dBFS
		f_{IN} = 238 MHz	76.2		dBFS
		f_{IN} = 398 MHz	TBD		dBFS
ENOB	Effective Number of Bits	f_{IN} = 10 MHz	11.7		Bits
		f_{IN} = 70 MHz	11.5	**TBD**	Bits
		f_{IN} = 169 MHz	11.2		Bits
		f_{IN} = 238 MHz	11.0		Bits
		f_{IN} = 398 MHz	TBD		Bits
THD	Total Harmonic Disortion	f_{IN} = 10 MHz	82.4		dBFS
		f_{IN} = 70 MHz	80.3	**TBD**	dBFS
		f_{IN} = 169 MHz	77.1		dBFS
		f_{IN} = 238 MHz	71.9		dBFS
		f_{IN} = 398 MHz	TBD		dBFS
H2	Second Harmonic Distortion	f_{IN} = 10 MHz	91.2		dBFS
		f_{IN} = 70 MHz	92.4		dBFS
		f_{IN} = 169 MHz	80.1		dBFS
		f_{IN} = 238 MHz	76.3		dBFS
		f_{IN} = 398 MHz	TBD		dBFS
H3	Third Harmonic Distortion	f_{IN} = 10 MHz	87.1		dBFS
		f_{IN} = 70 MHz	85.2		dBFS
		f_{IN} = 169 MHz	83.6		dBFS
		f_{IN} = 238 MHz	83.4		dBFS
		f_{IN} = 398 MHz	TBD		dBFS

Dynamic Converter Electrical Characteristics (Continued)

Unless otherwise specified, the following specifications apply: AGND = DGND = DRGND = 0V, $V_A = V_D = +3.3V$, $V_{DR} = +1.8V$, Internal $V_{REF} = +1.0V$, $f_{CLK} = 155$ MHz, $V_{CM} = V_{RM}$, $t_r = t_f =$ TBD ns, $C_L = 5$ pF/pin, Differential Clock Mode, Offset Binary Format. Typical values are for $T_A = 25^\circ C$. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for $T_A = 25^\circ C$ (Note 6) (Notes 7, 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 9)	Units (Limits)
SINAD	Signal-to-Noise and Distortion Ratio	$f_{IN} = 10$ MHz	72.2		dBFS
		$f_{IN} = 70$ MHz	70.9	**TBD**	dBFS
		$f_{IN} = 169$ MHz	69.1		dBFS
		$f_{IN} = 238$ MHz	67.9		dBFS
		$f_{IN} = 398$ MHz	TBD		dBFS
IMD	Intermodulation Distortion	$f_{IN} = 19.5$ MHz and 20.5 MHz, each = −6.5 dBFS	TBD		dBFS

Logic and Power Supply Electrical Characteristics

Unless otherwise specified, the following specifications apply: AGND = DGND = DRGND = 0V, $V_A = V_D = +3.3V$, $V_{DR} = +1.8V$, Internal $V_{REF} = +1.0V$, $f_{CLK} = 155$ MHz, $V_{CM} = V_{RM}$, $t_r = t_f =$ TBD ns, $C_L = 5$ pF/pin, Differential Clock Mode, Offset Binary Format. Typical values are for $T_A = 25^\circ C$. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for $T_A = 25^\circ C$ (Notes 6, 7, 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 9)	Units (Limits)
DIGITAL INPUT CHARACTERISTICS (CLK, PD/DCS, CLK_SEL/DF)					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_D = 3.6V$		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$V_D = 3.0V$		**1.0**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 3.3V$	10		µA
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$	−10		µA
C_{IN}	Digital Input Capacitance		5		pF
DIGITAL OUTPUT CHARACTERISTICS (D0–D13, DRDY, OVR)					
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_{OUT} = -0.5$ mA , $V_{DR} = 1.8V$		**1.2**	V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_{OUT} = 1.6$ mA, $V_{DR} = 1.8V$		**0.4**	V (max)
$+I_{SC}$	Output Short Circuit Source Current	$V_{OUT} = 0V$	−10		mA
$-I_{SC}$	Output Short Circuit Sink Current	$V_{OUT} = V_{DR}$	10		mA
C_{OUT}	Digital Output Capacitance		5		pF
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	Full Operation Powerdown (No Clock)	286 1.5	**TBD**	mA (max) mA
I_D	Digital Supply Current	Full Operation Powerdown	9 0	**TBD**	mA (max) mA
I_{DR}	Digital Output Supply Current	Full Operation (Note 13) Powerdown	15 0	**TBD**	mA (max) mA
	Power Consumption	Excludes I_{DR} (Note 13)	974	**TBD**	mW (max)
	Power Down Power Consumption	Clock disabled	5		mW
PSRR	Power Supply Rejection Ratio	Ratio of Full-Scale Output with V_A =3.0V vs. 3.6V	TBD		dB

Timing and AC Characteristics

Unless otherwise specified, the following specifications apply: AGND = DGND = DRGND = 0V, V_A = V_D = +3.3V, V_{DR} = +1.8V, Internal V_{REF} = +1.0V, f_{CLK} = 155 MHz, V_{CM} = V_{RM}, t_r = t_f = TBD ns, C_L = 5 pF/pin, Differential Clock Mode, Offset Binary Format. Typical values are for T_A = 25˚C. Timing measurements are taken at 50% of the signal amplitude. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for T_A = 25˚C (Notes 6, 7, 8)

Parameter	Conditions	Typical (Note 9)	Limits (Note 9)	Units (Limits)
Maximum Clock Frequency			**155**	MHz (max)
Minimum Clock Frequency			**5**	MHz (min)
Clock High Time		TBD		ns (min)
Clock Low Time		TBD		ns (min)
Conversion Latency			**8**	Clock Cycles
Output Delay of CLK to DATA	Relative to falling edge of CLK	2.0	**TBD**	ns (max)
Data Output Setup Time	Relative to DRDY	2.1	**1.5**	ns (min)
Data Output Hold Time	Relative to DRDY	2.1	**1.5**	ns (min)
Aperture Delay		TBD		ns
Aperture Jitter		0.08		ps rms
Power Down Recovery Time	0.1 µF on pins 43, 44; 10 µF and 0.1 µF between pins 43, 44; 0.1 µF and 10 µF on pins 46, 46	3		ms

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is guaranteed to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.

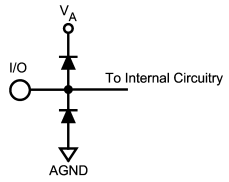
Note 2: All voltages are measured with respect to GND = AGND = DGND = DRGND = 0V, unless otherwise specified.

Note 3: When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or V_{IN} > V_A), the current at that pin should be limited to 5 mA. The TBD mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to TBD.

Note 4: The maximum allowable power dissipation is dictated by $T_{J,max}$, the junction-to-ambient thermal resistance, (θ_{JA}), and the ambient temperature, (T_A), and can be calculated using the formula $P_{D,max} = (T_{J,max} - T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions should always be avoided.

Note 5: Reflow temperature profiles are different for lead-free and non-lead-free packages.

Note 6: The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per (Note 3). However, errors in the A/D conversion can occur if the input goes above 2.6V or below GND as described in the Operating Ratings section.



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Note 7: To guarantee accuracy, it is required that $|V_A - V_D| \le 100$ mV and separate bypass capacitors are used at each power supply pin.

Note 8: With the test condition for V_{REF} = +1.0V ($2V_{P-P}$ differential input), the 14-bit LSB is 122.1 µV.

Note 9: Typical figures are at T_A = 25˚C and represent most likely parametric norms at the time of product characterization. The typical specifications are not guaranteed.

Note 10: Integral Non Linearity is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive and negative full-scale.

Note 11: The input capacitance is the sum of the package/pin capacitance and the sample and hold circuit capacitance.

Note 12: Optimum performance will be obtained by keeping the reference input in the 0.9V to 1.1V range. The LM4051CIM3-ADJ (SOT-23 package) is recommended for external reference applications.

Note 13: I_{DR} is the current consumed by the switching of the output drivers and is primarily determined by load capacitance on the output pins, the supply voltage, V_{DR}, and the rate at which the outputs are switching (which is signal dependent). $I_{DR}=V_{DR}(C_0 \times f_0 + C_1 \times f_1 + ...C_{11} \times f_{11})$ where V_{DR} is the output driver power supply voltage, C_n is total capacitance on the output pin, and f_n is the average frequency at which that pin is toggling.

Specification Definitions

APERTURE DELAY is the time after the falling edge of the clock to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

CLOCK DUTY CYCLE is the ratio of the time during one cycle that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

COMMON MODE VOLTAGE (V_{CM}) is the common DC voltage applied to both input terminals of the ADC.

CONVERSION LATENCY is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated as:

Gain Error = Positive Full Scale Error – Negative Full Scale Error

It can also be expressed as Positive Gain Error and Negative Gain Error, which are calculated as:

PGE = Positive Full Scale Error - Offset Error
NGE = Offset Error - Negative Full Scale Error

INTEGRAL NON LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is $V_{FS}/2^n$, where "V_{FS}" is the full scale input voltage and "n" is the ADC resolution in bits.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC14155 is guaranteed not to have any missing codes.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL SCALE ERROR is the difference between the actual first code transition and its ideal value of ½ LSB above negative full scale.

OFFSET ERROR is the difference between the two input voltages [(V_{IN}+) – (V_{IN}-)] required to cause a transition from code 8191 to 8192.

OUTPUT DELAY is the time delay after the falling edge of the clock before the data update is presented at the output pins.

PIPELINE DELAY (LATENCY) See CONVERSION LATENCY.

POSITIVE FULL SCALE ERROR is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well the ADC rejects a change in the power supply voltage. PSRR is the ratio of the Full-Scale output of the ADC with the supply at the minimum DC supply limit to the Full-Scale output of the ADC with the supply at the maximum DC supply limit, expressed in dB.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

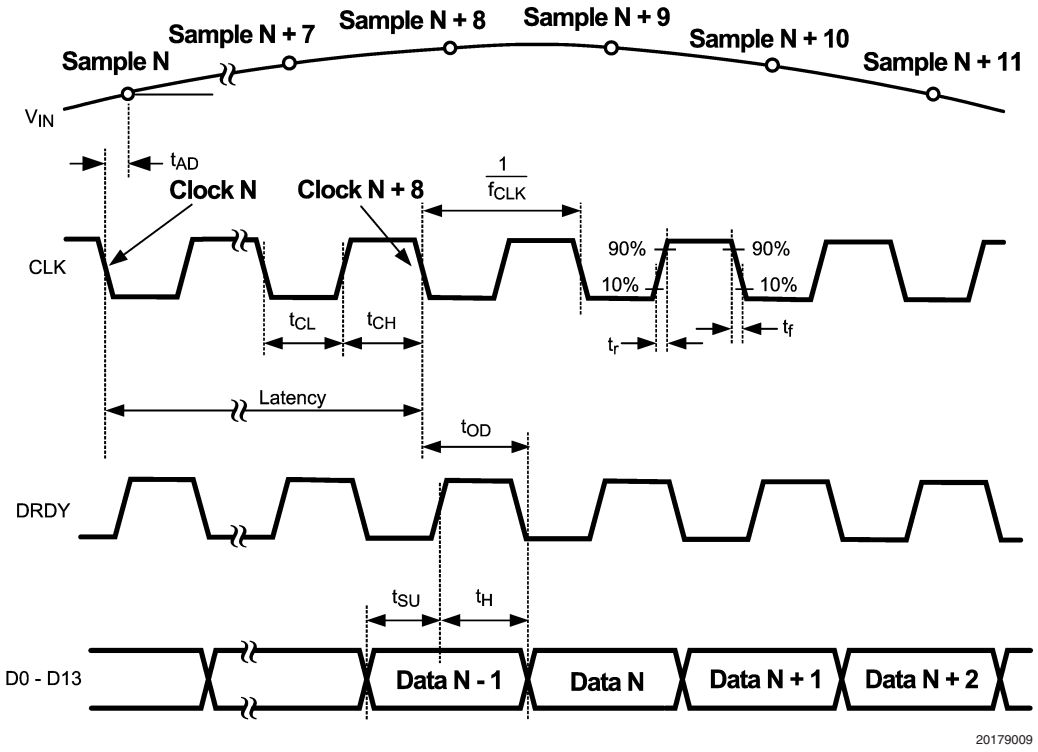
$$THD = 20 \times \log \sqrt{\frac{f_2^2 + \ldots + f_{10}^2}{f_1^2}}$$

where f_1 is the RMS power of the fundamental (output) frequency and f_2 through f_{10} are the RMS power of the first 9 harmonic frequencies in the output spectrum.

SECOND HARMONIC DISTORTION (2ND HARM) is the difference expressed in dB, between the RMS power in the input frequency at the output and the power in its 2nd harmonic level at the output.

THIRD HARMONIC DISTORTION (3RD HARM) is the difference, expressed in dB, between the RMS power in the input frequency at the output and the power in its 3rd harmonic level at the output.

Timing Diagram



Output Timing

Transfer Characteristic

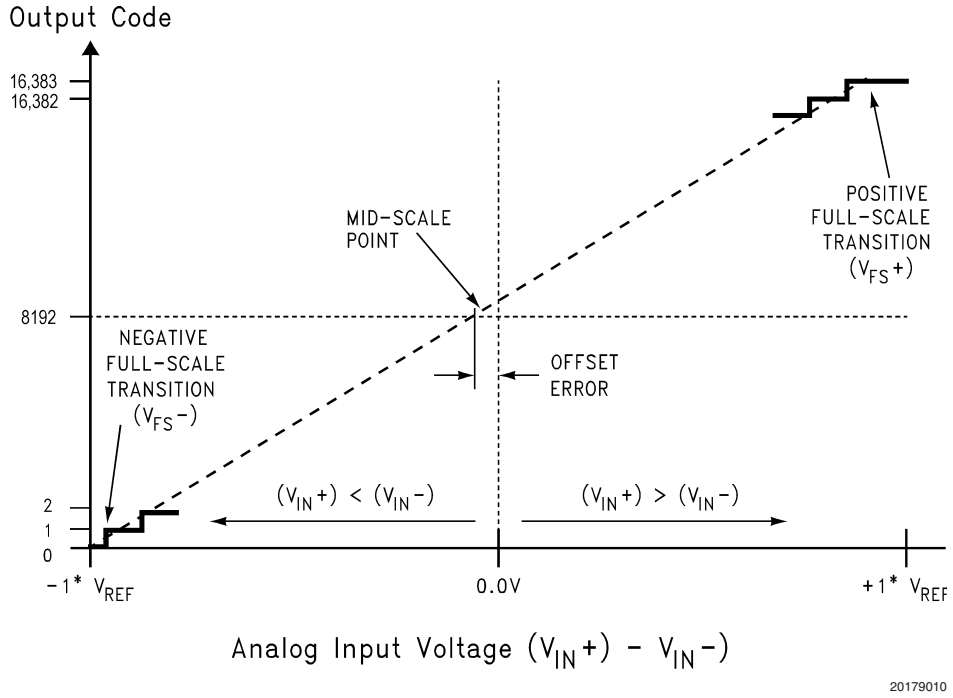
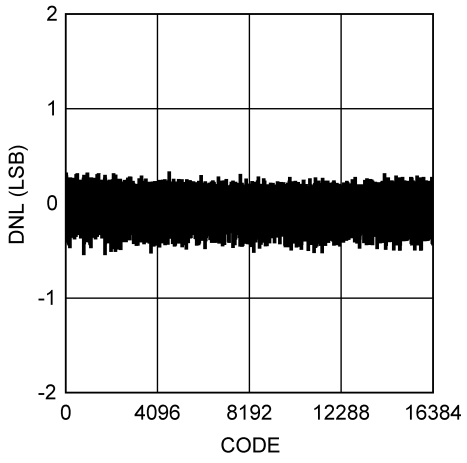


FIGURE 1. Transfer Characteristic

Typical Performance Characteristics, DNL, INL

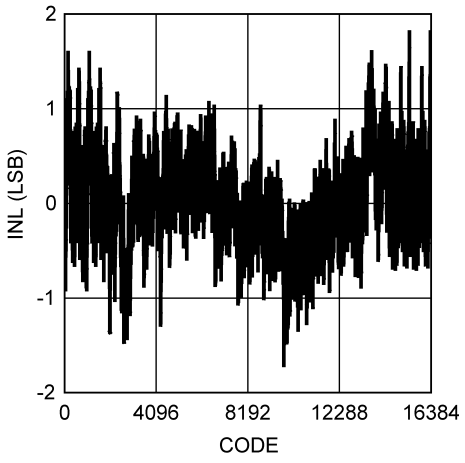
Unless otherwise specified, the following specifications apply: AGND = DGND = DRGND = 0V, $V_A = V_D = +3.3V$, $V_{DR} = +1.8V$, Internal $V_{REF} = +1.0V$, $f_{CLK} = 155$ MHz, $V_{CM} = V_{RM}$, $t_r = t_f$ = TBD ns, $C_L = 5$ pF/pin, Offset Binary Format. Typical values are for $T_A = 25^{\circ}C$. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for $T_A = 25^{\circ}C$ (Notes 6, 7, 8)

DNL



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INL

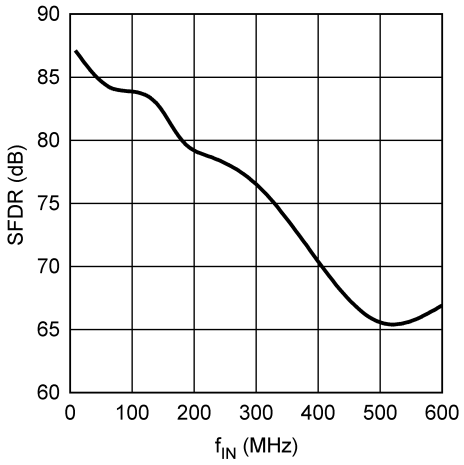


20179062

Typical Performance Characteristics, Dynamic Performance

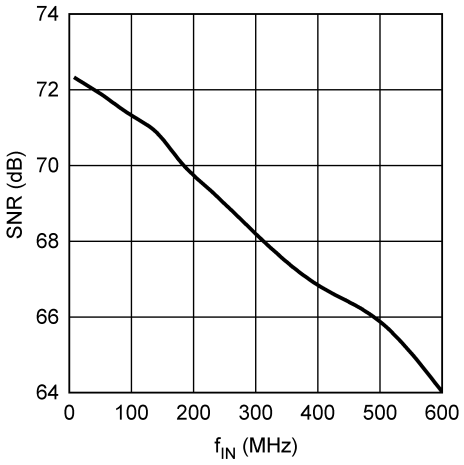
Unless otherwise specified, the following specifications apply: AGND = DGND = DRGND = 0V, $V_A = V_D = +3.3V$, $V_{DR} = +1.8V$, Internal $V_{REF} = +1.0V$, $f_{CLK} = 155$ MHz, $V_{CM} = V_{RM}$, $t_r = t_f =$ TBD ns, $C_L = 5$ pF/pin, Offset Binary Format. Typical values are for $T_A = 25^\circ C$. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$.** All other limits apply for $T_A = 25^\circ C$

SFDR vs. f_{IN}



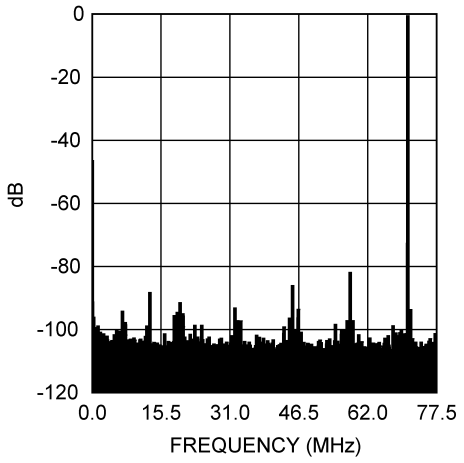
20179071

SNR vs. f_{IN}



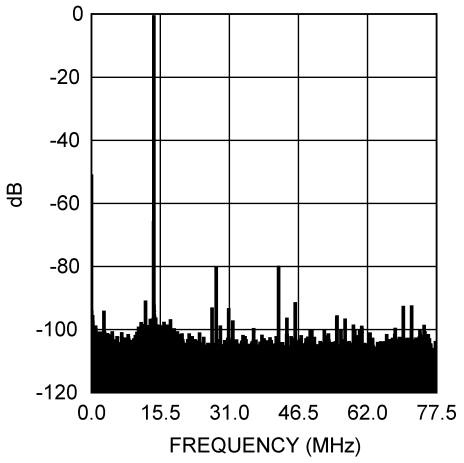
20179072

Spectral Response @ 70 MHz Input



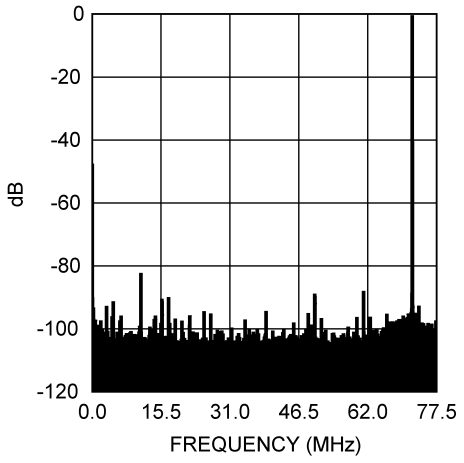
20179092

Spectral Response @ 169 MHz Input



20179093

Spectral Response @ 238 MHz Input



20179094

Functional Description

Operating on dual +3.3V and +1.8V supplies, the ADC14155 digitizes a differential analog input signal to 14 bits, using a differential pipelined architecture with error correction circuitry and an on-chip sample-and-hold circuit to ensure maximum performance.

The user has the choice of using an internal 1.0V stable reference, or using an external reference. The ADC14155 will accept an external reference between 0.8V and 1.2V (1.0V recommended) which is buffered on-chip to ease the task of driving that pin. The +1.8V output driver supply reduces power consumption and decreases the noise at the output of the converter.

The quad state function pin CLK_SEL/DF (pin 8) allows the user to choose between using a single-ended or a differential clock input and between offset binary or 2's complement output data format. The digital outputs are CMOS compatible signals that are clocked by a synchronous data ready output signal (DRDY, pin 34) at the same rate as the clock input. For the ADC14155 the clock frequency can be between 5 MSPS and 155 MSPS (typical) with fully specified performance at 155 MSPS. The analog input is acquired at the falling edge of the clock and the digital data for a given sample is output on the falling edge of the DRDY signal and is delayed by the pipeline for 8 clock cycles. The data should be captured on the rising edge of the DRDY signal.

Power-down is selectable using the PD pin (pin 7). A logic high on the PD pin disables everything except the voltage reference circuitry and reduces the converter power consumption to 5 mW with no clock running. For normal operation, the PD pin should be connected to the analog ground (AGND). A duty cycle stabilizer maintains performance over a wide range of clock duty cycles.

Applications Information

1.0 OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC14155:

$3.0V \le V_A \le 3.6V$

$V_D = V_A$

$V_{DR} = 1.8V$

$5\ MHz \le f_{CLK} \le 155\ MHz$

1.0V internal reference

$0.9V \le V_{REF} \le 1.1V$ (for an external reference)

$V_{CM} = 1.5V$ (from V_{RM})

2.0 ANALOG INPUTS

2.1 Signal Inputs

2.1.1 Differential Analog Input Pins

The ADC14155 has one pair of analog signal input pins, $V_{IN}+$ and $V_{IN}-$, which form a differential input pair. The input signal, V_{IN}, is defined as

$$V_{IN} = (V_{IN}+) - (V_{IN}-)$$

Figure 2 shows the expected input signal range. Note that the common mode input voltage, V_{CM}, should be 1.5V. Using V_{RM} (pin 45) for V_{CM} will ensure the proper input common mode level for the analog input signal. The peaks of the individual input signals should each never exceed 2.6V. Each analog input pin of the differential pair should have a peak-to-peak voltage equal to the reference voltage, V_{REF}, be 180˚ out of phase with each other and be centered around V_{CM}.The peak-to-peak voltage swing at each analog input pin should not exceed the value of the reference voltage or the output data will be clipped.

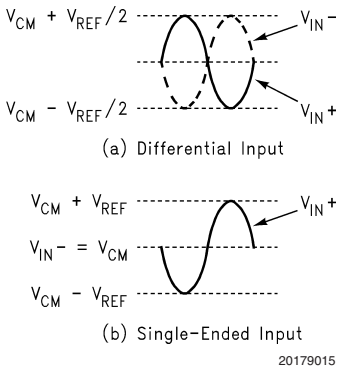


FIGURE 2. Expected Input Signal Range

For single frequency sine waves the full scale error in LSB can be described as approximately

$$E_{FS} = 16384\ (\ 1 - \sin(90^\circ + dev))$$

Where dev is the angular difference in degrees between the two signals having a 180˚ relative phase relationship to each other (see *Figure 3*). For single frequency inputs, angular errors result in a reduction of the effective full scale input. For complex waveforms, however, angular errors will result in distortion.

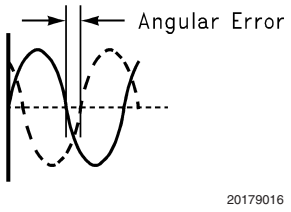


FIGURE 3. Angular Errors Between the Two Input Signals Will Reduce the Output Level or Cause Distortion

It is recommended to drive the analog inputs with a source impedance less than 100Ω. Matching the source impedance for the differential inputs will improve even ordered harmonic performance (particularly second harmonic).

Table 1 indicates the input to output relationship of the ADC14155.

Applications Information (Continued)

TABLE 1. Input to Output Relationship

V_{IN}^+	V_{IN}^-	Binary Output	2's Complement Output	
$V_{CM} - V_{REF}/2$	$V_{CM} + V_{REF}/2$	00 0000 0000 0000	10 0000 0000 0000	Negative Full-Scale
$V_{CM} - V_{REF}/4$	$V_{CM} + V_{REF}/4$	01 0000 0000 0000	11 0000 0000 0000	
V_{CM}	V_{CM}	10 0000 0000 0000	00 0000 0000 0000	Mid-Scale
$V_{CM} + V_{REF}/4$	$V_{CM} - V_{REF}/4$	11 0000 0000 0000	01 0000 0000 0000	
$V_{CM} + V_{REF}/2$	$V_{CM} - V_{REF}/2$	11 1111 1111 1111	01 1111 1111 1111	Positive Full-Scale

2.1.2 Driving the Analog Inputs

The V_{IN}+ and the V_{IN}– inputs of the ADC14155 have an internal sample-and-hold circuit which consists of an analog switch followed by a switched-capacitor amplifier. The analog inputs are connected to the sampling capacitors through NMOS switches, and each analog input has parasitic capacitances associated with it.

When the clock is high, the converter is in the sample phase. The analog inputs are connected to the sampling capacitor through the NMOS switches, which causes the capacitance at the analog input pins to appear as the pin capacitance plus the internal sample and hold circuit capacitance (approximately 9 pF). While the clock level remains high, the sampling capacitor will track the changing analog input voltage. When the clock transitions from high to low, the converter enters the hold phase, during which the analog inputs are disconnected from the sampling capacitor. The last voltage that appeared at the analog input before the clock transition will be held on the sampling capacitor and will be sent to the ADC core. The capacitance seen at the analog input during the hold phase appears as the sum of the pin capacitance and the parasitic capacitances associated with the sample and hold circuit of each analog input (approximately 6 pF). Once the clock signal transitions from low to high, the analog inputs will be reconnected to the sampling capacitor to capture the next sample. Usually, there will be a difference between the held voltage on the sampling capacitor and the new voltage at the analog input. This will cause a charging glitch that is proportional to the voltage difference between the two samples to appear at the analog input pin. The input circuitry must be fast enough to allow the sampling capacitor to fully charge before the clock signal goes high again, as incomplete settling can degrade the SFDR performance.

A single-ended to differential conversion circuit is shown in *Figure 4*. A transformer is preferred for high frequency input signals. Terminating the transformer on the secondary side provides two advantages. First, it presents a real broadband impedance to the ADC inputs and second, it provides a common path for the charging glitches from each side of the differential sample-and-hold circuit.

One short-coming of using a transformer to achieve the single-ended to differential conversion is that most RF transformers have poor low frequency performance. A differential amplifier can be used to drive the analog inputs for low frequency applications. The amplifier must be fast enough to settle from the charging glitches on the analog input resulting from the sample-and-hold operation before the clock goes high and the sample is passed to the ADC core.

The SFDR performance of the converter depends on the external signal conditioning circuity used, as this affects how quickly the sample-and-hold charging glitch will settle. An external resistor and capacitor network as shown in *Figure 4* should be used to isolate the charging glitches at the ADC input from the external driving circuit and to filter the wideband noise at the converter input. These components should be placed close to the ADC inputs because the analog input of the ADC is the most sensitive part of the system, and this is the last opportunity to filter that input. For Nyquist applications the RC pole should be at the ADC sample rate. The ADC input capacitance in the sample mode should be considered when setting the RC pole. For wideband undersampling applications, the RC pole should be set at about 1.5 to 2 times the maximum input frequency to maintain a linear delay response.

2.1.3 Input Common Mode Voltage

The input common mode voltage, V_{CM}, should be in the range of 1.4V to 1.6V and be a value such that the peak excursions of the analog signal do not go more negative than ground or more positive than 2.6V. It is recommended to use V_{RM} (pin 45) as the input common mode voltage.

2.2 Reference Pins

The ADC14155 is designed to operate with an internal 1.0V reference, or an external 1.0V reference, but performs well with external reference voltages in the range of 0.8V to 1.2V. The internal 1.0 Volt reference is the default condition when no external reference input is applied to the V_{REF} pin. If a voltage in the range of 0.8V to 1.2V is applied to the V_{REF} pin, then that voltage is used for the reference. The V_{REF} pin should always be bypassed to ground with a 0.1 µF capacitor close to the reference input pin. Lower reference voltages will decrease the signal-to-noise ratio (SNR) of the ADC14155. Increasing the reference voltage (and the input signal swing) beyond 1.2V may degrade THD for a full-scale input, especially at higher input frequencies.

It is important that all grounds associated with the reference voltage and the analog input signal make connection to the ground plane at a single, quiet point to minimize the effects of noise currents in the ground path.

The Reference Bypass Pins (V_{RP}, V_{RM}, and V_{RN}) are made available for bypass purposes. All these pins should each be bypassed to ground with a 0.1 µF capacitor. A 0.1 µF and a 10 µF capacitor should be placed between the V_{RP} and V_{RN} pins, as shown in *Figure 4*. This configuration is necessary to avoid reference oscillation, which could result in reduced SFDR and/or SNR. V_{RM} may be loaded to 1mA for use as a temperature stable 1.5V reference. The remaining pins should not be loaded.

Smaller capacitor values than those specified will allow faster recovery from the power down mode, but may result in degraded noise performance. Loading any of these pins, other than V_{RM}, may result in performance degradation.

The nominal voltages for the reference bypass pins are as follows:

V_{RM} = 1.5 V

Applications Information (Continued)

$V_{RP} = V_{RM} + V_{REF} / 2$

$V_{RN} = V_{RM} - V_{REF} / 2$

3.0 DIGITAL INPUTS

Digital CMOS compatible inputs consist of CLK+, CLK–, PD/DCS and CLK_SEL/DF.

3.1 Clock Inputs

The CLK+ and CLK– signals control the timing of the sampling process. The CLK_SEL/DF pin (pin 8) allows the user to configure the ADC for either differential or single-ended clock mode (see Section 3.3). The differential mode is recommended to obtain the best distortion performance. In differential clock mode, the two clock signals should be exactly 180˚ out of phase from each other and of the same amplitude. If a slight degradation in distortion performance is acceptable, the single-ended clock mode may be used. In this configuration, the clock signal should be routed to the CLK+ input and the CLK– input should be tied to AGND in combination with the correct setting from *Table 3*.

To achieve the optimum noise performance, the clock inputs should be driven with a stable, low jitter clock signal in the range indicated in the Electrical Table with rise and fall times of TBD ns or less. The trace carrying the clock signal should be as short as possible and should not cross any other signal line, analog or digital, not even at 90˚. *Figure 4* shows the recommended differential clock input circuit.

The clock signal also drives an internal state machine. If the clock is interrupted, or its frequency is too low, the charge on the internal capacitors can dissipate to the point where the accuracy of the output data will degrade. This is what limits the minimum sample rate.

The clock line should be terminated at its source in the characteristic impedance of that line. Take care to maintain a constant clock line impedance throughout the length of the line. Refer to Application Note AN-905 for information on setting characteristic impedance.

It is highly desirable that the the source driving the ADC clock pins only drive that pin. However, if that source is used to drive other things, each driven pin should be AC terminated with a series RC to ground, such that the resistor value is equal to the characteristic impedance of the clock line and the capacitor value is

$$C \geq \frac{4 \times t_{PD} \times L}{Z_o}$$

where t_{PD} is the signal propagation rate down the clock line, "L" is the line length and Z_O is the characteristic impedance of the clock line. This termination should be as close as possible to the ADC clock pin but beyond it as seen from the clock source. Typical t_{PD} is about 150 ps/inch (60 ps/cm) on FR-4 board material. The units of "L" and t_{PD} should be the same (inches or centimeters).

The duty cycle of the clock signal can affect the performance of the A/D Converter. Because achieving a precise duty cycle is difficult, the ADC14155 has a Duty Cycle Stabilizer. It is designed to maintain performance over a clock duty cycle range of 30% to 70%.

3.2 Power-Down (PD)

Power-down can be enabled through this two-state input pin. *Table 2* shows how to power-down the ADC14155.

TABLE 2. Power Down Selection Table

PD Input Voltage	Power State
V_A	Power-down
AGND	On

The power-down mode allows the user to conserve power when the converter is not being used. In the power-down state all bias currents of the analog circuitry, excluding the reference are shut down which reduces the power consumption to 5 mW with no clock running. The output data pins are undefined and the data in the pipeline is corrupted while in the power-down mode.

The Power-down Mode Exit Cycle time is determined by the value of the capacitors on the V_{RP}, V_{RM} and V_{RN} reference bypass pins (pins 43, 44 and 45) and is about 3 ms with the recommended component values. These capacitors lose their charge in the power-down mode and must be recharged by on-chip circuitry before conversions can be accurate. Smaller capacitor values allow slightly faster recovery from the power down mode, but can result in a reduction in SNR, SINAD and ENOB performance.

3.3 Clock Mode Select/Data Format (CLK_SEL/DF)

Single-ended versus differential clock mode and output data format are selectable using this quad-state function pin. *Table 3* shows how to select between the clock modes and the output data formats.

TABLE 3. Clock Mode and Data Format Selection Table

CLK_SEL/DF Input Voltage	Clock Mode	Output Data Format
V_A	Differential	2's Complement
(2/3) * V_A	Differential	Offset Binary
(1/3) * V_A	Single-Ended	2's Complement
AGND	Single-Ended	Offset Binary

4.0 DIGITAL OUTPUTS

Digital outputs consist of the 1.8V CMOS signals D0-D13, DRDY and OVR.

The ADC14155 has 16 CMOS compatible data output pins: 14 data output bits corresponding to the converted input value, a DRDY signal that should be used to capture the output data and an over-range indicator (OVR) which is set high when the sample amplitude exceeds the 14-bit conversion range. Valid data is present at these outputs while the PD pins is low.

Data should be captured with the DRDY signal and the rising edge of the DRDY signal should be used to latch the data. Depending on the setup and hold time requirements of the receiving circuit (ASIC), either the rising edge or the falling edge of the DRDY signal can be used to latch the data. Generally, rising-edge capture would maximize setup time with minimal hold time; while falling-edge-capture would maximize hold time with minimal setup time. However, actual timing for the falling-edge case depends greatly on the CLK frequency and both cases also depend on the delays inside the ASIC. Refer to the AC Electrical Characterisitics table.

Be very careful when driving a high capacitance bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through V_{DR} and DRGND. These large charging current spikes can cause on-chip ground noise and couple into the

Applications Information (Continued)

analog circuitry, degrading dynamic performance. Adequate bypassing, limiting output capacitance and careful attention to the ground plane will reduce this problem. Additionally, bus capacitance beyond the specified 5 pF/pin will cause t_{OD} to increase, reducing the setup and hold time of the ADC output data. The result could be an apparent reduction in dynamic performance.

To minimize noise due to output switching, minimize the load currents at the digital outputs. This can be done by connecting a 1.8V to 3.3V level translator such as the SN74AVCA164245 between the ADC outputs and any other circuitry. Only one load should be connected to each output pin. Additionally, inserting series resistors of about 22Ω at the digital outputs, close to the ADC pins, will isolate the outputs from trace and other circuit capacitances and limit the output currents, which could otherwise result in performance degradation. See *Figure 4*.

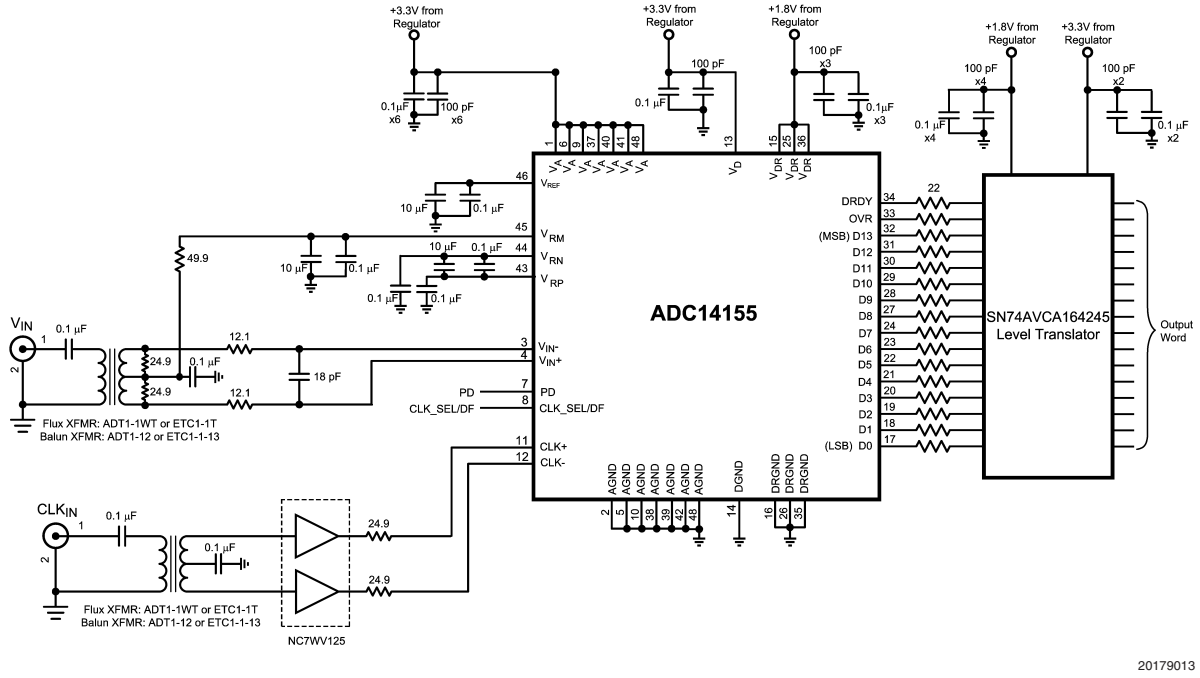


FIGURE 4. Application Circuit using Transformer Drive Circuit

5.0 POWER SUPPLY CONSIDERATIONS

The power supply pins should be bypassed with a 0.1 µF capacitor and with a 100 pF ceramic chip capacitor close to each power pin. Leadless chip capacitors are preferred because they have low series inductance.

As is the case with all high-speed converters, the ADC14155 is sensitive to power supply noise. Accordingly, the noise on the analog supply pin should be kept below 100 mV_{P-P}.

No pin should ever have a voltage on it that is in excess of the supply voltages, not even on a transient basis. Be especially careful of this during power turn on and turn off.

The V_{DR} pin provides power for the output drivers and may be operated from a supply in the range of 1.6V to 2.0V. This enables lower power operation, reduces the noise coupling effects from the digital outputs to the analog circuitry and simplifies interfacing to lower voltage devices and systems. Note, however, that t_{OD} increases with reduced V_{DR}. Also note that a level translator may be required.

6.0 LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. Maintaining separate analog and digital areas of the board, with the ADC14155 between these areas, is required to achieve specified performance.

The ground return for the data outputs (DRGND) carries the ground current for the output drivers. The output current can exhibit high transients that could add noise to the conversion process. To prevent this from happening, the DRGND pins should NOT be connected to system ground in close proximity to any of the ADC14155's other ground pins.

Capacitive coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry, and to keep the clock line as short as possible.

The effects of the noise generated from the ADC output switching can be minimized through the use of 22Ω resistors in series with each data output line. Locate these resistors as close to the ADC output pins as possible.

Since digital switching transients are composed largely of high frequency components, total ground plane copper

Applications Information (Continued)

weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane area.

Generally, analog and digital lines should cross each other at 90˚ to avoid crosstalk. To maximize accuracy in high speed, high resolution systems, however, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. Even the generally accepted 90˚ crossing should be avoided with the clock line as even a little coupling can cause problems at high frequencies. This is because other lines can introduce jitter into the clock line, which can lead to degradation of SNR. Also, the high speed clock can introduce noise into the analog chain.

Best performance at high frequencies and at high resolution is obtained with a straight signal path. That is, the signal path through all components should form a straight line wherever possible.

Be especially careful with the layout of inductors and transformers. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors and transformers should *not* be placed side by side, even with just a small part of their bodies beside each other. For instance, place transformers for the analog input and the clock input at 90˚ to one another to avoid magnetic coupling.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane.

All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed in the analog area of the board. All digital circuitry and dynamic I/O lines should be placed in the digital area of the board. The ADC14155 should be between these two areas. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the ground plane at a single, quiet point. All ground connections should have a low inductance path to ground.

7.0 DYNAMIC PERFORMANCE

To achieve the best dynamic performance, the clock source driving the CLK input must have a sharp transition region and be free of jitter. Isolate the ADC clock from any digital circuitry with buffers, as with the clock tree shown in *Figure 5* . The gates used in the clock tree must be capable of operating at frequencies much higher than those used if added jitter is to be prevented. Best performance will be obtained with a differential clock input drive, compared with a single-ended drive.

As mentioned in Section 6.0, it is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal, which can lead to reduced SNR performance, and the clock can introduce noise into other lines. Even lines with 90˚ crossings have capacitive coupling, so try to avoid even these 90˚ crossings of the clock line.

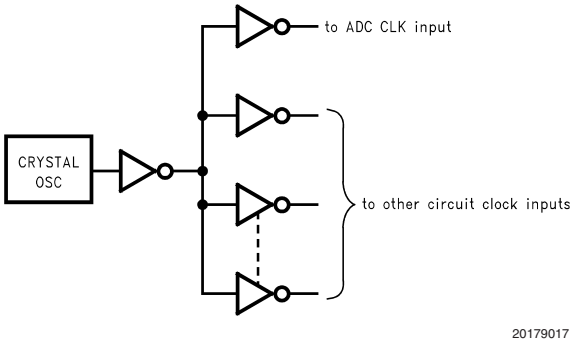
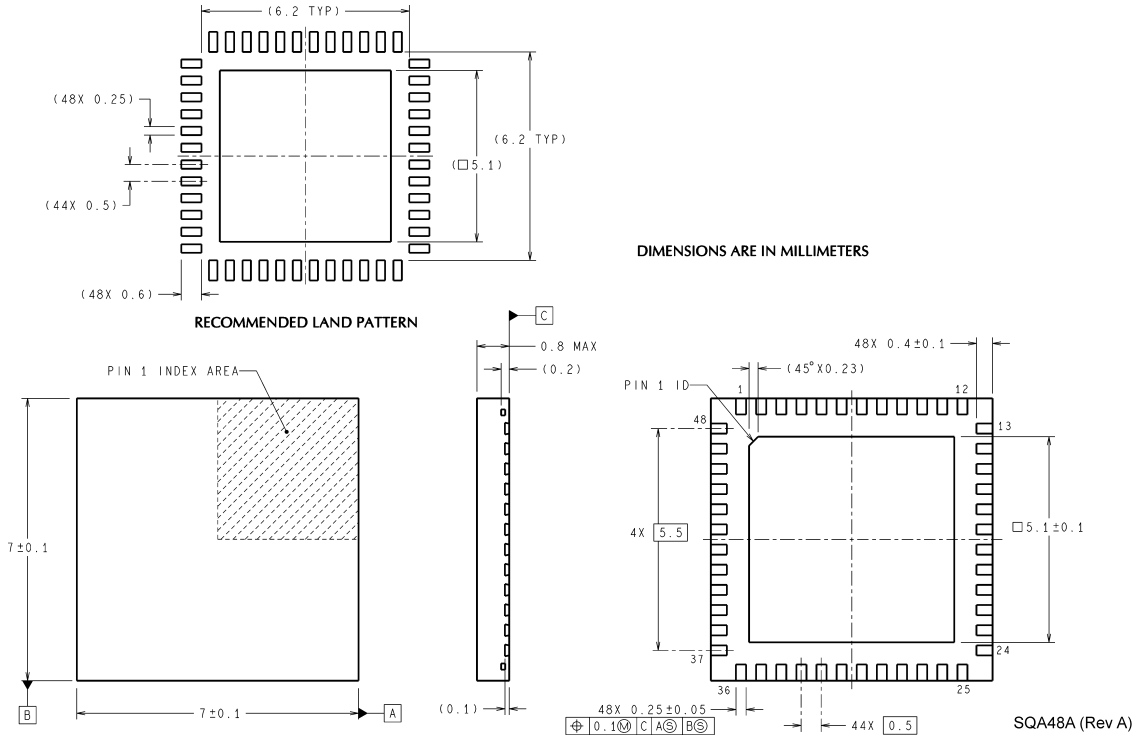


FIGURE 5. Isolating the ADC Clock from other Circuitry with a Clock Tree

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead LLP Package
Ordering Number ADC14155CISQ
NS Package Number SQA48A

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