Description

The ICS501 LOCO™ is the most cost effective way to generate a high-quality, high-frequency clock output from a lower frequency crystal or clock input. The name LOCO stands for Low Cost Oscillator, as it is designed to replace crystal oscillators in most electronic systems. Using Phase-Locked Loop (PLL) techniques, the device uses a standard fundamental mode, inexpensive crystal to produce output clocks up to 160 MHz.

Stored in the chip's ROM is the ability to generate nine different multiplication factors, allowing one chip to output many common frequencies (see table on page 2).

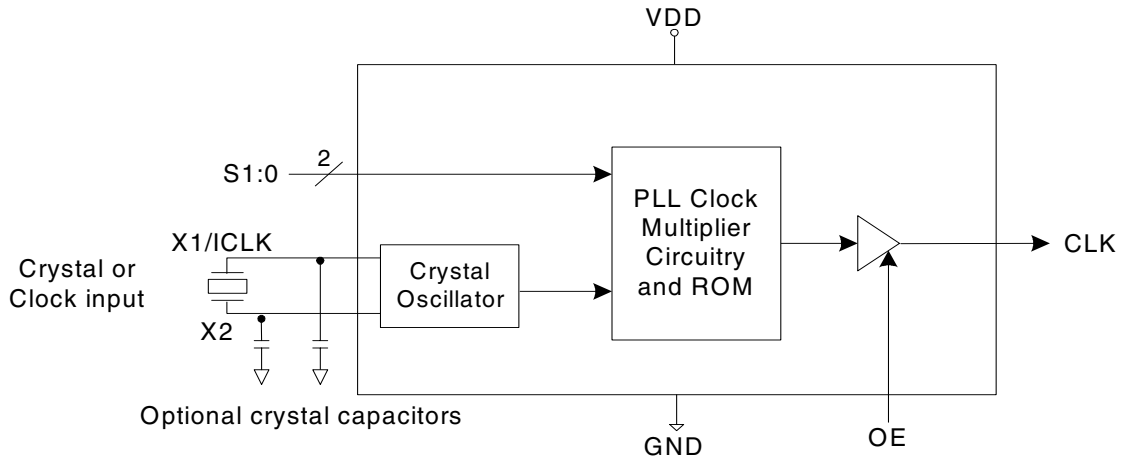
The device also has an output enable pin which tri-states the clock output when the OE pin is taken low.

This product is intended for clock generation. It has low output jitter (variation in the output period), but input to output skew and jitter are not defined or guaranteed. For applications which require defined input to output skew, use the ICS570B.

Features

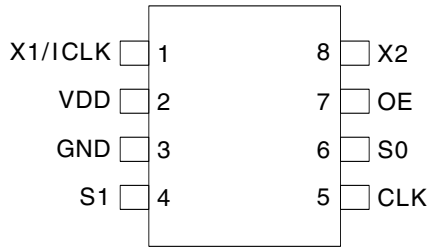
- Packaged as 8-pin SOIC or die
- Available in Pb (lead) free package
- ICS' lowest cost PLL clock
- Zero ppm multiplication error
- Input crystal frequency of 5 - 27 MHz
- Input clock frequency of 2 - 50 MHz
- Output clock frequencies up to 160 MHz
- Extremely low jitter of 25 ps (one sigma)
- Compatible with all popular CPUs
- Duty cycle of 45/55 up to 160 MHz
- Nine selectable frequencies
- Operating voltage of 3.3V or 5.5V
- Tri-state output for board level testing
- 25mA drive capability at TTL levels
- Ideal for oscillator replacement
- Industrial temperature version available
- Advanced, low-power CMOS process

Block Diagram



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Pin Assignment



8 Pin (150 mil) SOIC

Clock Output Table

S1	S0	CLK	Minimum Input
0	0	4X input	per page 4
0	M	5.3125X input	20 MHz
0	1	5X input	per page 4
M	0	6.25X input	4 MHz
M	M	2X input	per page 4
M	1	3.125X input	8 MHz
1	0	6X input	per page 4
1	M	3X input	per page 4
1	1	8X input	per page 4

0 = connect directly to ground
1 = connect directly to VDD
M = leave unconnected (floating)

Common Output Frequency Examples (MHz)

Output	**20**	**24**	**30**	**32**	**33.33**	**37.5**	**40**	**48**	**50**	**60**	**62.5**
Input	10	12	10	16	16.66	12	10	12	16.66	10	20
Selection (S1, S0)	M, M	M, M	1, M	M, M	M, M	M, 1	0, 0	0, 0	1, M	1, 0	M, 1
Output	**64**	**66.66**	**72**	**75**	**80**	**83.33**	**90**	**100**	**106.25**	**120**	**125**
Input	16	16.66	12	12	10	16.66	15	20	20	15	20
Selection (S1, S0)	0, 0	0, 0	1, 0	M, 0	1, 1	0, 1	1, 0	0, 1	0, M	1, 1	M, 0

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	XI/ICLK	Input	Crystal connection or clock input.
2	VDD	Power	Connect to +3.3 V or +5 V.
3	GND	Power	Connect to ground.
4	S1	Tri-level Iinput	Select 1 for output clock. Connect to GND or VDD or float.
5	CLK	Output	Clock output per table above.
6	S0	Tri-level Input	Select 0 for output clock. Connect to GND or VDD or float.
7	OE	Input	Output enable. Tri-states CLK output when low. Internal pull-up.
8	X2	Output	Crystal connection. Leave unconnected for clock input.

External Components

Decoupling Capacitor

As with any high-performance mixed-signal IC, the ICS501 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between VDD and the GND. It must be connected close to the ICS501 to minimize lead inductance. No external power supply filtering is required for the ICS501.

Series Termination Resistor

A 33Ω terminating resistor can be used next to the CLK pin for trace lengths over one inch.

Crystal Load Capacitors

The total on-chip capacitance is approximately 12 pF. A parallel resonant, fundamental mode crystal should be used. The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors, if needed, must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal (C_L -12 pF)*2. In this equation, C_L= crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 8 pF [(16-12) x 2] = 8.

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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS501. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	-40 to +85°C
Storage Temperature	-65 to +150°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+5.5	V

DC Electrical Characteristics

VDD=5.0 V ±5% , Ambient temperature 0 to +70°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Input High Voltage, ICLK only	V_{IH}	ICLK (pin 1)	(VDD/2)+1			V
Input Low Voltage, ICLK only	V_{IL}	ICLK (pin 1)			(VDD/2)-1	V
Input High Voltage	V_{IH}	OE (pin 7)	2.0			V
Input Low Voltage	V_{IL}	OE (pin 7)			0.8	V
Input High Voltage	V_{IH}	S0, S1	VDD-0.5			V
Input Low Voltage	V_{IL}	S0, S1			0.5	V
Output High Voltage	V_{OH}	I_{OH} = -25 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 25 mA			0.4	V
IDD Operating Supply Current, 20		No load, 100M		20		mA
Short Circuit Current		CLK output		±70		mA

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
On-Chip Pull-up Resistor		Pin 7		270		kΩ
Input Capacitance, S1, S0, and OE		Pins 4, 6, 7		4		pF
Nominal Output Impedance				20		Ω

AC Electrical Characteristics

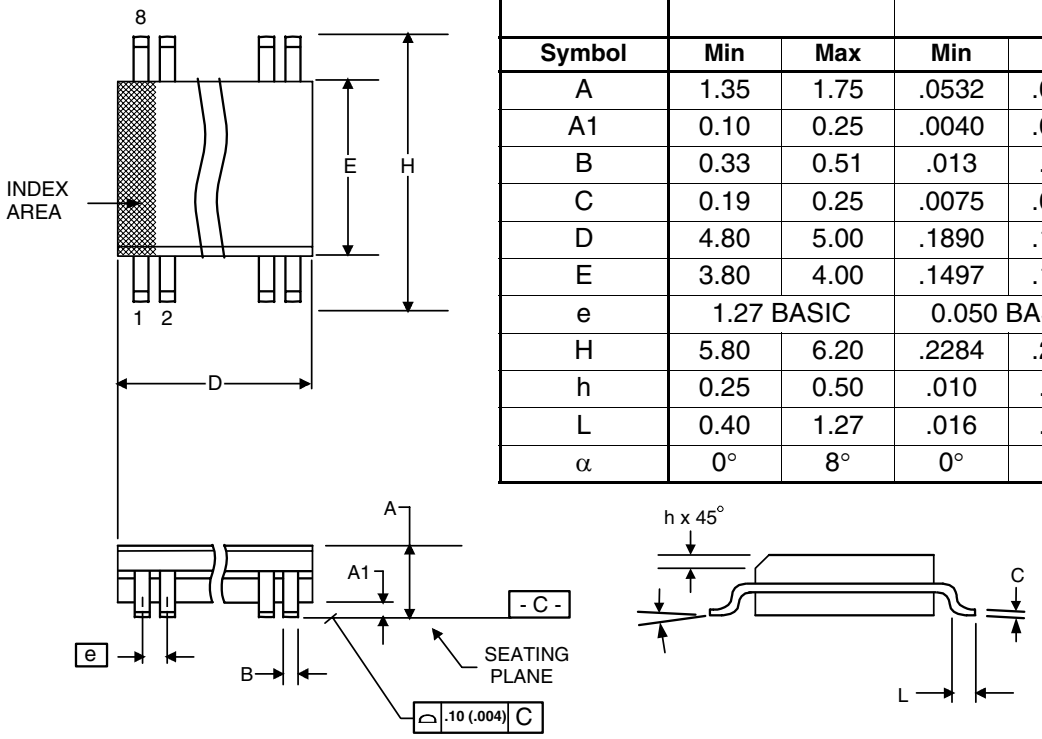
VDD = 5.0 V ±5%, Ambient Temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency, crystal input	F_{IN}		5		27	MHz
Input Frequency, clock input	F_{IN}		2		50	MHz
Output Frequency, VDD = 4.5 to 5.5 V	F_{OUT}	0°C to +70°C	13		160	MHz
		-40°C to +85°C	13		140	MHz
Output Frequency, VDD = 3.0 to 3.6 V	F_{OUT}	0°C to +70°C	13		100	MHz
		-40°C to +85°C	13		90	MHz
Output Clock Rise Time	t_{OR}	0.8 to 2.0 V, Note 1		1		ns
Output Clock Fall Time	t_{OF}	2.0 to 8.0 V, Note 1		1		ns
Output Clock Duty Cycle	t_{OD}	1.5 V, up to 160 MHz	45	49-51	55	%
PLL Bandwidth			10			kHz
Output Enable Time, OE high to output on				50		ns
Output Disable Time, OE low to tri-state				50		ns
Absolute Clock Period Jitter	t_{ja}	Deviation from mean		±70		ps
One Sigma Clock Period Jitter	t_{js}			25		ps

Note 1: Measured with 15 pF load.

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
ICS501M	ICS501M	Tubes	8-pin SOIC	0 to +70° C
ICS501MT	ICS501M	Tape and Reel	8-pin SOIC	0 to +70° C
ICS501MI	ICS501I	Tubes	8-pin SOIC	-40 to +85° C
ICS501MIT	ICS501I	Tape and Reel	8-pin SOIC	-40 to +85° C
ICS501MLF	501MLF	Tubes	8-pin SOIC	0 to +70° C
ICS501MLFT	501MLF	Tape and Reel	8-pin SOIC	0 to +70° C
ICS501-DWF	-	Die on uncut, probed wafers		0 to +70° C
ICS501-DPK	-	Tested die in waffle pack		0 to +70° C

"LF" denotes Pb (lead) free package.

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