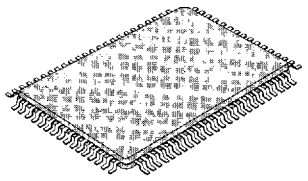
DOT MATRIX LCD CONTROLLER & DRIVER

The KS0066 is a dot matrix LCD driver & controller LSI which is fabricated by low power CMOS technology

80 QFP



FUNCTION

- Character type dot matrix LCD driver & controller
- Internal driver: 16 common and 40 segment signal output.
- Display character format; 5 × 7 dots + cursor, 5 × 10 dots + cursor
- Easy interface with a 4-bit or 8-bit MPU
- Display character pattern: refer to table 2.
  5 × 7 dots format: 192 kinds, 5 × 10 dots format: 32kinds
- The special character pattern can be programmable by Character Generator RAM directly.
- A customer character pattern can be programmable by mask option. (KS0066F00, F03, F04, F05, F06, F59; Standard type)

F00	English	Numberal	Japanese
F03	English	Numberal	French
F04	English	Numberal	Japanese
F05	English	Numberal	European
F06	English	Numberal	
F59	English	Numberal	

- Automatic power on reset function.
- It can drive a maximum 80 characters by using the KS0065 or KS0063 externally.
- It is possible to read both Character Generator and Display Data RAM from MPU.

FEATURES

- Internal Memory
  - Character Generator ROM: 8320bits
  - Character Generator RAM: 512 bits
  - Display Data RAM: 80 × 8bits for 80 digits.
- Power Supply Voltage; +5V ±10%
- Supply voltage for display: −5V
- CMOS process
- 1/8 duty, 1/11 duty or 1/16 duty: selectable
  (1/8 duty; 5 × 7 dots format 1 line, 1/11 duty; 5 × 10 dots format 1 line, 1/16 duty: 5 × 7 dots format 2 line)
- 80 QFP or bare chip available.

BLOCK DIAGRAM

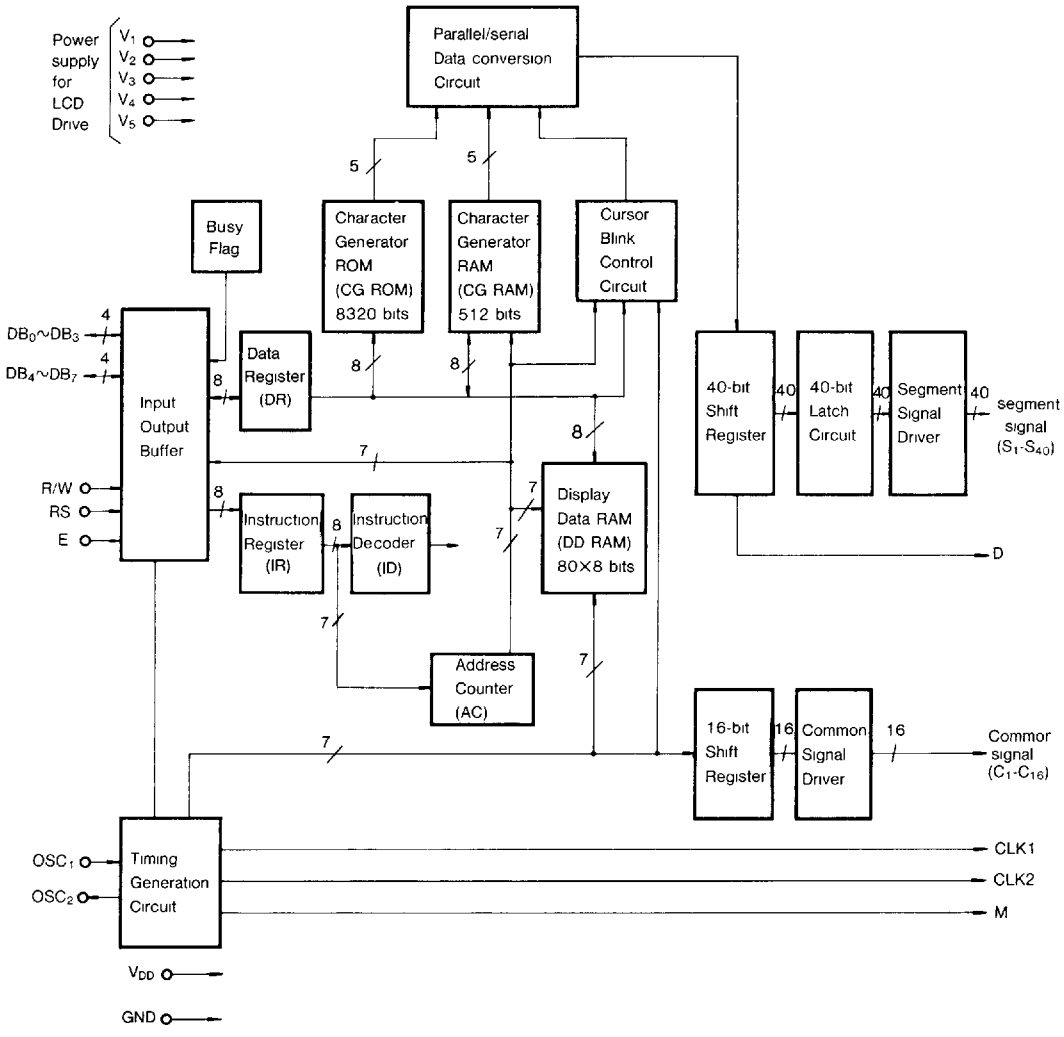


Fig 1 KS0066 functional block diagram

PIN CONFIGURATION

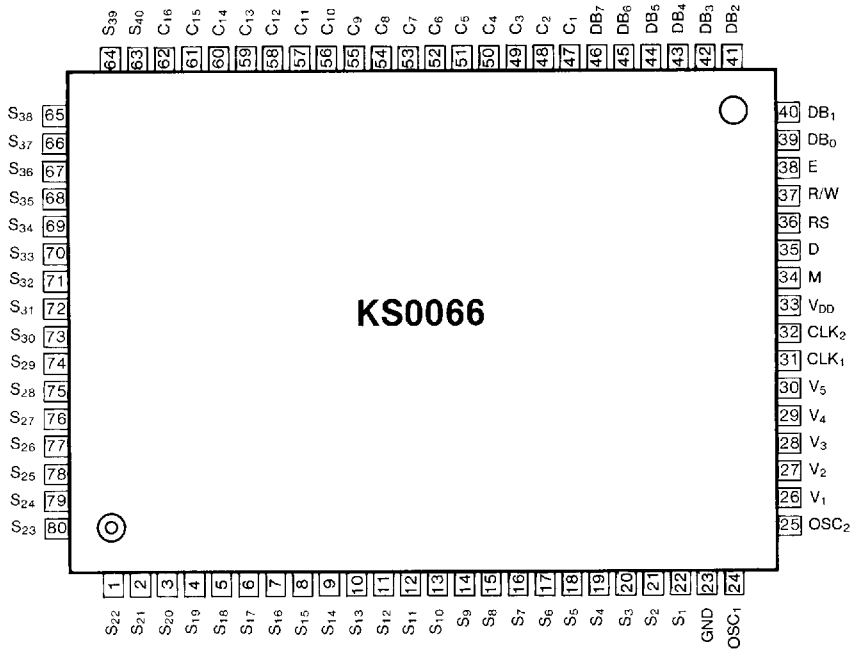


Fig 2 80 QFP Top View

PIN DESCRIPTION

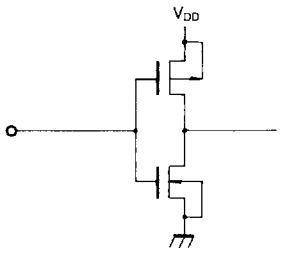
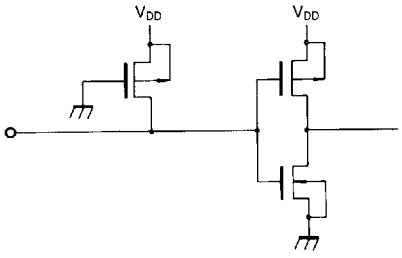
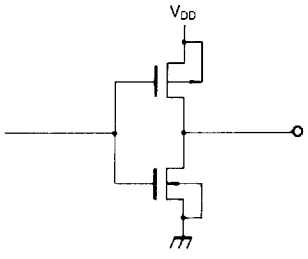
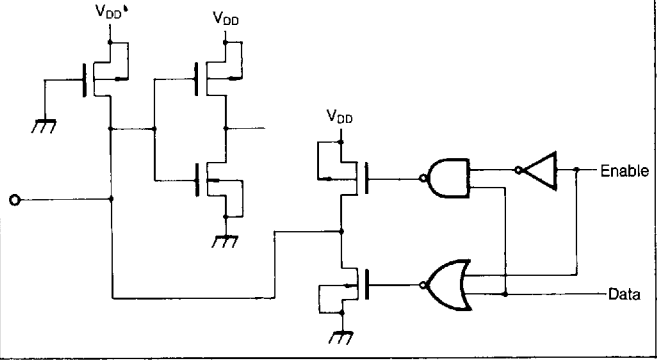
Pin (No)	Input/output	Name	Description	Interface
V_{DD}(33)		Power Supply	for logical circuit (+5V±10%)	Power Supply
V_{SS}(GND) (23)			0V (GND)	
V_1-V_5(26-30)			Bias voltage level for LCD driving	
S_1-S_{40} (1-22, 63-80)	Output	Segment output	Segment signal output for LCD driving	LCD
C_1-C_{16} (47-62)	Output	Common output	Common signal output for LCD driving	LCD
OSC_1, OSC_2 (24) (25)	Input (OSC1) Output (OSC2)	Oscillator	Both pin connected to Rf resistor or ceramic resonator for internal oscillator circuit In case of external frequency use only, the frequency is input to OSC1 terminal	resistor or ceramic resonator
CLK1 (31)	Output	Data latch Clock	Clock output terminal for the serially transfered data to be latched to the driver	KS0065
CLK2 (32)		Data shift clock	Clock output terminal used when D terminal data output shifts the inside of the driver	
M (34)		Alternated signal for LCD driver output	The alternating signal to convert LCD drive waveform to AC	
D (35)		Display data interface	Character pattern data, which is corresponding to each common signal, is supplied to driver serially.	
E(38)	Input	Enable	Start enable signal to read or write the data	MPU
R/W (37)		read/write	R/W signal input is used to select the read/write mode	
RS (36)		Register select	register selection input	
DB_0-DB_7 (39-46)	Input/Output	Data interface	Used for data transfer between the MPU and KS0066 These terminals are for data bus with bidirectional three-state Initial 4 bit (DB_0-DB_3) are not used during 4-bit operation (DB_7 can be used as a busy flag)	

High	Selection
Low	Non selection

High	Read mode
Low	Write mode

High	Data register (for read and write)
Low	Instruction register (for write), Busy flag, address counter (for read)

Internal logic of input/output terminal

Input/Output	Logic diagram		Applicable pin
Input	No Pull up		E
	with pull up		RS, R/W
Output			CLK1, CLK2 M D
Input Output			DB_0-DB_7

MAXIMUM ABSOLUTE LIMIT (T_a=25°C)

Characteristic	Symbol	Value	Unit
Power supply voltage	V_{DD}	−0.3∼+7.0	V
Driver supply voltage	V_{LCD}	V_{DD}−13.5∼V_{DD}+0.3	V
Input voltage	V_{IN}	−0 3 to V_{DD}+0.3	V
Power dissipation	P_d	500	mw
Operating temperature	T_{opr}	−20∼+75	°C
Storage temperature	T_{stg}	−55∼+125	°C

* Voltage greater than above may damage to the circuit ($V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$)

ELECTRICAL CHARACTERISTICS

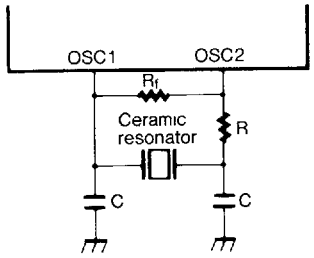
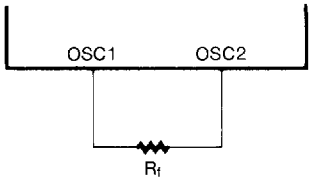
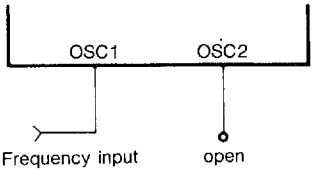
DC Characteristics (V_{DD}=+5V±10%, V_{SS}=0V, Ta=25°C)

Characteristic		Symbol	Test condition	Min	Typ	Max	Unit	Applicable Pin
Operating Voltage		V_{DD}	—	4.5	—	5.5	V	
Supply Current (*1)		I_{DD1}	Ceramic resonator fosc=250KHz	—	0.55	0.8	mA	
		I_{DD2}	Resistor oscilation external clock operation fosc=270KHz	—	0.35	0.6		
Input Voltage 1	High	V_{IH1}	—	2.2	—	V_{DD}	V	E, DB_0-DB_7, R/W, RS
	Low	V_{IL1}	—	−0.3	—	0.6		
Input voltage 2	High	V_{IH2}	—	V_{DD}−1 0	—	V_{DD}		OSC1
	Low	V_{IL2}	—	−0.2	—	1.0		
Output Voltage 1	High	V_{OHI}	I_{OH}=−0.205mA	2.4	—	—		DB_0-DB_7
	Low	V_{OLI}	I_{OL}=1.2mA	—	—	0 4		
Output Voltage 2	High	V_{OH2}	I_O=−40μA	0.9V_{DD}	—	—		CLK1, CLK2, M
	LOW	V_{OL2}	I_O=40μA	—	—	0.1V_{DD}		D
Voltage drop (*2)	COM	Vd_{COM}	I_O=±0 1mA	—	—	1		C1-C16
	SEG	Vd_{SEG}		—	—	1		S1-S40
Input leakage current		I_{IL}	V_{IN}=0 or V_{DD}	−1	—	1	μA	E
Low input current		I_{IN}	V_{DD}=5V (test pull up R)	−50	−125	−250		RS, R/W, DB_0-DB_7
External clock	frequency(*3)	f_{EC}	—	125	250	350	KHz	OSC1
	duty	duty		45	50	55	%	
	rise time	tr		—	—	0.2	μS	
	fall time	t_f		—	—	0 2	μS	
Internal clock frequency(*3)		f_{IC}	Rf=91KΩ±2%	190	270	350	kHz	OSC1, OSC2
Ceramic resonator oscillation frequency (*3)		f_{CD}		245	250	255		
LCD driving voltage (*4)		V_{LCD1}	V_{DD}-V_5 1/5 bias	4.6	—	11.0	V	V_1-V_5
		V_{LCD2}	V_{DD}-V_5 1/4 bias	3.0	—	11 0		

Note: *1) Applies to the current value flown in terminal V_{DD} when power is input as follows, V_{DD}=5V, GND=0V, V1=3 4V, V2=1 8V, V3=0 2V, V4=−1 4V and V5=−3V

*2) Applied to the voltage drop occuring from terminals V_{DD}, V1, V4 and V5 to each common terminal (C1-C16) when 0 1μA is flown in or out to and from all COM and SEG terminals, and also to voltage drop occuring from terminals V_{DD}, V2, V3 and V5 to each SEG terminal (S1-S40). When the output level is at V_{DD}, V1 or V2 level, 0.1mA is flown out, while 0 1mA flow in when the output level is at V3, V4, or V5 level. This occurs when 5V or −5V is input to V_{DD}, V1 and V3 or to V2, V4, and V5 respectively

*3) Oscillator circuit

Ceramic resonator circuit	Resistor circuit	External clock circuit
		

Rf	1MΩ±10%
C	680pF±10%
R	3.3kΩ±5%

Rf 91kΩ±2%

*4) Input the voltage listed in the table below to V_1-V_5

Power supply \ Duty / Bias	1/8, 1/11	1/16
	1/4	1/5
V_1	$V_{DD}-\frac{V_{LCD}}{4}$	$V_{DD}-\frac{V_{LCD}}{5}$
V_2	$V_{DD}-\frac{V_{LCD}}{2}$	$V_{DD}-\frac{2V_{LCD}}{5}$
V_3	$V_{DD}-\frac{V_{LCD}}{2}$	$V_{DD}-\frac{3V_{LCD}}{5}$
V_4	$V_{DD}-\frac{3V_{LCD}}{4}$	$V_{DD}-\frac{4V_{LCD}}{5}$
V_5	$V_{DD}-V_{LCD}$	$V_{DD}-V_{LCD}$

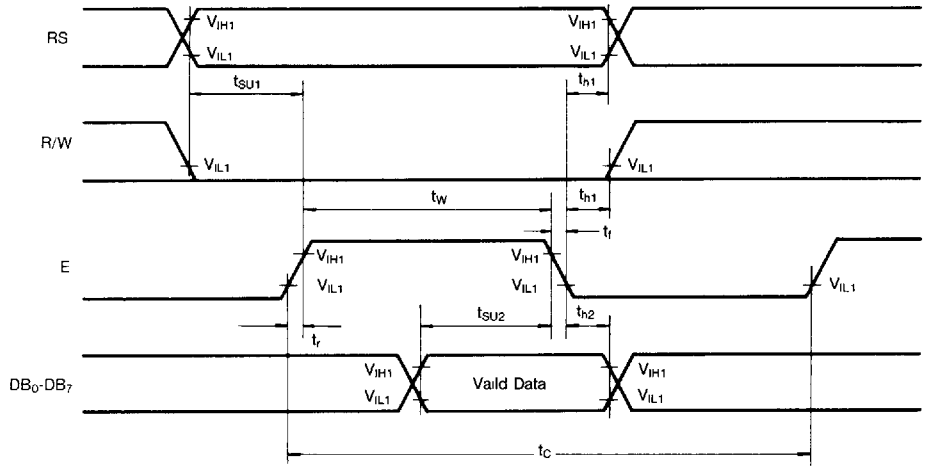
*V_{LCD} is the LCD driving voltage, refer to the initial set of the instruction code.

SAMSUNG ELECTRONICS

AC characteristics (V_{DD}=5V±10%, V_{SS}=0V Ta=25°C)

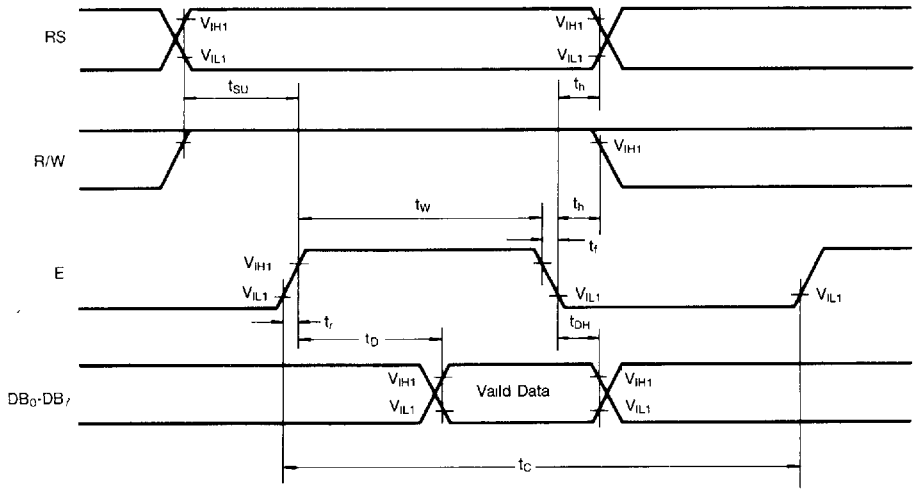
(1) Write mode

Characteristic	Symbol	Min	Typ	Max	Unit	Test pin
E cycle time	t_C	500	—	—	ns	E
E rise time	t_r	—	—	25	ns	E
E fall time	t_r	—	—	25	ns	E
E pulse width (High, Low)	t_W	220	—	—	ns	E
R/W and RS set-up time	t_{SU1}	40	—	—	ns	R/W, RS
R/W and RS hold time	t_{h1}	10	—	—	ns	R/W, RS
Data set-up time	t_{SU2}	60	—	—	ns	DB_0~DB_7
Data hold time	t_{h2}	10	—	—	ns	DB_0~DB_7



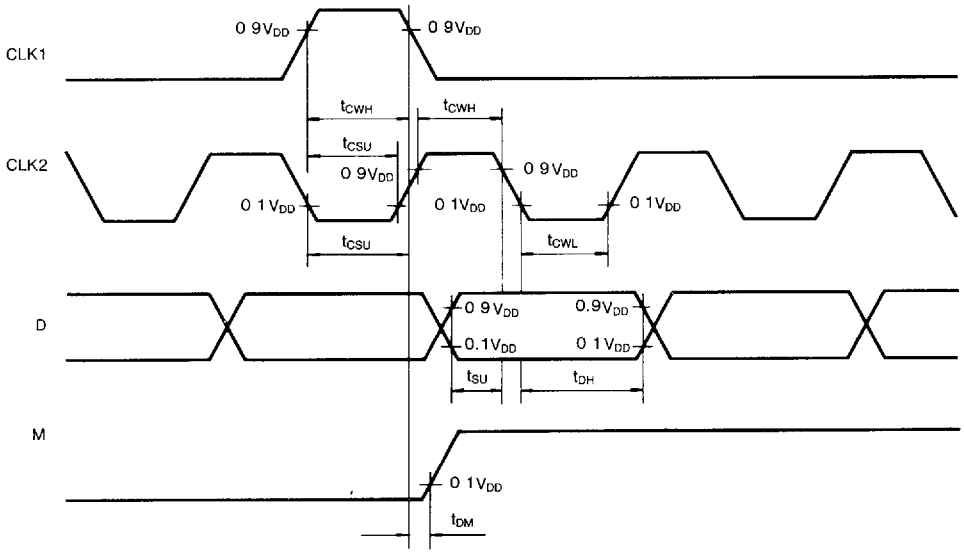
(2) Read mode

Characteristic	Symbol	Min	Typ	Max	Unit	TEST pin
E cycle time	t_C	500	—	—	ns	E
E rise time	t_r	—	—	25	ns	E
E fall time	t_f	—	—	25	ns	E
E pulse width	t_W	220	—	—	ns	E
R/W and RS set-up time	t_{SU}	40	—	—	ns	R/W, RS
R/W and RS hold time	t_h	10	—	—	ns	R/W, RS
Data output delay time	t_D	60	—	120	ns	DB_0-DB_7
Data hold time	t_{DH}	20	—	—	ns	DB_0-DB_7



(3) Interface mode with KS0065, KS0063

Characteristic	Symbol	Min	Typ	Max	Unit	Test pin
Clock pulse width High	t_{CWH}	800	—	—	ns	CLK
Clock pulse width Low	t_{CWL}	800	—	—	ns	CLK
Data set-up time	t_{SU}	300	—	—	ns	DB_0-DB_7
Data hold time	t_{DH}	300	—	—	ns	DB_0-DB_7
Clock set-up time	t_{CSU}	500	—	—	ns	CLK
M Delay time	t_{DM}	−1000	—	1000	ns	M



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CONTROL and DISPLAY COMMAND

Command	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	excution time (fosc = 250kHz)	Remark
DISPLAY CLEAR	L	L	L	L	L	L	L	L	L	H	1 64ms	
RETURN HOME	L	L	L	L	L	L	L	L	H	X	1.64ms	cursor move to first digit
ENTRY MODE SET	L	L	L	L	L	L	L	H	I/D	SH	40μs	•I/D; set cursor move direction I/D: H Increase; L Decrease •SH. Specifies shift of display SH: H display is shifted; L display is not shifted
DISPLAY ON/OFF	L	L	L	L	L	L	H	D	C	B	40μS	• Display D: H Display on; L Display off • Cursor C: H Cursor on; L Cursor off •Blinking B: H Blinking on; L Blinking off
SHIFT	L	L	L	L	L	H	S/C	R/L	X	X	40μS	SC: H Display shift; L Cursor move R/L: H Right shift; L Left shift
SET FUNCTION	L	L	L	L	H	DL	N	F	X	X	40μS	DL: H 8 bits interface; L 4 bits interface N: H 2 line display; L 1 line display F: H 5×10 dots; L 5×7 dots

Table 1.

CONTROL and DISPLAY COMMAND (continued)

Command	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Excution time (fosc = 250kHz)	Remark
SET CG RAM ADDRESS	L	L	L	H	CG RAM address (corresponds to cursor address)						40μS	CG RAM Data is sent and received after this setting
SET DD RAM ADDRESS	L	L	H	DD RAM address							40μS	DD RAM Data is sent and received after this setting
READ BUSY FLAG & ADDRESS	L	H	BF	Address Counter used for Both DD & CG RAM address							0μS	BF: H = Busy, L = Ready — Reads BF indication internal operating is being performed. — reads address counter contents
WRITE DATA	H	L	Write Data								40μS	Write data into DD or CG RAM
READ DATA	H	H	Read Data								40μS	Read data from DD or CGRAM

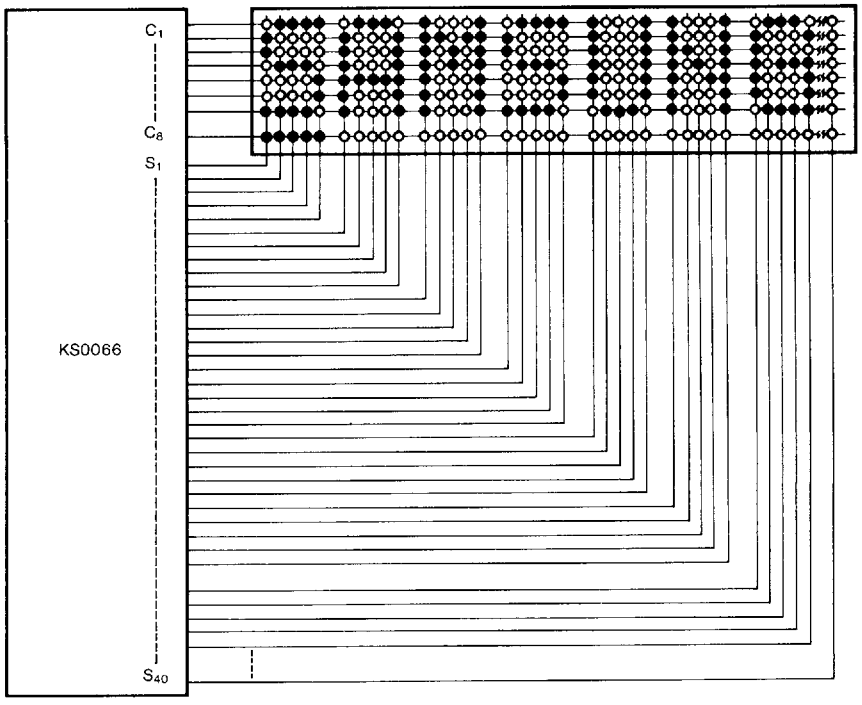
X Don't care

(table 1)

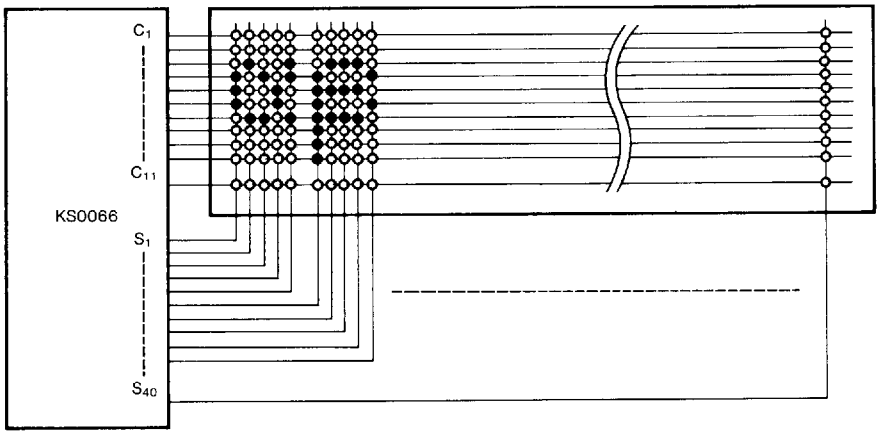
2

APPLICATION INFORMATION ACCORDING TO LCD PANEL

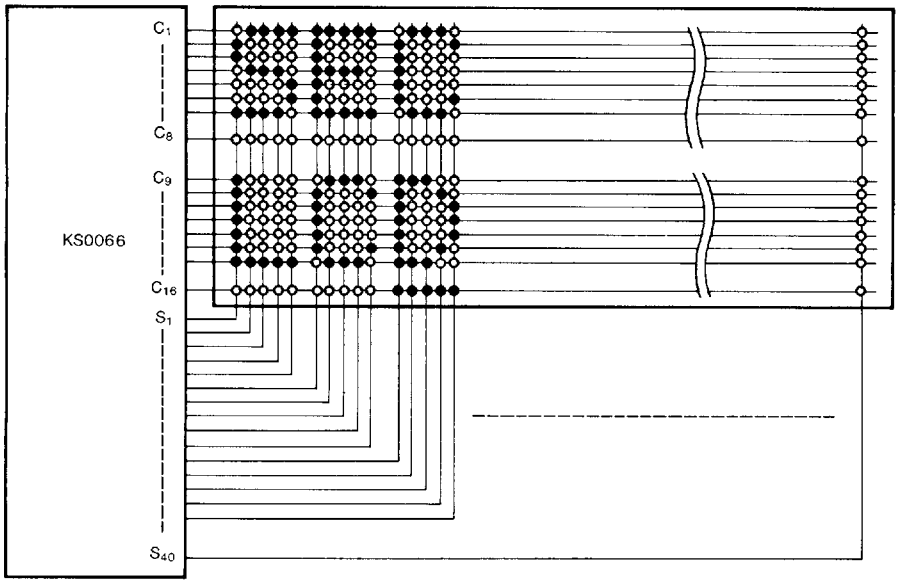
1) LCD Panel· 8 character × 1 line character format, 5×7 dots + 1 cursor line (1/4 bias, 1/8 duty)



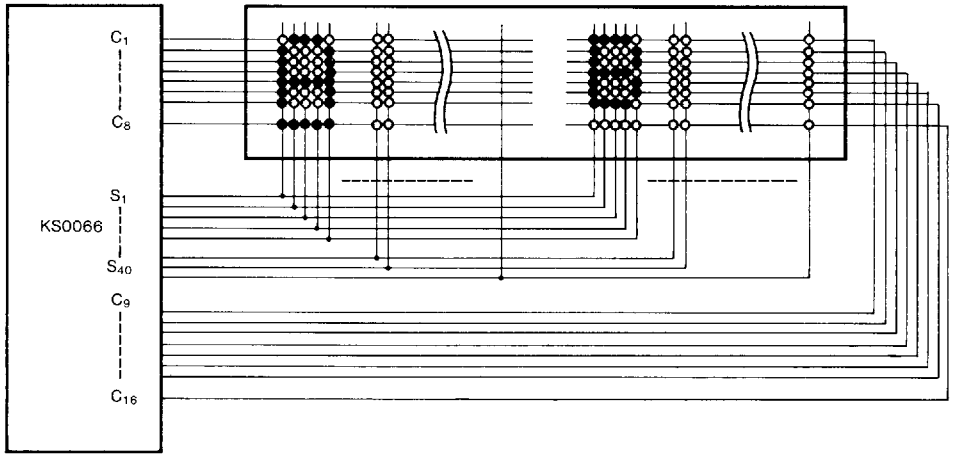
2) LCD Panel 8 character × 1 line character format; 5×10 dots +1 cursor line (1/4 bias, 1/11 duty)



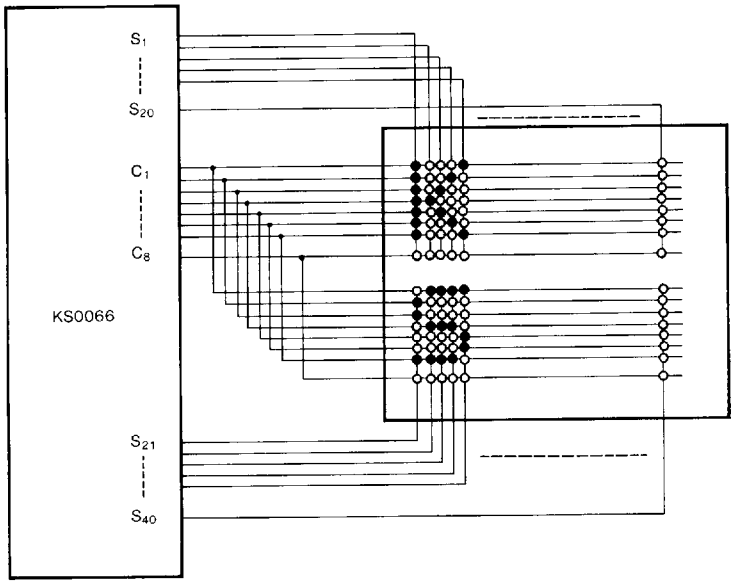
3) LCD Panel. 8 character × 2 line character format, 5×7 dots + 1 cursor line (1/5 bias, 1/16 duty)



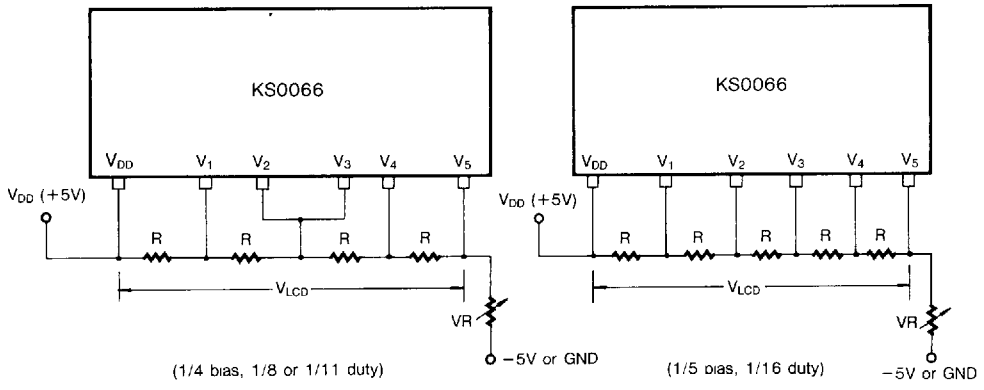
4) LCD Panel 16 character × 1 line Character format, 5×7 dots +1 cursor line (1/5 bias, 1/16 duty)



5) LCD panel: 4 character × 2 line character format: 5 × 7 dots+1 cursor line (1/4 bias, 1/8 duty)



BIAS VOLTAGE DIVIDE CIRCUIT



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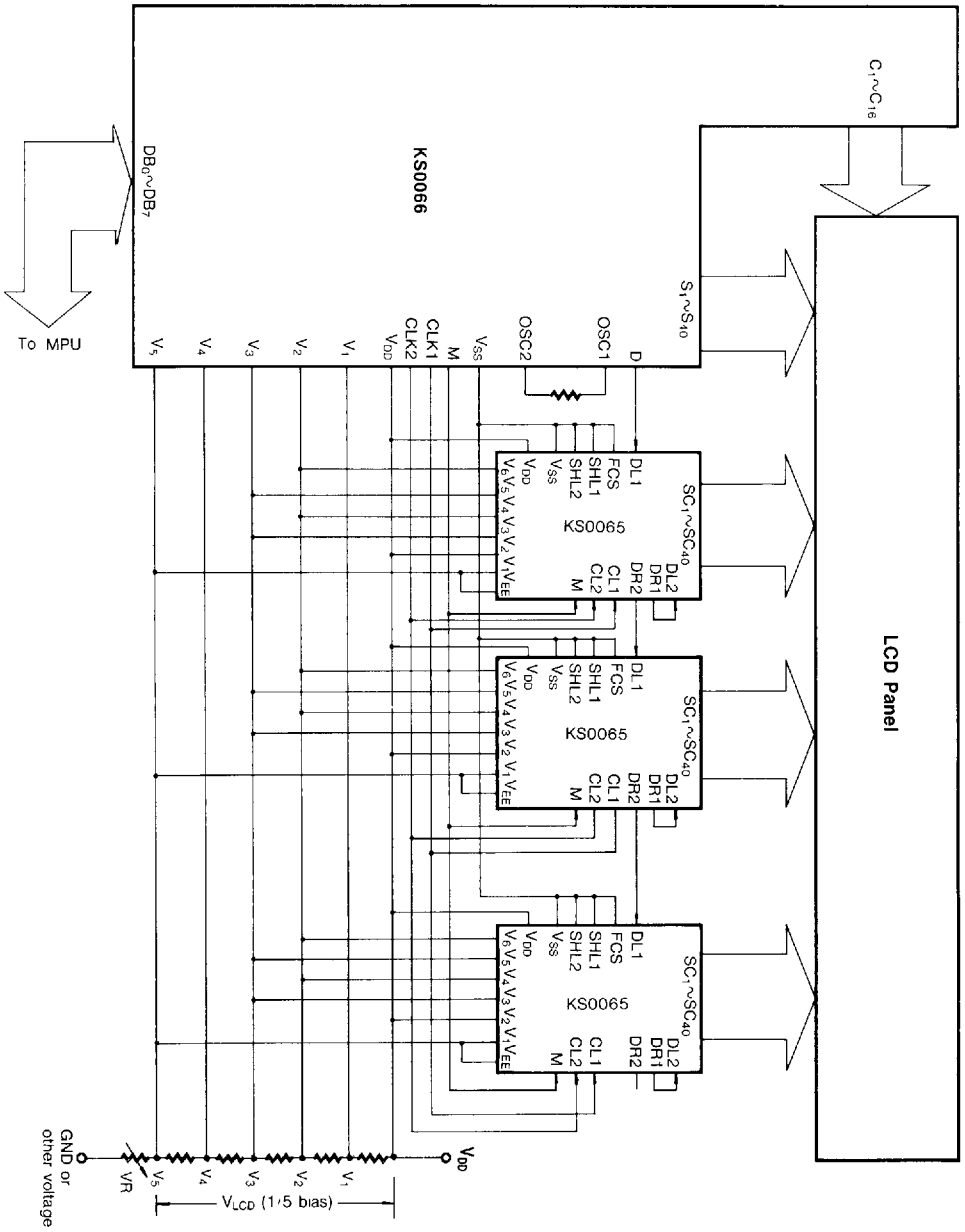
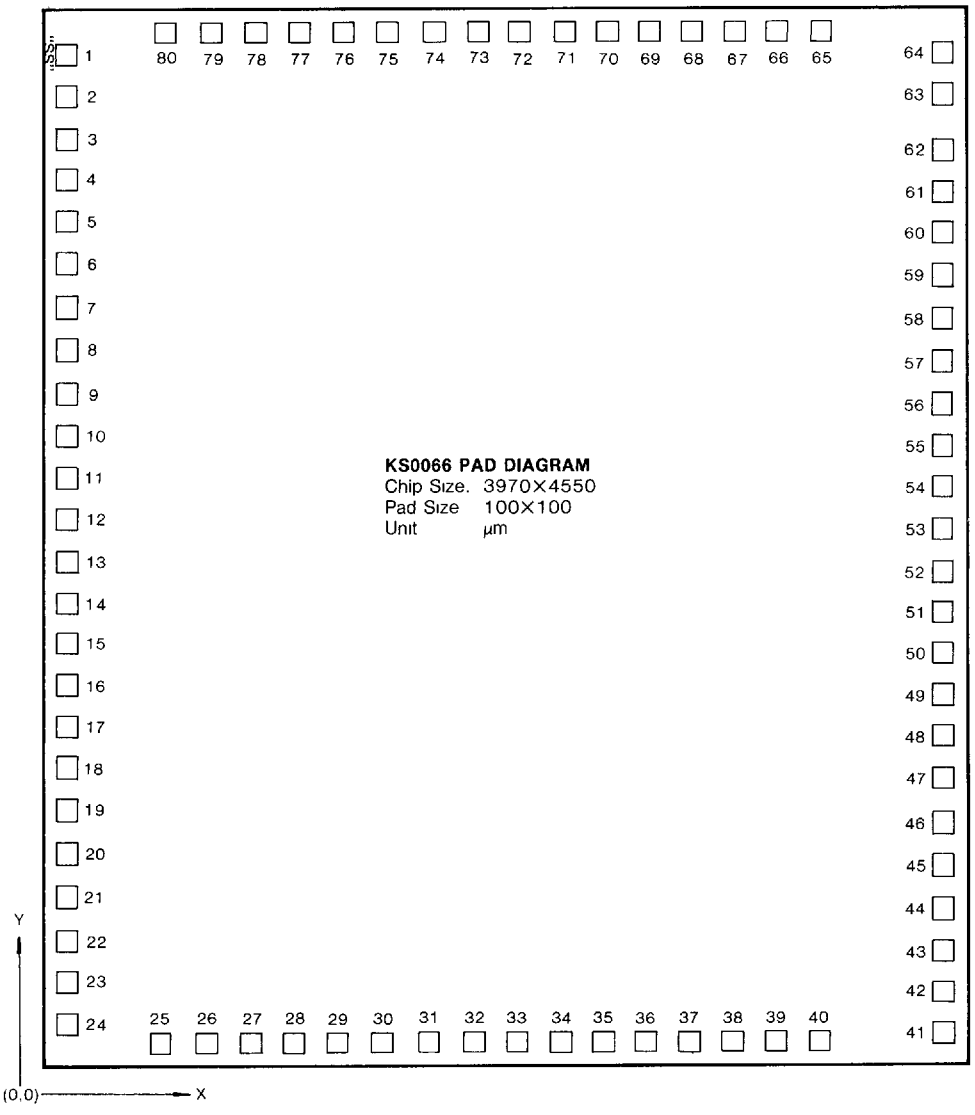
APPLICATION CIRCUIT



When KS0065 is externally connected to the KS0066, you can increase the number of display digits up to 80 characters

PAD DIAGRAM



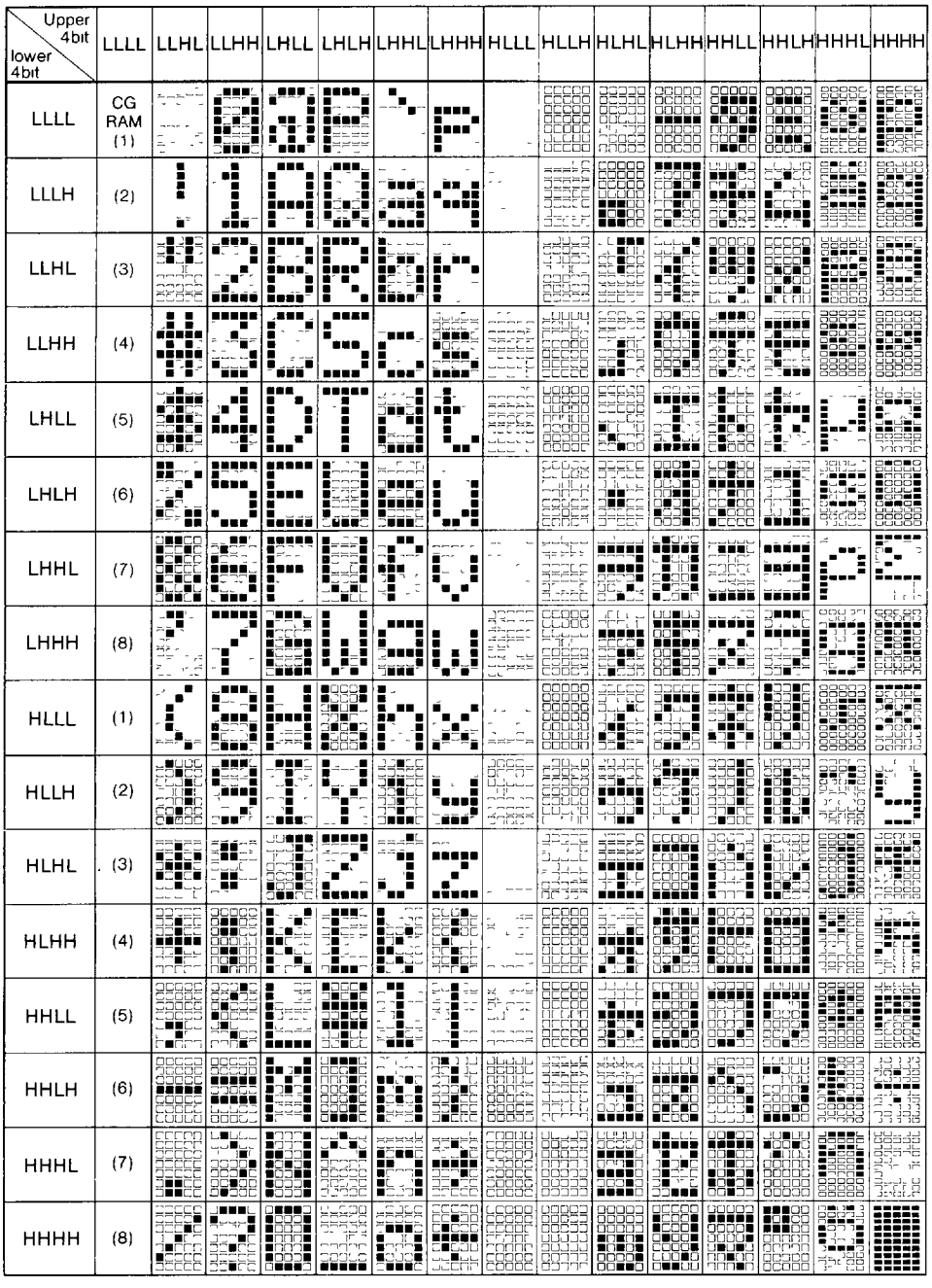
• "SS" Marking easy to find the pad No 1

PAD LOCATION

(Unit μm)

PAD	PAD	Coordinate		PAD	PAD	Coordinate		PAD	PAD	Coordinate		PAD	PAD	Coordinate	
No	Name	X	Y	No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
1	S22	130	4347	21	S2	130	747	41	DB2	3862	156	61	C15	3862	3764
2	S21	130	4167	22	S1	130	567	42	DB3	3862	336	62	C16	3862	3944
3	S20	130	3987	23	GND	130	387	43	DB4	3862	516	63	S40	3862	4188
4	S19	130	3807	24	OSC1	130	204	44	DB5	3862	696	64	S39	3862	4368
5	S18	130	3627	25	OSC2	612	130	45	DB6	3862	876	65	S38	3236	4446
6	S17	130	3447	26	V1	812	130	46	DB7	3862	1056	66	S37	3056	4446
7	S16	130	3267	27	V2	992	130	47	C1	3862	1244	67	S36	2876	4446
8	S15	130	3087	28	V3	1172	130	48	C2	3862	1424	68	S35	2696	4446
9	S14	130	2907	29	V4	1352	130	49	C3	3862	1604	69	S34	2516	4446
10	S13	130	2727	30	V5	1532	130	50	C4	3862	1784	70	S33	2336	4446
11	S12	130	2547	31	CLK1	1730	130	51	C5	3862	1964	71	S32	2156	4446
12	S11	130	2367	32	CLK2	1910	130	52	C6	3862	2144	72	S31	1976	4446
13	S10	130	2187	33	V_{DD}	2090	130	53	C7	3862	2324	73	S30	1796	4446
14	S9	130	2007	34	M	2270	130	54	C8	3862	2504	74	S29	1616	4446
15	S8	130	1827	35	D	2450	130	55	C9	3862	2684	75	S28	1436	4446
16	S7	130	1647	36	RS	2630	130	56	C10	3862	2864	76	S27	1256	4446
17	S6	130	1467	37	R/W	2810	130	57	C11	3862	3044	77	S26	1076	4446
18	S5	130	1287	38	E	2990	130	58	C12	3862	3224	78	S25	896	4446
19	S4	130	1107	39	DB0	3170	130	59	C13	3862	3404	79	S24	716	4446
20	S3	130	927	40	DB1	3350	130	60	C14	3862	3584	80	S23	536	4446

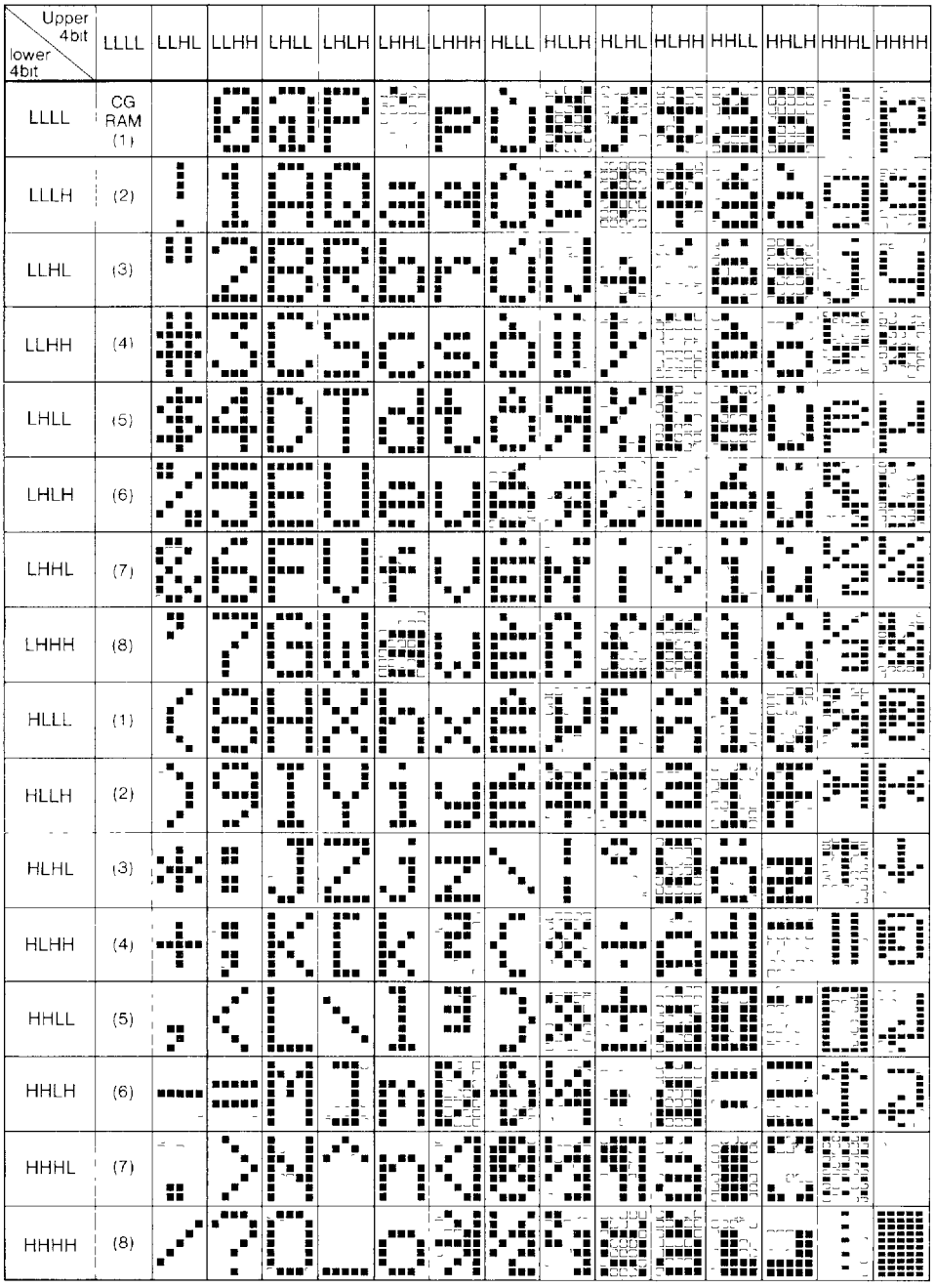
Standard Character Pattern (KS0066F00)



(Table 2-1)

SAMSUNG ELECTRONICS

Standard Character Pattern(KS0066F03)



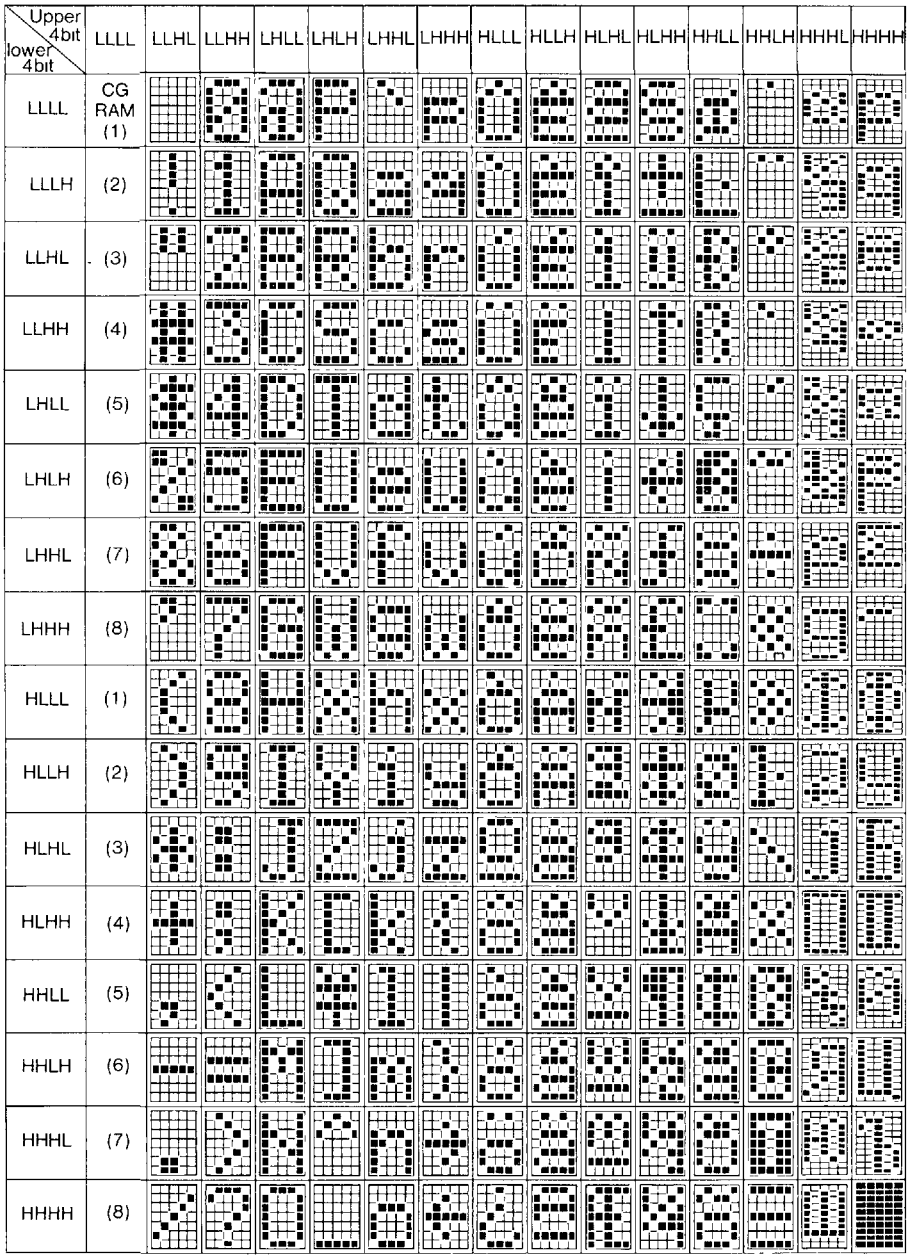
(Table 2-2)

Standard Character Pattern(KS0066F04)

Upper 4bit / lower 4bit	LLLL	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)														
LLLH	(2)														
LLHL	(3)														
LLHH	(4)														
LHLL	(5)														
LHLH	(6)														
LHHL	(7)														
LHHH	(8)														
HLLL	(1)														
HLLH	(2)														
HLHL	(3)														
HLHH	(4)														
HHLL	(5)														
HHLH	(6)														
HHHL	(7)														
HHHH	(8)														

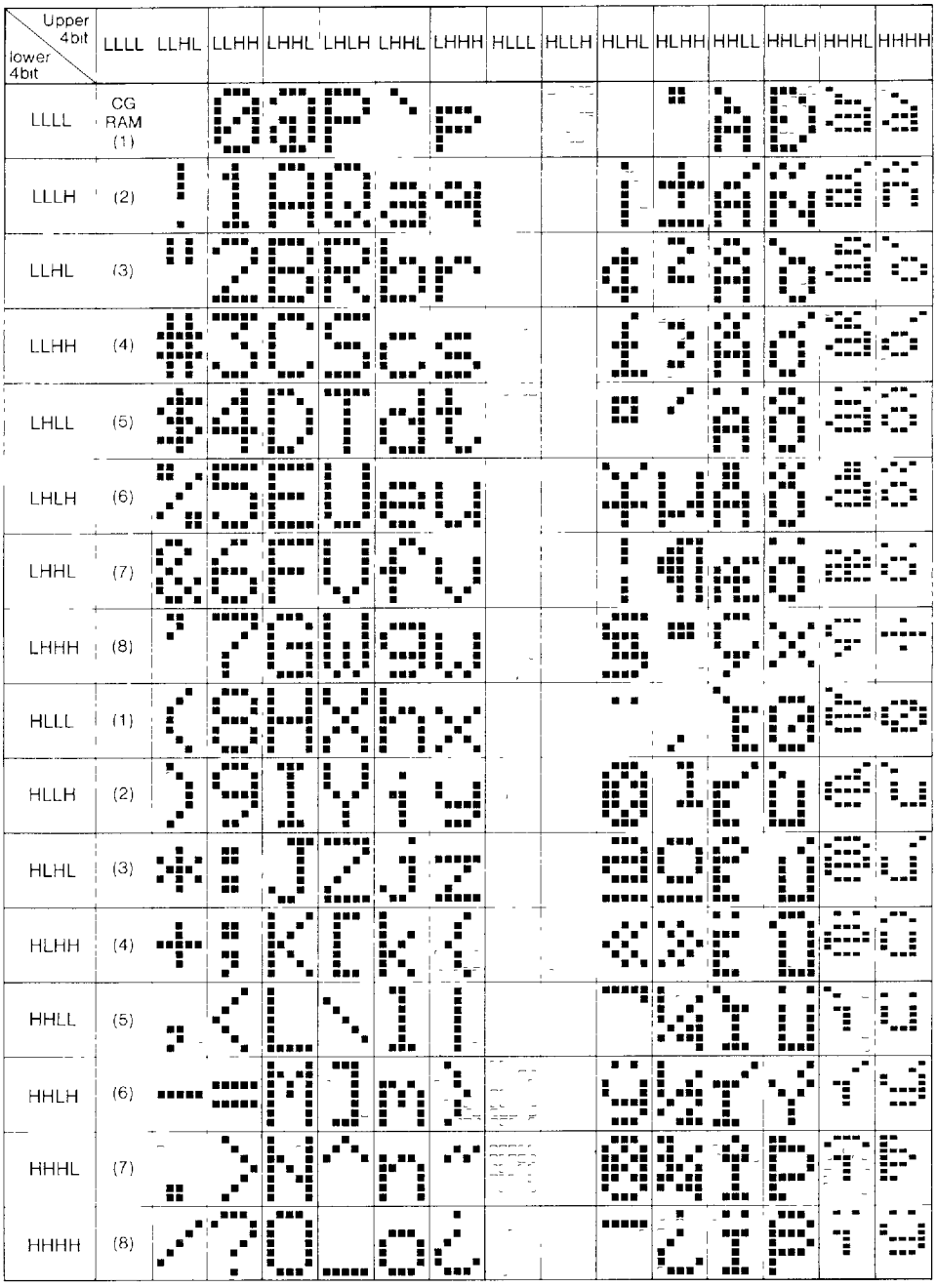
(Table 2-3)

Standard Character Pattern (KS0066F05)



(Table 2-4)

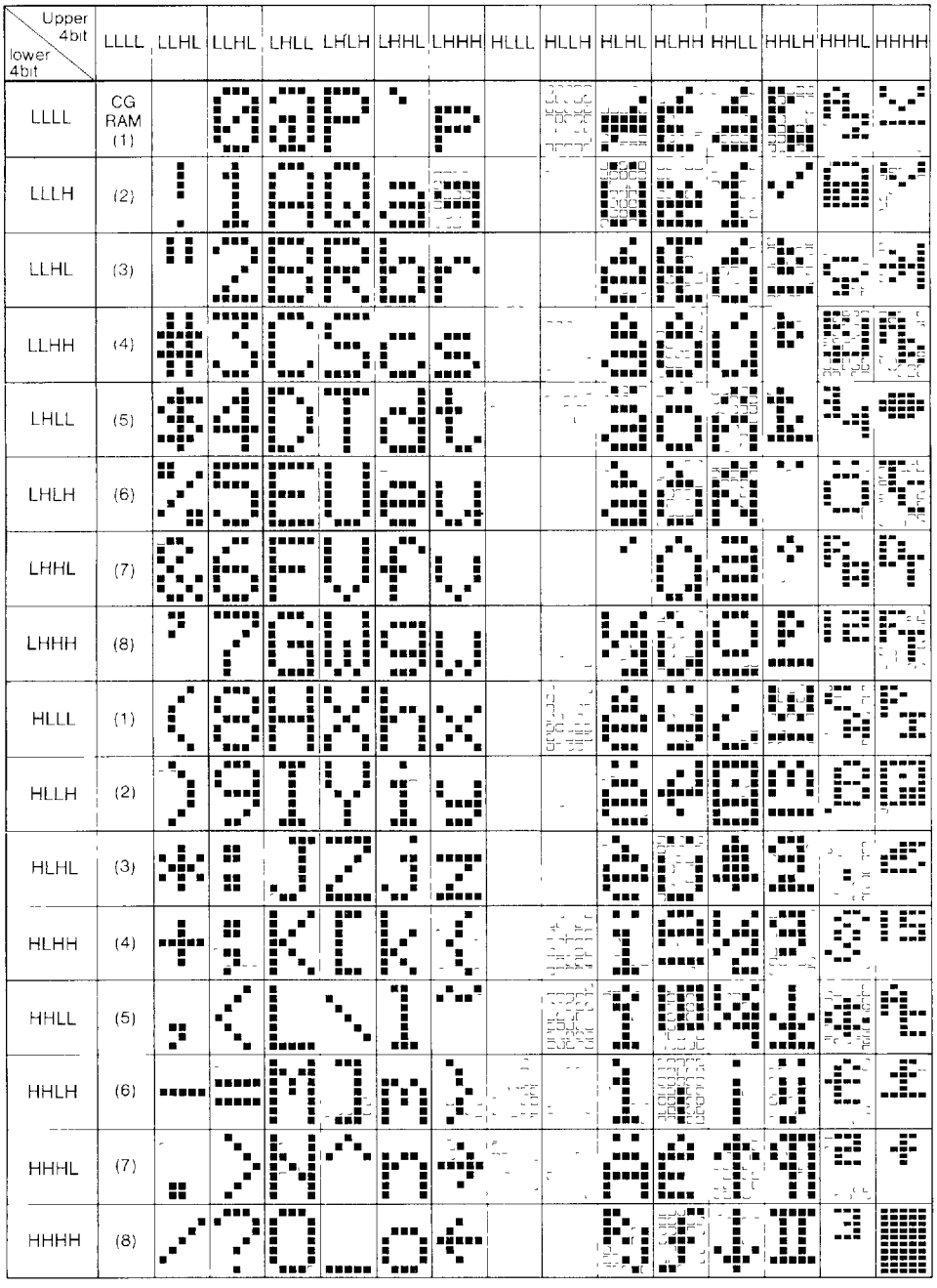
Standard Character Pattern(KS0066F06)



(Table 2-5)

SAMSUNG ELECTRONICS

Standard Character Pattern(KS0066F59)



(Table 2-6)

SAMSUNG ELECTRONICS

KS0066 FONT SHEET FOR CUSTOM ORDER

Upper 4bit / lower 4bit	LLLL	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)														
LLLH	(2)														
LLHL	(3)														
LLHH	(4)														
LHLL	(5)														
LHLH	(6)														
LHHL	(7)														
LHHH	(8)														
HLLL	(1)														
HLLH	(2)														
HLHL	(3)														
HLHH	(4)														
HHLL	(5)														
HHLH	(6)														
HHHL	(7)														
HHHH	(8)														