

HD151TS302ARP

Spread Spectrum Clock for EMI Solution

REJ03D0019-0500Z
(Previous ADE-205-690D(Z))
Rev.5.00
May.19.2003

Description

The HD151TS302A is a high-performance Spread Spectrum Clock modulator. It is suitable for low EMI solution.

Features

- Supports 10 MHz to 60 MHz operation. (Designed for XIN = 24 MHz and 48 MHz)
- 1 copy of clock out with spread spectrum modulation @3.3 V
- 1 copy of reference clock @3.3 V
- Programmable spread spectrum modulation (–0.5%, –1.0%, –3.0% down spread modulation and spread spectrum disable mode.)
- SOP–8pin
- Pin to pin compatible with HD151TS302RP

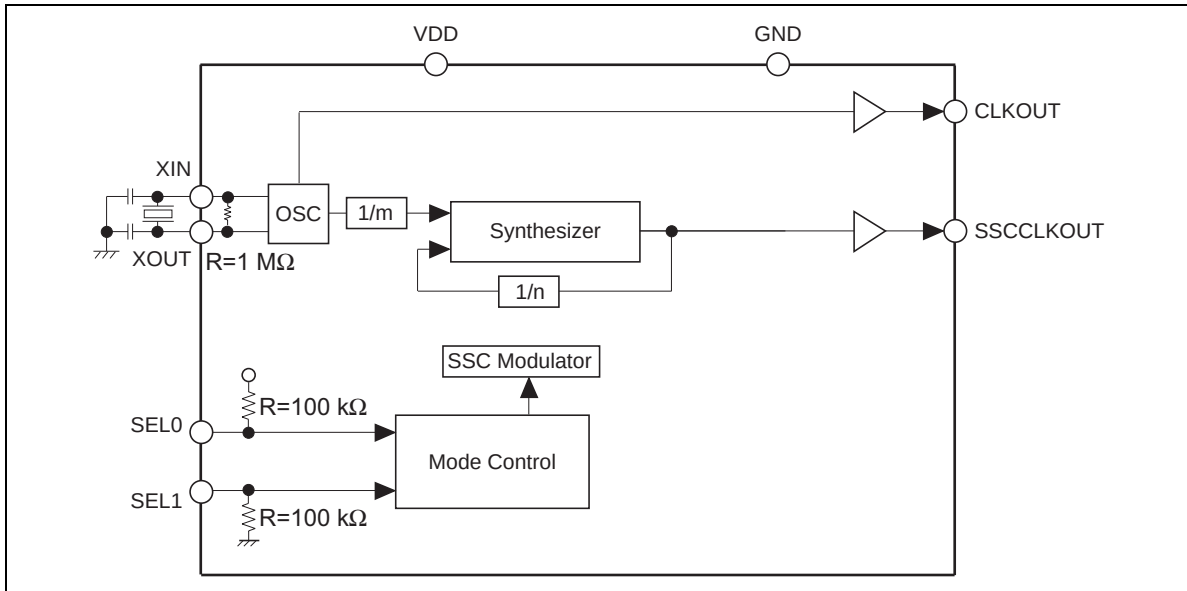
Key Specifications

- Supply voltages : VDD = 3.3 V $\pm$ 0.165 V
- Ta = 0 to 70°C operating range
- Clock output duty cycle = 50 $\pm$ 5%
- Cycle to cycle jitter = $\pm$ 250 ps typ.
- Output slew rate = 0.8V/ns min.
- Ordering Information

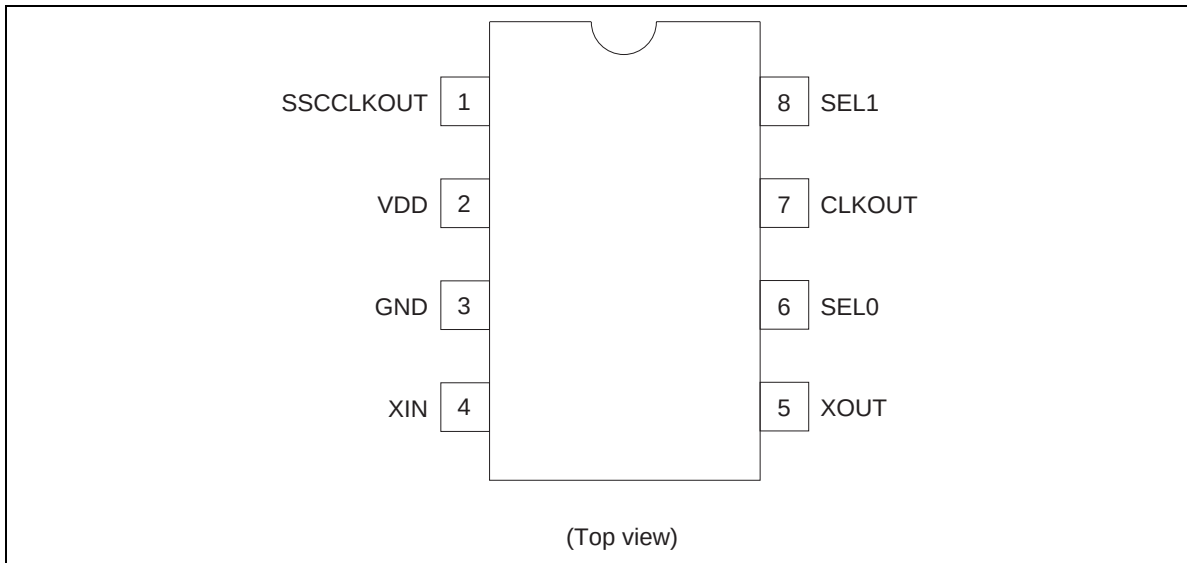
Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD151TS302ARPEL	SOP-8 pin (JEDEC)	FP-8DC	RP	EL (2,500 pcs / Reel)

Note: Please consult the sales office for the above package availability.

Block Diagram



Pin Arrangement



SSC Function Table

SEL1 :0	Spread Percentage
0 0	−1.0%
0 1	−3.0%
1 0	SSC OFF
1 1	−0.5%

Note: −3.0% SSC is selected for default by internal pull-up & down resistors.

Clock Frequency Table

XIN(MHz)	SSCCLKOUT(MHz)	CLKOUT(MHz)
48	48 ^{*1}	48 ^{*2}
24	24 ^{*1}	24 ^{*2}

Notes: 1. With spread spectrum modulation.
2. Without spread spectrum modulation.

Pin Descriptions

Pin name	No.	Type	Description
GND	3	Ground	GND pin
VDD	2	Power	Power supplies pin. Normally 3.3 V.
CLKOUT	7	Output	Normally 3.3 V reference clock output.
SSCCLKOUT	1	Output	Spread spectrum modulated clock output.
XIN	4	Input	Oscillator input.
XOUT	5	Output	Oscillator output.
SEL0	6	Input	SSC mode select pin. LVCMOS level input. Pull-up by internal resistor. (100 kΩ).
SEL1	8	Input	SSC mode select pin. LVCMOS level input. Pull-down by internal resistor (100 kΩ).

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	VDD	−0.5 to 4.6	V	
Input voltage	V _I	−0.5 to 4.6	V	
Output voltage ^{*1}	V _O	−0.5 to VDD+0.5	V	
Input clamp current	I _{IK}	−50	mA	V _I < 0
Output clamp current	I _{OK}	−50	mA	V _O < 0
Continuous output current	I _O	±50	mA	V _O = 0 to VDD
Maximum power dissipation at T _a = 55°C (in still air)		0.7	W	
Storage temperature	T _{stg}	−65 to +150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	VDD	3.135	3.3	3.465	V	
DC input signal voltage		−0.3	—	VDD+0.3	V	
High level input voltage	V _{IH}	2.0	—	VDD+0.3	V	
Low level input voltage	V _{IL}	−0.3	—	0.8	V	
Operating temperature	T _a	0	—	70	°C	
Input clock duty cycle		45	50	55	%	

DC Electrical Characteristics

Ta = 0 to 70°C, VDD = 3.3 V±5%

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input low voltage	V _{IL}	—	—	0.8	V	
Input high voltage	V _{IH}	2.0	—	—	V	
Input current	I _I	—	—	±10	μA	V _I = 0 V or 3.465 V, VDD = 3.465 V, XIN pin
		—	—	±100		V _I = 0 V or 3.465 V, VDD = 3.465 V, SEL0, SEL1 pins
Input capacitance	C _I	—	—	4	pF	SEL0, SEL1
Operating current		—	7	—	mA	XIN = 24 MHz, C _L = 0 pF, VDD = 3.3 V

DC Electrical Characteristics / Clock Output & SSC Clock Output

Ta = 0 to 70°C, VDD = 3.3 V±5%

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage	V _{OH}	3.1	—	—	V	I _{OH} = -1 mA, VDD = 3.3 V
	V _{OL}	—	—	50	mV	I _{OL} = 1 mA, VDD = 3.3 V
Output current* ¹	I _{OH}	—	-30	—	mA	V _{OH} = 1.5 V
	I _{OL}	—	30	—		V _{OL} = 1.5 V

Note: 1. Parameters are target of design. Not 100% tested in production.

AC Electrical Characteristics / Clock Output & SSC Clock Output

Ta = 25°C, VDD = 3.3 V, CL = 15 pF

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Cycle to cycle jitter ^{*1, 2}	t _{CCS}	—	250	300	ps	SSCCLKOUT, 24 MHz	SSCOFF SEL1:0 = 10 Fig1
		—	250	300		SSCCLKOUT, 48 MHz	
		—	250	300		SSCCLKOUT, 24 MHz	SSC = -0.5% SEL1:0 = 11 Fig1
		—	250	300		SSCCLKOUT, 48 MHz	
		—	250	300		SSCCLKOUT, 24 MHz	SSC = -3.0% SEL1:0 = 01 Fig1
		—	250	300		SSCCLKOUT, 48 MHz	
		—	250	300		CLKOUT, 24 MHz & 48 MHz	Fig1
		—	250	300			
Output frequency ^{*1, 2}		23.8	—	24.2	MHz	SSCCLKOUT, XIN = 24 MHz	SSCOFF SEL1:0 = 10
		47.3	—	48.7		SSCCLKOUT, XIN = 48 MHz	
		23.7	—	24.2		SSCCLKOUT, XIN = 24 MHz	SSC = -0.5% SEL1:0 = 11
		47.0	—	48.7		SSCCLKOUT, XIN = 48 MHz	
		23.1	—	24.2		SSCCLKOUT, XIN = 24 MHz	SSC = -3.0% SEL1:0 = 01
		45.9	—	48.7		SSCCLKOUT, XIN = 48 MHz	
		23.8	—	24.2		CLKOUT, 24 MHz	
		47.3	—	48.7		CLKOUT, 48 MHz	
Slew rate ^{*1}	t _{SL}	0.8	—	—	V/ns	@48 MHz CLKOUT	0.4 V to 2.4 V
Clock duty cycle ^{*1}		45	50	55	%		
Output impedance ^{*1}		—	40	—	Ω		
Spread spectrum modulation frequency ^{*1}		—	33	—	KHz	@48 MHz SSCCLKOUT	
Input clock frequency		10	—	60	MHz		
Stabilization time ^{*1,3}		—	—	2	ms		

Notes: 1. Parameters are target of design. Not 100% tested in production.
2. Cycle to cycle jitter and output frequency are included spread spectrum modulation.
3. Stabilization time is the time required for the integrated circuit to obtain phase lock of its input signal after power up.

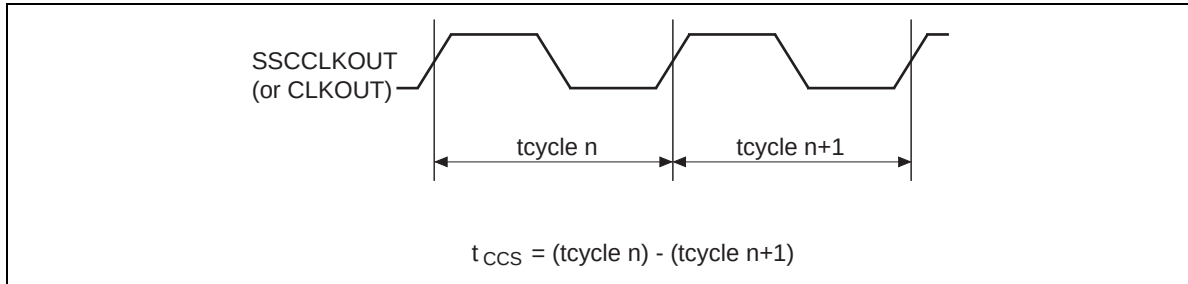


Figure 1 Cycle to cycle jitter

Application Information

1. Recommended Circuit Configuration

The power supply circuit of the optimal performance on the application of a system should refer to Fig. 2.

VDD decoupling is important to both reduce Jitter and EMI radiation.

The C1 decoupling capacitor should be placed as close to the VDD pin as possible, otherwise the increased trace inductance will negate its decoupling capability.

The C2 decoupling capacitor shown should be a tantalum type.

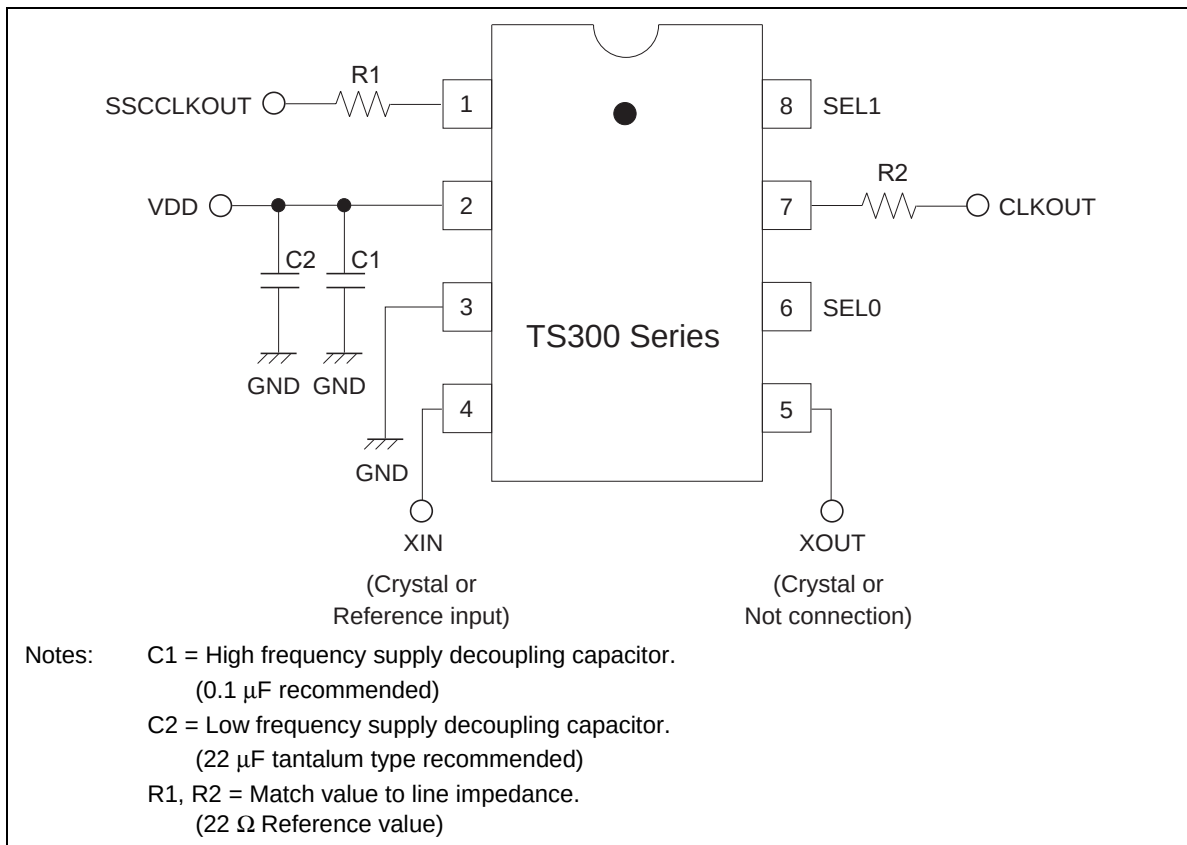


Figure 2 Recommended circuit configuration

2. Example Board Layout Configuration

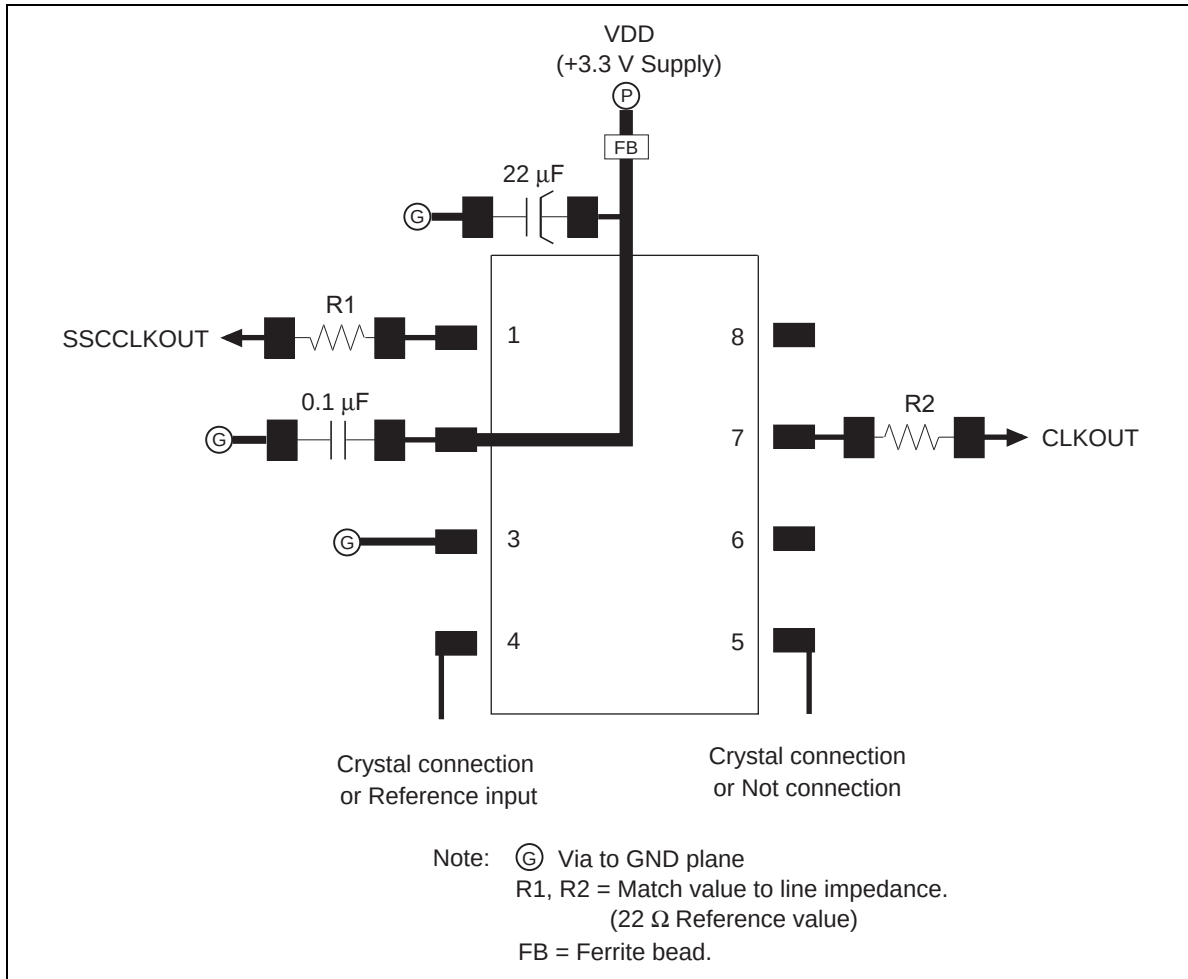


Figure 3 Example Board Layout

3. Example of TS300 EMI Solution IC's Application

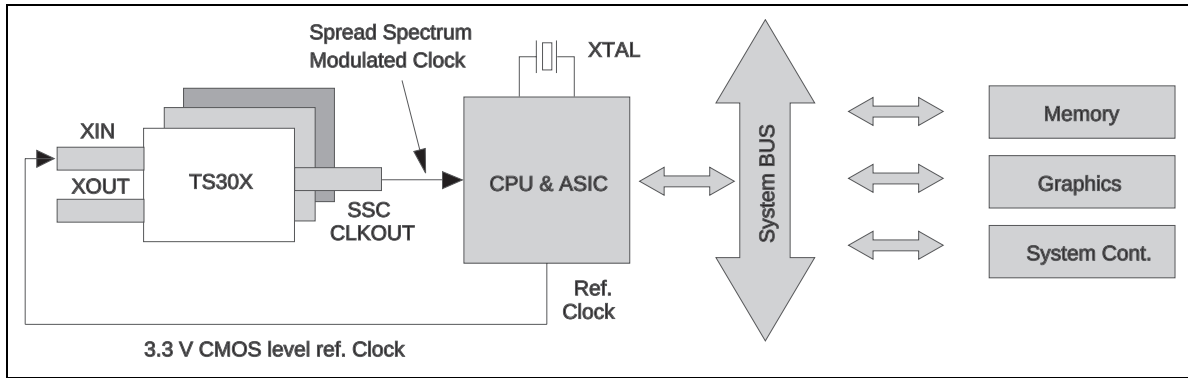


Fig 4 Ref. Clock Input Example

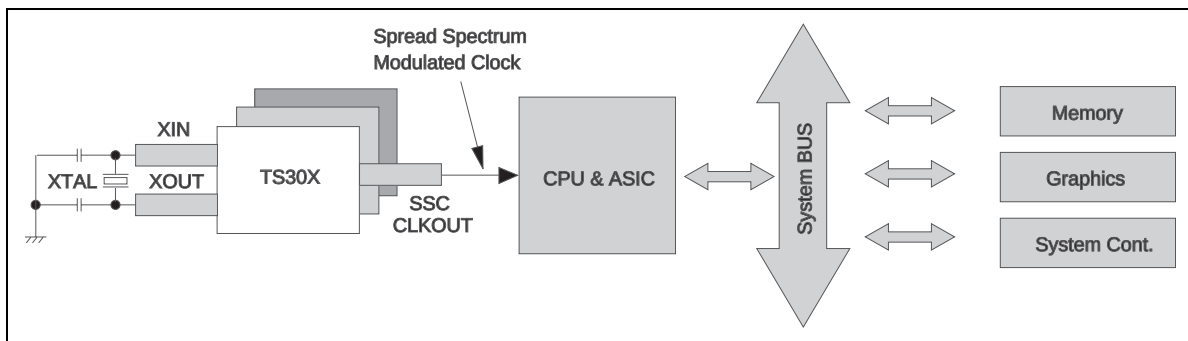
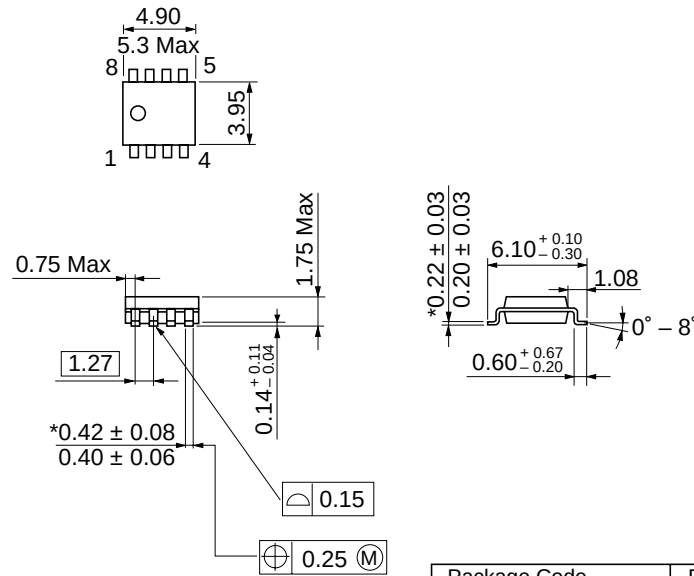


Fig 5 XTAL Ref. Clock Input Example

Package Dimensions

As of January, 2003

Unit: mm



*Dimension including the plating thickness
Base material dimension

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corporation product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corporation or a third party.
 2. Renesas Technology Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
 3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corporation by various means, including the Renesas Technology Corporation Semiconductor home page (<http://www.renesas.com>).
 4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
 5. Renesas Technology Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
 6. The prior written approval of Renesas Technology Corporation is necessary to reprint or reproduce in whole or in part these materials.
 7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
 8. Please contact Renesas Technology Corporation for further details on these materials or the products contained therein.
-



<http://www.renesas.com>

Copyright © 2003. Renesas Technology Corporation, All rights reserved. Printed in Japan.
Colophon 0.0