élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2142C
Differential Line Receiver

Features

- Differential input range ±2.3V
- 150 MHz 3 dB bandwidth
- 400 V/μs slewrate
- ±5V supplies or single supply
- 50 mA minimum output current
- Output swing (100Ω load) to within 1.5V of supplies
- Low power −11 mA typical

Applications

- Twisted pair receiver
- Differential line receiver
- VGA over twisted pair
- ADSL/HDSL receiver
- Differential to single ended amplification.
- Reception of analog signals in a noisy environment.

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2142CN	−40°C to +85°C	8-pin DIP	MDP0031
EL2142CS	−40°C to +85°C	8-pin SOIC	MDP0027

General Description

The EL2142C is a very high bandwidth amplifier designed to extract the difference signal from noisy environments, and is thus primarily targeted for applications such as receiving signals from twisted pair lines, or any application where common mode noise injection is likely to occur.

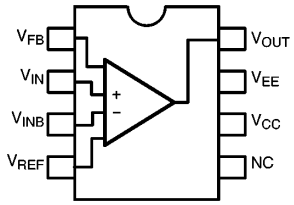
The EL2142C is stable for a gain of one, and requires two external resistors to set the voltage gain.

The output common mode level is set by the reference pin (V_{REF}), which has a −3 dB bandwidth of over 100 MHz. Generally, this pin is grounded, but it can be tied to any voltage reference.

The output can deliver a minimum of ±50 mA and is short circuit protected to withstand a temporary overload condition.

Connection Diagrams

EL2142C SO, P-DIP



2142-1

Note: All information contained in this data sheet has been carefully checked and is believed to be accurate as of the date of publication; however, this data sheet cannot be a "controlled document". Current revisions, if any, to these specifications are maintained at the factory and are available upon your request. We recommend checking the revision level before finalization of your design documentation.

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Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_{CC}–V_{EE})	0V to 12.6V	Operating Junction Temperature	+150°C
Maximum Output Current	±60 mA	Lead Temperature (<5 sec)	+300°C
Storage Temperature Range	−65°C to +150°C	Recommended Operating Temperature	−40°C to +85°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics
(V_{CC} = +5V, V_{EE} = −5V, T_A = 25C, V_{IN} = 0V, R_L = 100, unless otherwise specified)

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{supply}	Supply Operating Range (V_{CC}–V_{EE})	±3.0	±5.0	±6.3	I	V
I_S	Power Supply Current (no load)		11	14	I	mA
V_{OS}	Input Referred Offset Voltage	−25	10	40	I	mV
I_{IN}	Input Bias Current (V_{IN}, V_{INB}, V_{REF})	−20	6	20	I	µA
Z_{IN}	Differential Input Resistance		400		V	KΩ
C_{IN}	Differential Input Capacitance		1		V	pF
V_{DIFF}	Differential Input Range	±2.0	±2.3		I	V
A_{VOL}	Open Loop Voltage Gain		75		V	dB
V_{IN}	Input Common Mode Voltage Range	−2.6		+4.0	I	V
V_{OUT}	Output Voltage Swing (50Ω load to GND)	±2.9	±3.1		I	V
I_{OUT}(min)	Minimum Output Current	50	60		I	mA
V_N	Input Referred Voltage Noise		36		V	nV/√ Hz
V_{REF}	Output Voltage Control Range	−2.5		+3.3	I	V
PSRR	Power Supply Rejection Ratio	60	70		I	dB
CMRR2	Input Common Mode Rejection Ratio (V_{IN} = ±2V)	60	70		I	dB
CMRR1	Input Common Mode Rejection Ratio (full V_{IN} range)	50	60		I	dB

TD is 3.3in

AC Electrical Characteristics

(V_{CC} = +5V, V_{EE} = −5V, T_A = 25C, V_{IN} = 0V, R_{LOAD} = 100, unless otherwise specified)

Parameter	Description	Min	Typ	Max	Test Level	Units
BW(−3dB)	−3 dB Bandwidth (Gain =1)		150		V	MHz
SR	Slewrate		400		V	V/μs
T_{stl}	Settling time to 1%		15		V	ns
GBWP	Gain bandwidth product		200		V	MHz
V_{REF}BW(−3 dB)	V_{REF} −3dB Bandwidth		130		V	MHz
V_{REF}SR	V_{REF} Slewrate		100		V	V/μsec
dG	Differential gain at 3.58 MHz.		0.2		V	%
dθ	Differential phase at 3.58 MHz.		0.2		V	

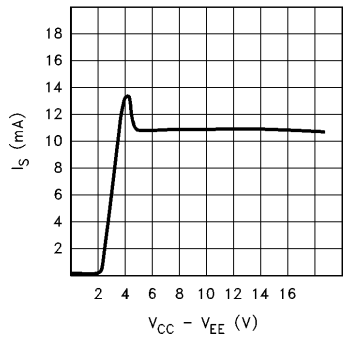
Pin Description

Pin Number	Pin Name	Function
1	V_{FB}	Feedback input
2	V_{IN}	Non-inverting input
3	V_{INB}	Inverting input
4	V_{REF}	Sets output voltage level to V_{REF} when V_{IN} = V_{INB}
5	NC	
6	V_{CC}	Positive supply voltage
7	V_{EE}	Negative supply voltage
8	V_{OUT}	Output voltage

TD is 1.8in

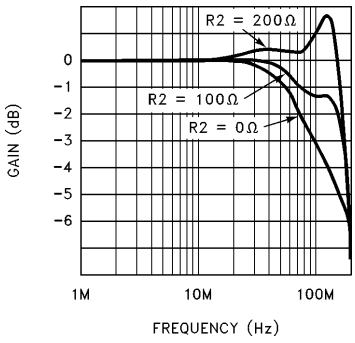
Typical Performance Curves

I_S vs Supply Voltage



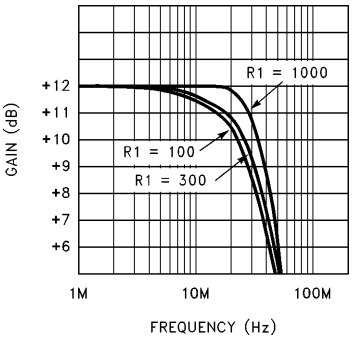
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Frequency Response (Gain = 1)



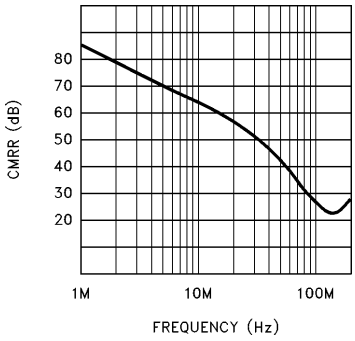
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Frequency Response vs Resistor R1 (Gain = 4)



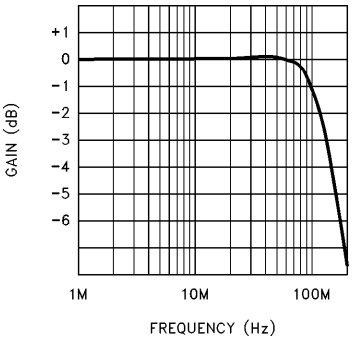
2142-4

CMRR vs Frequency



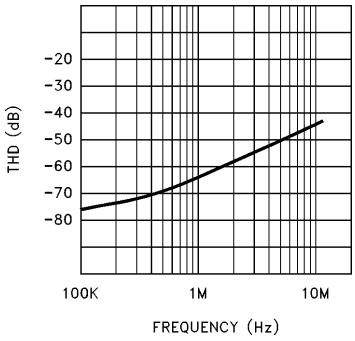
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V_{REF} Frequency Response



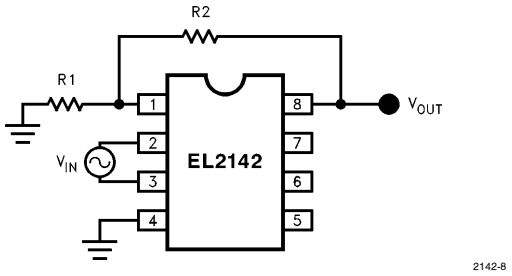
2142-6

Distortion vs Frequency
(GAIN = 3, R_{LOAD} = 100Ω)
V_{IN} = 2V pk/pk



2142-7

Applications Information



Gain Equation

$V_{OUT} = ((R2+R1)/R1) \times (V_{IN}\text{-}V_{INB}+V_{REF})$ when R1 tied to GND
$V_{OUT} = ((R2+R1)/R1) \times (V_{IN}\text{-}V_{INB})$ when R1 tied to V_{REF}

Choice of Feedback Resistor

For a gain of one, V_{OUT} may be shorted back to V_{FB}, but 100Ω–200Ω improves the bandwidth. For gains greater than one, there is little to be gained from choosing resistor R1 value below 200Ω, for it would only result in increased power dissipation and potential signal distortion. Above 200Ω, the bandwidth response will develop some peaking (for a gain of one), but substantially higher R1 values may be used for higher voltage gains, such as up to 1 kΩ at a gain of four before peaking will develop.

Capacitance Considerations

As with many high bandwidth amplifiers, the EL2142C prefers not to drive highly capacitive loads. It is best if the capacitance on V_{OUT} is kept below 10 pF if the user does not want gain peaking to develop. The V_{FB} node forms a potential pole in the feedback loop, so capacitance should be minimized on this node for maximum bandwidth.

The amount of capacitance tolerated on any of these nodes in an actual application will also be dependent on the gain setting and the resistor values in the feedback network.

Typical Applications

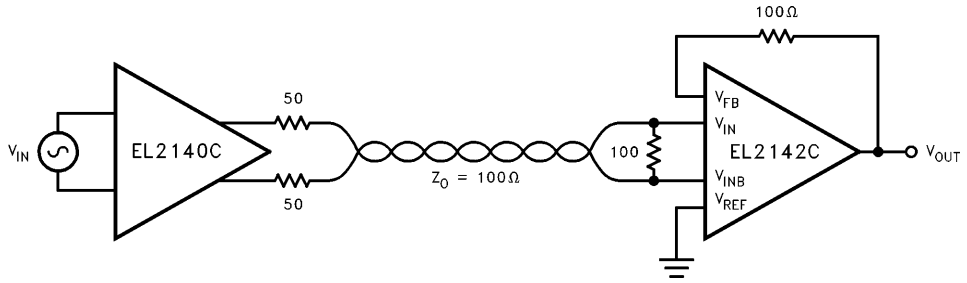


Figure 1. Typical Twisted Pair Application

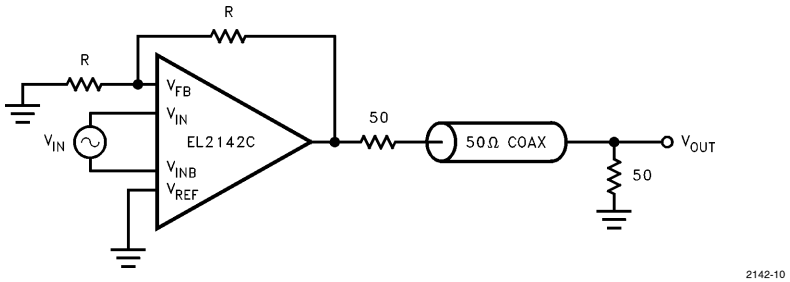


Figure 2. Coaxial Cable Driver

Typical Applications — Contd.

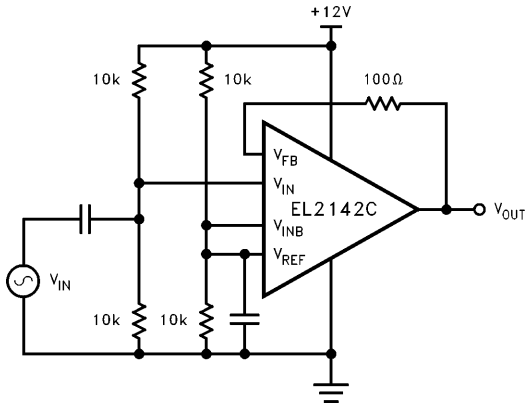
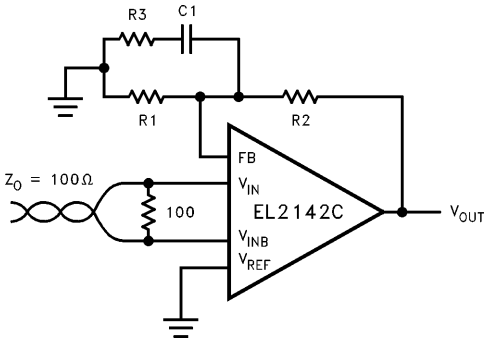


Figure 3. Single Supply Receiver



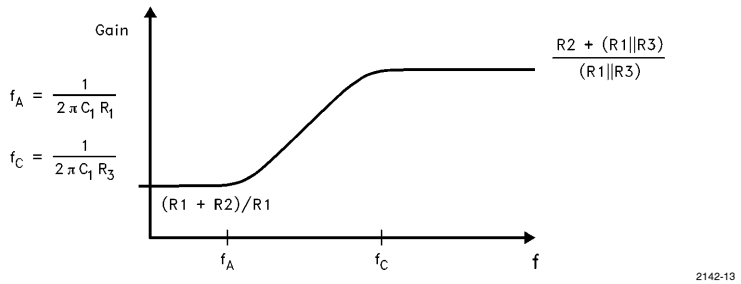


Figure 4. Compensated Line Receiver

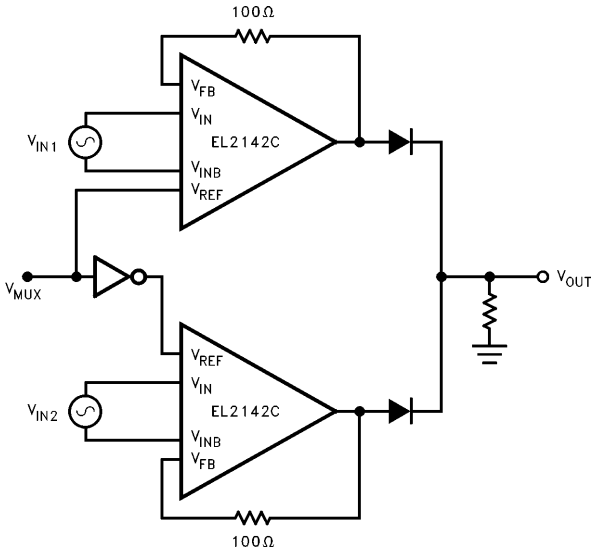


Figure 5. Two Channel Multiplexer

General Disclaimer

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Elantec, Inc.
1996 Tarob Court
Milpitas, CA 95035
Telephone: (408) 945-1323
(800) 333-6314
Fax: (408) 945-9305
European Office: 44-71-482-4596

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