Document Number: MC33887
Rev. 14.0, 3/2011

RoHS

5.0 A H-Bridge with Load Current Feedback

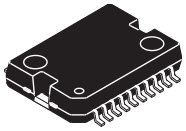
33887

H-BRIDGE

The 33887 is a monolithic H-Bridge Power IC with a load current feedback feature making it ideal for closed-loop DC motor control. The IC incorporates internal control logic, charge pump, gate drive, and low $R_{DS(ON)}$ MOSFET output circuitry. The 33887 is able to control inductive loads with continuous DC load currents up to 5.0 A, and with peak current active limiting between 5.2 A and 7.8 A. Output loads can be pulse width modulated (PWM-ed) at frequencies up to 10 kHz. The load current feedback feature provides a proportional (1/375th of the load current) constant-current output suitable for monitoring by a microcontroller's A/D input. This feature facilitates the design of closed-loop torque/speed control as well as open load detection.

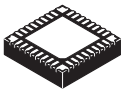
A Fault Status output pin reports undervoltage, short circuit, and overtemperature conditions. Two independent inputs provide polarity control of two half-bridge totem-pole outputs. Two disable inputs force the H-Bridge outputs to tri-state (exhibit high-impedance).

The 33887 is parametrically specified over a temperature range of -40°C ≤ T_A ≤ 125°C and a voltage range of 5.0 V ≤ V+ ≤ 28 V. Operation with voltages up to 40 V with derating of the specifications.

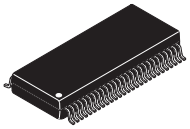


VW SUFFIX (Pb-FREE)
98ASH70702A
20-PIN HSOP

FK SUFFIX
98ASA10583D
36-PIN PQFN



Bottom View



EK SUFFIX (Pb-FREE)
98ASA10506D
54-PIN SOICW-EP

Features

- Fully specified operation 5.0 V to 28 V
- Limited operation with reduced performance up to 40 V
- 120 mΩ $R_{DS(ON)}$ Typical H-Bridge MOSFETs
- TTL/CMOS Compatible Inputs
- PWM Frequencies up to 10 kHz
- Active Current Limiting (Regulation)
- Fault Status Reporting
- Sleep Mode with Current Draw ≤50 μA (Inputs Floating or Set to Match Default Logic States)

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33887APVW/R2	-40°C to 125°C	20 HSOP
MC33887PFK/R2		36 PQFN
MC33887PEK/R2		54 SOICW-EP

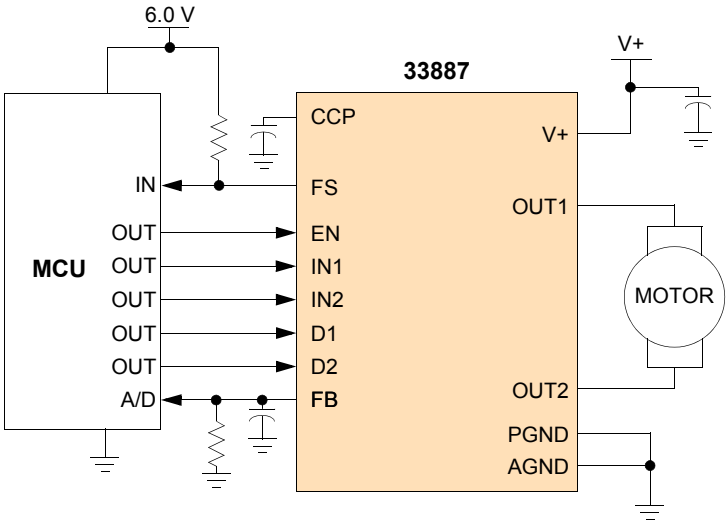


Figure 1. 33887 Simplified Application Diagram

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INTERNAL BLOCK DIAGRAM

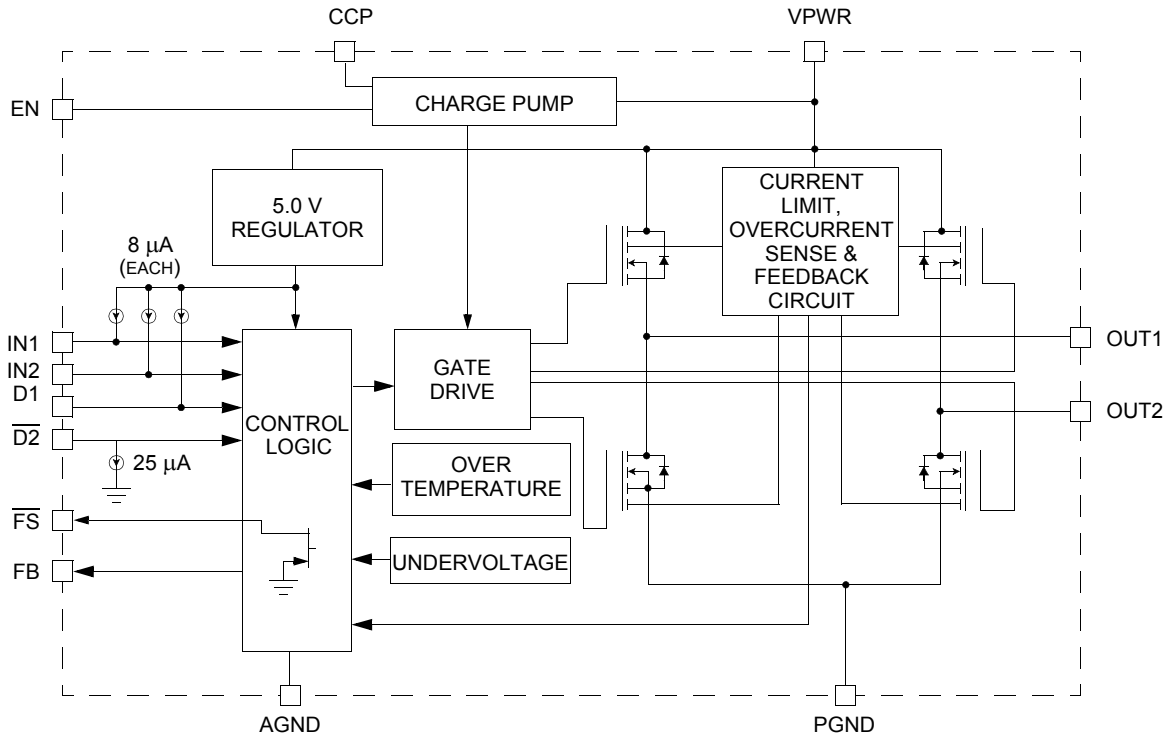


Figure 2. 33887 Simplified Internal Block Diagram

PIN CONNECTIONS

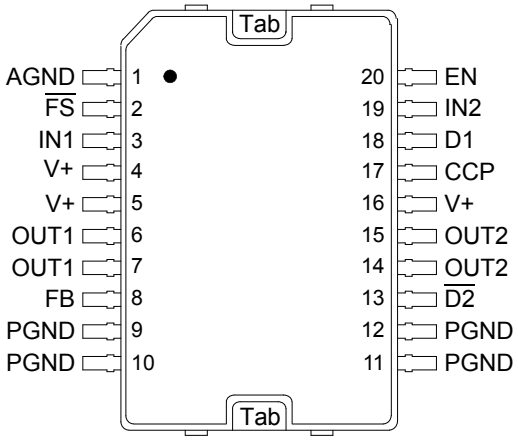


Figure 3. 33887 Pin Connections

Table 1. 33887 HSOP PIN DEFINITIONS

A functional description of each pin can be found in the Functional Pin DescriptionS section, page 21.

Pin	Pin Name	Formal Name	Definition
1	AGND	Analog Ground	Low-current analog signal ground.
2	$\overline{FS}$	Fault Status for H-Bridge	Open drain active LOW Fault Status output requiring a pull-up resistor to 5.0 V.
3	IN1	Logic Input Control 1	Logic input control of OUT1 (i.e., IN1 logic HIGH = OUT1 HIGH).
4, 5, 16	V+	Positive Power Supply	Positive supply connections
6, 7	OUT1	H-Bridge Output 1	Output 1 of H-Bridge.
8	FB	Feedback for H-Bridge	Current sensing feedback output providing ground referenced 1/375th (0.00266) of H-Bridge high-side current.
9–12	PGND	Power Ground	High-current power ground.
13	$\overline{D2}$	Disable 2	Active LOW input used to simultaneously tri-state disable both H-Bridge outputs. When $\overline{D2}$ is Logic LOW, both outputs are tri-stated.
14, 15	OUT2	H-Bridge Output 2	Output 2 of H-Bridge.
17	CCP	Charge Pump Capacitor	External reservoir capacitor connection for internal charge pump capacitor.
18	D1	Disable 1	Active HIGH input used to simultaneously tri-state disable both H-Bridge outputs. When D1 is Logic HIGH, both outputs are tri-stated.
19	IN2	Logic Input Control 2	Logic input control of OUT2 (i.e., IN2 logic HIGH = OUT2 HIGH).
20	EN	Enable	Logic input Enable control of device (i.e., EN logic HIGH = full operation, EN logic LOW = Sleep Mode).
Tab/Pad	Thermal Interface	Exposed Pad Thermal Interface	Exposed pad thermal interface for sinking heat from the device. **Note** Must be DC-coupled to analog ground and power ground via very low impedance path to prevent injection of spurious signals into IC substrate.

Transparent Top View of Package

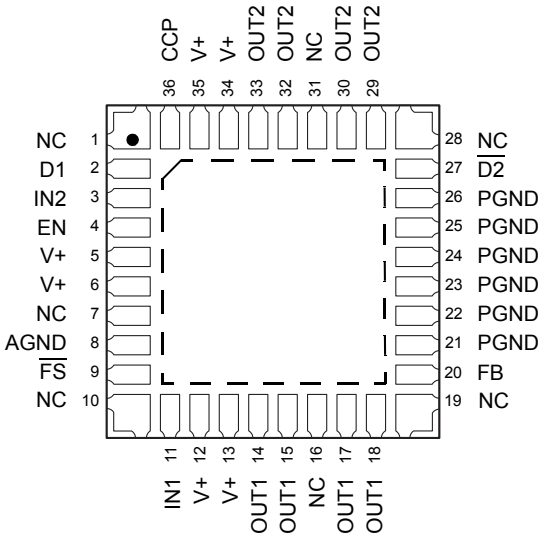


Figure 4. 33887 Pin Connections

Table 2. PQFN PIN DEFINITIONS

A functional description of each pin can be found in the Functional Pin DescriptionS section, page 21.

Pin	Pin Name	Formal Name	Definition
1, 7, 10, 16, 19, 28, 31	NC	No Connect	No internal connection to this pin.
2	D1	Disable 1	Active HIGH input used to simultaneously tri-state disable both H-Bridge outputs. When D1 is Logic HIGH, both outputs are tri-stated.
3	IN2	Logic Input Control 2	Logic input control of OUT2 (i.e., IN2 logic HIGH = OUT2 HIGH).
4	EN	Enable	Logic input Enable control of device (i.e., EN logic HIGH = full operation, EN logic LOW = Sleep Mode).
5, 6, 12, 13, 34, 35	V+	Positive Power Supply	Positive supply connections.
8	AGND	Analog Ground	Low-current analog signal ground.
9	$\overline{FS}$	Fault Status for H-Bridge	Open drain active LOW Fault Status output requiring a pull-up resistor to 5.0 V.
11	IN1	Logic Input Control 1	Logic input control of OUT1 (i.e., IN1 logic HIGH = OUT1 HIGH).
14, 15, 17, 18	OUT1	H-Bridge Output 1	Output 1 of H-Bridge.
20	FB	Feedback for H-Bridge	Current feedback output providing ground referenced 1/375th ratio of H-Bridge high-side current.
21–26	PGND	Power Ground	High-current power ground.
27	$\overline{D2}$	Disable 2	Active LOW input used to simultaneously tri-state disable both H-Bridge outputs. When $\overline{D2}$ is Logic LOW, both outputs are tri-stated.
29, 30, 32, 33	OUT2	H-Bridge Output 2	Output 2 of H-Bridge.
36	CCP	Charge Pump Capacitor	External reservoir capacitor connection for internal charge pump capacitor.
Pad	Thermal Interface	Exposed Pad Thermal Interface	Exposed pad thermal interface for sinking heat from the device. **Note:** Must be DC-coupled to analog ground and power ground via very low impedance path to prevent injection of spurious signals into IC substrate.

Transparent Top View of Package

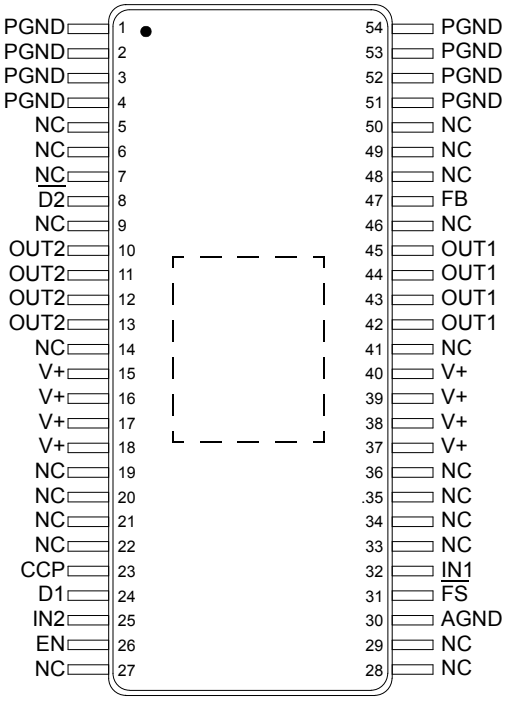


Figure 5. 33887 Pin Connections

Table 3. SOICW-EP PIN DEFINITIONS

A functional description of each pin can be found in the Functional Pin DescriptionS section, page 21.

Pin	Pin Name	Formal Name	Definition
1–4, 51–54	PGND	Power Ground	High-current power ground.
5–7, 9, 14, 19–22, 27–29, 33–36, 41, 46, 48–50	NC	No Connect	No internal connection to this pin.
8	$\overline{D2}$	Disable 2	Active LOW input used to simultaneously tri-state disable both H-Bridge outputs. When $\overline{D2}$ is Logic LOW, both outputs are tri-stated.
10–13	OUT2	H-Bridge Output 2	Output 2 of H-Bridge.
15–18, 37–40	V+	Positive Power Supply	Positive supply connections.
23	CCP	Charge Pump Capacitor	External reservoir capacitor connection for internal charge pump capacitor.
24	D1	Disable 1	Active HIGH input used to simultaneously tri-state disable both H-Bridge outputs. When D1 is Logic HIGH, both outputs are tri-stated.
25	IN2	Logic Input Control 2	Logic input control of OUT2 (i.e., IN2 logic HIGH = OUT2 HIGH).
26	EN	Enable	Logic input Enable control of device (i.e., EN logic HIGH = full operation, EN logic LOW = Sleep Mode).
30	AGND	Analog Ground	Low-current analog signal ground.
31	$\overline{FS}$	Fault Status for H-Bridge	Open drain active LOW Fault Status output requiring a pull-up resistor to 5.0 V.
32	IN1	Logic Input Control 1	Logic input control of OUT1 (i.e., IN1 logic HIGH = OUT1 HIGH).

Table 3. SOICW-EP PIN DEFINITIONS

A functional description of each pin can be found in the Functional Pin DescriptionS section, page 21.

Pin	Pin Name	Formal Name	Definition
42–45	OUT1	H-Bridge Output 1	Output 1 of H-Bridge.
47	FB	Feedback for H-Bridge	Current feedback output providing ground referenced 1/375th ratio of H-Bridge high-side current.
Pad	Thermal Interface	Exposed Pad Thermal Interface	Exposed pad thermal interface for sinking heat from the device. **Note** Must be DC-coupled to analog ground and power ground via very low impedance path to prevent injection of spurious signals into IC substrate.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltage [1]	V+	-0.3 to 40	V
Input Voltage [2]	V_{IN}	-0.3 to 7.0	V
$\overline{FS}$ Status Output [3]	$V_{\overline{FS}}$	-0.3 to 7.0	V
Continuous Current [4]	I_{OUT}	5.0	A
DH Suffix HSOP ESD Voltage [5]			V
Human Body Model			
Each Pin to AGND	V_{ESD1}	±1000	
Each Pin to PGND	V_{ESD1}	±1500	
Each Pin to V+	V_{ESD1}	±2000	
Each I/O to All Other I/Os	V_{ESD1}	±2000	
Machine Model	V_{ESD2}	±200	
VW Suffix HSOP, SOICW-EP, and PQFN ESD Voltage [5]			V
Human Body Model	V_{ESD1}	±2000	
Machine Model	V_{ESD2}	±200	
THERMAL RATINGS			
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature [6]			°C
Ambient	T_A	-40 to 125	
Junction	T_J	-40 to 150	
Peak Package Reflow Temperature During Reflow [7], [8]	T_{PPRT}	Note 8.	°C

Notes

1. Performance at voltages greater than 28V is degraded.See Electrical Performance Curves on page 18 and 19 for typical performance. Extended operation at higher voltages has not been fully characterized and may reduce the operational lifetime.
2. Exceeding the input voltage on IN1, IN2, EN, D1, or $\overline{D2}$ may cause a malfunction or permanent damage to the device.
3. Exceeding the pull-up resistor voltage on the open Drain $\overline{FS}$ pin may cause permanent damage to the device.
4. Continuous current capability so long as junction temperature is ≤ 150°C.
5. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
6. The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking provided. Brief nonrepetitive excursions of junction temperature above 150°C can be tolerated as long as duration does not exceed 30 seconds maximum. (nonrepetitive events are defined as not occurring more than once in 24 hours.)
7. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
8. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

MAXIMUM RATINGS (continued)

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
THERMAL RESISTANCE (AND PACKAGE DISSIPATION) RATINGS [9], [10], [11], [12]			
Junction-to-Board (Bottom Exposed Pad Soldered to Board)	$R_{\theta JB}$		°C/W
HSOP (6.0 W)		~7.0	
PQFN (4.0 W)		~8.0	
SOICW-EP (2.0 W)		~9.0	
Junction-to-Ambient, Natural Convection, Single-Layer Board (1s) [13]	$R_{\theta JA}$		°C/W
HSOP (6.0 W)			
PQFN (4.0 W)		~41	
SOICW-EP (2.0 W)		~50	
		~62	
Junction-to-Ambient, Natural Convection, Four-Layer Board (2s2p) [14]	$R_{\theta JMA}$		°C/W
HSOP (6.0 W)		~18	
PQFN (4.0 W)		~21	
SOICW-EP (2.0 W)		~23	
Junction-to-Case (Exposed Pad) [15]	$R_{\theta JC}$		°C/W
HSOP (6.0 W)		~0.8	
PQFN (4.0 W)		~1.2	
SOICW-EP (2.0 W)		~2.0	

Notes

9 The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking.

10 Exposed heatsink pad plus the power and ground pins comprise the main heat conduction paths. The actual $R_{\theta JB}$ (junction-to-PC board) values will vary depending on solder thickness and composition and copper trace thickness. Maximum current at maximum die temperature represents ~16 W of conduction loss heating in the diagonal pair of output MOSFETs. Therefore, the $R_{\theta JC}$-total must be less than 5.0 °C/W for maximum load at 70°C ambient. Module thermal design must be planned accordingly.

11 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

12 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

13 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

14 Per JEDEC JESD51-6 with the board horizontal.

15 Indicates the maximum thermal resistance between the die and the exposed pad surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

STATIC ELECTRICAL CHARACTERISTICS

Table 4. STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 5.0 V ≤ V+ ≤ 28 V and -40°C ≤ T_A ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Voltage Range (16)	V+	5.0	–	28	V
Sleep State Supply Current (17) I_{OUT} = 0 A, V_{EN} = 0 V	$I_{Q(SLEEP)}$	–	25	50	µA
Standby Supply Current I_{OUT} = 0 A, V_{EN} = 5.0 V	$I_{Q(STANDBY)}$	–	–	20	mA
Threshold Supply Voltage Switch-OFF Switch-ON Hysteresis	 $V+_{(THRES-OFF)}$ $V+_{(THRES-ON)}$ $V+_{(HYS)}$	 4.15 4.5 150	 4.4 4.75 –	 4.65 5.0 –	 V V mV
CHARGE PUMP					
Charge Pump Voltage V+ = 5.0 V 8.0 V ≤ V+ ≤ 28 V	V_{CP} - V+	 3.35 –	 – –	 – 20	V
CONTROL INPUTS					
Input Voltage (IN1, IN2, D1, $\overline{D2}$) Threshold HIGH Threshold LOW Hysteresis	 V_{IH} V_{IL} V_{HYS}	 3.5 – 0.7	 – – 1.0	 – 1.4 –	V
Input Current (IN1, IN2, D1) V_{IN} - 0.0 V	I_{INP}	-200	-80	–	µA
Input Current ($\overline{D2}$, EN) $V_{\overline{D2}}$ = 5.0 V	I_{INP}	–	25	100	µA

Notes

16 Specifications are characterized over the range of 5.0 V ≤ V+ ≤ 28 V. See See Electrical Performance Curves on page 18 and 19 and the See Functional Description on page 21 for information about operation outside of this range.

17 $I_{Q(sleep)}$ is with sleep mode function enabled.

Table 4. STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 5.0 V ≤ V+ ≤ 28 V and -40°C ≤ T_A ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLY					
POWER OUTPUTS (OUT1, OUT2)					
Output ON-Resistance (18)	$R_{DS(ON)}$				mΩ
5.0 V ≤ V+ ≤ 28 V, T_J = 25°C		–	120	–	
8.0 V ≤ V+ ≤ 28 V, T_J = 150°C		–	–	225	
5.0 V ≤ V+ ≤ 8.0 V, T_J = 150°C		–	–	300	
Active Current Limiting Threshold (via Internal Constant OFF-Time PWM) on Low-Side MOSFETs (19)	I_{LIM}	5.2	6.5	7.8	A
High-Side Short Circuit Detection Threshold	I_{SCH}	11	–	–	A
Low-Side Short Circuit Detection Threshold	I_{SCL}	8.0	–	–	A
Leakage Current (20)	$I_{OUT(LEAK)}$				µA
V_{OUT} = V+		–	100	200	
V_{OUT} = Ground		–	30	60	
Output MOSFET Body Diode Forward Voltage Drop	V_F				V
I_{OUT} = 3.0 A		–	–	2.0	
Overtemperature Shutdown					°C
Thermal Limit	T_{LIM}	175	–	225	
Hysteresis	T_{HYS}	10	–	30	
HIGH-SIDE CURRENT SENSE FEEDBACK					
Feedback Current	I_{FB}				
I_{OUT} = 0 mA		–	–	600	µA
I_{OUT} = 500 mA		1.07	1.33	1.68	mA
I_{OUT} = 1.5 A		3.6	4.0	4.62	mA
I_{OUT} = 3.0 A		7.2	8.0	9.24	mA
I_{OUT} = 6.0 A		14.4	16	18.48	mA
FAULT STATUS (21)					
Fault Status Leakage Current (22)	$I_{\overline{FS}(LEAK)}$				µA
$V_{\overline{FS}}$ = 5.0 V		–	–	10	
Fault Status SET Voltage (23)	$V_{\overline{FS}(LOW)}$				V
$I_{\overline{FS}}$ = 300 µA		–	–	1.0	

Notes
18 Output-ON resistance as measured from output to V+ and ground.
19 Active current limitation applies only for the low-side MOSFETs.
20 Outputs switched OFF with D1 or $\overline{D2}$.
21 Fault Status output is an open Drain output requiring a pull-up resistor to 5.0 V.
22 Fault Status Leakage Current is measured with Fault Status HIGH and *not* SET.
23 Fault Status Set Voltage is measured with Fault Status LOW and SET with $I_{\overline{FS}}$ = 300 µA.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 5.0 V ≤ V+ ≤ 28 V and -40°C ≤ T_A ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
TIMING CHARACTERISTICS					
PWM Frequency [24]	f_{PWM}	–	10	–	kHz
Maximum Switching Frequency During Active Current Limiting [25]	f_{MAX}	–	–	20	kHz
Output ON Delay [26] V+ = 14 V	$t_{D(ON)}$	– –	– –	18 18	µs
Output OFF Delay [26] V+ = 14 V	$t_{D(OFF)}$	– –	– –	18 18	µs
I_{LIM} Output Constant-OFF Time for Low-Side MOSFETs [27], [28]	t_A	15	20.5	26	µs
I_{LIM} Blanking Time for Low-Side MOSFETs [29], [28]	t_B	12	16.5	21	µs
Output Rise and Fall Time [30] V+ = 14 V, I_{OUT} = 3.0 A	t_F, t_R	2.0	5.0	8.0	µs
Disable Delay Time [31]	$t_{D(DISABLE)}$	–	–	8.0	µs
Power-ON Delay Time [32]	t_{POD}	–	1.0	5.0	ms
Wake-Up Delay Time [32]	t_{WUD}	–	1.0	5.0	ms
Output MOSFET Body Diode Reverse Recovery Time [33]	t_{RR}	100	–	–	ns

Notes

24 The outputs can be PWM-controlled from an external source. This is typically done by holding one input high while applying a PWM pulse train to the other input. The maximum PWM frequency obtainable is a compromise between switching losses and switching frequency. See Typical Switching Waveforms, Figures 12 through 19, pp. 14–17.

25 The Maximum Switching Frequency during active current limiting is internally implemented. The internal current limit circuitry produces a constant-OFF-time pulse-width modulation of the output current. The output load's inductance, capacitance, and resistance characteristics affect the total switching period (OFF-time + ON-time) and thus the PWM frequency during current limit.

26 Output Delay is the time duration from the midpoint of the IN1 or IN2 input signal to the 10% or 90% point (dependent on the transition direction) of the OUT1 or OUT2 signal. If the output is transitioning HIGH-to-LOW, the delay is from the midpoint of the input signal to the 90% point of the output response signal. If the output is transitioning LOW-to-HIGH, the delay is from the midpoint of the input signal to the 10% point of the output response signal. See Figure 6, page 12.

27 I_{LIM} Output Constant-OFF Time is the time during which the internal constant-OFF time PWM current regulation circuit has tri-stated the output bridge.

28 Load currents ramping up to the current regulation threshold become limited at the I_{LIM} value. The short circuit currents possess a di/dt that ramps up to the I_{SCH} or I_{SCL} threshold during the I_{LIM} blanking time, registering as a short circuit event detection and causing the shutdown circuitry to force the output into an immediate tri-state latch-OFF. See Figures 10 and 11, page 13. Operation in Current Limit mode may cause junction temperatures to rise. Junction temperatures above ~160°C will cause the output current limit threshold to progressively "fold back", or decrease with temperature, until ~175°C is reached, after which the T_{LIM} thermal latch-OFF will occur. Permissible operation within this fold-back region is limited to nonrepetitive transient events of duration not to exceed 30 seconds. See Figure 9, page 12.

29 I_{LIM} Blanking Time is the time during which the current regulation threshold is ignored so that the short-circuit detection threshold comparators my have time to act.

30 Rise Time is from the 10% to the 90% level and Fall Time is from the 90% to the 10% level of the output signal. See Figure 8, page 12.

31 Disable Delay Time is the time duration from the midpoint of the D (disable) input signal to 10% of the output tri-state response. See Figure 7, page 12.

32 Parameter has been characterized but not production tested.

33 Parameter is guaranteed by design but not production tested.

TIMING DIAGRAMS

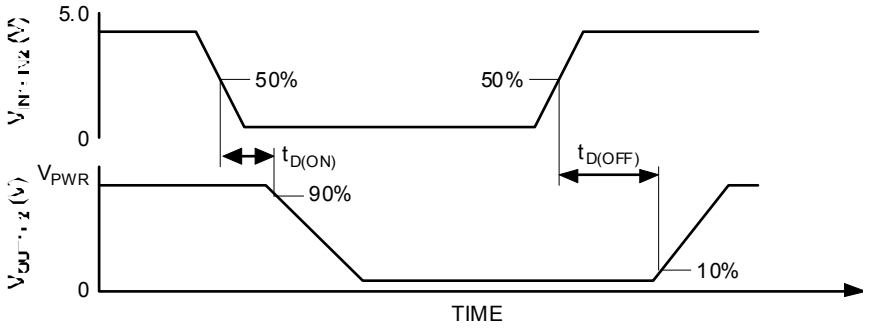


Figure 6. Output Delay Time

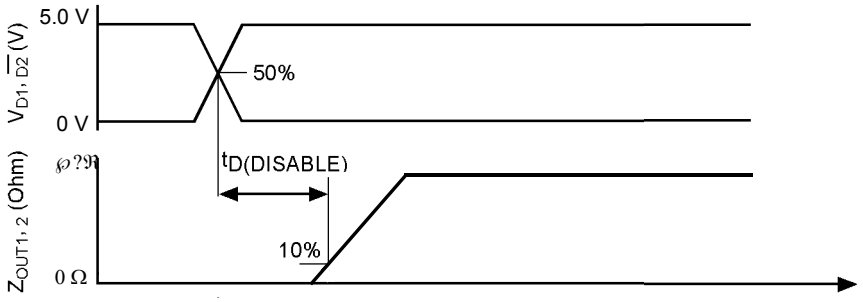


Figure 7. Disable Delay Time

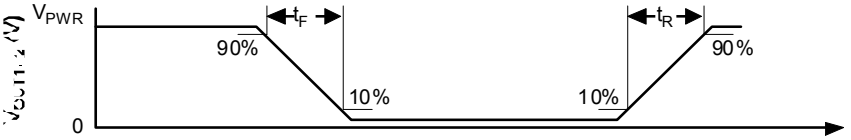


Figure 8. Output Switching Time

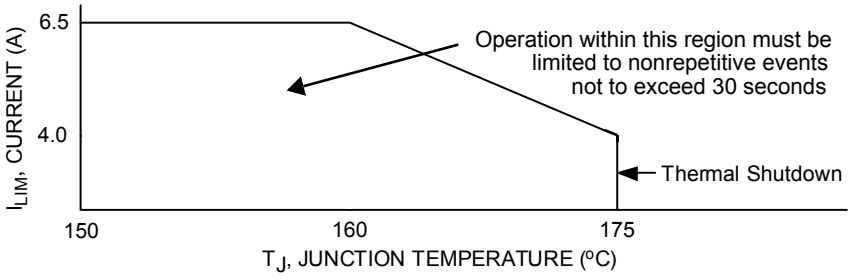


Figure 9. Active Current Limiting Versus Temperature (Typical)

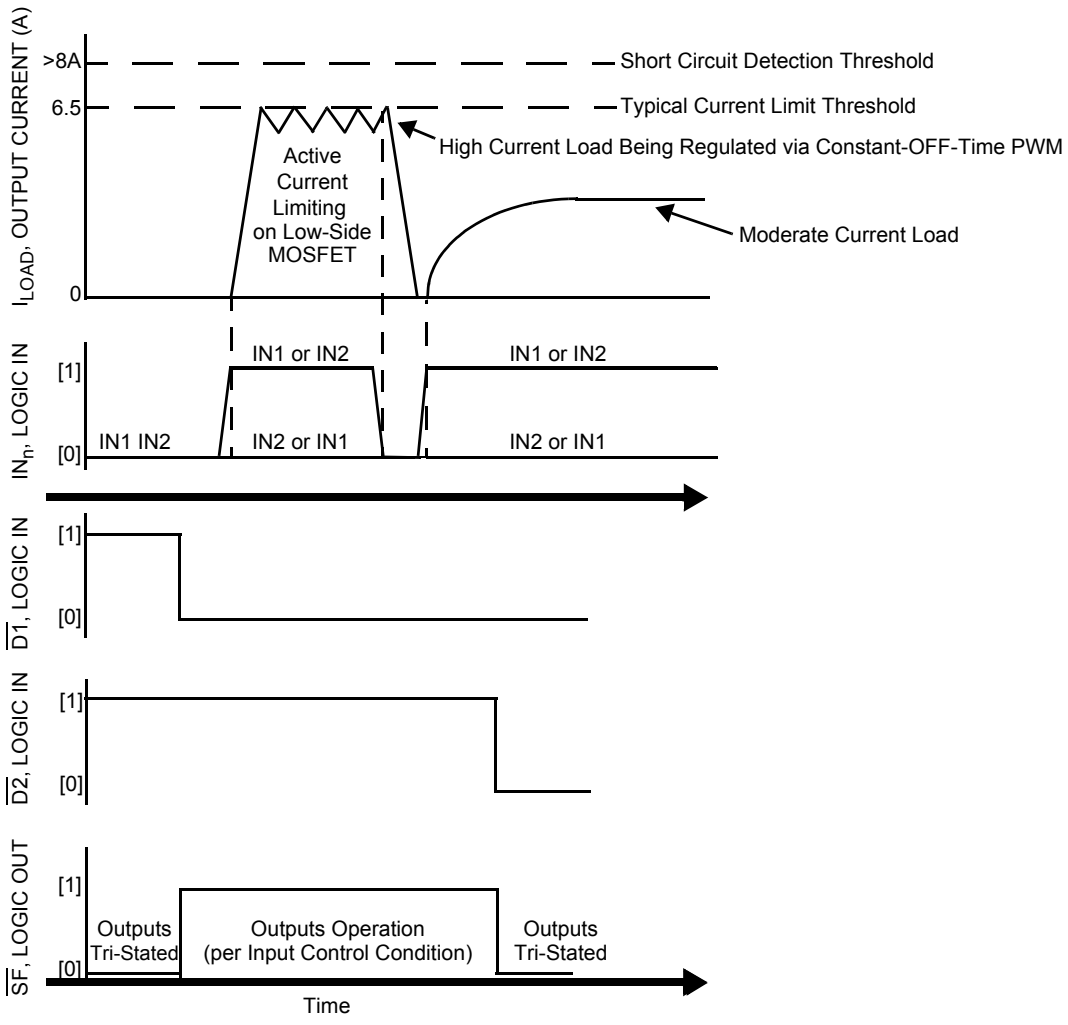


Figure 10. Operating States

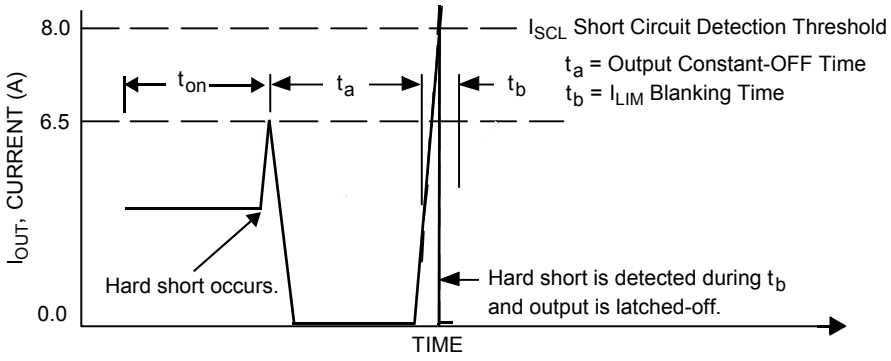


Figure 11. Example Short Circuit Detection Detail on Low-Side MOSFET

TYPICAL SWITCHING WAVEFORMS

Important For all plots, the following applies:

- Ch2=2.0 A per division
- L_{LOAD}=533 μH @ 1.0 kHz
- L_{LOAD}=530 μH @ 10.0 kHz
- R_{LOAD}=4.0 Ω

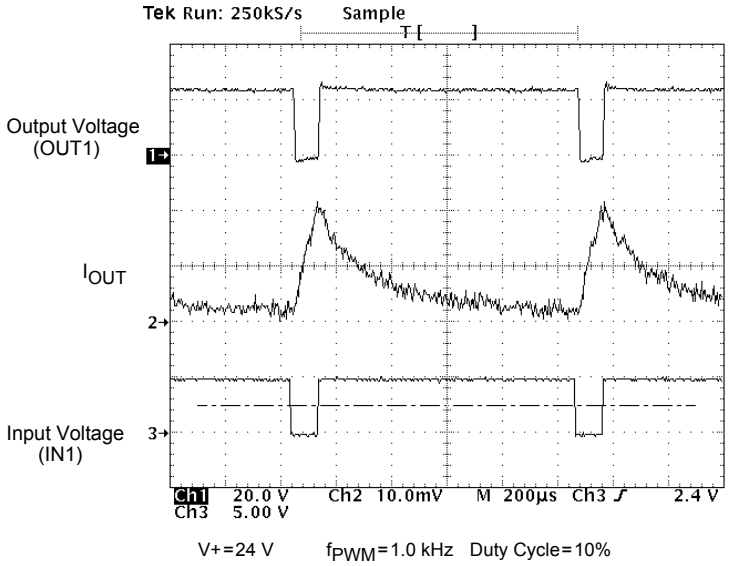


Figure 12. Output Voltage and Current vs. Input Voltage at V+ = 24 V, PMW Frequency of 1.0 kHz, and Duty Cycle of 10%

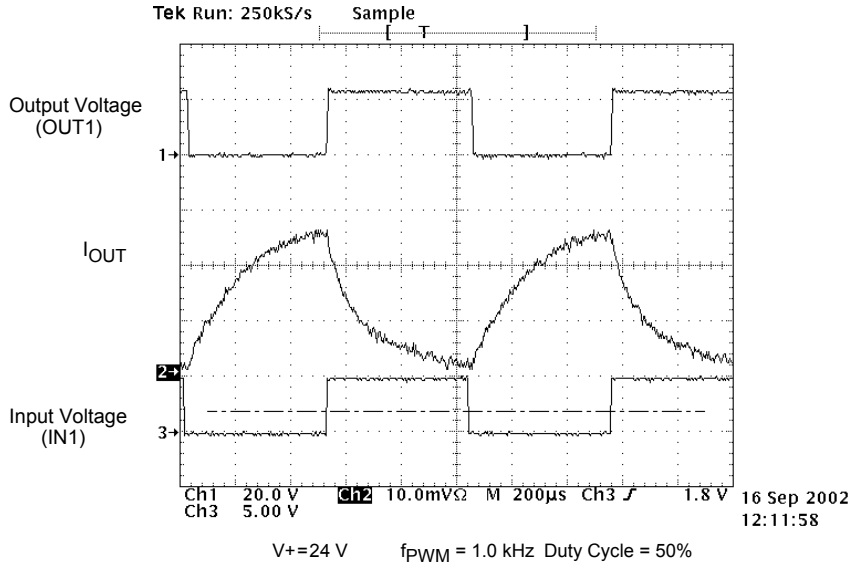


Figure 13. Output Voltage and Current vs. Input Voltage at V+ = 24 V, PMW Frequency of 1.0 kHz, and Duty Cycle of 50%

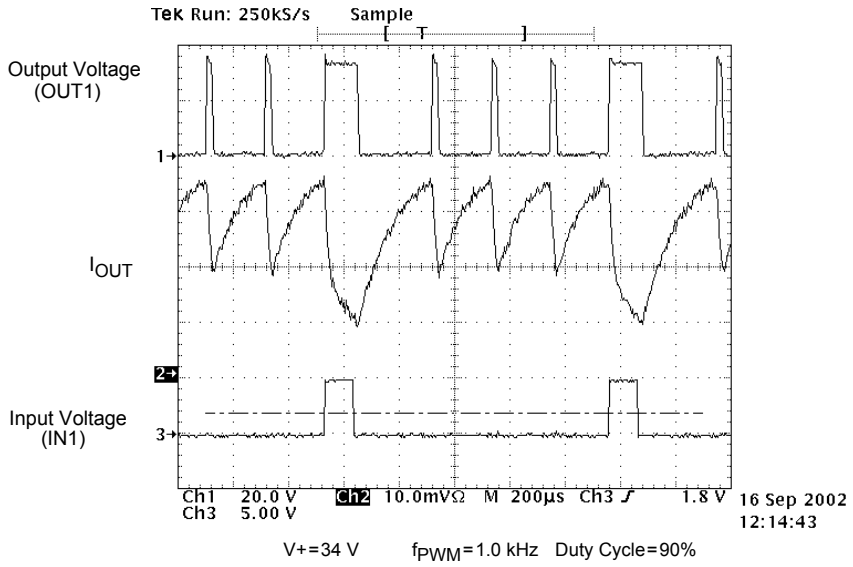


Figure 14. Output Voltage and Current vs. Input Voltage at V+ = 34 V, PMW Frequency of 1.0 kHz, and Duty Cycle of 90%, Showing Device in Current Limiting Mode

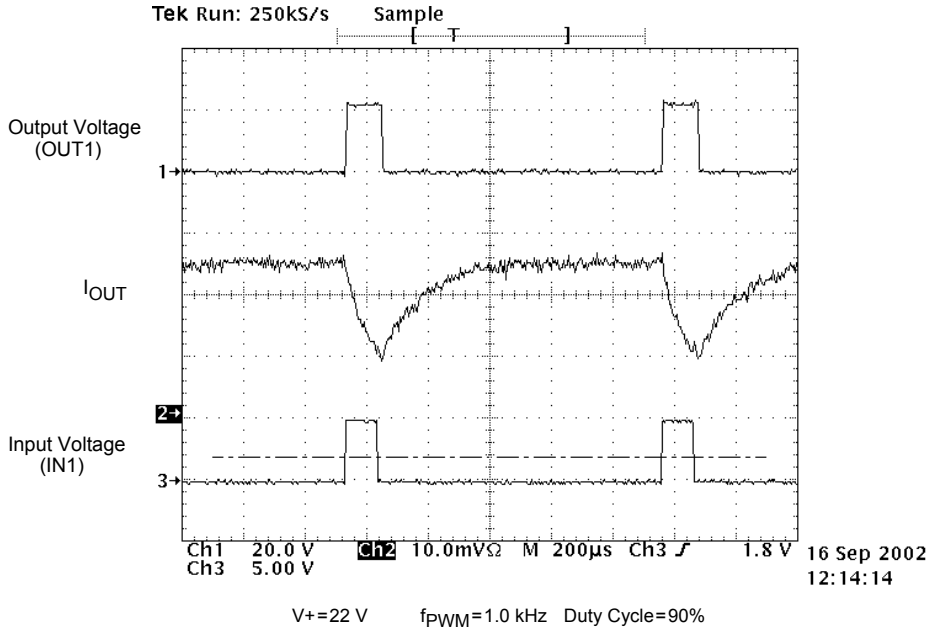


Figure 15. Output Voltage and Current vs. Input Voltage at V+ = 22 V, PMW Frequency of 1.0 kHz, and Duty Cycle of 90%

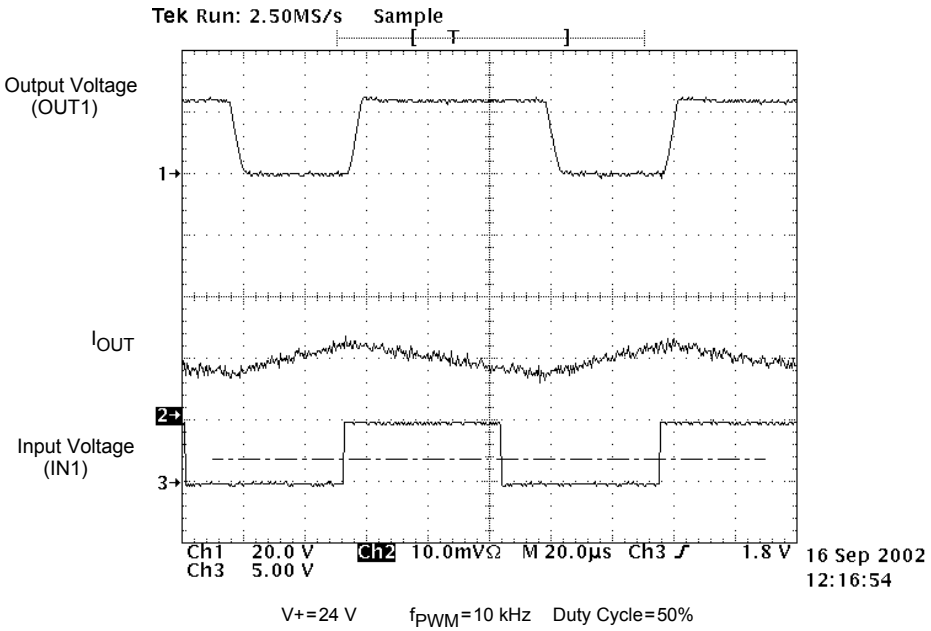


Figure 16. Output Voltage and Current vs. Input Voltage at V+ = 24 V, PMW Frequency of 10 kHz, and Duty Cycle of 50%

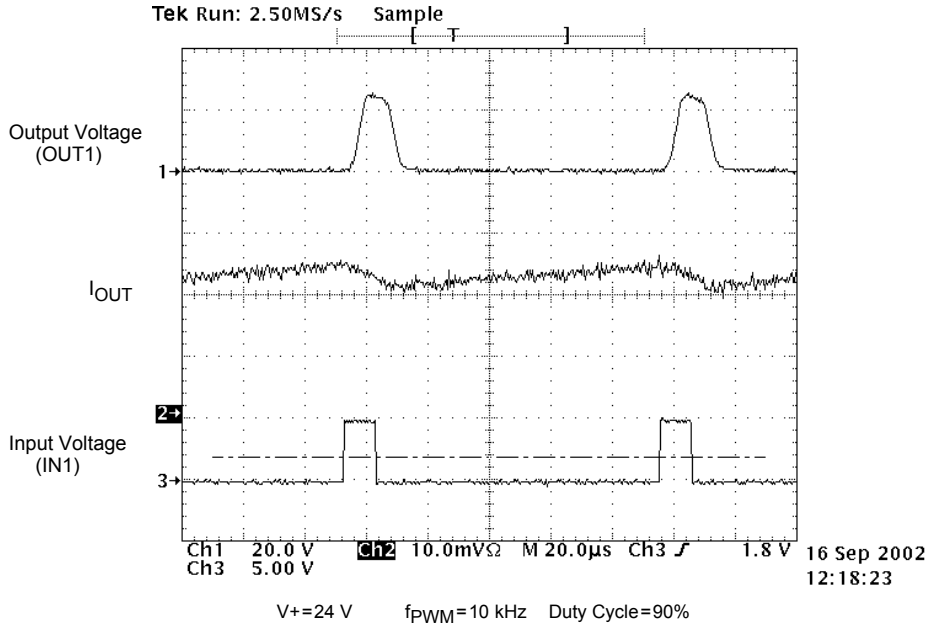


Figure 17. Output Voltage and Current vs. Input Voltage at V+ = 24 V, PMW Frequency of 10 kHz, and Duty Cycle of 90%

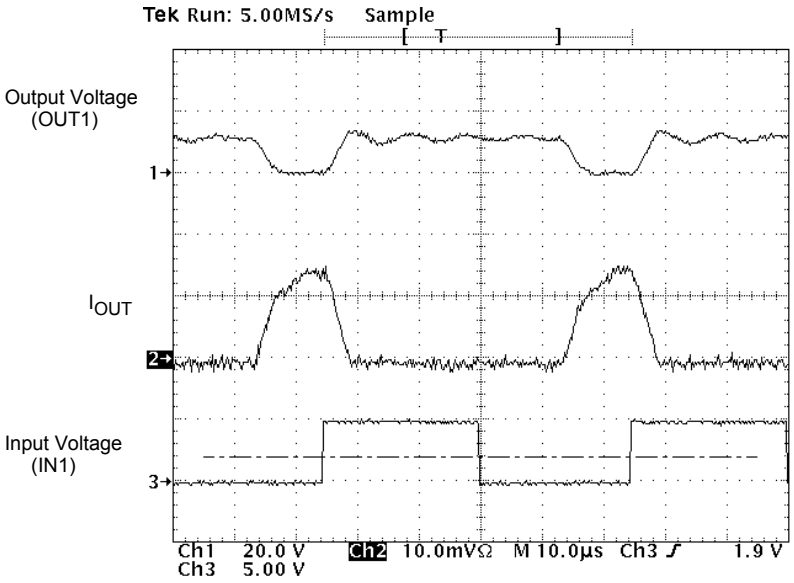


Figure 18. Output Voltage and Current vs. Input Voltage at V+ = 12 V, PMW Frequency of 20 kHz, and Duty Cycle of 50% for a Purely Resistive Load

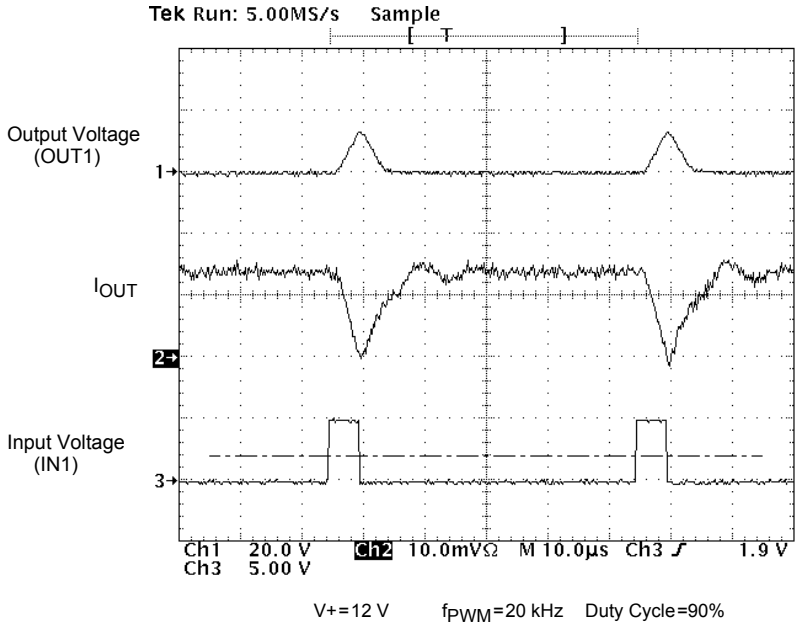


Figure 19. Output Voltage and Current vs. Input Voltage at V+ = 12 V, PMW Frequency of 20 kHz, and Duty Cycle of 90% for a Purely Resistive Load

ELECTRICAL PERFORMANCE CURVES

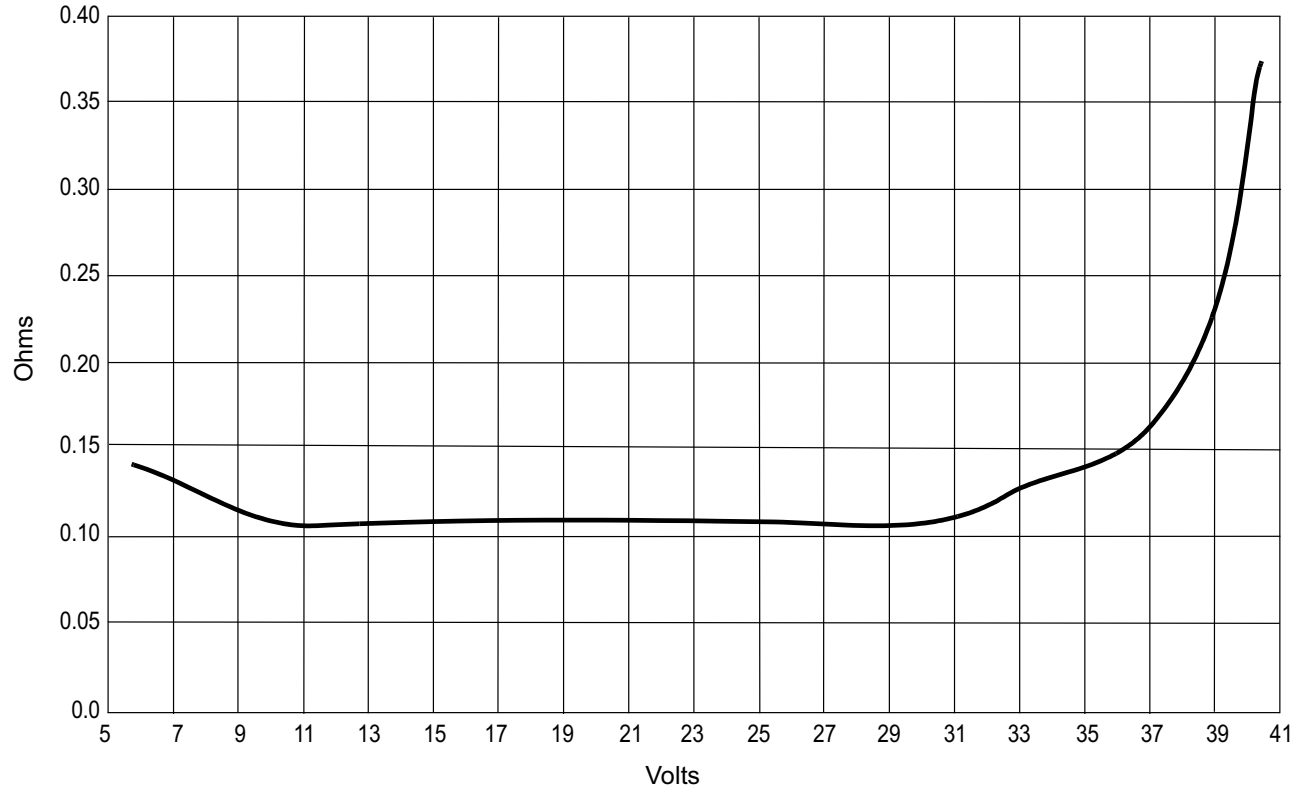


Figure 20. Typical High-Side $R_{DS(ON)}$ Versus V+

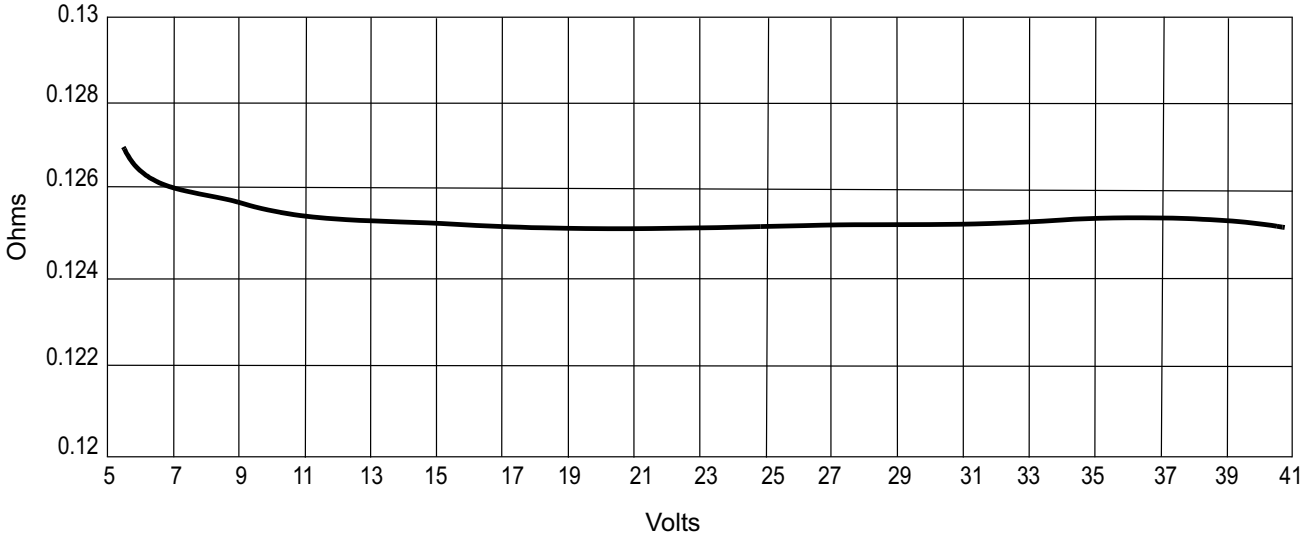


Figure 21. Typical Low-Side $R_{DS(ON)}$ Versus V+

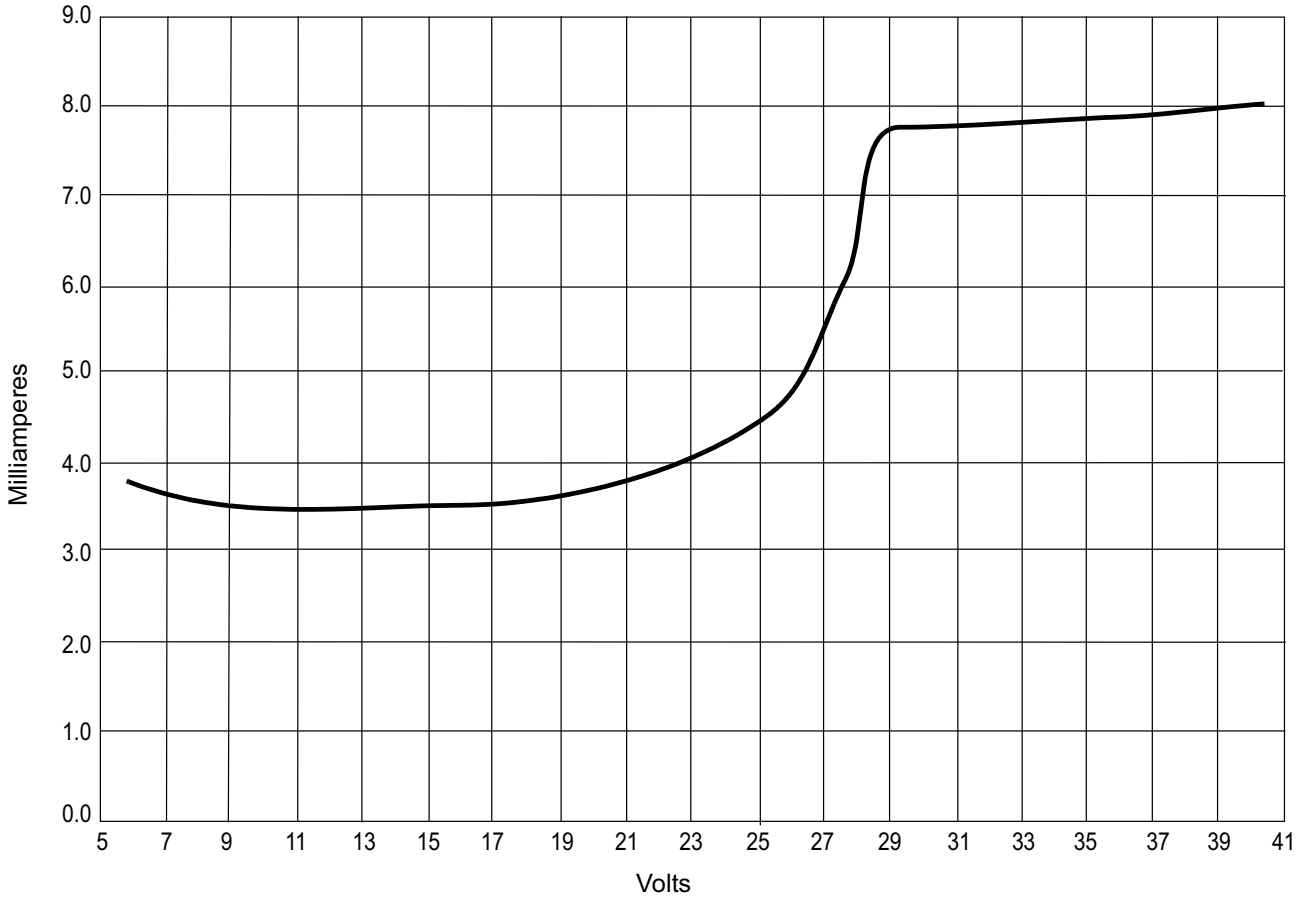


Figure 22. Typical Quiescent Supply Current Versus V+

Table 6. Truth Table

The tri-state conditions and the fault status are reset using D1 or $\overline{D2}$. The truth table uses the following notations: L = LOW, H = HIGH, X = HIGH or LOW, and Z = High impedance (all output power transistors are switched off).

Device State	**Input Conditions**					**Fault Status Flag**	**Output States**	
	EN	D1	$\overline{D2}$	IN1	IN2	$\overline{FS}$	OUT1	OUT2
Forward	H	L	H	H	L	H	H	L
Reverse	H	L	H	L	H	H	L	H
Freewheeling Low	H	L	H	L	L	H	L	L
Freewheeling High	H	L	H	H	H	H	H	H
Disable 1 (D1)	H	H	X	X	X	L	Z	Z
Disable 2 ($\overline{D2}$)	H	X	L	X	X	L	Z	Z
IN1 Disconnected	H	L	H	Z	X	H	H	X
IN2 Disconnected	H	L	H	X	Z	H	X	H
D1 Disconnected	H	Z	X	X	X	L	Z	Z
$\overline{D2}$ Disconnected	H	X	Z	X	X	L	Z	Z
Undervoltage (34)	H	X	X	X	X	L	Z	Z
Overtemperature (35)	H	X	X	X	X	L	Z	Z
Short Circuit (35)	H	X	X	X	X	L	Z	Z
Sleep Mode EN	L	X	X	X	X	H	Z	Z
EN Disconnected	Z	X	X	X	X	H	Z	Z

Notes

34 In the case of an undervoltage condition, the outputs tri-state and the fault status is SET logic LOW. Upon undervoltage recovery, fault status is reset automatically or automatically cleared and the outputs are restored to their original operating condition.

35 When a short circuit or overtemperature condition is detected, the power outputs are tri-state latched-OFF independent of the input signals and the fault status flag is SET logic LOW.

FUNCTIONAL DESCRIPTION

INTRODUCTION

Numerous protection and operational features (speed, torque, direction, dynamic braking, PWM control, and closed-loop control), in addition to the 5.0 A current capability, make the 33887 a very attractive, cost-effective solution for controlling a broad range of small DC motors. In addition, a pair of 33887 devices can be used to control bipolar stepper motors. The 33887 can also be used to excite transformer primary windings with a switched square wave to produce secondary winding AC currents.

FUNCTIONAL PIN DESCRIPTIONS

POWER GROUND AND ANALOG GROUND (PGND AND AGND)

Power and analog ground pins should be connected together with a very low impedance connection.

POSITIVE POWER SUPPLY (V+)

V+ pins are the power supply inputs to the device. All V+ pins must be connected together on the printed circuit board with as short as possible traces offering as low impedance as possible between pins.

V+ pins have an undervoltage threshold. If the supply voltage drops below a V+ undervoltage threshold, the output power stage switches to a tri-state condition and the fault status flag is SET and the Fault Status pin voltage switched to a logic LOW. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input pins and the fault status flag is automatically reset logic HIGH.

As V+ increases in value above 28 V, the charge pump performance begins to degrade. At +40 V, the charge pump is effectively non-functional. Operation at this high voltage level will result in the output FETs not being enhanced when turned on. This means that the voltage on the output will be $V_{OUT} = (V+) – V_{GS}$. This increased voltage drop under load will produce a higher power dissipation.

FAULT STATUS ($\overline{FS}$)

The $\overline{FS}$ pin is the device fault status output. This output is an active LOW open drain structure requiring a pull-up resistor to 5.0 V. Refer to Table 6, Truth Table, **page** 20**.**

LOGIC INPUT CONTROL AND DISABLE (IN1, IN2, D1, AND $\overline{D2}$)

These pins are input control pins used to control the outputs. These pins are 5.0 V CMOS-compatible inputs with hysteresis. The IN1 and IN2 independently control OUT1 and OUT2, respectively. D1 and $\overline{D2}$ are complementary inputs used to tri-state disable the H-Bridge outputs.

When either D1 or $\overline{D2}$ is SET (D1 = logic HIGH or $\overline{D2}$ = logic LOW) in the disable state, outputs OUT1 and OUT2 are both tri-state disabled; however, the rest of the circuitry is fully operational and the supply $I_{Q(standby)}$ current is reduced to a few milliamperes. Refer to Table 6, Truth Table**,** and STATIC ELECTRICAL CHARACTERISTICS table, page 9.

H-BRIDGE OUTPUT (OUT1 AND OUT2)

These pins are the outputs of the H-Bridge with integrated output MOSFET body diodes. The bridge output is controlled using the IN1, IN2, D1, and $\overline{D2}$ inputs. The low-side MOSFETs have active current limiting above the I_{LIM} threshold. The outputs also have thermal shutdown (tri-state latch-OFF) with hysteresis as well as short circuit latch-OFF protection.

A disable timer (time t_b) USED to detect currents that are higher than current limit is activated at each output activation to facilitate hard short detection (see Figure 11, page 13).

Charge Pump Capacitor (CCP)

A filter capacitor (up to 33 nF) can be connected from the charge pump output pin and PGND. The device can operate without the external capacitor, although the C_{CP} capacitor helps to reduce noise and allows the device to perform at maximum speed, timing, and PWM frequency.

ENABLE (EN)

The EN pin is used to place the device in a sleep mode so as to consume very low currents. When the EN pin voltage is a logic LOW state, the device is in the sleep mode. The device is enabled and fully operational when the EN pin voltage is logic HIGH. An internal pull-down resistor maintains the device in sleep mode in the event EN is driven through a high impedance I/O or an unpowered microcontroller, or the EN input becomes disconnected.

FEEDBACK FOR H-BRIDGE (FB)

The 33887 has a feedback output (FB) for “real time” monitoring of H-Bridge high-side current to facilitate closed-loop operation for motor speed and torque control.

The FB pin provides current sensing feedback of the H-Bridge high-side drivers. When running in forward or reverse direction, a ground referenced 1/375th (0.00266) of load current is output to this pin. Through an external resistor to ground, the proportional feedback current can be converted to a proportional voltage equivalent and the controlling microcontroller can “read” the current proportional

voltage with its analog-to-digital converter (ADC). This is intended to provide the user with motor current feedback for motor torque control. The resistance range for the linear operation of the FB pin is 100 $< R_{FB} <$ 200 Ω.

If PWM-ing is implemented using the disable pin inputs (either D1 or $\overline{D2}$), a small filter capacitor (1.0 μF or less) may be required in parallel with the external resistor to ground for fast spike suppression.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

The 33887 Simplified Internal Block Diagram shown in Figure 2, page 2, is a fully protected monolithic H-Bridge with Enable, Fault Status reporting, and High-Side current sense feedback to accommodate closed-loop PWM control. For a DC motor to run, the input conditions need be as follows: Enable input logic HIGH, D1 input logic LOW, $\overline{D2}$ input logic HIGH, $\overline{FS}$ flag cleared (logic HIGH), one IN logic LOW and the other IN logic HIGH (to define output polarity). The 33887 can execute dynamic braking by simultaneously turning on either both high-side MOSFETs or both low-side MOSFETs in the output H-Bridge; e.g., IN1 and IN2 logic HIGH or IN1 and IN2 logic LOW.

The 33887 outputs are capable of providing a continuous DC load current of 5.0 A from a 28 V V+ source. An internal charge pump supports PWM frequencies to 10 kHz. An external pull-up resistor is required at the $\overline{FS}$ pin for fault status reporting. The 33887 has an analog feedback (current mirror) output pin (the FB pin) that provides a constant-current source ratioed to the active high-side MOSFET. This can be used to provide “real time” monitoring of load current to facilitate closed-loop operation for motor speed/torque control.

Two independent inputs (IN1 and IN2) provide control of the two totem-pole half-bridge outputs. Two disable inputs (D1 and $\overline{D2}$) provide the means to force the H-Bridge outputs to a high-impedance state (all H-Bridge switches OFF). An EN pin controls an enable function that allows the 33887 to be placed in a power-conserving sleep mode.

The 33887 has undervoltage shutdown with automatic recovery, active current limiting, output short-circuit latch-OFF, and overtemperature latch-OFF. An undervoltage shutdown, output short-circuit latch-OFF, or overtemperature latch-OFF fault condition will cause the outputs to turn OFF (i.e., become high impedance or tri-stated) and the fault output flag to be set LOW. Either of the Disable inputs or V+ must be “toggled” to clear the fault flag.

Active current limiting is accomplished by a constant OFF-time PWM method employing active current limiting threshold triggering. The active current limiting scheme is unique in that it incorporates a junction temperature-dependent current limit threshold. This means the active current limiting threshold is “ramped down” as the junction temperature increases above 160°C, until at 175°C the current will have been decreased to about 4.0 A. Above 175°C, the overtemperature shutdown (latch-OFF) occurs. This combination of features allows the device to remain in operation for 30 seconds at junction temperatures above 150°C for nonrepetitive unexpected loads.

PROTECTION AND DIAGNOSTIC FEATURES

SHORT CIRCUIT PROTECTION

If an output short circuit condition is detected, the power outputs tri-state (latch-OFF) independent of the input (IN1 and IN2) states, and the fault status output flag is SET logic LOW. If the D1 input changes from logic HIGH to logic LOW, or if the $\overline{D2}$ input changes from logic LOW to logic HIGH, the output bridge will become operational again and the fault status flag will be reset (cleared) to a logic HIGH state.

The output stage will always switch into the mode defined by the input pins (IN1, IN2, D1, and $\overline{D2}$), provided the device junction temperature is within the specified operating temperature range.

ACTIVE CURRENT LIMITING

The maximum current flow under normal operating conditions is internally limited to I_{LIM} (5.2 A to 7.8 A). When the maximum current value is reached, the output stages are tri-stated for a fixed time (t_a) of 20 μs typical. Depending on the time constant associated with the load characteristics, the current decreases during the tri-state duration until the next output ON cycle occurs (see Figures 11 and 14, page 13 and page 15, respectively).

The current limiting threshold value is dependent upon the device junction temperature. When -40°C ≤ T_J ≤ 160°C, I_{LIM} is between 5.2 A to 7.8 A. When T_J exceeds 160°C, the I_{LIM} current decreases linearly down to 4.0 A typical at 175°C. Above 175°C the device overtemperature circuit detects T_{LIM} and overtemperature shutdown occurs (see Figure 9, page 12). This feature allows the device to remain operational for a longer time but at a regressing output performance level at junction temperatures above 160°C.

Output Avalanche Protection

An inductive fly-back event, namely when the outputs are suddenly disabled and V+ is lost, could result in electrical overstress of the drivers. To prevent this the V+ input to the 33887 should not exceed the maximum rating during a fly-back condition. This may be done with either a zener clamp and/or an appropriately valued input capacitor with sufficiently low ESR.

OVERTEMPERATURE SHUTDOWN AND HYSTERESIS

If an overtemperature condition occurs, the power outputs are tri-stated (latched-OFF) and the fault status flag is SET to logic LOW.

To reset from this condition, D1 must change from logic HIGH to logic LOW, or $\overline{D2}$ must change from logic LOW to logic HIGH. When reset, the output stage switches ON again, provided that the junction temperature is now below the overtemperature threshold limit minus the hysteresis.

Note Resetting from the fault condition will clear the fault status flag.

TYPICAL APPLICATIONS

Figure 23 shows a typical application schematic. For precision high-current applications in harsh, noisy environments, the V+ by-pass capacitor may need to be substantially larger.

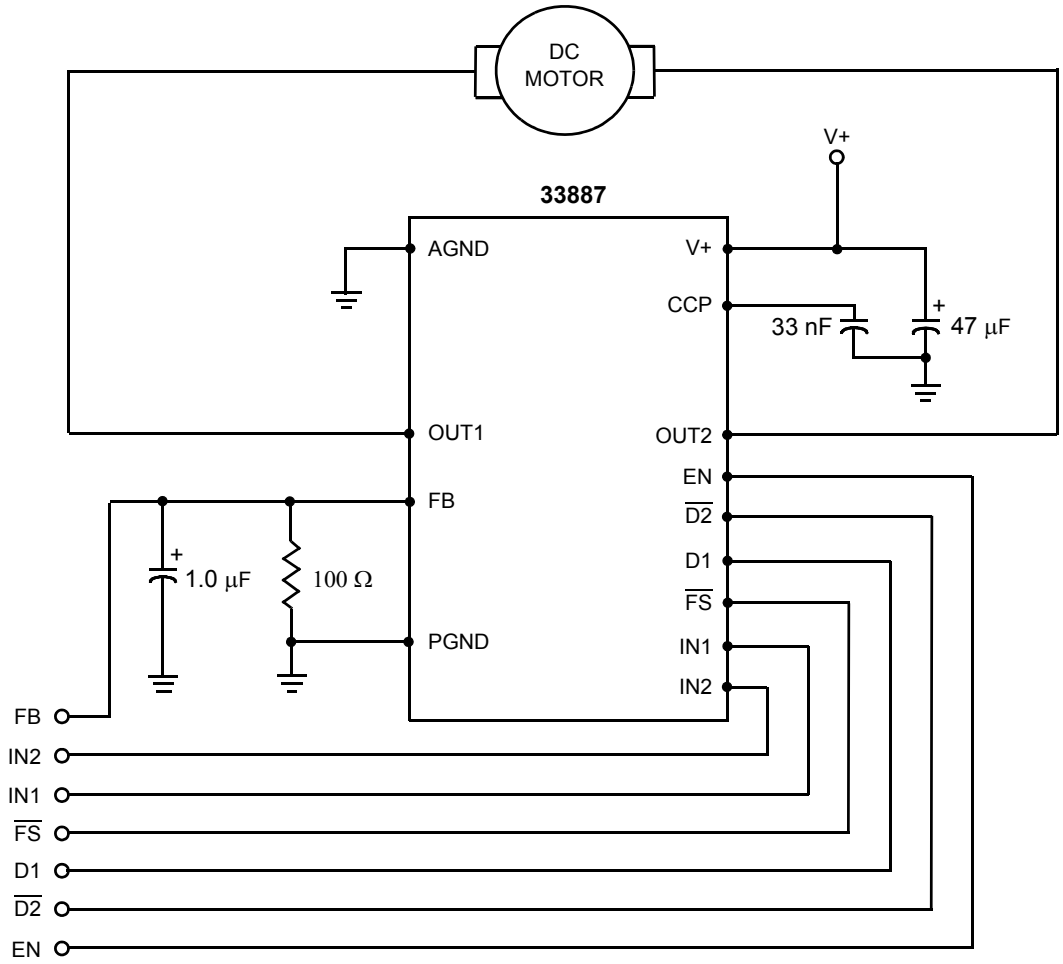


Figure 23. 33887 Typical Application Schematic

PACKAGING

SOLDERING INFORMATION

The 33887 packages are designed for thermal performance. The significant feature of these packages is the exposed pad on which the power die is soldered. When soldered to a PCB, this pad provides a path for heat flow to the ambient environment. The more copper area and thickness on the PCB, the better the power dissipation and transient behavior will be.

Example Characterization on a double-sided PCB: bottom side area of copper is 7.8 cm^2; top surface is 2.7 cm^2 (see Figure); grid array of 24 vias 0.3 mm in diameter

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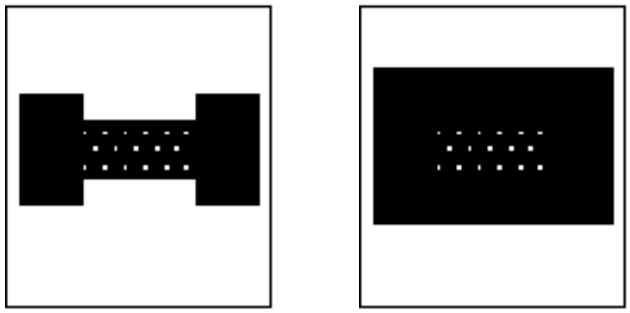
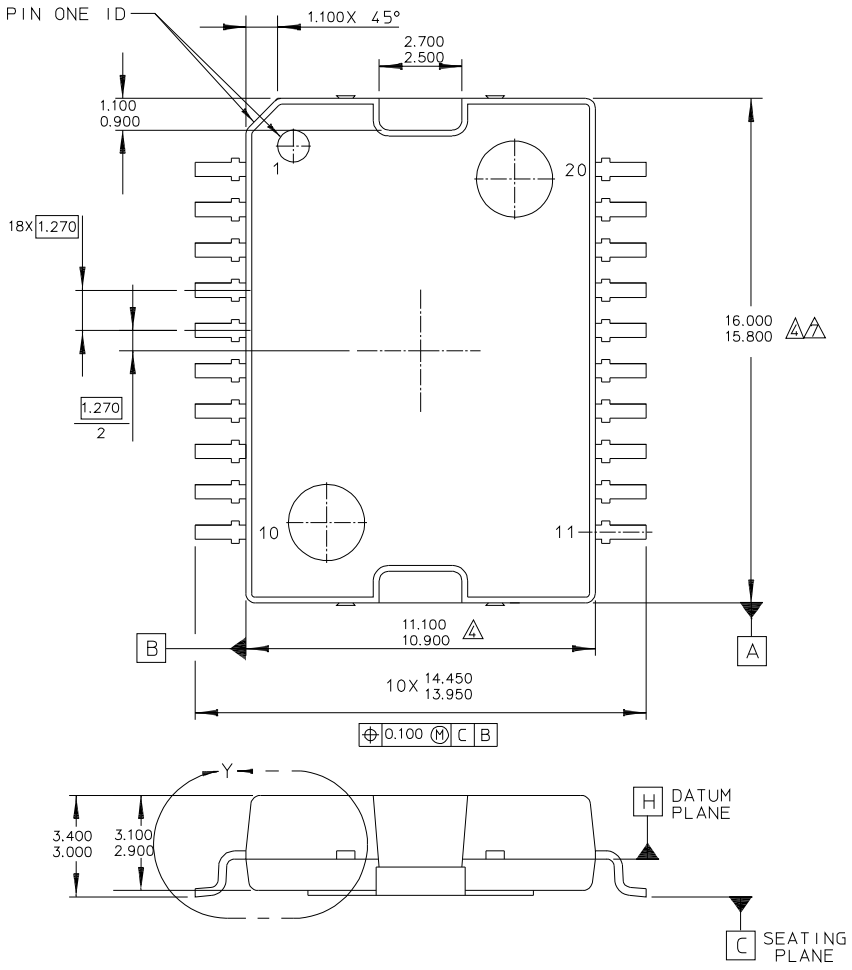


Figure 24. PCB Test Layout

PACKAGING DIMENSIONS

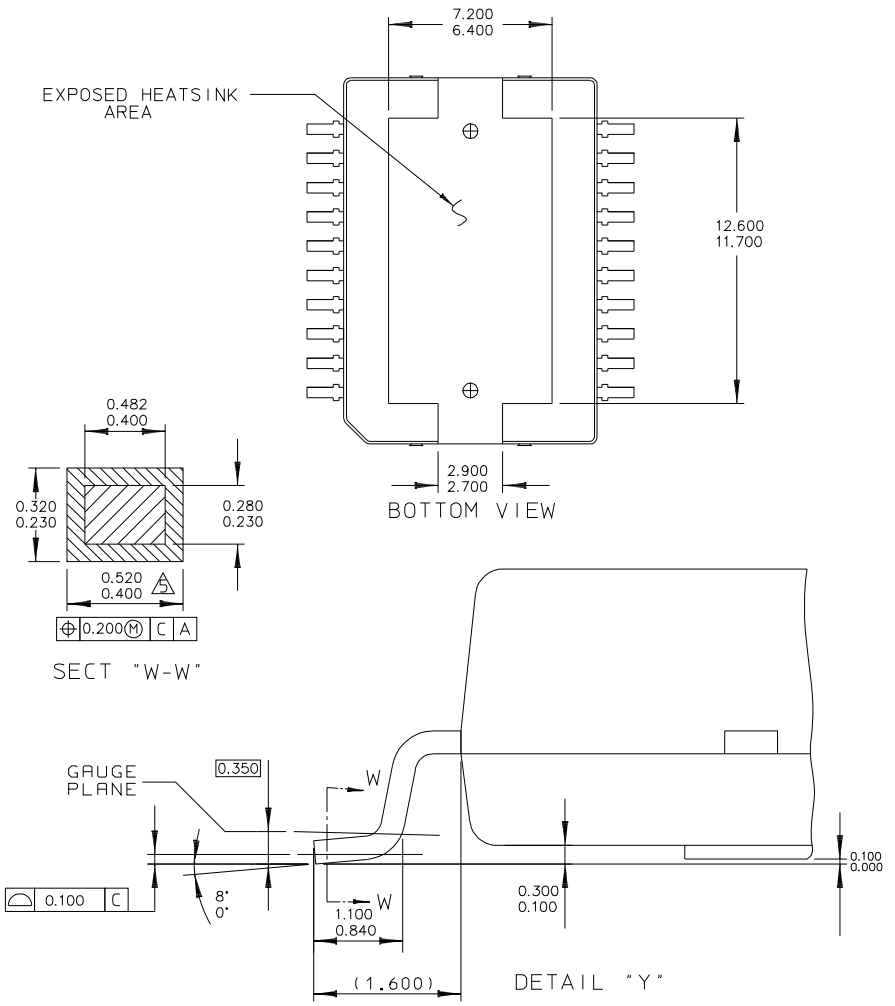
Important For the most current revision of the package, visit www.freescale.com and perform a keyword search on the 98A drawing number below



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TITLE: 20 LEAD HSOP W/PROTRUDING HEATSINK	DOCUMENT NO: 98ASH70702A	REV: B	
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	STANDARD: NON-JEDEC		

VW SUFFIX
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98ASH70702A
ISSUE B

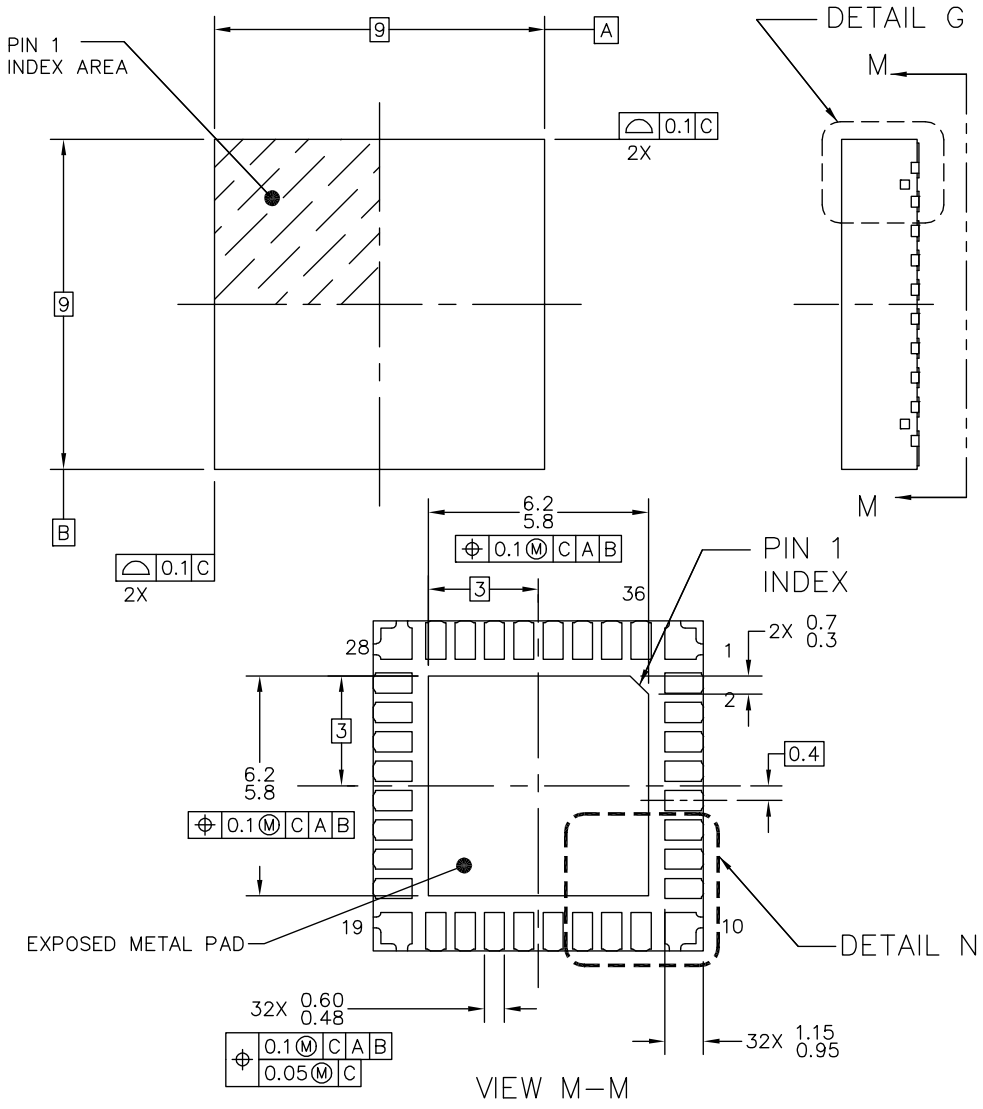
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ISSUE B

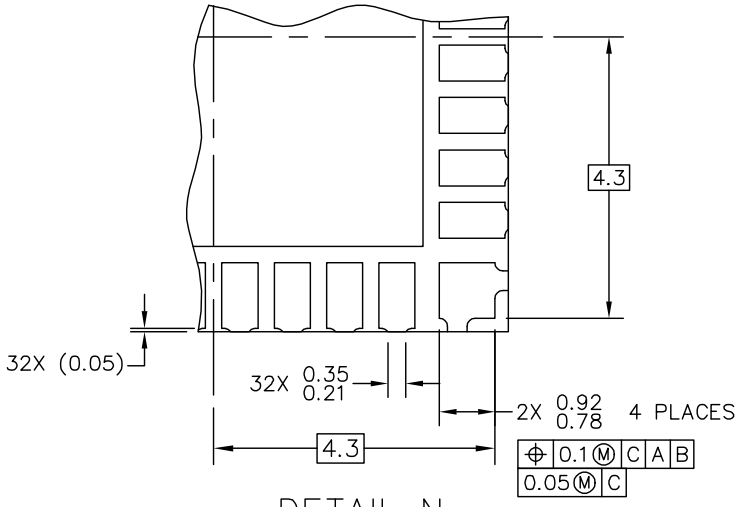
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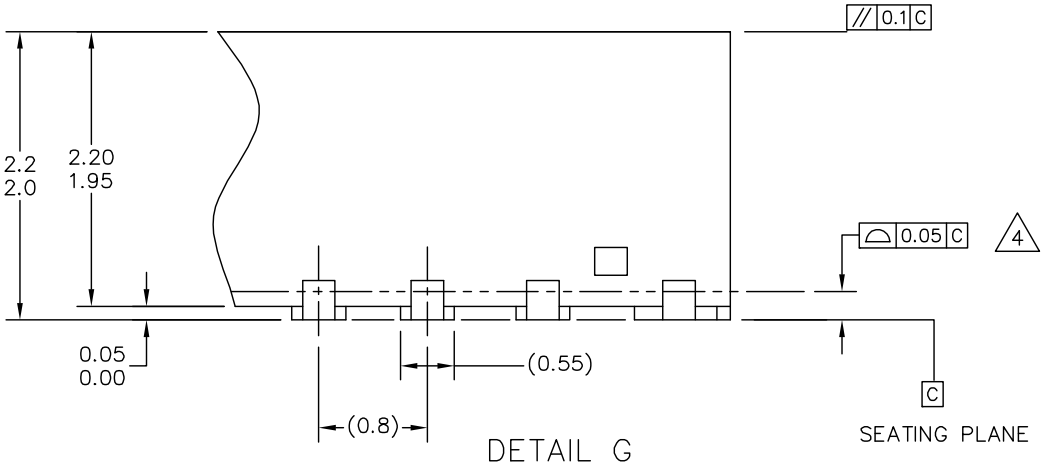
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	CASE NUMBER: 1503–04	14 JUL 2005
	STANDARD: JEDEC MO–251A AEEB–1	

FK (Pb-FREE) SUFFIX
36-PIN PQFN
98ASA10583D
ISSUE C

33887



DETAIL N
CORNER CONFIGURATION



DETAIL G
VIEW ROTATED 90° CW
SEATING PLANE

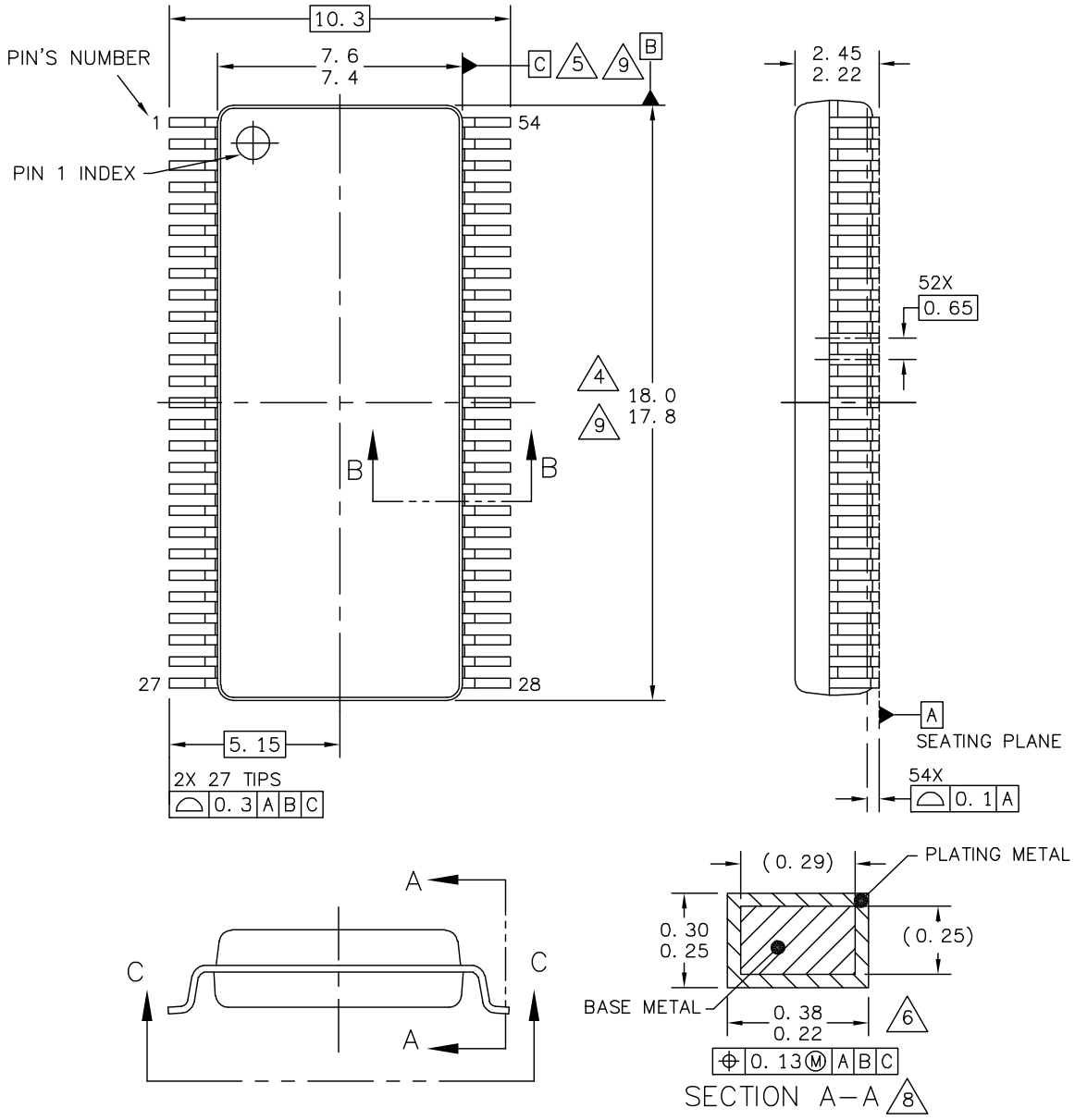
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	CASE NUMBER: 1503–04	14 JUL 2005
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FK (Pb-FREE) SUFFIX
36-PIN PQFN
98ASA10583D
ISSUE C

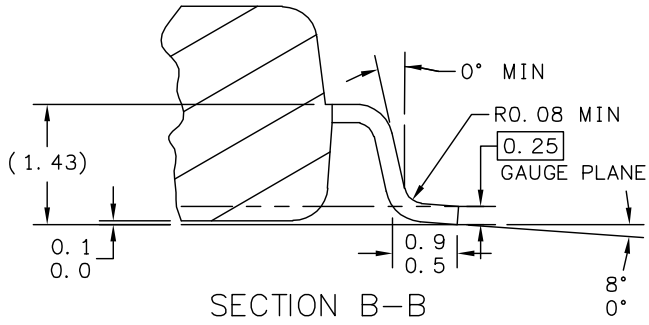
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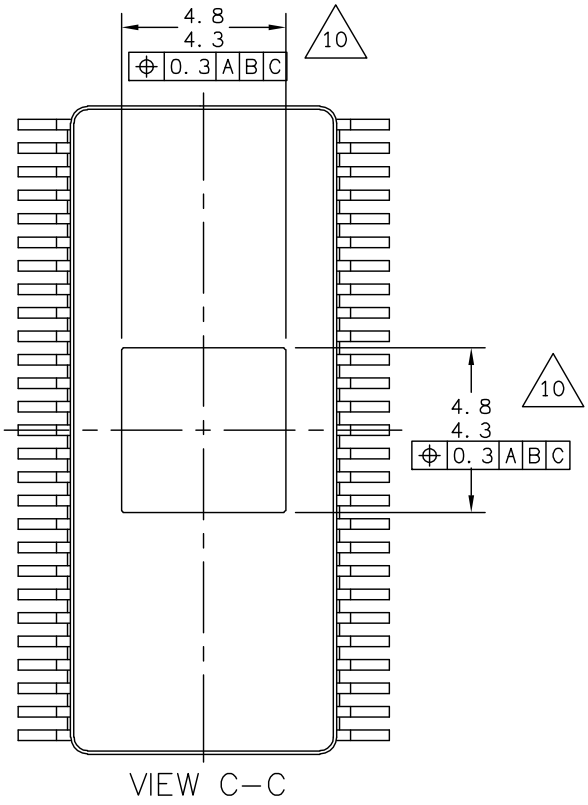


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	CASE NUMBER: 1390–02	11 MAR 2005
	STANDARD: NON–JEDEC	

EK SUFFIX (PB-FREE)
54-PIN SOICW EXPOSED PAD
98ASA10506D
ISSUE C

33887





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TITLE: 54LD SOIC W/B, 0.65 PITCH 4.6 X 4.6 EXPOSED PAD, CASE–OUTLINE	DOCUMENT NO: 98ASA10506D	REV: C
	CASE NUMBER: 1390–02	11 MAR 2005
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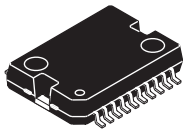
EK SUFFIX (PB-FREE)
54-PIN SOICW EXPOSED PAD
98ASA10506D
ISSUE C

33887

ADDITIONAL DOCUMENTATION

33887HSOP

**20-PIN
HSOP-EP**



**VW SUFFIX
98ASH70273A
20-PIN HSOP-EP**

Note For package dimensions, refer to the 33887 device data sheet.

THERMAL ADDENDUM (REV 2.0)

Introduction

This thermal addendum is provided as a supplement to the MC33887 technical data sheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application, and packaging information is provided in the data sheet.

Packaging and Thermal Considerations

The MC33887 is offered in a 20 pin HSOP exposed pad, single die package. There is a single heat source (P), a single junction temperature (T_J), and thermal resistance ($R_{\theta JA}$).

$$\{ T_J \} = [R_{\theta JA}] \cdot \{ P \}$$

The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

Standards

Table 7. Thermal Performance Comparison

Thermal Resistance	[°C/W]
$R_{\theta JA}$ (1),(2)	20
$R_{\theta JB}$ (2),(3)	6.0
$R_{\theta JA}$ (1), (4)	52
$R_{\theta JC}$ (5)	1.0

NOTES:

1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-5 and JESD51-7.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the center lead.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad surface; cold plate attached to the package bottom side, remaining surfaces insulated

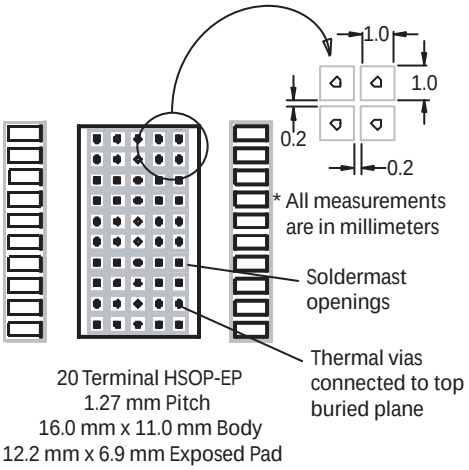


Figure 25. Thermal Land Pattern for Direct Thermal Attachment According to JESD51-5

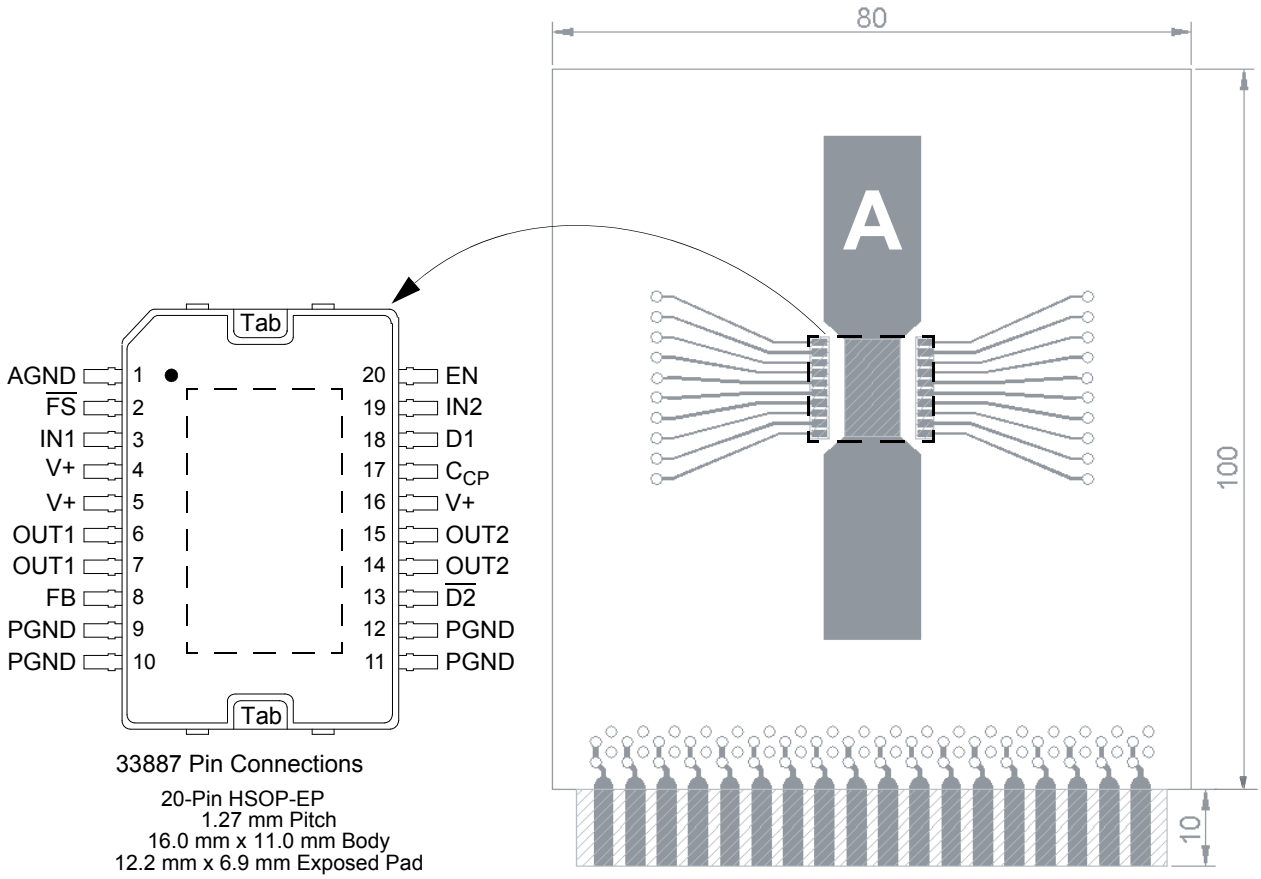


Figure 26. Thermal Test Board

Device on Thermal Test Board

Material:	Single layer printed circuit board FR4, 1.6 mm thickness Cu traces, 0.07 mm thickness
Outline:	80 mm x 100 mm board area, including edge connector for thermal testing
Area **A**:	Cu heat spreading areas on board surface
Ambient Conditions:	Natural convection, still air

Table 8. Thermal Resistance Performance

Thermal Resistance	Area A (mm^2)	°C/W
$R_{\theta JA}$	0.0	52
	300	36
	600	32
$R_{\theta JS}$	0.0	10
	300	7.0
	600	6.0

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.

$R_{\theta JS}$ is the thermal resistance between die junction and the reference location on the board surface near a center lead of the package (see Figure 26).

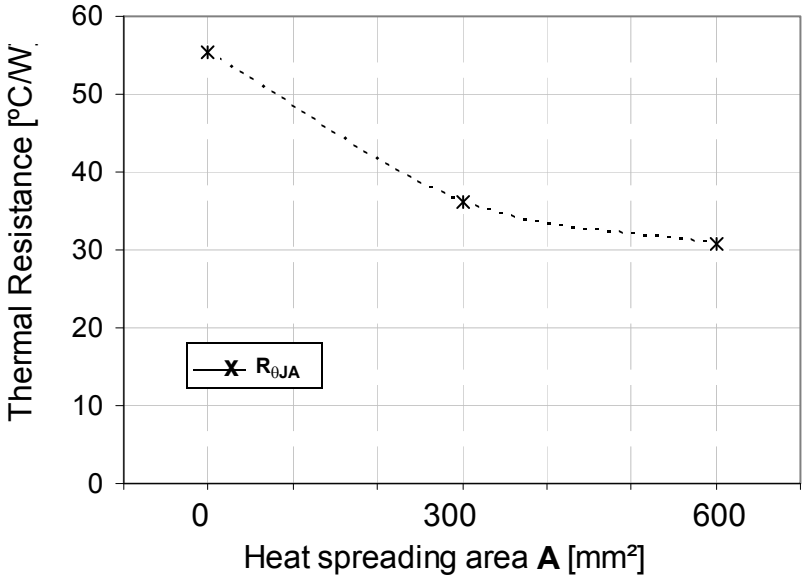


Figure 27. Device on Thermal Test Board $R_{\theta JA}$

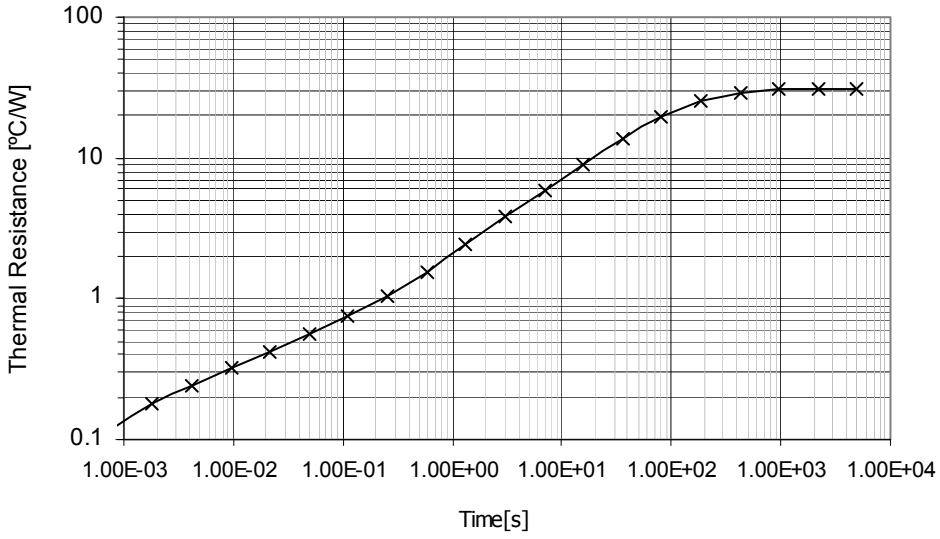


Figure 28. Transient Thermal Resistance $R_{\theta JA}$
Device on Thermal Test Board Area A = 600 (mm^2)

REVISION HISTORY

REVISION	DATE	DESCRIPTION
10.0	7/2005	• Added Thermal Addendum & Converted to Freescale format, Revised PQFN drawing, made several minor spelling correction. Added 33887A
11.0	11/2006	• Updated Ordering information block with new epp information • Changed the supply/ operating voltage from 40 V to 28 V • Updated all package drawings to the current revision • Adjusted to match device performance characteristics • Updated the document to the prevailing Freescale form and style • Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from Maximum Ratings on page 7. • Added note (8) • Added MCZ33887EK/R2 to the Ordering Information on Page 1 • Removed the 33887A from the data sheet and deleted Product Variation section now that is no longer needed.
12.0	1/2007	• Changed the third paragraph of the introduction on page 1 • Altered feature number 1 on page 1 • Added feature number 2 on page 1 • Changed Maximum Supply Voltage (1) to 0.3 to 40 V • Added note (1) • Changed note (16) • Added a third paragraph to Positive Power Supply (V+) on page 21 • Replaced Figure 20, Figure 21, and Figure 22 with updated information.
13.0	10/2008	• Added Part Number MC33887AVW/R2 to Ordering Information Table on page 1.
14.0	3/2011	• Removed part numbers MC33887APVW/R2, MC33887DH/R2, MC33887DWB/R2, MC33887AVW/R2, MC33887PNB/R2 and MCZ33887EK/R2 and replaced with part numbers MC33887APVW/R2, MC33887PFK/R2 and MC33887PEK/R2 in Ordering Information Table on Page 1.

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