10-Bit, 65/80/105 MSPS, 3 V A/D Converter

Data Sheet

AD9215

FEATURES

Single 3 V supply operation (2.7 V to 3.3 V)
SNR = 58 dBc (to Nyquist)
SFDR = 77 dBc (to Nyquist)
Low power ADC core: 96 mW at 65 MSPS, 104 mW @ 80 MSPS, 120 mW at 105 MSPS
Differential input with 300 MHz bandwidth
On-chip reference and sample-and-hold amplifier
DNL = ±0.25 LSB
Flexible analog input: 1 V p-p to 2 V p-p range
Offset binary or twos complement data format
Clock duty cycle stabilizer

APPLICATIONS

Ultrasound equipment
IF sampling in communications receivers
Battery-powered instruments
Hand-held scopemeters
Low cost digital oscilloscopes

FUNCTIONAL BLOCK DIAGRAM

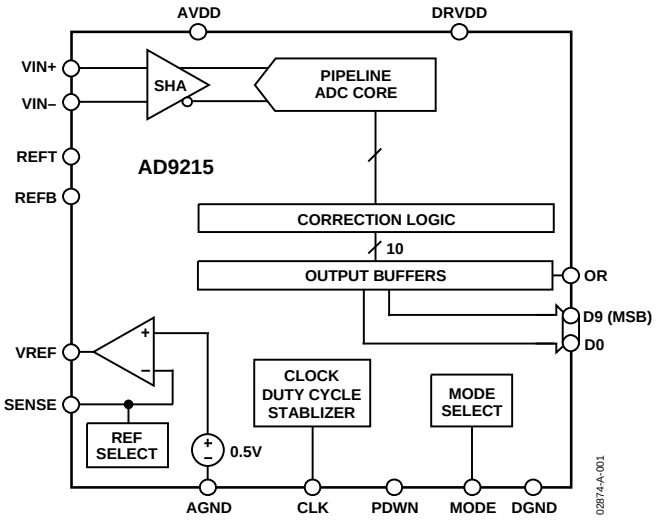


Figure 1.

PRODUCT DESCRIPTION

The AD9215 is a family of monolithic, single 3 V supply, 10-bit, 65/80/105 MSPS analog-to-digital converters (ADC). This family features a high performance sample-and-hold amplifier (SHA) and voltage reference. The AD9215 uses a multistage differential pipelined architecture with output error correction logic to provide 10-bit accuracy at 105 MSPS data rates and to guarantee no missing codes over the full operating temperature range.

The wide bandwidth, truly differential sample-and-hold amplifier (SHA) allows for a variety of user-selectable input ranges and offsets including single-ended applications. It is suitable for multiplexed systems that switch full-scale voltage levels in successive channels and for sampling single-channel inputs at frequencies well beyond the Nyquist rate. Combined with power and cost savings over previously available ADCs, the AD9215 is suitable for applications in communications, imaging, and medical ultrasound.

A single-ended clock input is used to control all internal conversion cycles. A duty cycle stabilizer compensates for wide variations in the clock duty cycle while maintaining excellent performance. The digital output data is presented in straight binary or twos complement formats. An out-of-range signal indicates an overflow condition, which can be used with the MSB to determine low or high overflow.

Fabricated on an advanced CMOS process, the AD9215 is available in both a 28-lead surface-mount plastic package and a 32-lead chip scale package and is specified over the industrial temperature range of −40°C to +85°C.

PRODUCT HIGHLIGHTS

1. The AD9215 operates from a single 3 V power supply and features a separate digital output driver supply to accommodate 2.5 V and 3.3 V logic families.
2. Operating at 105 MSPS, the AD9215 core ADC consumes a low 120 mW; at 80 MSPS, the power dissipation is 104 mW; and at 65 MSPS, the power dissipation is 96 mW.
3. The patented SHA input maintains excellent performance for input frequencies up to 200 MHz and can be configured for single-ended or differential operation.
4. The AD9215 is part of several pin compatible 10-, 12-, and 14-bit low power ADCs. This allows a simplified upgrade from 10 bits to 12 bits for systems up to 80 MSPS.
5. The clock duty cycle stabilizer maintains converter performance over a wide range of clock pulse widths.
6. The out of range (OR) output bit indicates when the signal is beyond the selected input range.

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REVISION HISTORY

2/13—Data Sheet Changed from a REV. A to a REV. B

Changes to Figure 4 and Added EPAD Note to Pin Configurations and Function Descriptions Section ... 7
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2/04—Data Sheet Changed from a REV. 0 to a REV. A

Renumbered Figures and Tables ... UNIVERSAL
Changes to Product Title ... 1
Changes to Features ... 1
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5/03—Revision 0: Initial Version

SPECIFICATIONS

AVDD = 3 V, DRVDD = 2.5 V, specified maximum conversion rate, 2 V p-p differential input, 1.0 V internal reference, unless otherwise noted.

Table 1. DC Specifications

			AD9215BRU-65/ AD9215BCP-65			AD9215BRU-80/ AD9215BCP-80			AD9215BRU-105/ AD9215BCP-105			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	VI	10			10			10			Bits
ACCURACY												
No Missing Codes	Full	VI		Guaranteed			Guaranteed			Guaranteed		
Offset Error[1]	Full	VI		±0.3	±2.0		±0.3	±2.0		±0.3	±2.0	% FSR
Gain Error[1]	Full	VI	0	+1.5	+4.0		+1.5	+4.0		+1.5	+4.0	% FSR
Differential Nonlinearity (DNL)[2]	Full	VI	−1.0	±0.5	+1.0	−1.0	±0.5	+1.0	−1.0	±0.6	+1.2	LSB
Integral Nonlinearity (INL)[2]	Full	VI		±0.5	±1.2		±0.5	±1.2		±0.65	±1.2	LSB
TEMPERATURE DRIFT												
Offset Error[1]	Full	V		+15			+15			+15		ppm/°C
Gain Error[1]	Full	V		+30			+30			+30		ppm/°C
Reference Voltage (1 V Mode)	Full	V		±230			±230			±230		ppm/°C
INTERNAL VOLTAGE REFERENCE												
Output Voltage Error (1 V Mode)	Full	VI		±2	±35		±2	±35		±2	±35	mV
Load Regulation @ 1.0 mA	Full	V		0.2			0.2			0.2		mV
Output Voltage Error (0.5 V Mode)	Full	V		± 1			±1			±1		mV
Load Regulation @ 0.5 mA	Full	V		0.2			0.2			0.2		mV
INPUT REFERRED NOISE												
VREF = 0.5 V	25°C	V		0.8			0.8			0.8		LSB rms
VREF = 1.0 V	25°C	V		0.4			0.4			0.4		LSB rms
ANALOG INPUT												
Input Span, VREF = 0.5 V	Full	IV		1			1			1		V p-p
Input Span, VREF = 1.0 V	Full	IV		2			2			2		V p-p
Input Capacitance[3]	Full	V		2			2			2		pF
REFERENCE INPUT RESISTANCE	Full	V		7			7			7		kΩ
POWER SUPPLIES												
Supply Voltage												
AVDD	Full	IV	2.7	3.0	3.3	2.7	3.0	3.3	2.7	3.0	3.3	V
DRVDD	Full	IV	2.25	2.5	3.6	2.25	2.5	3.6	2.25	2.5	3.6	V
Supply Current												
I_{AVDD}[2]	Full	VI		32	35		34.5	39		40	44	mA
I_{DRVDD}[2]	25°C	V		7.0			8.6			11.3		mA
PSRR	Full	V		± 0.1			± 0.1			± 0.1		% FSR
POWER CONSUMPTION												
Sine Wave Input[2]												
I_{AVDD}[2]	Full	VI		96			104			120		mW
I_{DRVDD}[2]	25°C	V		18			20			25		mW
Standby Power[4]	25°C	V		1.0			1.0			1.0		mW

[1] With a 1.0 V internal reference.
[2] Measured at f_{IN} = 2.4 MHz, full-scale sine wave, with approximately 5 pF loading on each output bit.
[3] Input capacitance refers to the effective capacitance between one differential input pin and AGND. Refer to Figure 5 for the equivalent analog input structure.
[4] Standby power is measured with a dc input, the CLK pin inactive (i.e., set to AVDD or AGND).

AVDD = 3 V, DRVDD = 2.5 V, specified maximum conversion rate, 2 V p-p differential input, 1.0 V internal reference, AIN = −0.5 dBFS, MODE = AVDD/3 (duty cycle stabilizer [DCS] enabled), unless otherwise noted.

Table 2. AC Specifications

			AD9215BRU-65/ AD9215BCP-65			AD9215BRU-80/ AD9215BCP-80			AD9215BRU-105/ AD9215BCP-105			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE RATIO (SNR)												
f_{IN} = 2.4 MHz	Full	VI	56.0	58.5		56.0	58.5			57.5		dB
	25°C	I	57.0	59.0		57.0	59.0		56.6	58.5		dB
f_{IN} = Nyquist[1]	Full	VI	56.0	58.0		56.0	58.0			57.5		dB
	25°C	I	56.5	58.5		56.5	58.5		56.4	58.0		dB
f_{IN} = 70 MHz	25°C	V					58.0			57.8		dB
f_{IN} = 100 MHz	25°C	V					57.5			57.7		dB
SIGNAL-TO-NOISE AND DISTORTION (SINAD)												
f_{IN} = 2.4 MHz	Full	VI	55.8	58.5		55.7	58.5			57.6		dB
	25°C	I	56.5	59.0		56.8	58.5		56.5	58.2		dB
f_{IN} = Nyquist[1]	Full	VI	55.8	58.0		55.5	58.0			57.3		dB
	25°C	I	56.3	58.5		56.3	58.5		56.1	57.8		dB
f_{IN} = 70 MHz	25°C	V					56.0			57.7		dB
f_{IN} = 100 MHz	25°C	V					55.5			57.4		dB
EFFECTIVE NUMBER OF BITS (ENOB)												
f_{IN} = 2.4 MHz	Full	VI	9.1	9.5		9.0	9.5			9.3		Bits
	25°C	I	9.2	9.6		9.3	9.5		9.2	9.5		Bits
f_{IN} = Nyquist[1]	Full	VI	9.1	9.4		9.0	9.4			9.4		Bits
	25°C	I	9.1	9.5		9.0	9.5		9.1	9.4		Bits
f_{IN} = 70 MHz	25°C	V					9.1			9.4		Bits
f_{IN} = 100 MHz	25°C	V					9.0			9.3		Bits
WORST HARMONIC (Second or Third)												
f_{IN} = 2.4 MHz	Full	VI		−78	−64		−78	−64		−78		dBc
	25°C	I		−80	−65		−80	−65		−84	−70	dBc
f_{IN} = Nyquist[1]	Full	VI		−77	−64		−76	−63		−74		dBc
	25°C	I		−78	−65		−78	−65		−75	−61	dBc
f_{IN} = 70 MHz	25°C	V					−70			−75		dBc
f_{IN} = 100 MHz	25°C	V					−70			−74		dBc
WORST OTHER (Excluding Second or Third)												
f_{IN} = 2.4 MHz	Full	VI		−77	−67		−77	−66		−73		dBc
	25°C	I		−78	−68		−77	−68		−75	−66	dBc
f_{IN} = Nyquist[1]	Full	VI		−77	−67		−77	−66		−71		dBc
	25°C	I		−78	−68		−77	−68		−75	−63	dBc
f_{IN} = 70 MHz	25°C	V					−80			-75		dBc
f_{IN} = 100 MHz	25°C	V					−80			−75		dBc
TWO-TONE SFDR (AIN = −7 dBFS)												
f_{IN1} = 70.3 MHz, f_{IN2} = 71.3 MHz	25°C	V					75			75		dBc
f_{IN1} = 100.3 MHz, f_{IN2} = 101.3 MHz	25°C	V					74			74		dBc
ANALOG BANDWIDTH	25°C	V		300			300			300		MHz

[1] Tested at f_{IN} = 35 MHz for AD9215-65; f_{IN} = 39 MHz for AD9215-80; and f_{IN} = 50 MHz for AD9215-105.

Table 3. Digital Specifications

			AD9215BRU-65/ AD9215BCP-65			AD9215BRU-80/ AD9215BCP-80			AD9215BRU-105/ AD9215BCP-105			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
LOGIC INPUTS (CLK, PDWN)												
High Level Input Voltage	Full	IV	2.0			2.0			2.0			V
Low Level Input Voltage	Full	IV			0.8			0.8			0.8	V
High Level Input Current	Full	IV	−650		+10	−650		+10	−650		+10	µA
Low Level Input Current	Full	IV	−70		+10	−70		+10	−70		+10	µA
Input Capacitance	Full	V		2			2			2		pF
LOGIC OUTPUTS[1] DRVDD = 2.5 V												
High Level Output Voltage	Full	IV	2.45			2.45			2.45			V
Low Level Output Voltage	Full	IV			0.05			0.05			0.05	V

[1] Output voltage levels measured with a 5 pF load on each output.

Table 4. Switching Specifications

			AD9215BRU-65/ AD9215BCP-65			AD9215BRU-80/ AD9215BCP-80			AD9215BRU-105/ AD9215BCP-105			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUT PARAMETERS												
Maximum Conversion Rate	Full	VI	65			80			105			MSPS
Minimum Conversion Rate	Full	V			5			5			5	MSPS
CLOCK Period	Full	V	15.4			12.5			9.5			ns
DATA OUTPUT PARAMETERS												
Output Delay[1] (t_{OD})	Full	VI	2.5	4.8	6.5	2.5	4.8	6.5	2.5	4.8	6.5	ns
Pipeline Delay (Latency)	Full	V		5			5			5		Cycles
Aperture Delay	25°C	V		2.4			2.4			2.4		ns
Aperture Uncertainty (Jitter)	25°C	V		0.5			0.5			0.5		ps rms
Wake-Up Time[2]	25°C	V		7			7			7		ms
OUT-OF-RANGE RECOVERY TIME	25°C	V		1			1			1		Cycles

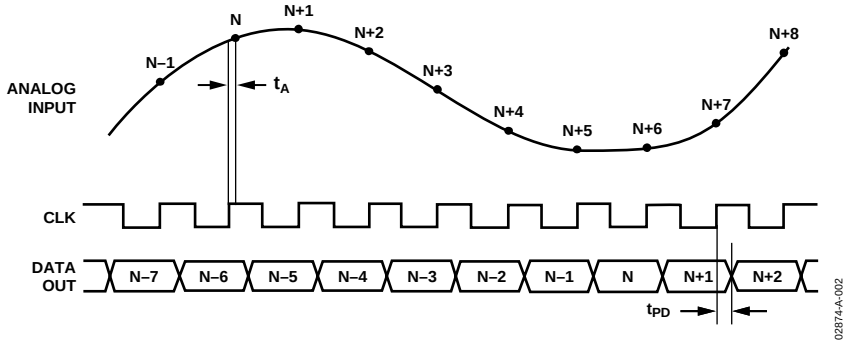


Figure 2. Timing Diagram

[1] Output delay is measured from CLK 50% transition to DATA 50% transition, with 5 pF load on each output.
[2] Wake-up time is dependent on the value of decoupling capacitors; typical values shown with 0.1 µF and 10 µF capacitors on REFT and REFB.

ABSOLUTE MAXIMUM RATINGS[1]

Table 5.

Mnemonic	With Respect to	Min	Max	Unit
ELECTRICAL				
AVDD	AGND	−0.3	+3.9	V
DRVDD	DRGND	−0.3	+3.9	V
AGND	DRGND	−0.3	+0.3	V
AVDD	DRVDD	−3.9	+3.9	V
Digital Outputs	DRGND	−0.3	DRVDD + 0.3	V
CLK, MODE	AGND	−0.3	AVDD + 0.3	V
VIN+, VIN−	AGND	−0.3	AVDD + 0.3	V
VREF	AGND	−0.3	AVDD + 0.3	V
SENSE	AGND	−0.3	AVDD + 0.3	V
REFB, REFT	AGND	−0.3	AVDD + 0.3	V
PDWN	AGND	−0.3	AVDD + 0.3	V
ENVIRONMENTAL[2]				
Operating Temperature		−40	+85	°C
Junction Temperature			150	°C
Lead Temperature (10 sec)			300	°C
Storage Temperature		−65	+150	°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances 28-lead TSSOP: θ_{JA} = 67.7°C/W, 32-lead LFCSP: θ_{JA} = 32.7°C/W; heat sink soldered down to ground plane.

EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested.

II 100% production tested at 25°C and sample tested at specified temperatures.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

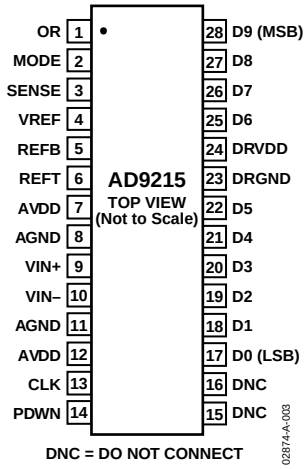


Figure 3. TSSOP (RU-28)

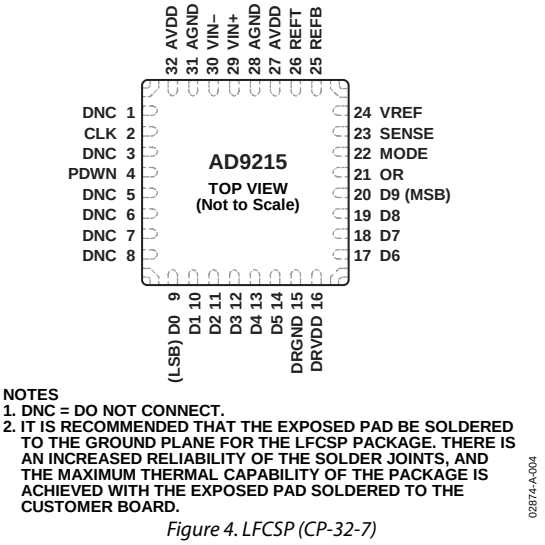


Figure 4. LFCSP (CP-32-7)

Table 6. Pin Function Descriptions

TSSOP Pin No.	LFCSP Pin No.	Mnemonic	Description
1	21	OR	Out-of-Range Indicator.
2	22	MODE	Data Format and Clock Duty Cycle Stabilizer (DCS) Mode Selection.
3	23	SENSE	Reference Mode Selection.
4	24	VREF	Voltage Reference Input/Output.
5	25	REFB	Differential Reference (Negative).
6	26	REFT	Differential Reference (Positive).
7, 12	27, 32	AVDD	Analog Power Supply.
8, 11	28, 31	AGND	Analog Ground.
9	29	VIN+	Analog Input Pin (+).
10	30	VIN–	Analog Input Pin (–).
13	2	CLK	Clock Input Pin.
14	4	PDWN	Power-Down Function Selection (Active High).
15 to 16	1, 3, 5 to 8	DNC	Do not connect, recommend floating this pin.
17 to 22, 25 to 28	9 to 14, 17 to 20	D0 (LSB) to D9 (MSB)	Data Output Bits.
23	15	DRGND	Digital Output Ground.
24	16	DRVDD	Digital Output Driver Supply. Must be decoupled to DRGND with a minimum 0.1 µF capacitor. Recommended decoupling is 0.1 µF in parallel with 10 µF.
N/A	33	EP	Exposed Pad. It is recommended that the exposed pad be soldered to the ground plane for the LFCSP package. There is an increased reliability of the solder joints, and the maximum thermal capability of the package is achieved with the exposed pad soldered to the customer board.

EQUIVALENT CIRCUITS

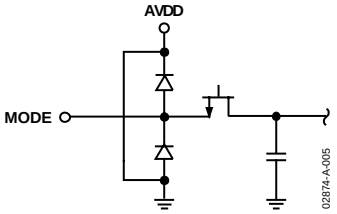


Figure 5. Equivalent Analog Input Circuit

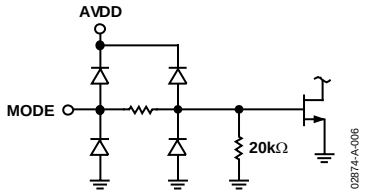


Figure 6. Equivalent MODE Input Circuit

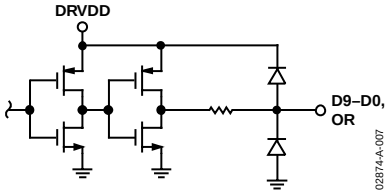


Figure 7. Equivalent Digital Output Circuit

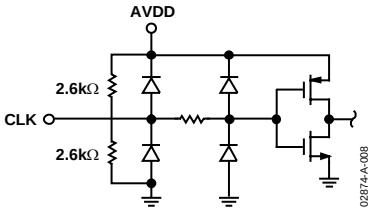


Figure 8. Equivalent Digital Input Circuit

DEFINITIONS OF SPECIFICATIONS

Aperture Delay

Aperture delay is a measure of the sample-and-hold amplifier (SHA) performance and is measured from the rising edge of the clock input to when the input signal is held for conversion.

Aperture Jitter

Aperture jitter is the variation in aperture delay for successive samples and can be manifested as frequency-dependent noise on the input to the ADC.

Clock Pulse Width and Duty Cycle

Pulse width high is the minimum amount of time that the clock pulse should be left in the Logic 1 state to achieve rated performance. Pulse width low is the minimum time the clock pulse should be left in the low state. At a given clock rate, these specifications define an acceptable clock duty cycle.

Differential Nonlinearity (DNL, No Missing Codes)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 10-bit resolution indicate that all 1024 codes, respectively, must be present over all operating ranges.

Effective Number of Bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula, it is possible to obtain a measure of performance expressed as *N*, the effective number of bits

$$N = (SINAD - 1.76)/6.02$$

Thus, the effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

Gain Error

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the positive full scale. Gain error is the deviation of the actual difference between the first and last code transitions and the ideal difference between the first and last code transitions.

Integral Nonlinearity (INL)

INL refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as negative full scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Maximum Conversion Rate

The clock rate at which parametric testing is performed.

Minimum Conversion Rate

The clock rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Offset Error

The major carry transition should occur for an analog value 1/2 LSB below VIN+ = VIN−. Zero error is defined as the deviation of the actual transition from that point.

Out-of-Range Recovery Time

Out-of-range recovery time is the time it takes for the ADC to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

Output Propagation Delay

The delay between the clock logic threshold and the time when all bits are within valid logic levels.

Power Supply Rejection

The specification shows the maximum change in full scale from the value with the supply at the minimum limit to the value

with the supply at its maximum limit.

Signal-to-Noise and Distortion (SINAD) Ratio

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

Temperature Drift

The temperature drift for zero error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

Two-Tone SFDR

The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. It may be reported in dBc (i.e., degrades as signal levels are lowered) or in dBFS (always related back to converter full scale).

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 3.0 V, DRVDD = 2.5 V with DCS enabled, T_A = 25°C, 2 V differential input, A_{IN} = −0.5 dBFS, VREF = 1.0 V, unless otherwise noted.

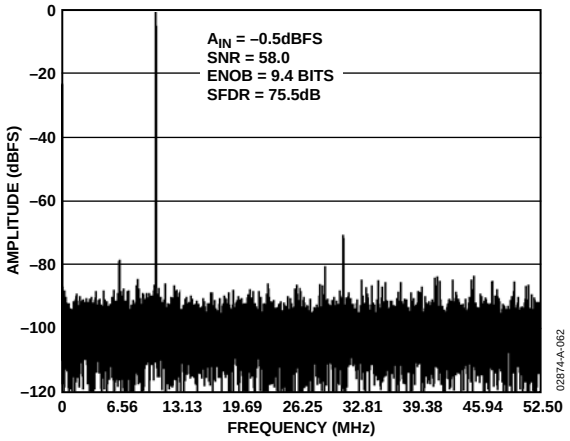


Figure 9. Single-Tone 32k FFT with f_{IN} = 10.3 MHZ, f_{SAMPLE} = 105 MSPS

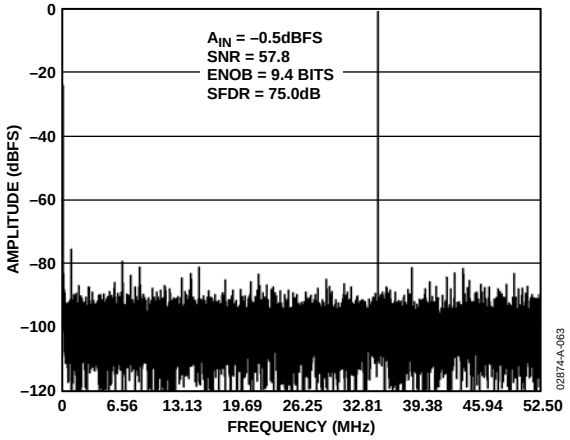


Figure 10. Single-Tone 32k FFT with f_{IN} = 70.3 MHz, f_{SAMPLE} = 105 MSPS

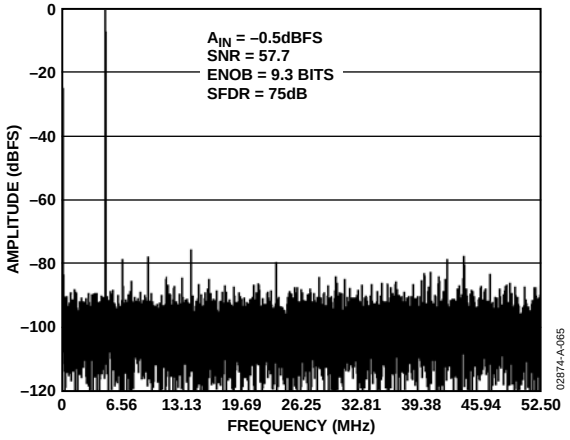


Figure 11. Single-Tone 32k FFT with f_{IN} = 100.3 MHz, f_{SAMPLE} = 105 MSPS

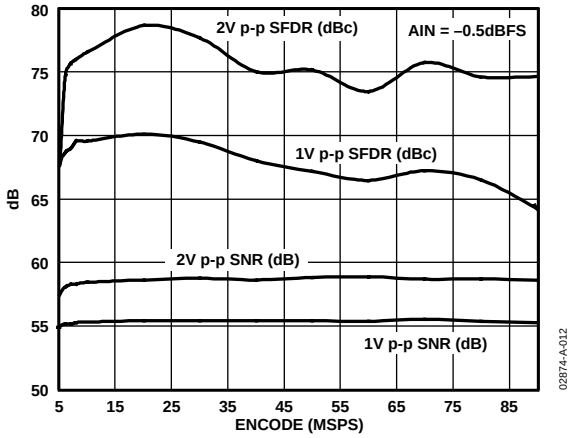


Figure 12. AD9215-80 SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 10.3 MHz

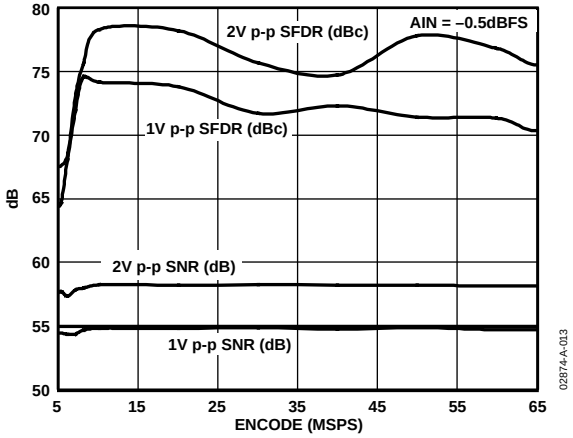


Figure 13. AD9215-65 SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 10.3 MHz

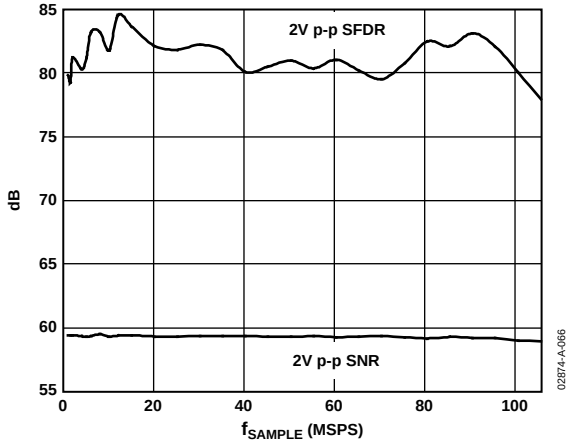


Figure 14. AD9215-105 SNR/SFDR vs. f_{SAMPLE}, f_{IN} = 10.3 MHz

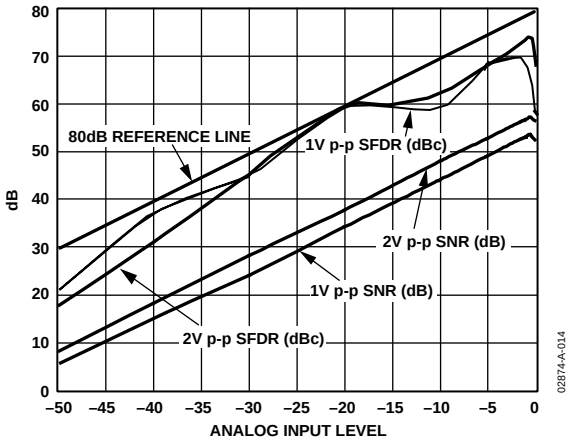


Figure 15. AD9215-80 SNR/SFDR vs. Analog Input Drive Level, f_{SAMPLE} = 80 MSPS, f_{IN} = 39.1 MHz

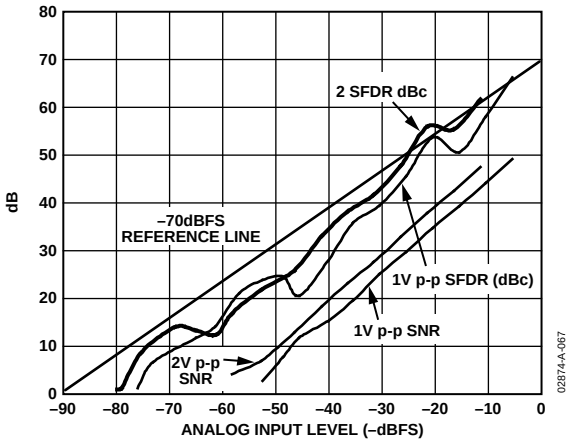


Figure 16. AD9215-105 SNR/SFDR vs. Analog Input Drive Level, f_{SAMPLE} = 105 MSPS, f_{IN} = 50.3 MHz

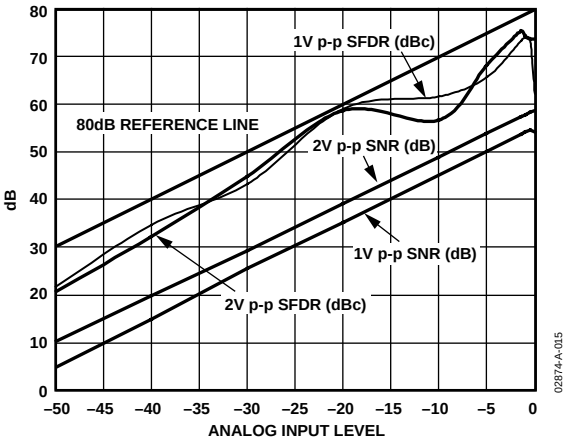


Figure 17. AD9215-65 SNR/SFDR vs. Analog Input Drive Level, f_{SAMPLE} = 65 MSPS, f_{IN} = 30.3 MHz

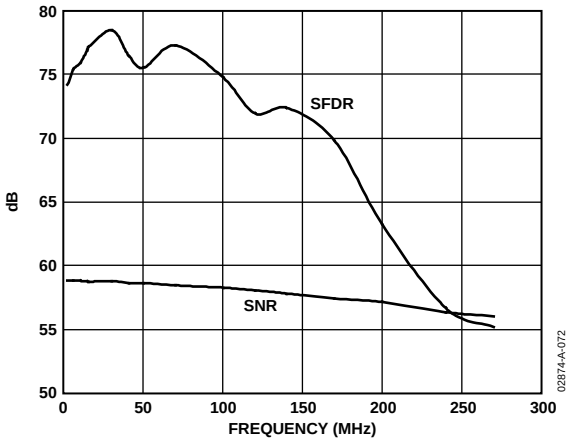


Figure 18. AD9215-105 SNR/SFDR vs. f_{IN}, A_{IN} = –0.5 dBFS, f_{SAMPLE} = 105 MSPS

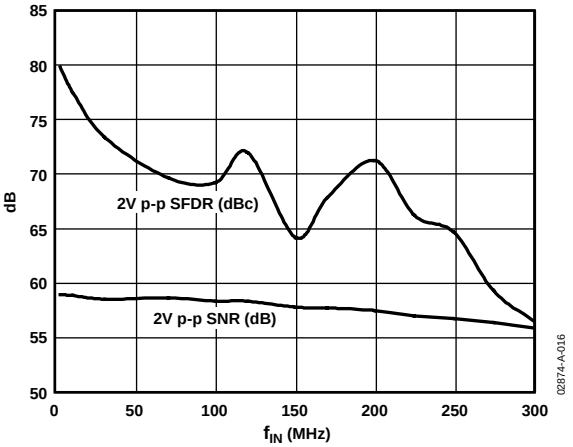


Figure 19. AD9215-80 SNR/SFDR vs. f_{IN}, A_{IN} = –0.5 dBFS, f_{SAMPLE} = 80 MSPS

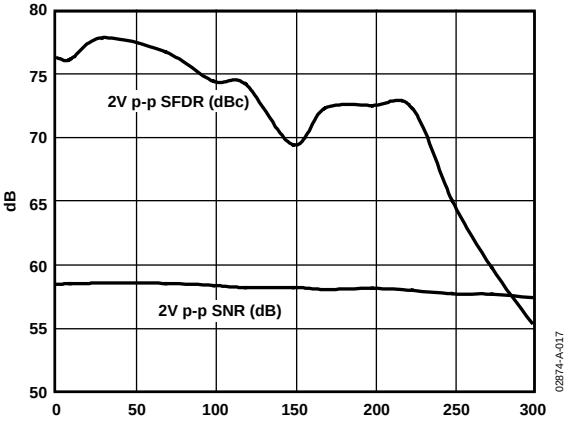


Figure 20. AD9215-65 SNR/SFDR vs. f_{IN}, A_{IN} = –0.5 dBFS, f_{SAMPLE} = 65 MSPS

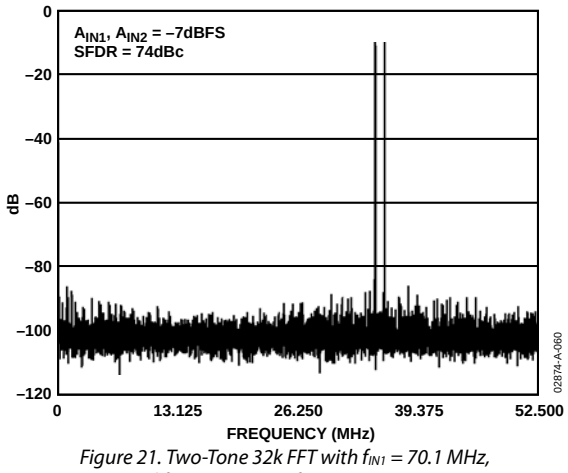


Figure 21. Two-Tone 32k FFT with f_{IN1} = 70.1 MHz, and f_{IN2} = 71.1 MHz, f_{SAMPLE} = 105 MSPS

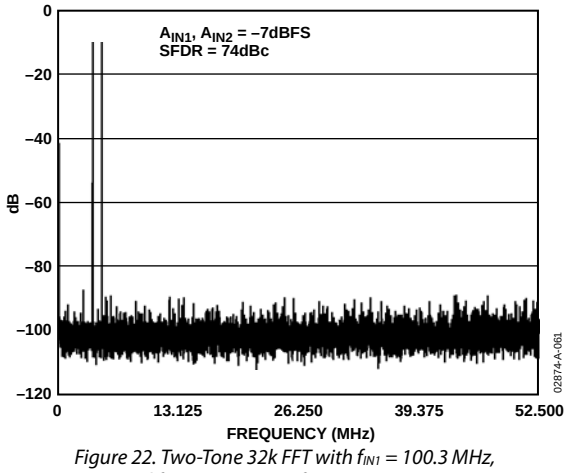


Figure 22. Two-Tone 32k FFT with f_{IN1} = 100.3 MHz, and f_{IN2} = 101.3 MHz, f_{SAMPLE} = 105 MSPS

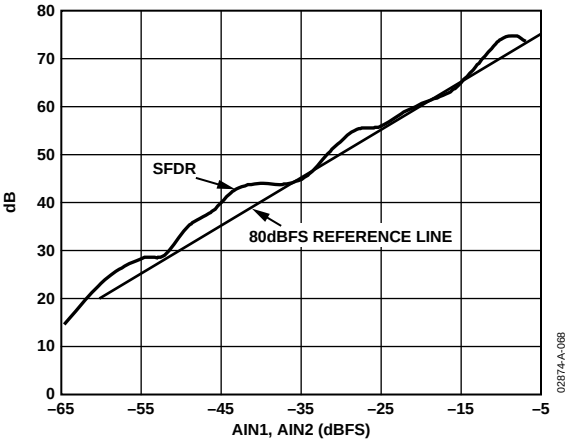


Figure 23. AD9215-105 Two-Tone SFDR vs. A_{IN}, f_{IN1} = 70.1 MHz, and f_{IN2} = 71.1 MHz, f_{SAMPLE} = 105 MSPS

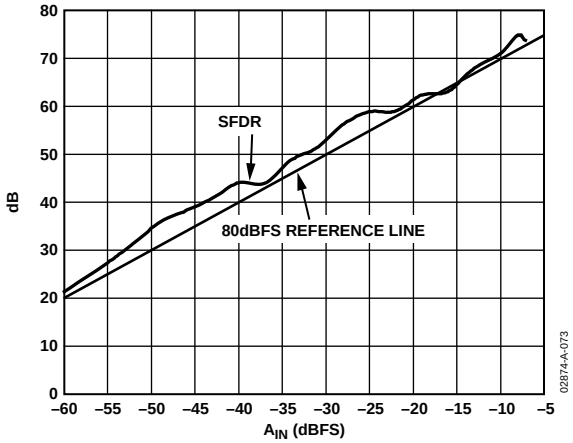


Figure 24. AD9215-80 Two-Tone SFDR vs. A_{IN}, f_{IN1} = 100.3 MHz, and f_{IN2} = 101.3 MHz, f_{SAMPLE} = 105 MSPS

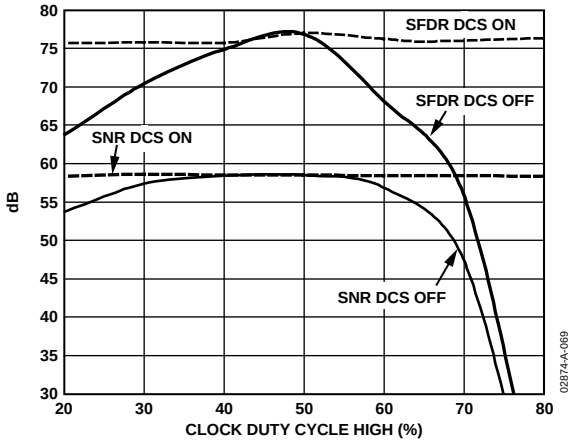


Figure 25. SINAD, SFDR vs. Clock Duty Cycle, f_{SAMPLE} = 105 MSPS, f_{IN} = 50.3 MH

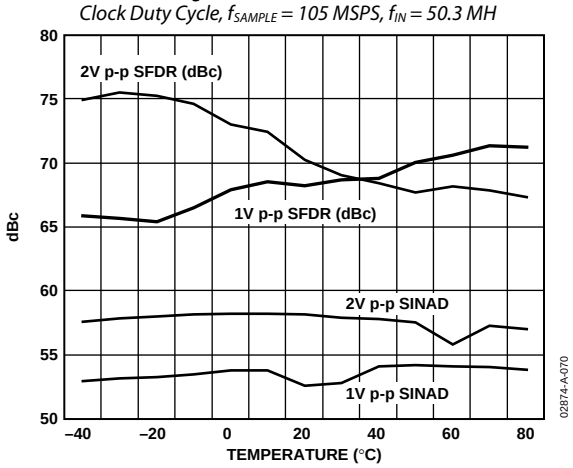


Figure 26. SINAD, SFDR vs. Temperature, f_{SAMPLE} = 105 MSPS, f_{IN} = 50 MHz

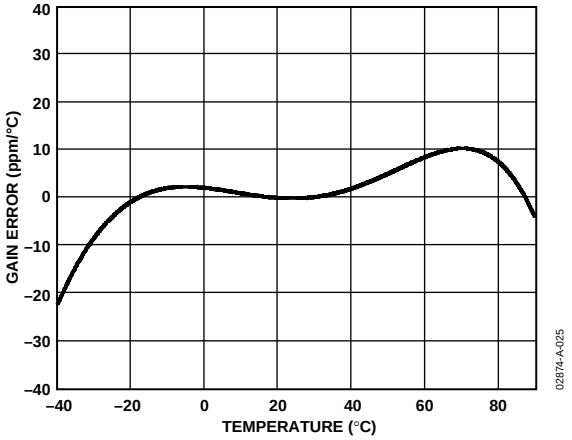


Figure 27. Gain vs. Temperature External 1 V Reference

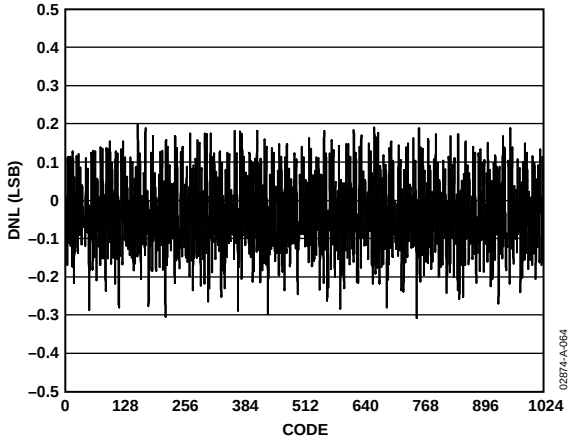


Figure 28. AD9215-105 Typical DNL, f_{SAMPLE} = 105 MSPS, f_{IN} = 2.3 MHz

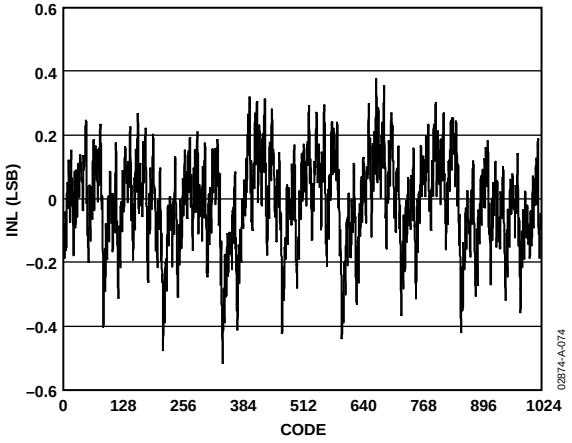


Figure 29. AD9215-105 Typical INL, f_{SAMPLE} = 105 MSPS, f_{IN} = 2.3 MHz

APPLYING THE AD9215 THEORY OF OPERATION

The AD9215 architecture consists of a front-end SHA followed by a pipelined switched capacitor ADC. Each stage provides sufficient overlap to correct for flash errors in the preceding stages. The quantized outputs from each stage are combined into a final 10-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample, while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

The input stage contains a differential SHA that can be configured as ac-coupled or dc-coupled in differential or single-ended modes. Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. Redundancy is used in each one of the stages to facilitate digital correction of flash errors.

The output-staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing. During power-down, the output buffers go into a high impedance state.

Analog Input and Reference Overview

The analog input to the AD9215 is a differential switched capacitor SHA that has been designed for optimum performance while processing a differential input signal. The SHA input can support a wide common-mode range and maintain excellent performance, as shown in Figure 31. An input common-mode voltage of midsupply minimizes signal-dependent errors and provides optimum performance.

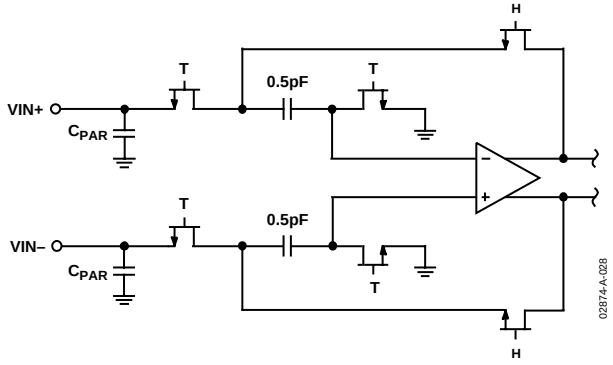


Figure 30. Switched-Capacitor SHA Input

The clock signal alternatively switches the SHA between sample mode and hold mode (see Figure 30). When the SHA is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. Also, a small shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC's input; therefore, the precise values are dependent upon the application. In IF undersampling applications, any shunt capacitors should be removed. In combination with the driving source impedance, they would limit the input bandwidth.

The analog inputs of the AD9215 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. $V_{CM} = AVDD/2$ is recommended for optimum performance, but the device functions over a wider range with reasonable performance (see Figure 31).

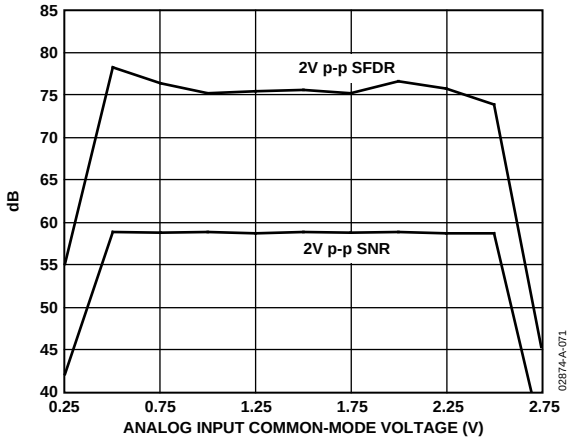


Figure 31. AD9215-105 SNR, SFDR vs. Common-Mode Voltage

For best dynamic performance, the source impedances driving VIN+ and VIN– should be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC.

An internal differential reference buffer creates positive and negative reference voltages, REFT and REFB, respectively, that define the span of the ADC core. The output common mode of the reference buffer is set to midsupply, and the REFT and REFB voltages and span are defined as

$$REFT = 1/2\ (AVDD + VREF)$$

$$REFB = 1/2\ (AVDD - VREF)$$

$$Span = 2 \times (REFT - REFB) = 2 \times VREF$$

It can be seen from the equations above that the REFT and REFB voltages are symmetrical about the midsupply voltage and, by definition, the input span is twice the value of the VREF voltage.

The internal voltage reference can be pin-strapped to fixed values of 0.5 V or 1.0 V or adjusted within the same range as discussed in the Internal Reference Connection section. Maximum SNR performance is achieved with the AD9215 set to the largest input span of 2 V p-p. The relative SNR degradation is 3 dB

when changing from 2 V p-p mode to 1 V p-p mode.

The SHA may be driven from a source that keeps the signal peaks within the allowable range for the selected reference voltage. The minimum and maximum common-mode input levels are defined as

$$VCM_{MIN} = VREF/2$$

$$VCM_{MAX} = (AVDD + VREF)/2$$

The minimum common-mode input level allows the AD9215 to accommodate ground-referenced inputs.

Although optimum performance is achieved with a differential input, a single-ended source may be driven into VIN+ or VIN−. In this configuration, one input accepts the signal, while the opposite input should be set to midscale by connecting it to an appropriate reference. For example, a 2 V p-p signal may be applied to VIN+ while a 1 V reference is applied to VIN−. The AD9215 then accepts a signal varying between 2 V and 0 V. In the single-ended configuration, distortion performance may degrade significantly as compared to the differential case. However, the effect is less noticeable at lower input frequencies.

Differential Input Configurations

As previously detailed, optimum performance is achieved while driving the AD9215 in a differential input configuration. For baseband applications, the AD8138 differential driver provides excellent performance and a flexible interface to the ADC. The output common-mode voltage of the AD8138 is easily set to *AVDD*/2, and the driver can be configured in a Sallen Key filter topology to provide band limiting of the input signal.

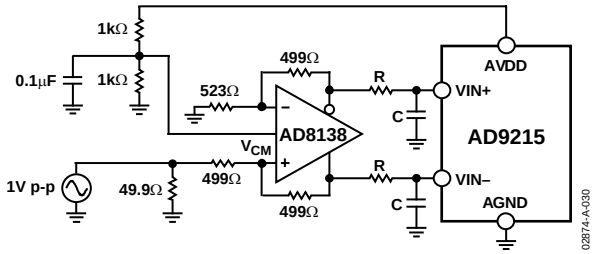


Figure 32. Differential Input Configuration Using the AD8138

At input frequencies in the second Nyquist zone and above, the performance of most amplifiers is not adequate to achieve the true performance of the AD9215. This is especially true in IF undersampling applications where frequencies in the 70 MHz to 200 MHz range are being sampled. For these applications, differential transformer coupling is the recommended input configuration. The value of the shunt capacitor is dependant on the input frequency and source impedance and should be reduced or removed. An example of this is shown in Figure 33.

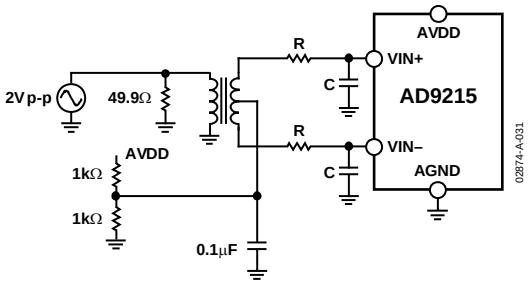


Figure 33. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few MHz, and excessive signal power can also cause core saturation, which leads to distortion.

Single-Ended Input Configuration

A single-ended input may provide adequate performance in cost-sensitive applications. In this configuration, there is a degradation in SFDR and distortion performance due to the large input common-mode swing. However, if the source impedances on each input are kept matched, there should be little effect on SNR performance. Figure 34 details a typical single-ended input configuration.

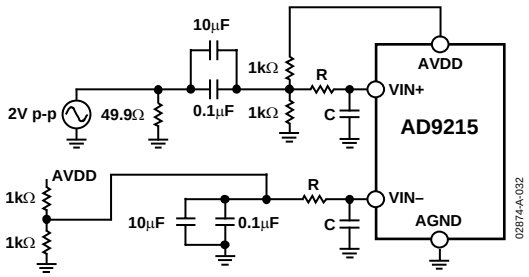


Figure 34. Single-Ended Input Configuration

CLOCK INPUT AND CONSIDERATIONS

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals, and as a result may be sensitive to clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9215 contains a clock duty cycle stabilizer that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9215. As shown in Figure 25, noise and distortion performance are nearly flat over a 50% range of duty cycle. For best ac performance, enabling the duty cycle stabilizer is recommended for all applications.

The duty cycle stabilizer uses a delay-locked loop (DLL) to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately 100 clock cycles to allow the DLL to acquire and lock to the new rate.

Table 7. Reference Configuration Summary

Selected Mode	External SENSE Connection	Internal Op Amp Configuration	Resulting VREF (V)	Resulting Differential Span (V p-p)
Externally Supplied Reference	AVDD	N/A	N/A	2 × External Reference
Internal 0.5 V Reference	VREF	Voltage Follower (G = 1)	0.5	1.0
Programmed Variable Reference	External Divider	Noninverting (1 < G < 2)	0.5 × (1 + *R2/R1*)	2 × VREF
Internally Programmed 1 V Reference	AGND to 0.2 V	Internal Divider	1.0	2.0

Table 8. Digital Output Coding

Code	VIN+ – VIN– Input Span = 2 V p-p (V)	VIN+ – VIN– Input Span = 1 V p-p (V)	Digital Output Offset Binary (D9••••••D0)	Digital Output Twos Complement (D9••••••D0)
1023	1.000	0.500	11 1111 1111	01 1111 1111
512	0	0	10 0000 0000	00 0000 0000
511	−0.00195	−0.000978	01 1111 1111	11 1111 1111
0	−1.00	−0.5000	00 0000 0000	10 0000 0000

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_{INPUT}) due only to aperture jitter (t_A) can be calculated with the following equation

$$SNR\ Degradation = 20 \times \log_{10} [2 \times \pi \times f_{INPUT} \times t_A]$$

In the equation, the rms aperture jitter, t_A, represents the root-sum square of all jitter sources, which include the clock input, analog input signal, and ADC aperture jitter specification. Undersampling applications are particularly sensitive to jitter.

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9215. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

Power Dissipation and Standby Mode

As shown in Figure 35, the power dissipated by the AD9215 is proportional to its sample rate. The digital power dissipation does not vary substantially between the three speed grades because it is determined primarily by the strength of the digital drivers and the load on each output bit. The maximum DRVDD current can be calculated as

$$I_{DRVDD} = V_{DRVDD} \times C_{LOAD} \times f_{CLOCK} \times N$$

where N is the number of output bits, 10 in the case of the AD9215. This maximum current is for the condition of every output bit switching on every clock cycle, which can only occur for a full-scale square wave at the Nyquist frequency, $f_{CLOCK}/2$. In practice, the DRVDD current is established by the average number of output bits switching, which are determined by the encode rate and the characteristics of the analog input signal.

Digital power consumption can be minimized by reducing the capacitive load presented to the output drivers. The data in Figure 35 was taken with a 5 pF load on each output driver.

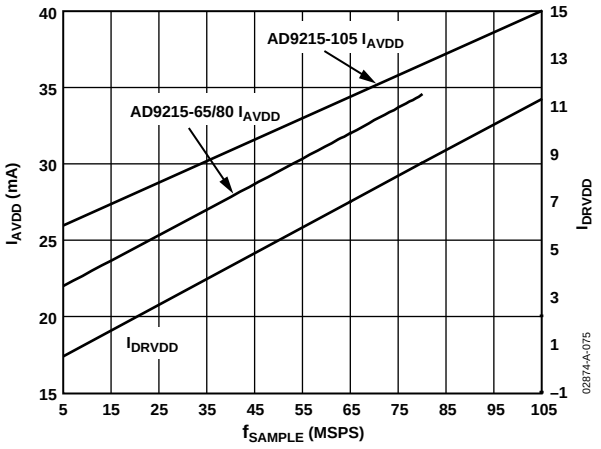


Figure 35. Supply Current vs. f_{SAMPLE} for f_{IN} = 10.3 MHz

The analog circuitry is optimally biased so that each speed grade provides excellent performance while affording reduced power consumption. Each speed grade dissipates a baseline power at low sample rates that increases linearly with the clock frequency.

By asserting the PDWN pin high, the AD9215 is placed in standby mode. In this state, the ADC typically dissipates 1 mW if the CLK and analog inputs are static. During standby, the output drivers are placed in a high impedance state. Reasserting the PDWN pin low returns the AD9215 into its normal operational mode.

In standby mode, low power dissipation is achieved by shutting down the reference, reference buffer, and biasing networks. The

decoupling capacitors on REFT and REFB are discharged when entering standby mode and then must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in standby mode, and shorter standby cycles result in proportionally shorter wake-up times. With the recommended 0.1 µF and 10 µF decoupling capacitors on REFT and REFB, it takes approximately one second to fully discharge the reference buffer decoupling capacitors and 7 ms to restore full operation.

Digital Outputs

The AD9215 output drivers can be configured to interface with 2.5 V or 3.3 V logic families by matching DRVDD to the digital supply of the interfaced logic. The output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause current glitches on the supplies that may affect converter performance. Applications requiring the ADC to drive large capacitive loads or large fanouts may require external buffers or latches.

Timing

The AD9215 provides latched data outputs with a pipeline delay of five clock cycles. Data outputs are available one propagation delay (t_{OD}) after the rising edge of the clock signal. Refer to Figure 2 for a detailed timing diagram.

The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9215; these transients can detract from the converter's dynamic performance.

The lowest typical conversion rate of the AD9215 is 5 MSPS. At clock rates below 5 MSPS, dynamic performance may degrade.

Voltage Reference

A stable and accurate 0.5 V voltage reference is built into the AD9215. The input range can be adjusted by varying the reference voltage applied to the AD9215, using either the internal reference or an externally applied reference voltage. The input span of the ADC tracks reference voltage changes linearly. Maximum SNR and DNL performance is achieved with the AD9215 set to the largest input span of 2 V p-p.

Internal Reference Connection

A comparator within the AD9215 detects the potential at the SENSE pin and configures the reference into four possible states, which are summarized in Table 1. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 36), setting VREF to 1 V. Connecting the SENSE pin to the VREF pin switches the amplifier output to the SENSE pin, configuring the internal op amp circuit as a voltage follower and providing a 0.5 V reference output. If an external resistor divider is connected as shown in Figure 37, the switch is again set to the SENSE pin. This puts the reference amplifier in a noninverting mode with the VREF output defined as

$$VREF = 0.5 \times \left(1 + \frac{R2}{R1}\right)$$

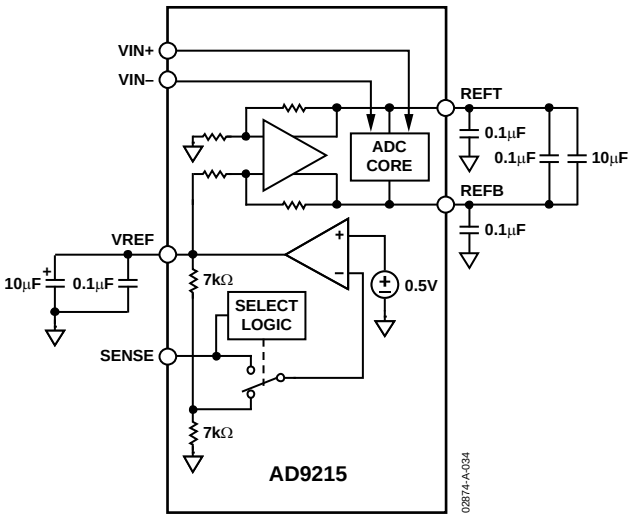


Figure 36. Internal Reference Configuration

In all reference configurations, REFT and REFB drive the ADC conversion core and establish its input span. The input range of the ADC always equals twice the voltage at the reference pin for either an internal or an external reference.

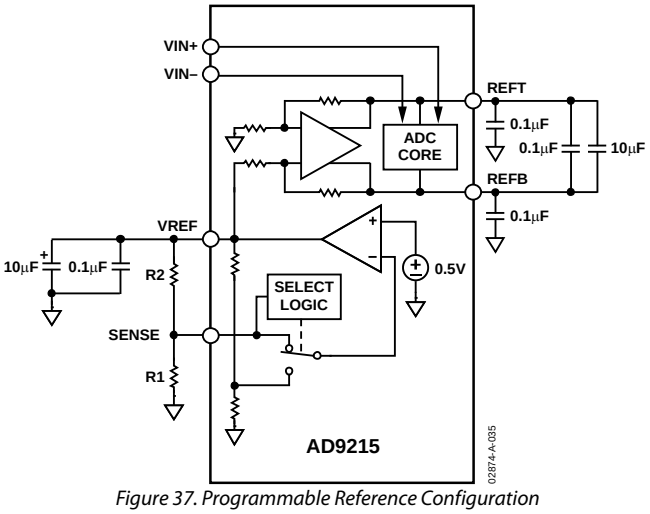


Figure 37. Programmable Reference Configuration

If the internal reference of the AD9215 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 38 depicts how the internal reference voltage is affected by loading.

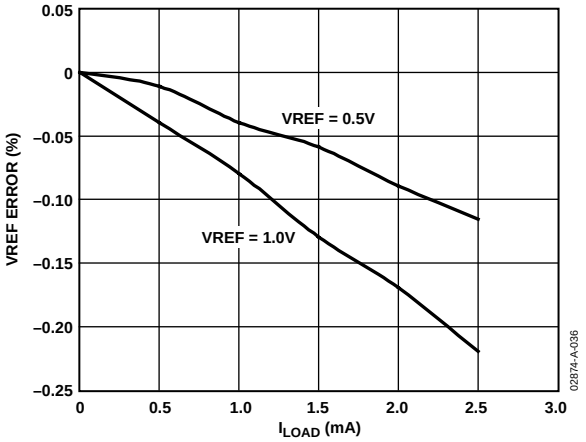


Figure 38. VREF Accuracy vs. Load

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. When multiple ADCs track one another, a single reference (internal or external) may be necessary to reduce gain matching errors to an acceptable level. A high precision external reference may also be selected to provide lower gain and offset temperature drift. Figure 39 shows the typical drift characteristics of the internal reference in both 1 V and 0.5 V modes.

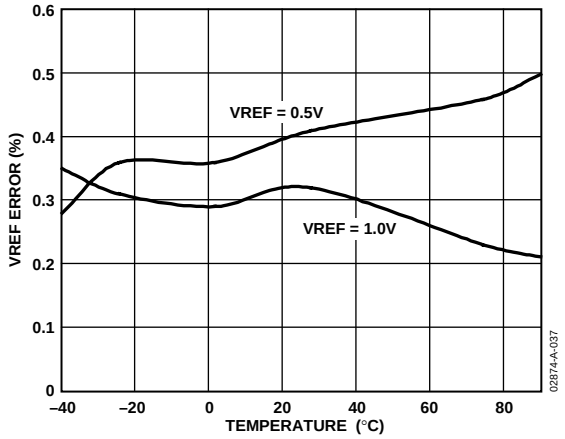


Figure 39. Typical VREF Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7 kΩ load. The internal buffer still generates the positive and negative full-scale references, REFT and REFB, for the ADC core. The input span is always twice the value of the reference voltage; therefore, the external reference must be limited to a maximum of 1 V.

Operational Mode Selection

As discussed earlier, the AD9215 can output data in either offset binary or twos complement format. There is also a provision for enabling or disabling the clock duty cycle stabilizer (DCS). The MODE pin is a multilevel input that controls the data format and DCS state. For best ac performance, enabling the duty cycle stabilizer is recommended for all applications. The input threshold values and corresponding mode selections are outlined in Table 9.

As detailed in Table 9, the data format can be selected for either offset binary or twos complement.

Table 9. Mode Selection

MODE Voltage	Data Format	Duty Cycle Stabilizer
AVDD	Twos Complement	Disabled
2/3 AVDD	Twos Complement	Enabled
1/3 AVDD	Offset Binary	Enabled
AGND (Default)	Offset Binary	Disabled

The MODE pin is internally pulled down to AGND by a 20 kΩ resistor.

EVALUATION BOARD

The AD9215 evaluation board is no longer in production. The following evaluation board documentation is provided for informational purposes only.

The AD9215 evaluation board provides all of the support circuitry required to operate the ADC in its various modes and configurations. The converter can be driven differentially through an AD8351 driver, a transformer, or single-ended. Separate power pins are provided to isolate the DUT from the support circuitry. Each input configuration can be selected by proper connection of various jumpers (refer to the schematics). Figure 40 shows the typical bench characterization setup used to evaluate the ac performance of the AD9215. It is critical that signal sources with very low phase noise (<1 ps rms jitter) be used to realize the ultimate performance of the converter. Proper filtering of the input signal, to remove harmonics and lower the integrated noise at the input, is also necessary to achieve the specified noise performance.

Complete schematics and layout plots follow that demonstrate the proper routing and grounding techniques that should be applied at the system level.

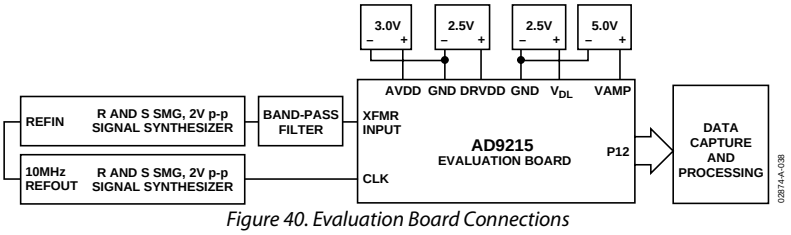


Figure 40. Evaluation Board Connections

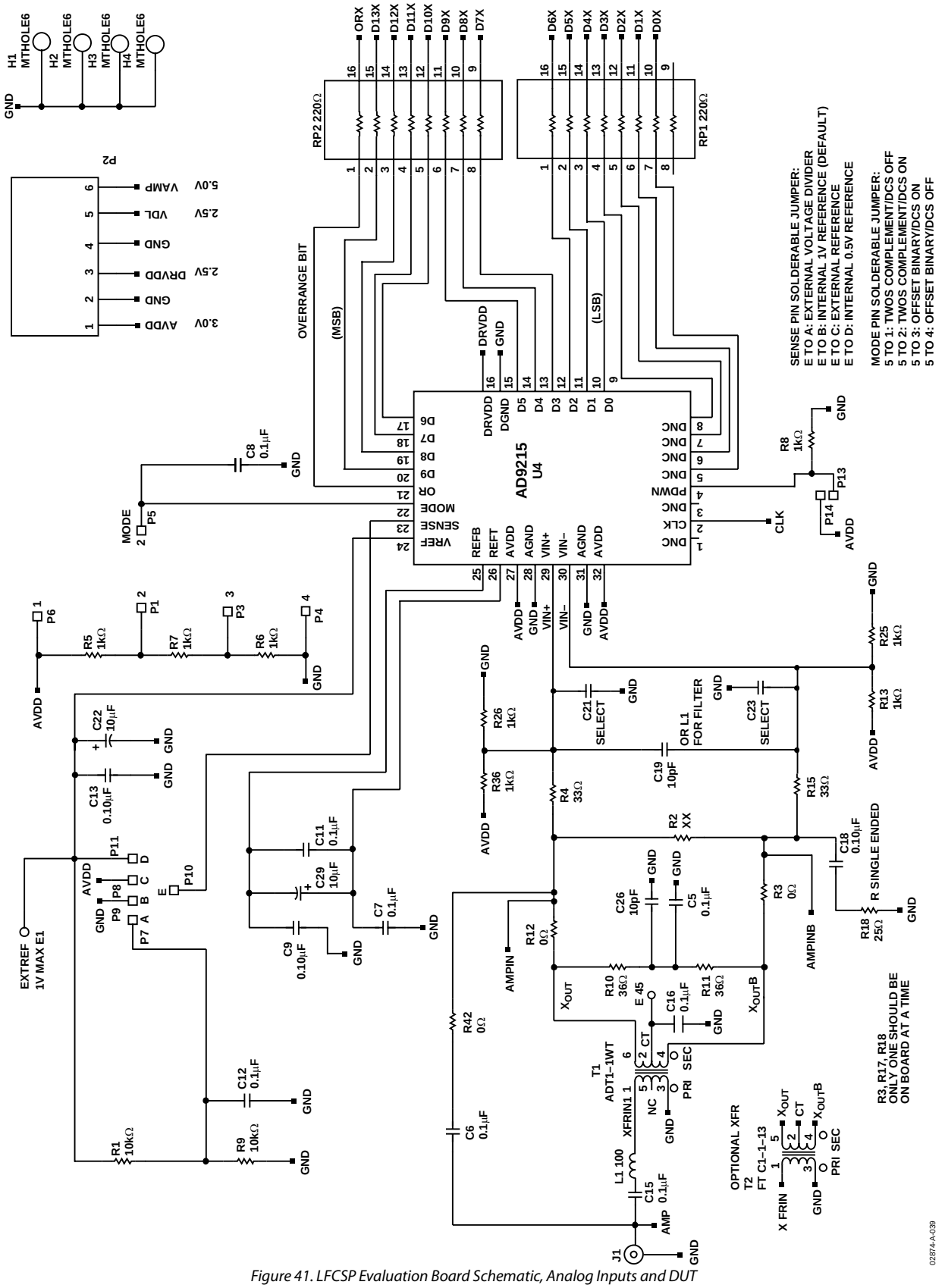


Figure 41. LFCSP Evaluation Board Schematic, Analog Inputs and DUT

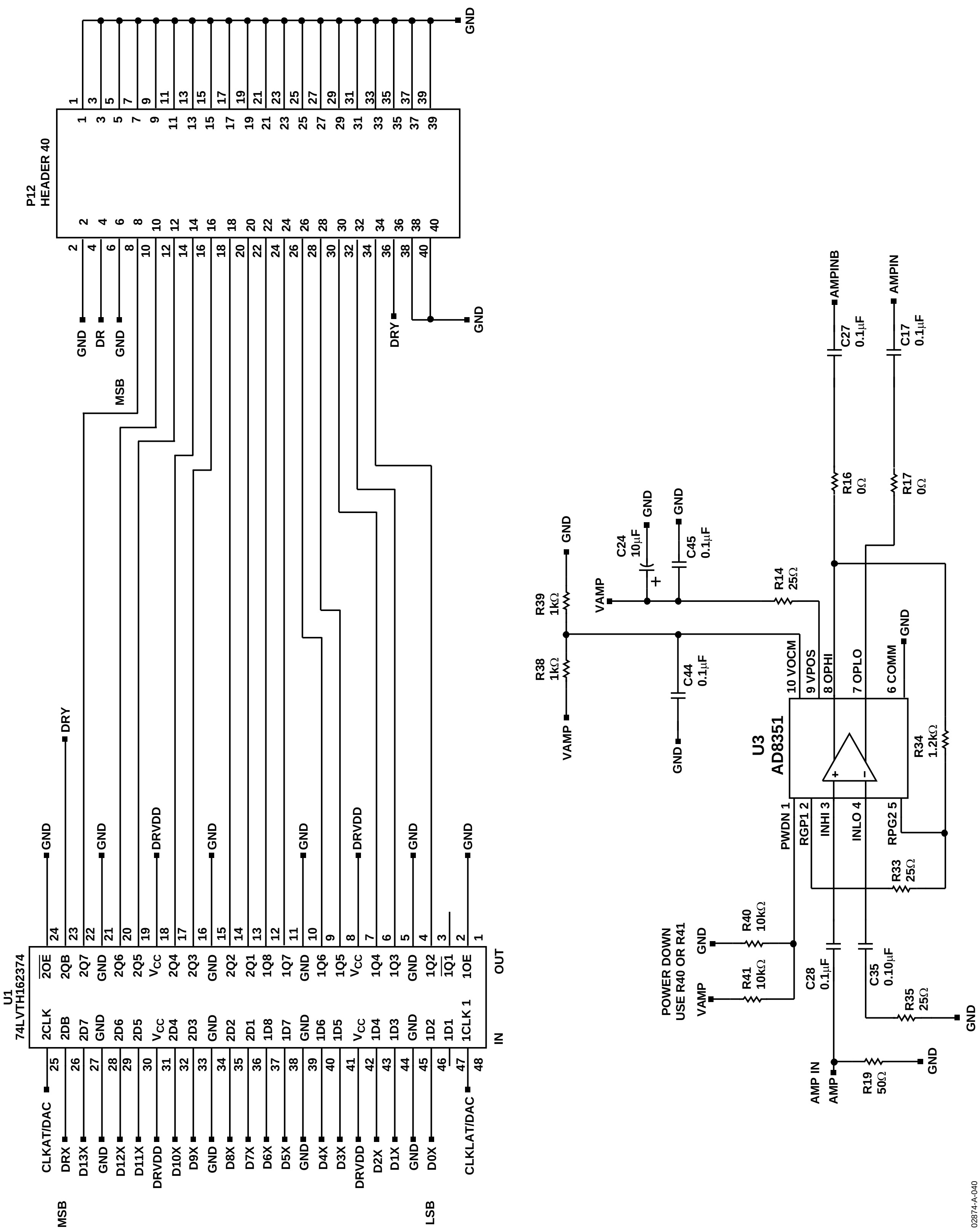


Figure 42. LFCSP Evaluation Board, Digital Path

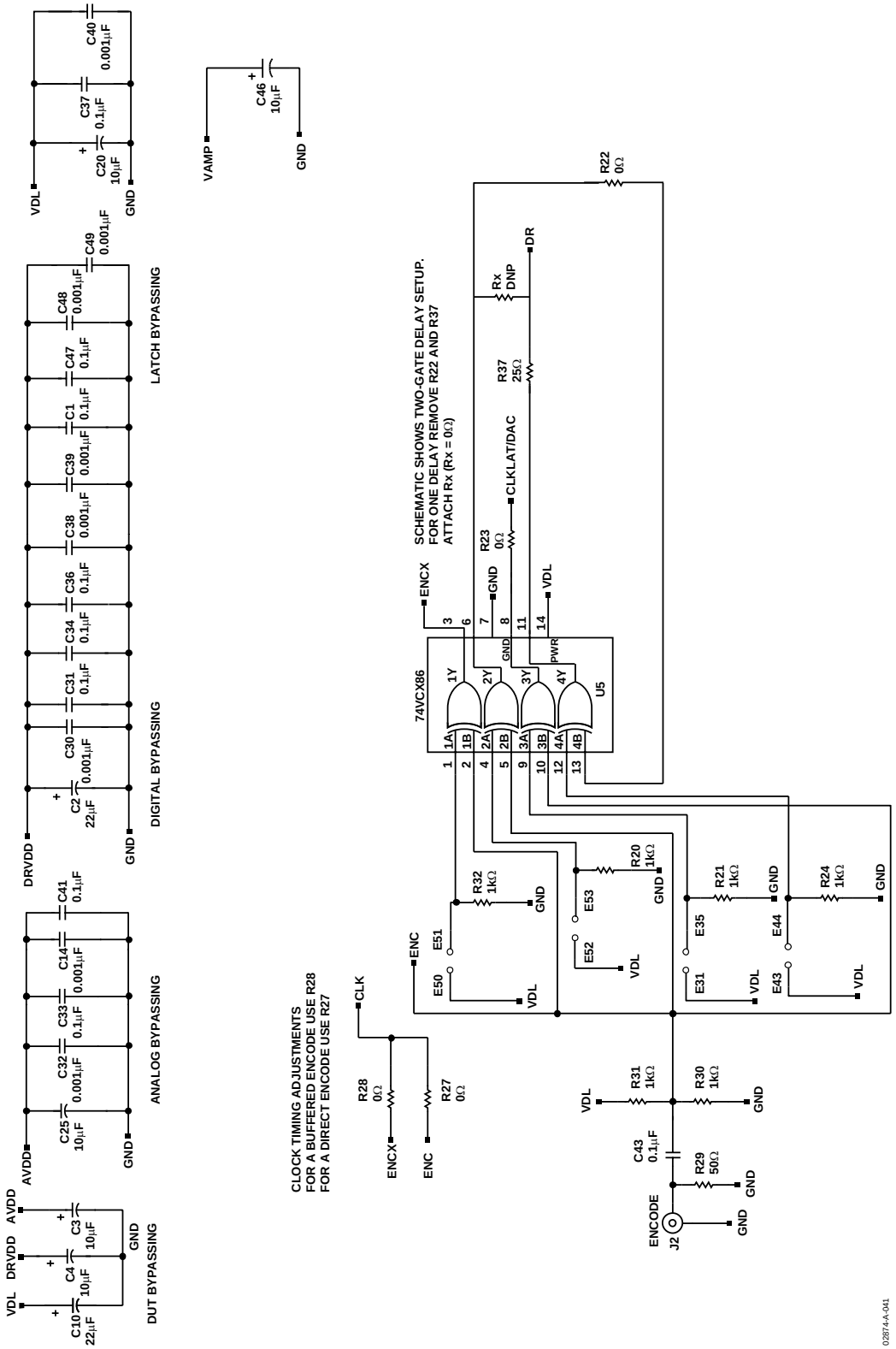


Figure 43. LFCSP Evaluation Board Schematic, Clock Input

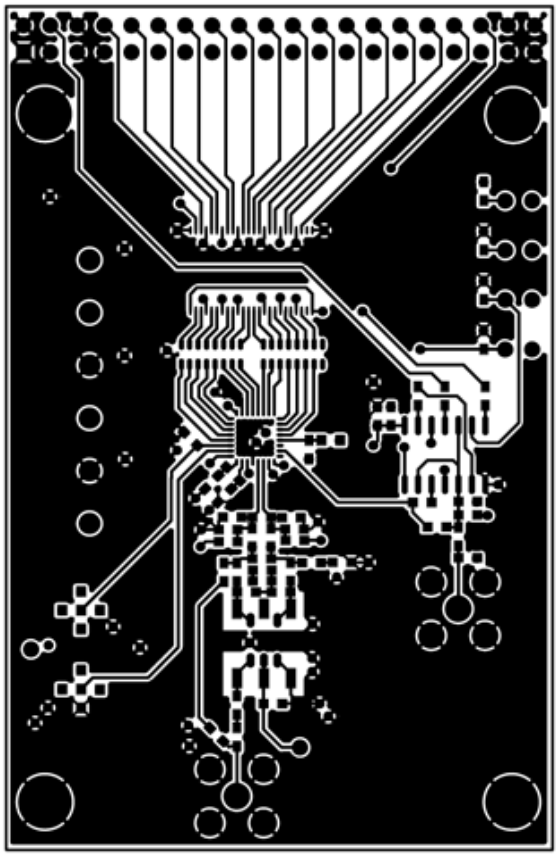


Figure 44. LFCSP Evaluation Board Layout, Primary Side

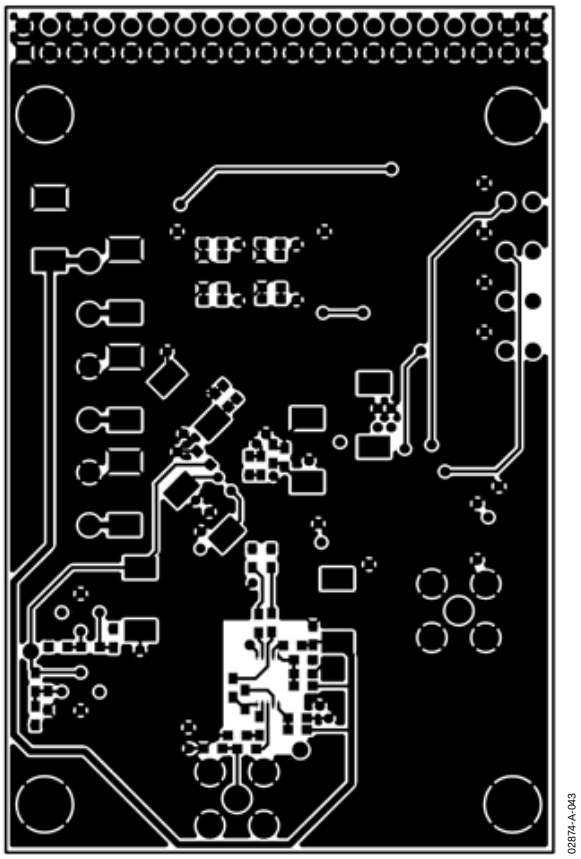


Figure 45. LFCSP Evaluation Board Layout, Secondary Side

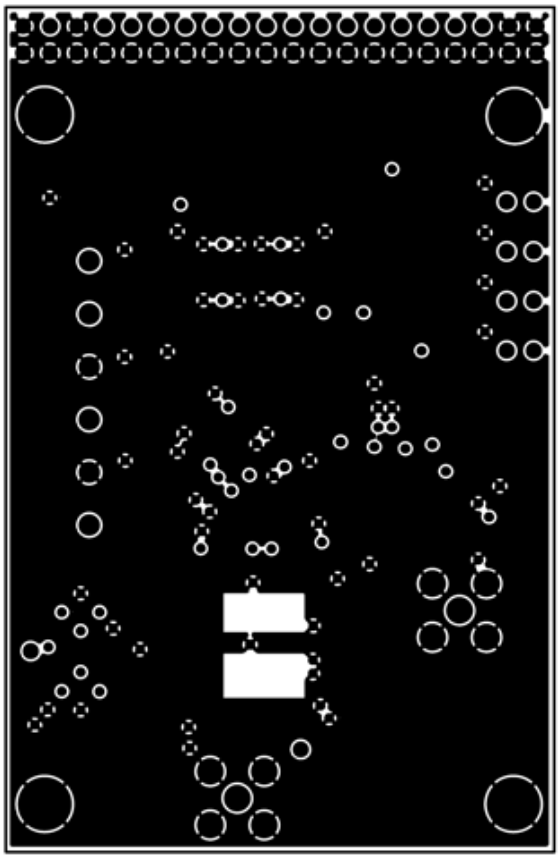


Figure 46. LFCSP Evaluation Board Layout, Ground Plane

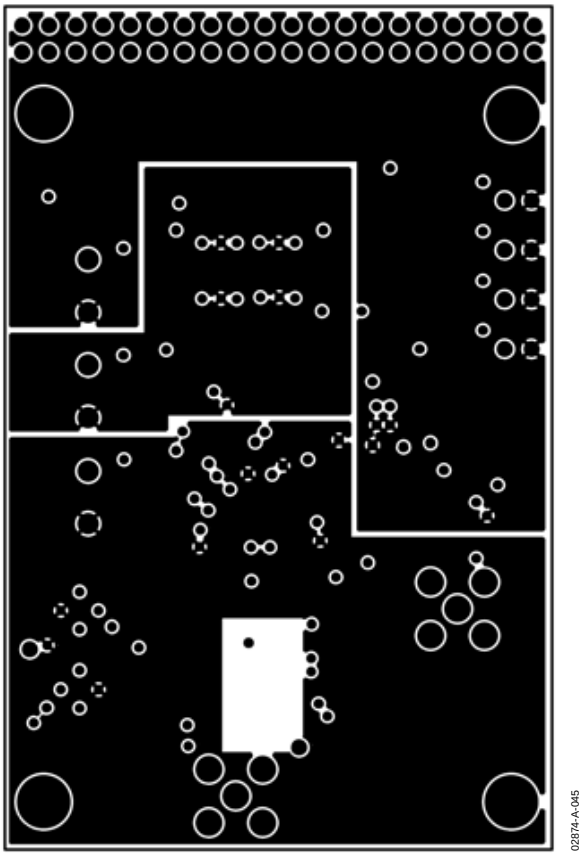


Figure 47. LFCSP Evaluation Board Layout, Power Plane

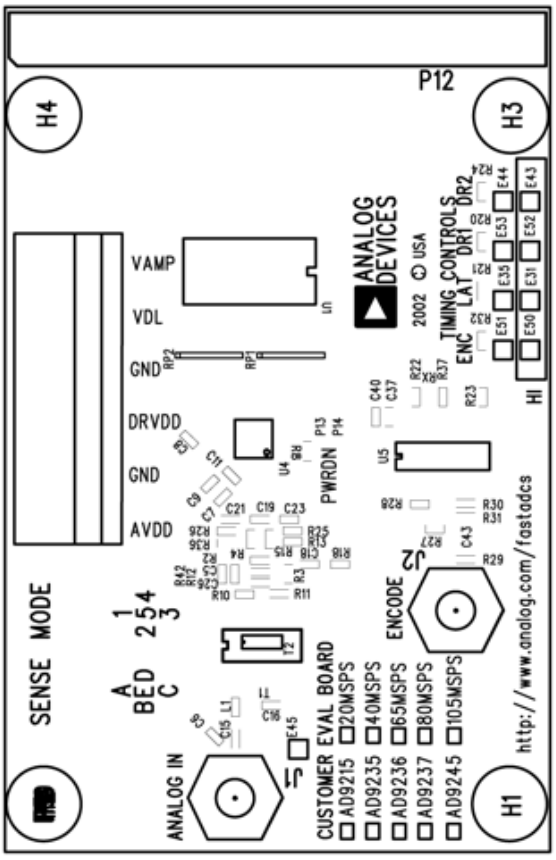


Figure 48. LFCSP Evaluation Board Layout, Primary Silkscreen

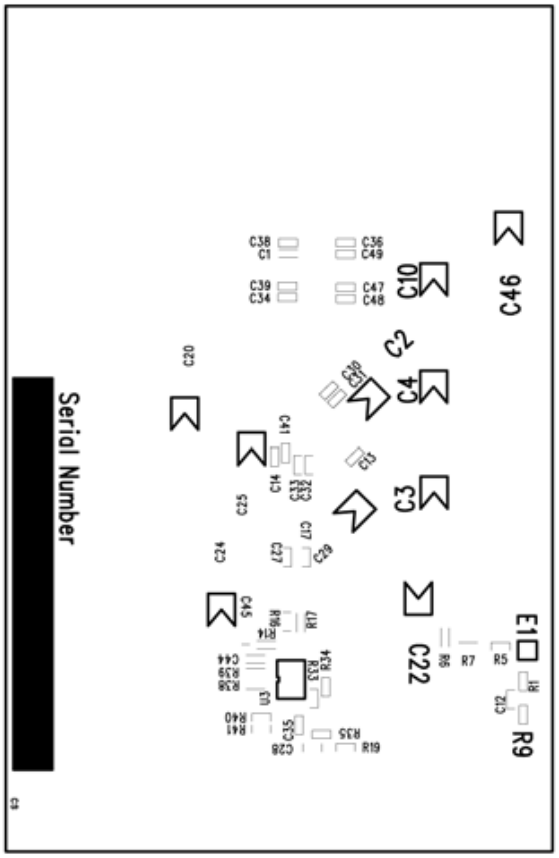


Figure 49. LFCSP Evaluation Board Layout, Secondary Silkscreen

Table 10. LFCSP Evaluation Board Bill of Materials (BOM)

Item	Qty	Omit[1]	Reference Designator	Device	Package	Value	Recommended Vendor/ Part Number
1	18		C1, C5, C7, C8, C9, C11, C12, C13, C15, C16, C31, C33, C34, C36, C37, C41, C43, C47	Chip Capacitor	0603	0.1 µF	
		8	C6, C18, C27, C17, C28, C35, C45, C44				
2	8		C2, C3, C4, C10, C20, C22, C25, C29	Tantalum Capacitor	TAJD	10 µF	
		2	C46, C24,				
3	8		C14, C30, C32, C38, C39 C40, C48, C49	Chip Capacitor	0603	0.001 µF	
4	1		C19	Chip Capacitor	0603	10 pF	
	2		C21, C23				
5	1		C26	Chip Capacitor	0603	10 pF	
6	9		E31, E35, E43, E44, E50, E51, E52, E53	Header	EHOLE		Jumper Blocks
		2	E1, E45				
7	2		J1, J2	SMA Connector/50 Ω	SMA		
8	1		L1	Inductor	0603	10 nH	Coilcraft/0603CS-10NXGBU
9	1		P2	Terminal Block	TB6		Wieland/25.602.2653.0 z5-530-0625-0
10	1		P12	Header Dual 20-Pin RT Angle	HEADER40		Digi-Key S2131-20-ND
11	5		R3, R12, R23, R18, RX	Chip Resistor	0603	0 Ω	
		6	R37, R22, R42, R16, R17, R27				
12	2		R4, R15	Chip Resistor	0603	33 Ω	
13	14		R5, R6, R7, R8, R13, R20, R21, R24, R25, R26, R30, R31, R32, R36	Chip Resistor	0603	1 Ω	
14	2		R10, R11	Chip Resistor	0603	36 Ω	
15	1		R29	Chip Resistor	0603	50 Ω	
		1	R19				
16	2		RP1, RR2	Resistor Pack	R_742	220 Ω	Digi-Key CTS/742C163220JTR
17	1		T1	ADT1-1WT	AWT1-T1		Mini-Circuits
18	1		U1	74LVTH162374 CMOS Register	TSSOP-48		
19	1		U4	AD9215BCP ADC (DUT)	CSP-32		Analog Devices, Inc.
20	1		U5	74VCX86M	SOIC-14		Fairchild
21	1		PCB	AD9XXBCP/PCB	PCB		Analog Devices, Inc.
22		1	U3	AD8351 Op Amp	MSOP-8		Analog Devices, Inc.
23		1	T2	MACOM Transformer	ETC1-1-13	1-1 TX	MACOM/ETC1-1-13
24		5	R9, R1, R2, R38, R39	Chip Resistor	0603	Select	
25		3	R18, R14, R35	Chip Resistor	0603	25 Ω	
26		2	R40, R41	Chip Resistor	0603	10 kΩ	
27		1	R34	Chip Resistor		1.2 kΩ	
28		1	R33	Chip Resistor		110 Ω	

[1] These items are included in the PCB design but are omitted at assembly.

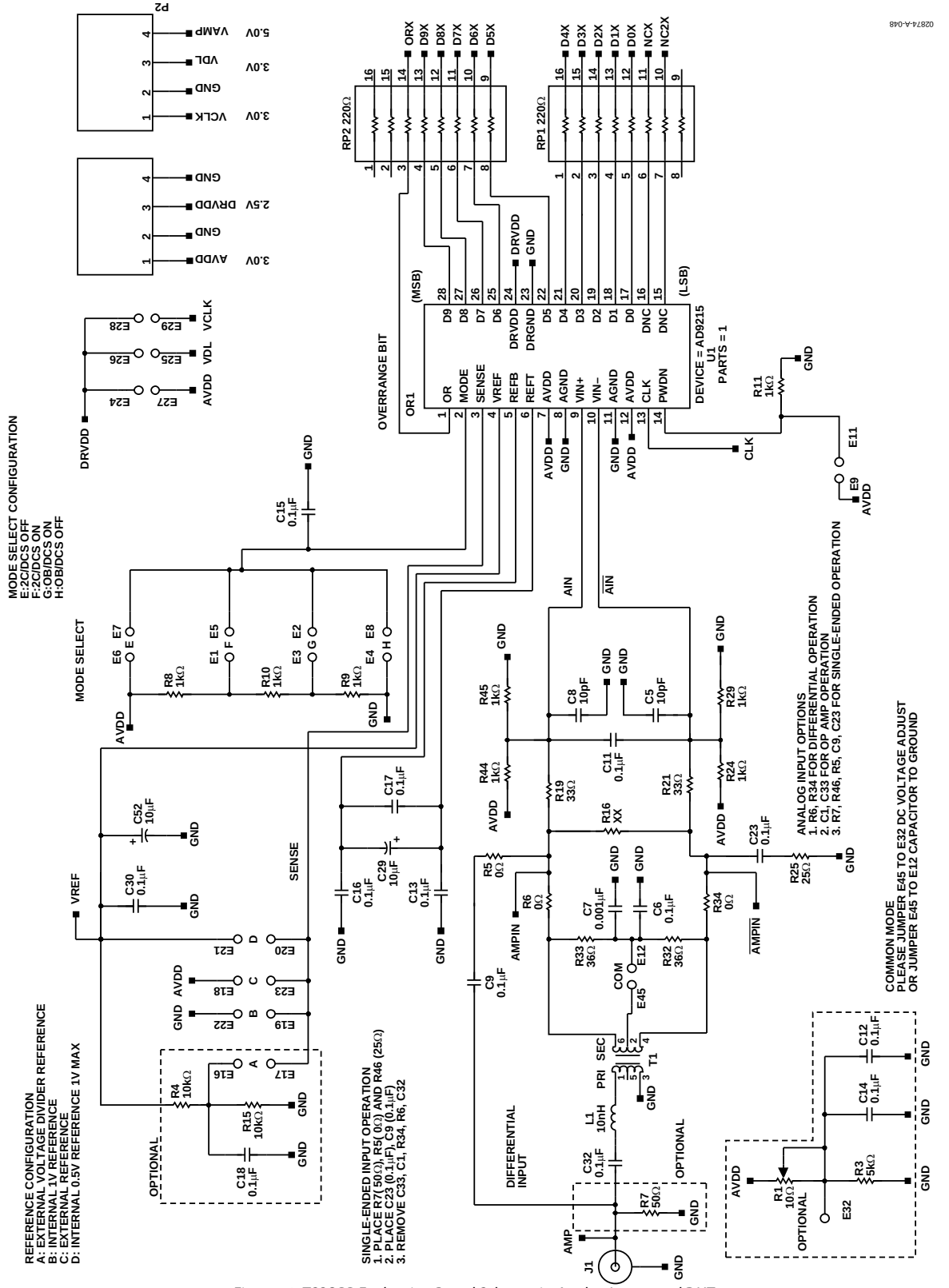


Figure 50. TSSOPP Evaluation Board Schematic, Analog Inputs and DUT

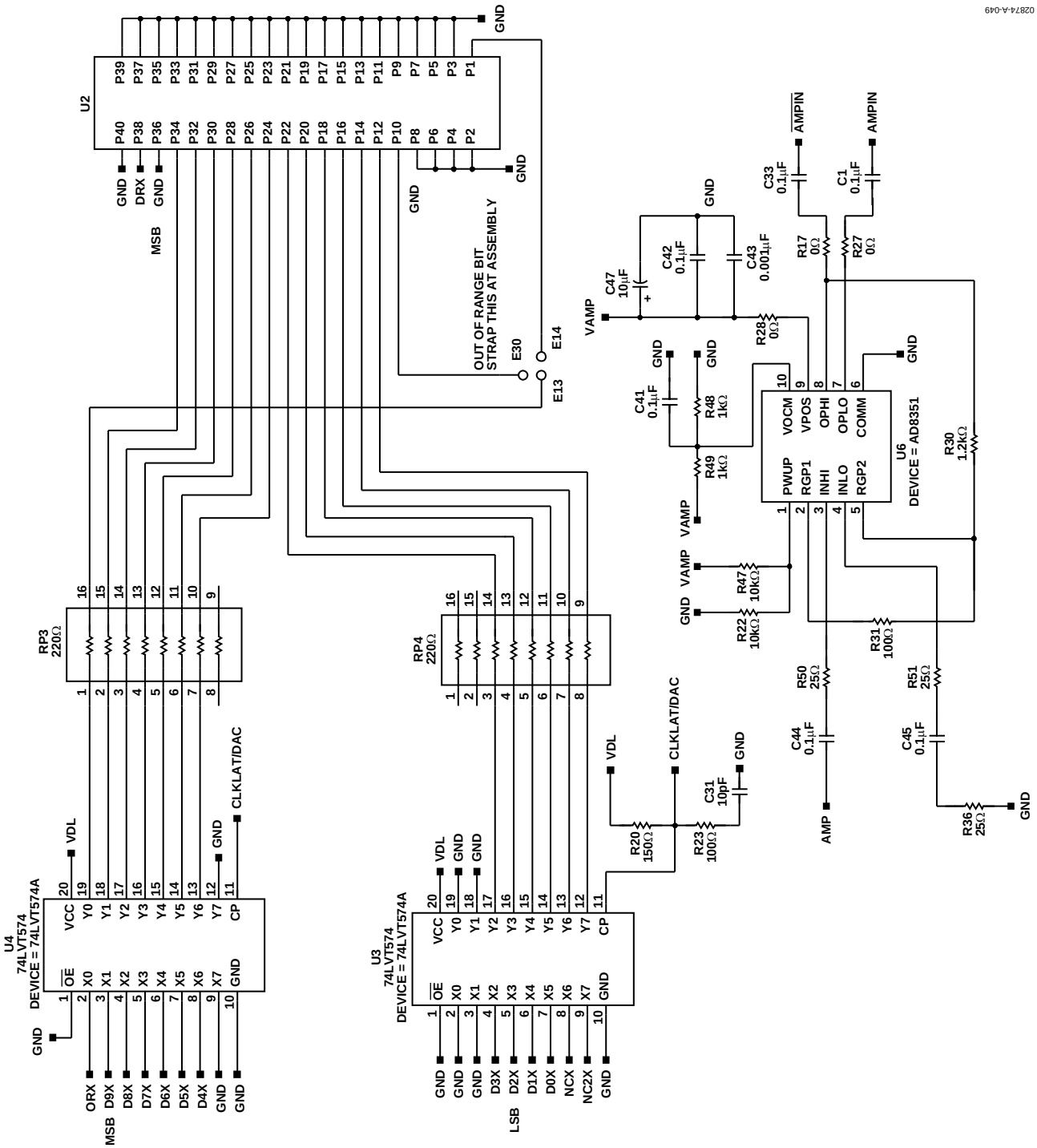


Figure 51. TSSOP Evaluation Board, Digital Path

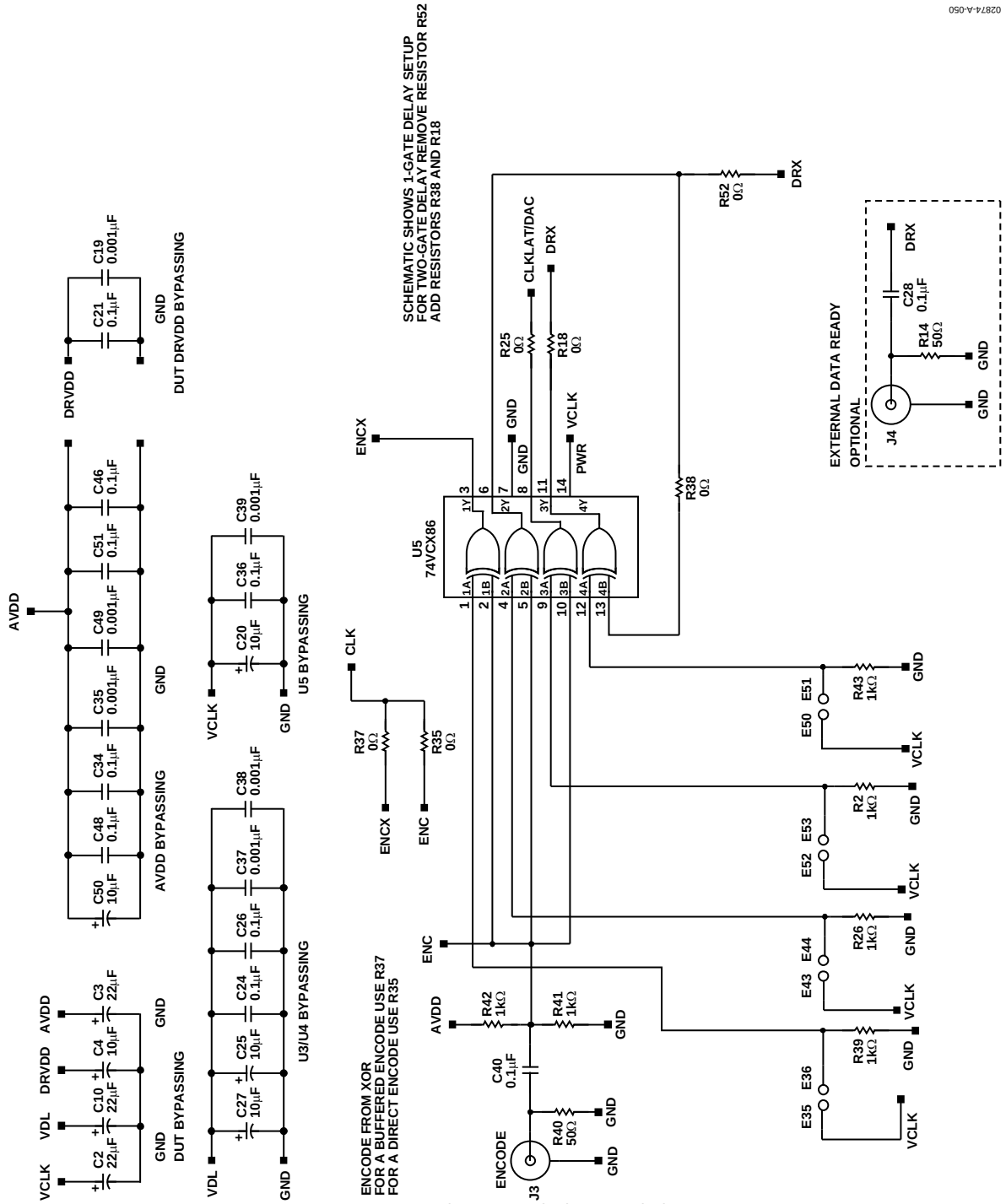


Figure 52. TSSOP Evaluation Board Schematic, Clock Input

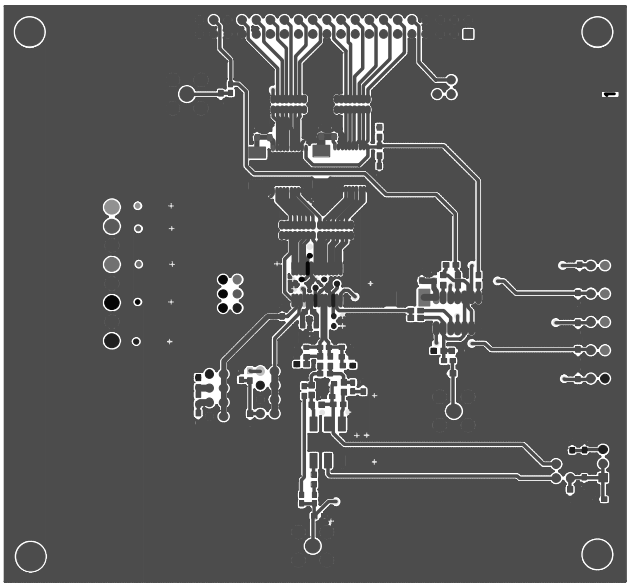


Figure 53. TSSOP Evaluation Board Layout, Primary Side

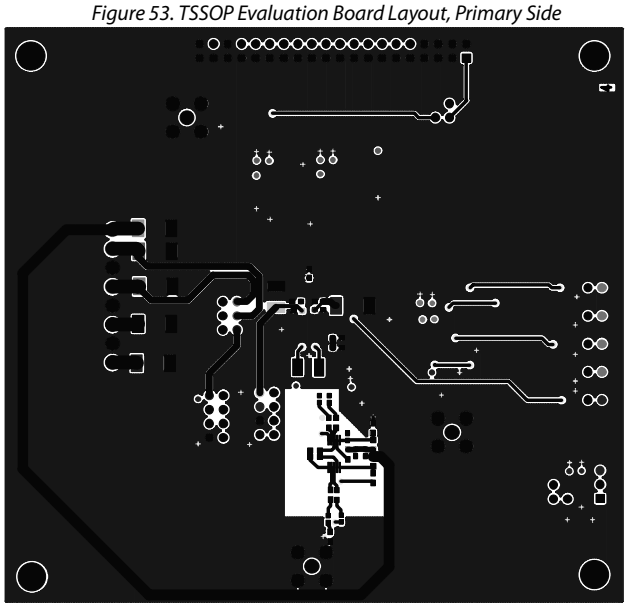


Figure 54. TSSOP Evaluation Board Layout, Secondary Side

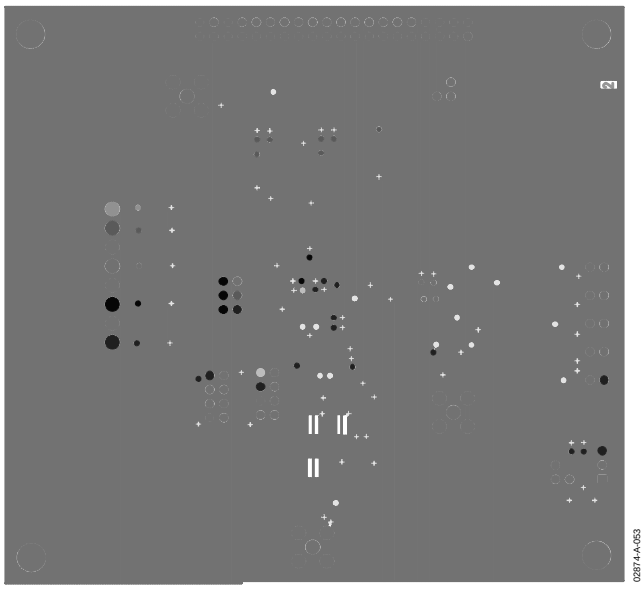


Figure 55. TSSOP Evaluation Board Layout, Ground Plane

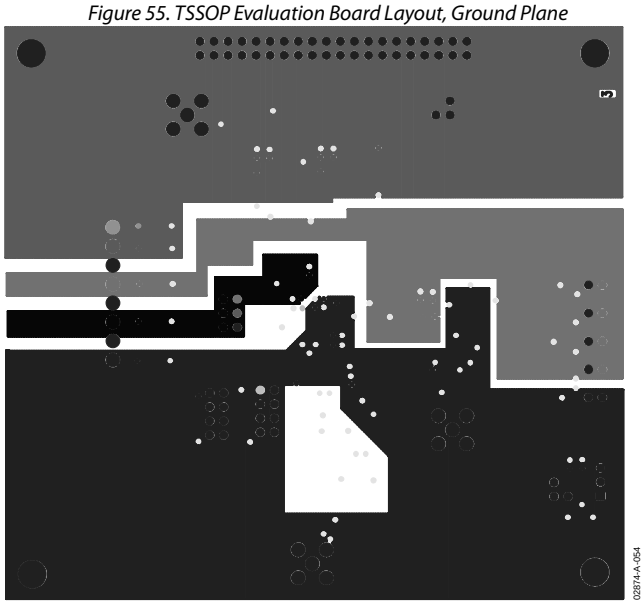


Figure 56. TSSOP Evaluation Board Layout, Power Plane

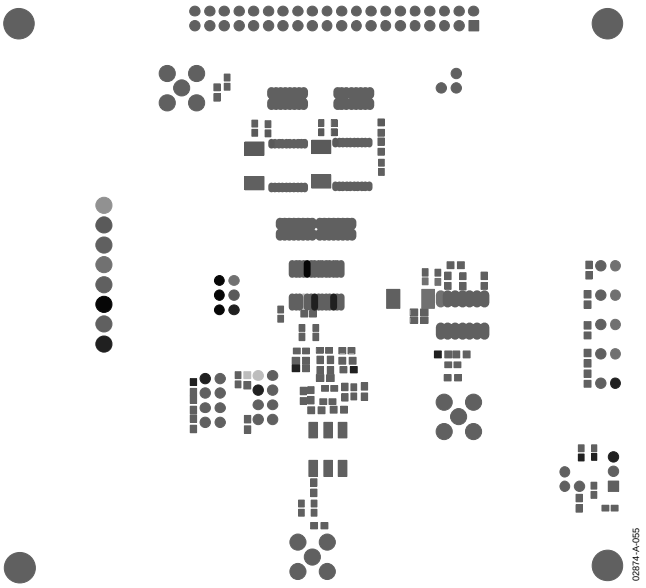


Figure 57. TSSOP Evaluation Board Layout, Primary Silkscreen

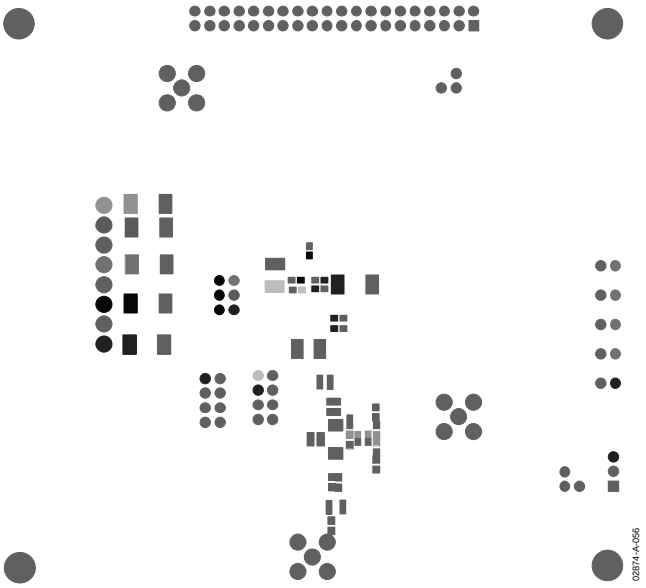


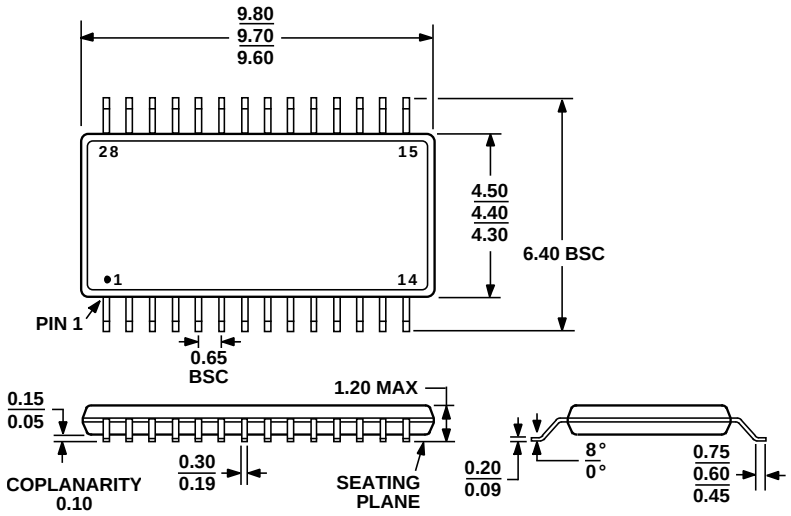
Figure 58. TSSOP Evaluation Board Layout, Secondary Silkscreen

Table 11. TSSOP Evaluation Board Bill of Materials (BOM)

Item	Qty.	Omit	Reference Designator	Device	Package	Value	Recommended Vendor/Part No.
1	11		C2 to C4, C10, C20, C25, C27, C29, C47, C50, C52	Tantalum Capacitor	TAJD	10 µF	
			C47				
2	2		C5,C8	Chip Capacitor	0603	10 pF	
		1	C31				
3	15		C6, C9, C13, C15 to C18, C21, C24, C26, C30, C32, C34, C36, C40, C46, C48, C51	Chip Capacitor	0603	0.1 µF	
4		3	C12, C14, C23, C28	Chip Capacitor	0603	Select	
5	8		C7, C19, C35, C19, C37 to C39, C49	Chip Capacitor	0603	0.001 µF	
6		6	C1,C33, C41 to C42, C44 to C5	BCAP0402	0402	0.1 µF	
7		1	C43	BCAP0402	0402	0.001 µF	
8		1	C11	BCAP0603	0603	Select	
9	11		R2, R8 to R11, R24, R26, R29, R39, R41 to R45	BRES603	0603A	1 kΩ	
		2	R48, R49				
10	4		R6, R25, R34, R37	BRES603	0603A	0 Ω	
		8	R5, R35, R17 to R18, R27 to R28, R38, R52				
11	2		R7, R40	BRES603	0603A	50 Ω	
		1	R14				
12	2		R19, R21	BRES603	0603A	33 Ω	
13	2		R32, R33	RES0603	0603A	36 Ω	
14	1		R16	BRES603	0603	Select	
15	2		R4, R15,	BRES603	0603	10 kΩ	
16		4	R20, R22 to R23, R47	BRES603	0603A	Select	
17		2	R48, R49	BRES603	0603	1 kΩ	
18		4	R36, R46, R50 to R51	BRES603	0603	25 Ω	
19		1	R31	BRES603	0603	100 Ω	
20		1	R30	BRES603	0603	1.2 kΩ	
21		1	R3	BRES603	0603	5 kΩ	
22		1	R1	Potentiometer	RJ24FW	10 kΩ	
23	4		RP1 to RP4	Resister Pack	220Ω	742C163221	

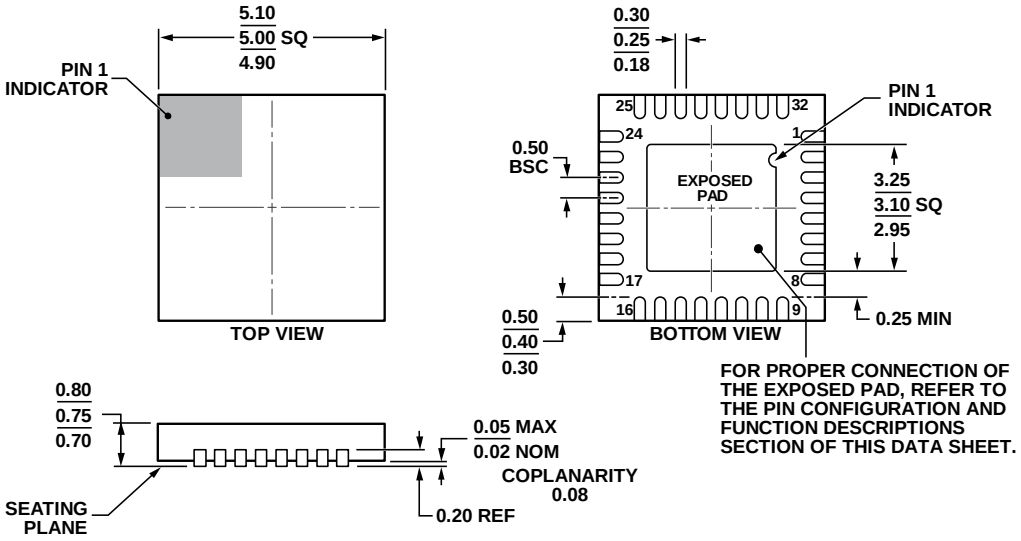
Item	Qty.	Omit	Reference Designator	Device	Package	Value	Recommended Vendor/Part No.
24	1		L1	Chip Inductor	0603	10 nH	Coilcraft/0603CS-10NXGBU
25	1		T1	1:1 RF Transformer	CD542		Mini-Circuits AWT1-1T
26	1		U1	ADC	28TSSOP		Analog Devices, Inc. AD9215
27	1		U2	Right Angle 40-Pin Header			Samtec TSW-120-08-T-D-RA
28	2		U3, U4	Octal D-Type Flip-Flop			Fairchild 74LVT57MSA
29	1		U5	Quad XOR Gate	SO14		Fairchild 74VCX86M
30		1	U6	High Speed Amplifier	SOMB10		Analog Devices, Inc. AD8351ARM
31	2		J1, J3	SMB Connecter	SMBP		
		1	J4				
32	2		P1, P2	Power Connector	PTMICRO4		Weiland Z5.531.3425.0 Posts 25.602.5453.0 Top
33	26		E1/E5, E2/E3, E4/E8, E9/E11, E6/E7, E16/E17, E19/E22, E18/E23, E21/20, E35/E51, E36/E50, E43/E53, E44/E52	Headers/Jumper Blocks			TSW-120-07-G-S SMT-100-BK-G
34		12	E24/E27, E25/E26, E28/E29, E13/E14/E30, E12/E32/E45	Wirehole			

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AE

Figure 59. 28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

Figure 60. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9215BRUZ-65	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9215BRUZ-80	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9215BRUZ-105	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9215BRUZRL7-65	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9215BRUZRL7-80	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9215BRUZRL7-105	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9215BCPZ-65	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-32-7
AD9215BCPZ-80	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-32-7
AD9215BCPZ-105	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-32-7

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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