Testing and specifying FAST logic AN202

INTRODUCTION

FAST™ is a second generation Schottky logic family that utilizes advanced oxide-isolation techniques to increase the speed and decrease the power dissipation beyond the levels achievable with conventional junction isolated families. The improved performance of the family is exhibited in two ways — first, the speed and power characteristics of the devices are improved, and second, the conditions under which speed and power are specified are much tighter. For instance, LS and S TTL families offer AC limits only at a nominal +5.00V V_{CC} supply voltage and at room temperature, 25°C. By contrast, FAST guarantees improved AC performance and specifies that performance over a supply variation of +5.00V ±10% and at temperatures from 0°C to 70°C. Thus the designer no longer needs to derate his propagation delays from the data sheet limits to compensate for speed degradation over the temperature range.

With every advance of this magnitude, there arise new considerations that must be kept in mind both by the system designer and the user setting up test procedures. FAST is no exception, and it is these considerations that will be addressed in this application note. This paper represents an attempt to describe the way the FAST logic parts are specified, why they are specified in the way they are, and how the parts may be tested in the qualification lab and at incoming inspection to verify their performance.

THE FAST DATA SHEET PHILOSOPHY

Philips Semiconductors FAST data sheets have been configured with an eye to quick usability … they are self contained and should require no reference to other sections for information. The typical propagation delays listed at the top of the page are the average between t_{PLH} and t_{PHL} for the most significant data path through the part. In the case of clocked products, this is sometimes the maximum frequency of operation, but in any event, this number is a 5.00V – 25°C typical specification. The I_{CC} typical current is shown in that same specification block is the average current (in the case of a gate, this will be the average of the I_{CCH} and I_{CCL} currents) at room temperature and V_{CC} = 5.00V. It represents the total current through the package, not the **current through individual functions**.

Other considerations are the Fanout and Loading tables. Some manufacturers relate these numbers in therms of 7400 gate loads … Philips Semiconductors feels that FAST is unlikely to be mixed with other logic families and so gives the loading factors in terms of FAST unit loads. A FAST unit load is defined to be 0.6mA in the Low state and 20μA in the High state. Thus in the case of the 74F00 gate, the inputs are specified as 1 Ful (FAST unit load) each … the outputs need a little explanation. The standard FAST output is specified with an I_{OL} sink current of 20mA and an I_{OH} of +1.0mA. Thus the fanout of this gate in the Low state is 20mA/0.6mA or 33 FAST unit loads. In the High state the fanout is 1mA/20μA or 50 FAST unit loads. In each case, the Fanout and Loading Table on the Philips data sheets states the High/Low fanout numbers … thus the 74F00 output fanout is specified as 50/33 Ful.

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings table carries the maximum limits to which the part can be subjected without damaging it … there is no implication that the part will function at these extreme conditions. Thus, specifications such as the most negative voltage that may be applied to the outputs only guarantees that if less than –0.5V is applied to the output pin, after that voltage is removed the part will still be functional and its useful life will not have been shortened — it is difficult to imagine the meaning of the term “functionality” WHILE that voltage is applied to the output.

Input voltage and output voltage specification in this table reflect the device breakdown voltages in the positive direction (+7.0V) and the effect of the clamping diodes in the negative direction (–0.5V).

RECOMMENDED OPERATING CONDITIONS

The Recommended Operating Conditions table has a dual purpose. In one sense, it sets some environmental conditions (operating free-air temperature), and in another, it sets the conditions under which the limits set forth in the DC Electrical Characteristics table and AC Electrical Characteristics table will be met. Another way of looking at this table is to think of it, not as a set of limits guaranteed by Philips Semiconductors, but as the conditions Philips Semiconductors uses to test the parts and guarantee that they will then meet the limits set forth in the DC and AC Electrical Characteristics tables.

Some care must be used in interpreting the numbers in this table. Philips Semiconductors feels strongly that the specifications set forth in a data sheet should reflect as accurately as possible the operation of the part in an actual system. In particular, the input threshold values of V_{IH} and V_{IL} can be tested by the user with parametric test equipment … if V_{IH} and V_{IL} are applied to the inputs, the outputs will be at the voltages guaranteed by the DC Electrical Characteristics table providing that there is adequate grounding and the input voltages are free from noise, otherwise a guardbanded V_{IH} and V_{IL} should be used, i.e., 2.5V instead of 2.0V and 0.5V instead of 0.8V. There is a tendency on the part of some users to use V_{IH} and V_{IL} as conditions applied to the inputs to test the part for functionality in a “truth-table exerciser” mode. This frequently causes problems because of the noise present at the test head of automated test equipment. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done fairly slowly, on the order of milliseconds, and any noise present at the inputs has settled out before the outputs are measured. (This is not the case with clocked or enabled parts and poor or moderate fixturing may induce oscillations or severe ground bounce if noise is present.) But in functionality testing, the outputs are examined much faster, before the noise on the inputs is settled out and the part has assumed its final and correct output state. Since these are unloaded outputs, having faster edge rates, this causes more noise, If the outputs are loaded, the 50pF per output pin can cause substantial ground bounce. Thus V_{IH} and V_{IL} should never be used in testing the functionality of any TTL part including FAST. For these types of tests input voltages of +4.5V and 0.0V should be used for the High and Low states respectively.

In no way does this imply that the devices are noise sensitive in the final system. The use of “hard” Highs and Lows during functional testing is done primarily to (1) reduce the effects of the large amounts of noise typically present at the test heads of automated test equipment with cables that may at times reach several feet and (2) deal with testing parts exhibiting fast edge rates and 50pF per output pin. The situation in a system on a PC board is less severe than in a noisy production environment.

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DC ELECTRICAL CHARACTERISTICS

This table reflects the DC limits used by Philips Semiconductors during its testing operations and conducted under the conditions set forth under the Recommended Operating Conditions table. V_{OH}, for example, is guaranteed to be no less than 2.7V when tested with V_{CC} = +4.75V, V_{IH} = 2.0V, V_{IL} = 0.8V, across the temperature range from 0° to 70°C, and with an output current of I_{OH} = –1.0mA. In this table, one sees the heritage of the original junction isolated Schottky family … V_{OL} = 0.5V at I_{OL} = 20mA. This gives the user a guaranteed worst-case Low state noise immunity of 0.3V. In the High state the noise immunity is 0.7V worst case. Although at first glance it would seem one-sided to have greater noise immunity in the High state than in the Low, this is a useful state of affairs. Because the impedance of an output in the High state is generally much higher than in the Low state, more noise immunity in the High state is needed. This is because the noise source couples noise onto the output connection of the device — that output tries to pull the noise source down by sinking the energy to ground or to V_{CC} depending on the state. The ability of the output to do that is determined by its output impedance. The lower half of the output stage is a very low-impedance transistor which can effectively pull the noise source down. Because of the higher impedance of the upper stage of the output, it is not as effective in shunting the noise energy to V_{CC}, so that an extra 0.4V of noise immunity in the High state compensates for the higher impedance. The result is a nice balance of sink and drive current capabilities with the optimum amount of noise immunity in both states.

I_I, the maximum input current at maximum input voltage, is a measure of the input leakage current at the guaranteed minimum input breakdown voltage of 7.0V. Although some users consider this to be a test of the input breakdown itself, that voltage is typically over 15V. At room temperature, this leakage current should be less than 10µA. (This is not the case with NPN input designated parts.)

Short-Circuit Output Current is a parameter that has appeared on digital data sheets since the inception of integrated circuit logic devices, but the meaning and implications of that **specification** have totally changed. Originally, I_{OS} was an attempt to reassure the user that if a stray oscilloscope probe accidentally shorted an output to ground the device would not be damaged. In this manner, an extremely long time was associated with the I_{OS} test. However, thermally induced malfunctions could occur after several seconds of sustained test. Over a period of time, I_{OS} became a measure of the ability of an output to charge line capacitance. Assume a device is driving a long line and is in the Low state. When the output is switched High, the rise time of the output waveform is limited by the rate at which the line capacitance can be charged to its new state of V_{OH}. At the instant that the output switches, the line capacitance looks like a short to ground. I_{OS} is the current demanded by the capacitive load as the voltage begins to rise and the demand decreases. The full value of I_{OS} need only be supplied for a few hundred microseconds at most, even with 1.0µF of line capacitance tied to the output, a load that is unrealistically high by several orders of magnitude.

The effective of a large I_{OS} surge through the relatively small transistors that make up the upper part of the output stage is not serious, AS LONG AS THAT CURRENT IS LIMITED TO A SHORT DURATION. If the hard short is allowed to remain, the full I_{OS} current will flow through that output state and may cause functional failure or damage to the structure. A test induced failure may occur if the I_{OS} test time is excessive. As long as the I_{OS} condition is very brief, typically 50ms or less with automated test equipment, the local heating does not reach the point where damage or functional failures might occur. As we have already seen, this is considerably longer than the time of the effective current surge that must be supplied by the device in the case of charging line capacitance. The Philips Semiconductors data sheet limits for I_{OS} reflect the conditions that the part will see in the system — full I_{OS} spikes for extremely short periods of time. Problems could occur if slow test equipment or test methods ground an output for too long a time causing functional failure or damage.

AC TESTING

FAST data sheets carry several types of AC information. The AC Characteristics table contains the guaranteed limits when tested under the conditions set forth under the AC Test Circuits and Waveforms. In some cases, the test conditions are further defined by the AC Setup Conditions — this is generally the case with counters and flip-flops where setup and hold times are involved. All of the AC Characteristics are guaranteed with 50pF load capacitances and with the fewest number possible of outputs switching, depending upon the functionality of the device. One of the sets of limits is specified at 25°C and +5.00V V_{CC} — these relate closely to the standard Schottky specification which are under similar conditions but use only 15pF load capacitances. While these numbers are convenient for comparing the two families, keep in mind that using full 50pF loads with the Schottky devices would add several nanoseconds to their propagation delays. These numbers are ideal for checking out test jigs and correlating data since they do not involve temperature or supply voltage spreads. For system design, full specifications are included that include temperature and supply voltage variations — in one case the military ranges and in the other, the commercial ranges.

AC TEST JIGS AND SETUPS

Each FAST data sheet spells out the test circuit used to check AC performance, the waveforms, measurement points, rep rate, test loads, etc., but these are only the quantifiable variables involved in this testing. There is another more complex side to the issue — test jigs and equipment setups.

To get an appreciation for the problems involved in testing FAST, consider these facts. The output rise and fall times on FAST outputs are very sharp. Translating these edge rates into the effective sine wave equivalents generates frequencies on the order of several hundred MHz. At these frequencies, attention to RF phenomena is required.

Because of these RF frequencies, it is necessary to have an AC test jig that has minimal modifying effect on the input and output waveforms. To do this, the jig must be constructed properly. The following items are key in dealing with AC jig construction.

BYPASSING CAPACITORS

Philips Semiconductors uses high quality capacitors that have good RF qualities to decouple the power supply lines on the test jig, right at the V_{CC} pin to the ground plane. Four capacitors with absolute minimum lead length are used. Microwave chip capacitors are recommended. (Note: In some sensitive test environments it is advisable to decouple the V_{CC}, as well as bypass. This is done by passing the V_{CC} through a wire wrapped around a ferrite core 6-8 times. The inductor created helps decouple the noise from V_{CC} and reduces dramatically the tendency for feedback oscillations through the V_{CC} and ground current loop. This is a key problem on clocked parts since the ground bounce created by the fast edge rates and high currents will effect V_{CC} and ground substantially and thereby effect internal thresholds.) These are one each, 10µF dipped tantalum, 0.1µF dipped tantalum or chip, 0.001µF chip and 100pF chip.

GROUNDING

One of the biggest contributors to waveform degradation is improper grounding. In reference to the test jig, the grounding is best done with one or more large ground planes that are directly connected to the ground pin of the test socket. The Philips Semiconductors AC Test Jigs, both DIP and SO styles, are constructed as a four layer PC board with the 2 internal layers as ground planes. Ground planes are also interdigitated between all signal lines to decrease crosstalk. There are holes drilled in these and they are plated through to connect with the internal 2 layers and the top and bottom layers. See Figure 3 to see the interdigitated ground planes on the PCB layout of the SO jig. This grounding scheme has been used with great success in 10k and 100k ECL fixturing. The board is laid out so that the characteristic impedance of the signal lines is 50Ω. This is done by using industry standard stripline techniques. The ground plane also passes down through the center of the part on the bottom side of the board and the ground pin is soldered to it using copper wire to connect the pin and the ground plane. On the top side of the board, the V_{CC} plane goes through the center of the part too, and connects to the V_{CC} pin in like manner as the ground pin. See Figure 1. As the V_{CC} is brought on board, the V_{CC} wire is wrapped around a $^1/_2$ inch ferrite core, 6-8 times, then makes connection with the V_{CC} plane on the top side.

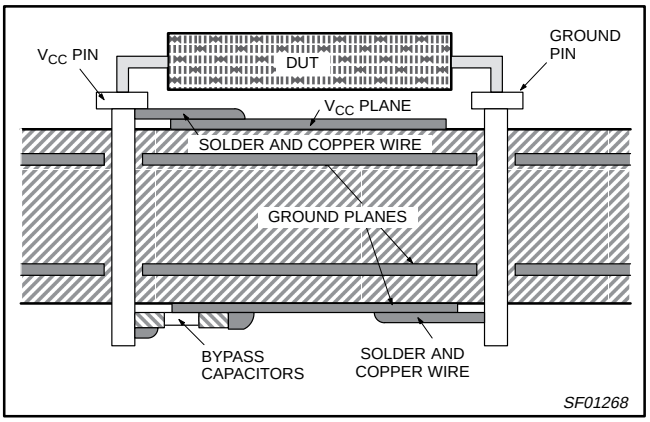


Figure 1.

INTERCONNECTS

The next concern is getting the input signal to the part and the output signal to the measurement system. As stated before, the Philips Semiconductors jig is laid out for a 50Ω characteristic impedance. We recommend that the user maintain a 50Ω environment for the input signal as close as possible to the input pin and then terminate in 50Ω. On our jig, we terminate with a 50Ω chip resistor. The signal is brought on board through an SMB connector to the 50Ω trace on the top side of the board. The signal is terminated by the chip resistor, R3, see Figure 2a and 2b. the signal proceeds to the DUT pin, a distance of about 0.5 inches, through Jumper 1 (in the Input Only position), and the rest of the trace. The same pin on the opposite side of the board has a 450Ω chip resistor soldered to it. The other side of this resistor, R1, is soldered to a 50Ω trace on the bottom side of the board that runs to an SMB connector on the edge of the jig. This connects to the 50Ω input of the Sampling Oscilloscope. This 450Ω resistor in series with the 50Ω input of the scope creates a 10X divided 500Ω probe for the scope and provides impedance matching for the scope. See Figure 2b. This circuit also doubles as the resistive portion of the FAST AC Output Load and thereby allows the output to be sensed in the same fashion. When the input is not used for a signal or generator input, the line may be switched to one of three voltage sources, $V_S1 – V_S3$, by use of a DIP switch on each pin. It may also be left open and the 50Ω pull-down resistor that is used for an input terminator pulls the line to ground and can be used as a hard low level. See Figure 2b. This scheme eliminates excessive cabling to each input to provide static input levels and thereby reduces parasitic inductances and cross-talk. It also eliminates the need for bulky and sometimes unreliable high impedance probes by using the 50Ω input of the Sampling Scope. With the designed-in flexibility of Jumper 1 and Jumper 2, and the selectable nature of V_{CC} and Ground pin designations, one can configure this board for any V_{CC} and Ground pin designations, select which pins are outputs or inputs and even provide the proper pull-up for 3-State outputs. This makes the board entirely universal for designated V_{CC}/Ground configurations. To explain this, the output of the device is connected to its capacitive load by Jumper 1 in the Output Only position. This means that no pin can be both output and input at the same time, but can be either. Jumper 2 allows an output to be connected to the 3-State pull-up resistor, R2, and have that connected to the needed 7V. See Figure 2a and 2b. The scope is connected in the same way as the input, with the 450Ω resistor and the 50Ω of the scope comprising the 500Ω needed for the FAST load. One other consideration exists. In small part quantity testing, the elimination of a socket is very desirable, using inserted pins that are flush with the jig. In larger quantity testing, sockets may be needed, however. If this is the case, some degradation in the performance will occur due to the increased lead inductance for each pin, which is observable, and the addition of group delay through the socket may alter or affect the readings obtained.

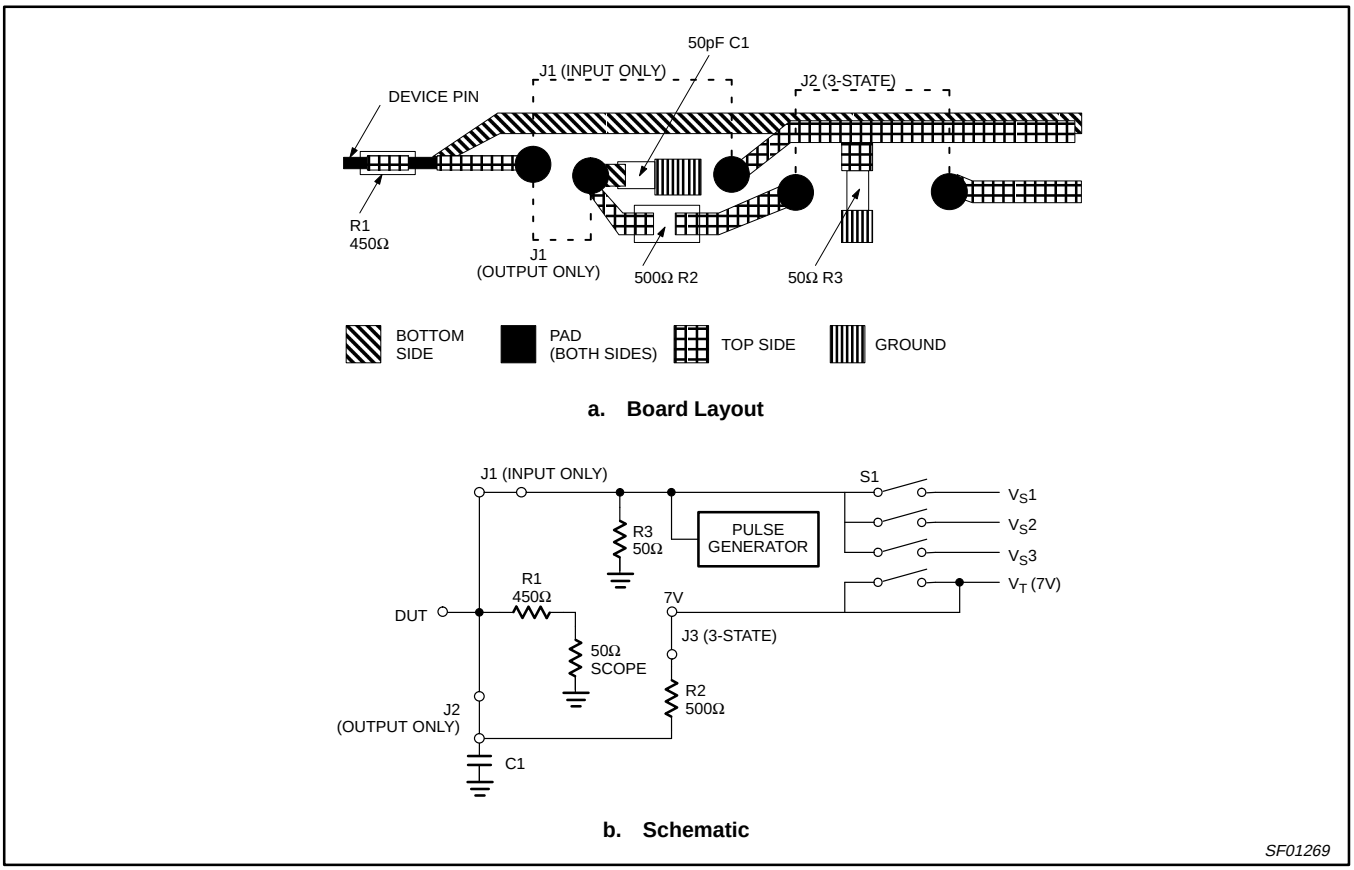


Figure 2. FAST AC Test Fixture

HIGH-FREQUENCY DESIGN

The exact jig delay time is determined by the size of the universal jig that is being used. It is important to know that the frequency response of the jig must be High to prevent any delay factor from varying with the edge rates. The frequency response of the jig indicates how constant the impedance remains over frequency. The characteristics impedance of a transmission line is expressed as:

$$Z_O = \frac{V}{I} = \sqrt{\frac{L_O}{C_O}}$$

Where L_O is the inductance per unit length, C_O is the capacitance per unit length, Z_O is in Ohms, L_O in Henrys, and C_O in Farads. Propagation velocity and its inverse, delay per unit length d, are also expressed in L_O and C_O …

$$V = \frac{1}{\sqrt{L_O C_O}} \qquad \delta = \sqrt{L_O C_O}$$

where δ is expressed in nanoseconds, L_O is in microhenrys per unit length, and C_O in microfarads per unit length. From this, it is clear that if the Z_O changes over frequency, then the delay per unit length will vary as well. Therefore, it is imperative to know how the jig responds over frequency and that all measurement line lengths are identical.

Frequency response also depends on the phase as well as the magnitude of the impedance. If the phase changes so does the delay, since delay is the derivative of phase change with frequency. An S-parameter analysis is needed in evaluating jig performance.

UNIVERSAL JIG CONSTRUCTION

Jig universality is with respect to chip pin count and V_{CC} and ground pin placements and as such, separate universal test jigs are built for 14, 16, 20, 24, and 28 pin parts.

An S-parameter analysis was performed in a network analyzer to optimize the jig layout. This assured that the jig had a flat frequency response over the spectrum of interest for FAST products. Figure 2b shows the schematic of the fixture and Figure 2a shows a drawing of the board layout, component placement and signal paths. The equipment used to analyze the jigs and loads was: HP8505A Network Analyzer, HP8503A S-Parameter Test Set and HP8501A Storage Normalizer. In some measurements the equipment was driven by an HP9845B desk-top computer.

Jigs produced in this way should have minimal lead length to reduce the characteristic inductance. This in turn minimizes reflections with their accompanying waveform distortions. and measurement inaccuracies.

AC TEST LOADS FOR THE PHILIPS SEMICONDUCTORS JIG

As stated previously, the Network Analyzer was also used to design and optimize AC test loads to be used with the universal jig. FAST product loads require 50pF load capacitance and 500Ω resistance to ground.

Philips Semiconductors meets the 50pF requirement through the use of a 45pF load, 4pF jig capacitance, and 3pF probe capacitance. The result, 52pF, is slightly more stringent than required.

A few words about load capacitors are in order. All capacitors have an associated inductance. Due to this inductance, a capacitor will form a series resonant circuit at some frequency. For single 50pF capacitors, this typically occurs between 200 and 600MHz depending on the type of capacitor. Above this resonant frequency, the capacitor has inductive characteristics and does not present a capacitive load. this is very important with FAST because harmonics due to the sharp edge transition rates occur at 600MHz and above.

The Philips Semiconductors FAST loads solve this problem by reducing the load capacitor lead inductance by paralleling three 15pF chip capacitors. The resulting load is 45pF. At the same time, since smaller value caps are used to build up the capacitive load, the associated series resonant point is above 1.2GHz.

The load resistors are 1/8W selected 510Ω ± 10Ω chip resistors.

The entire load assembly is constructed on the jig PCB along with the input termination, and the jumpers which select an input or output path. The load circuit is detailed on the FAST data sheets for 3-State parts.

CORRELATION

While numerous ATE systems are available and are very efficient, it is imperative that the ATE correlate to a user's bench setup. Since the Philips Semiconductors FAST parts are all characterized on the setup described in this note, it is just as important that the user's bench jigs meet the same performance criteria. Without similar jigs, it will be very difficult to correlate AC data.

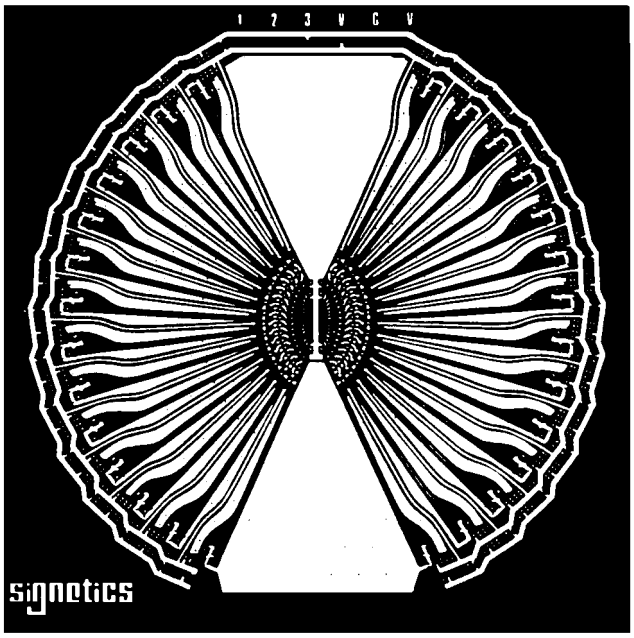


Figure 3.