FT28C010-xxxxx-X

128K x 8 Bit 5V EEPROM

FEATURES

- Access Time: 120ns
- Simple Byte and Page Write
  - —Single 5V Supply
  - —No External High Voltages or VPP Control Circuits
  - —Self-Timed
    - —No Erase Before Write
    - —No Complex Programming Algorithms
    - —No Overerase Problem
- Low Power CMOS:
  - —Active: 50mA
  - —Standby: 500µA
- Software Data Protection
  - —Protects Data Against System Level Inadvertant Writes
- High Speed Page Write Capability
- Highly Reliable Cell
  - —Endurance: 100,000 Write Cycles
  - —Data Retention: 100 Years
- Early End of Write Detection
  - —$\overline{\text{DATA}}$ Polling
  - —Toggle Bit Polling
- -X Manufactured using Xicor Die

DESCRIPTION

The Force FT28C010 is a 128K x 8 E^{2}PROM, fabricated with, high performance, floating gate CMOS technology. Like most Force programmable nonvolatile memories the FT28C010 is a 5V only device. The FT28C010 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard EPROMs.

The FT28C010 supports a 256-byte page write operation, effectively providing a 19 µs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The FT28C010 also features $\overline{\text{DATA}}$ Polling and Toggle Bit Polling, system software support schemes used to indicate the early completion of a write cycle. In addition, the FT28C010 supports Software Data Protection option.

Force E^{2}PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 100 years.

FT28C010-xxxxx-AT

128K x 8 Bit 5V EEPROM

FEATURES

- Fast Read Access Time 120ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 128-Bytes Internal Control Timer
- Fast Write Cycle Time
  - Page Write Cycle Time - 10 ms Maximum
  - 1 to 128-Byte Page Write Operation
- Low Power Dissipation
  - 80 mA Active Current
  - 300 µA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10^4
  - Data Retention: 10 Years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- -AT Manufactured using Atmel Die

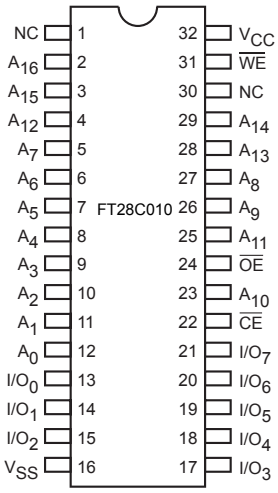
DESCRIPTION

The FT28C010 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its one megabit of memory isorganised as 131,072 words by 8 bits. Manufactured with advanced nonvolatile CMOS technology, the device offersaccess times to 120 ns with power dissipation of just 440 mW. When the device isdeselected, the CMOS standby current is less than 300 mA. (Cont)

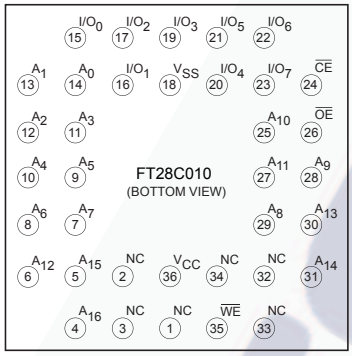
FT28C010-xxxxx-X

PIN CONFIGURATIONS

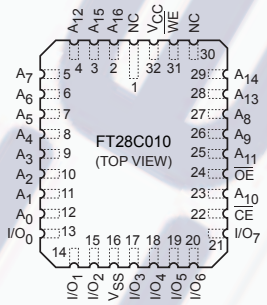
CERDIP
FLAT PACK
SOIC (R)



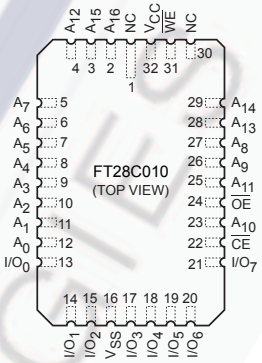
PGA



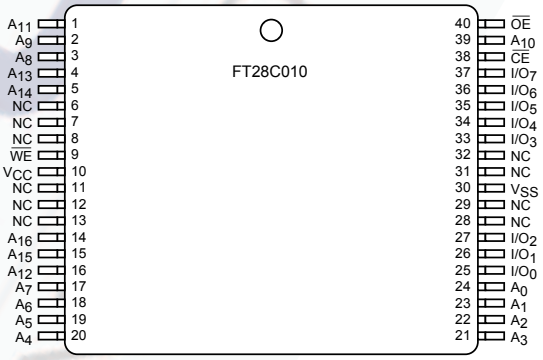
PLCC
LCC



EXTENDED LCC



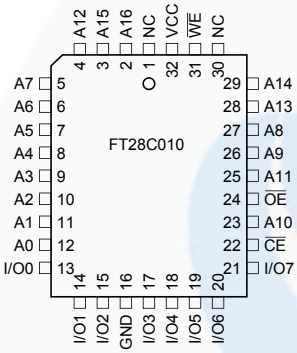
TSOP



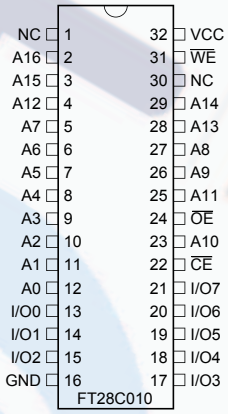
FT28C010-xxxxx-AT

PIN CONFIGURATIONS

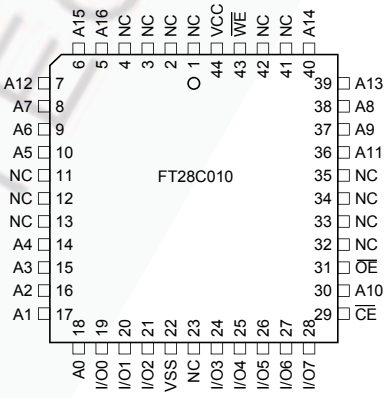
32 LCC
Top View



CERDIP, FLATPACK
Top View



44LCC
Top View



PGA
Top View

4 A6	3 A7	1 A14	27 $\overline{WE}$	26 A13
5 A5	2 A12	28 VCC	24 A9	25 A8
7 A3	6 A4	29 A15	22 $\overline{OE}$	23 A11
9 A1	8 A2	30 A16	20 $\overline{CE}$	21 A10
11 I/O0	10 A0	14 GND	16 I/O4	19 I/O7
12 I/O1	13 I/O2	15 I/O3	17 I/O5	18 I/O6

FT28C010

PIN DESCRIPTIONS

Addresses (A_0–A_{16})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the FT28C010 through the I/O pins.

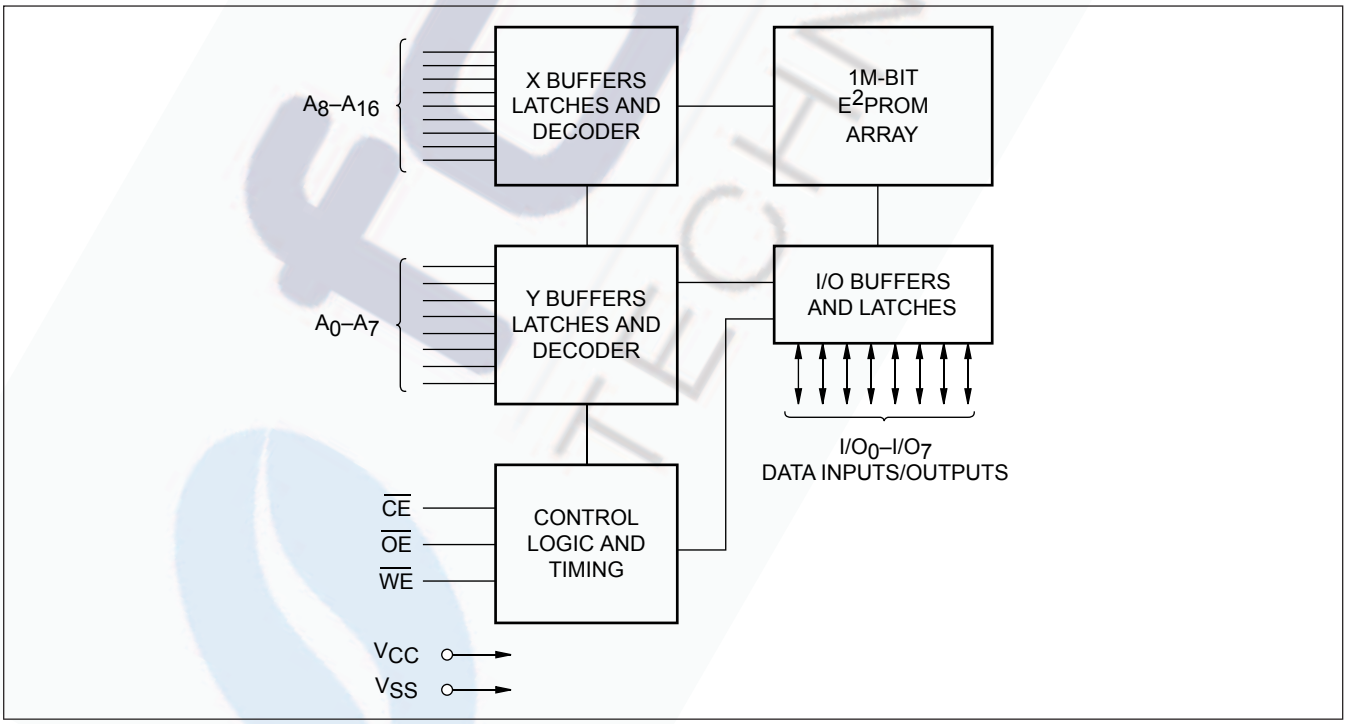
Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the FT28C010.

PIN NAMES

Symbol	Description
A_0–A_{16}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The FT28C010 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

Page Write Operation

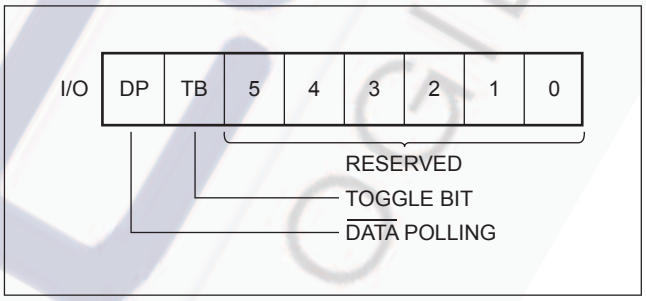
The page write feature of the FT28C010 allows the entire memory to be written in 5 seconds. Page write allows two to two hundred fifty-six bytes of data to be consecutively written to the FT28C010 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_8 through A_{16}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to two hundred fifty six bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

Write Operation Status Bits

The FT28C010 provides the user two write operation status bits. These can be used to optimise a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)

The FT28C010 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the FT28C010, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the FT28C010 is in the protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)

The FT28C010 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle, I/O_6 will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{DATA}$ Polling I/O_7

Figure 2. $\overline{DATA}$ Polling Bus Sequence

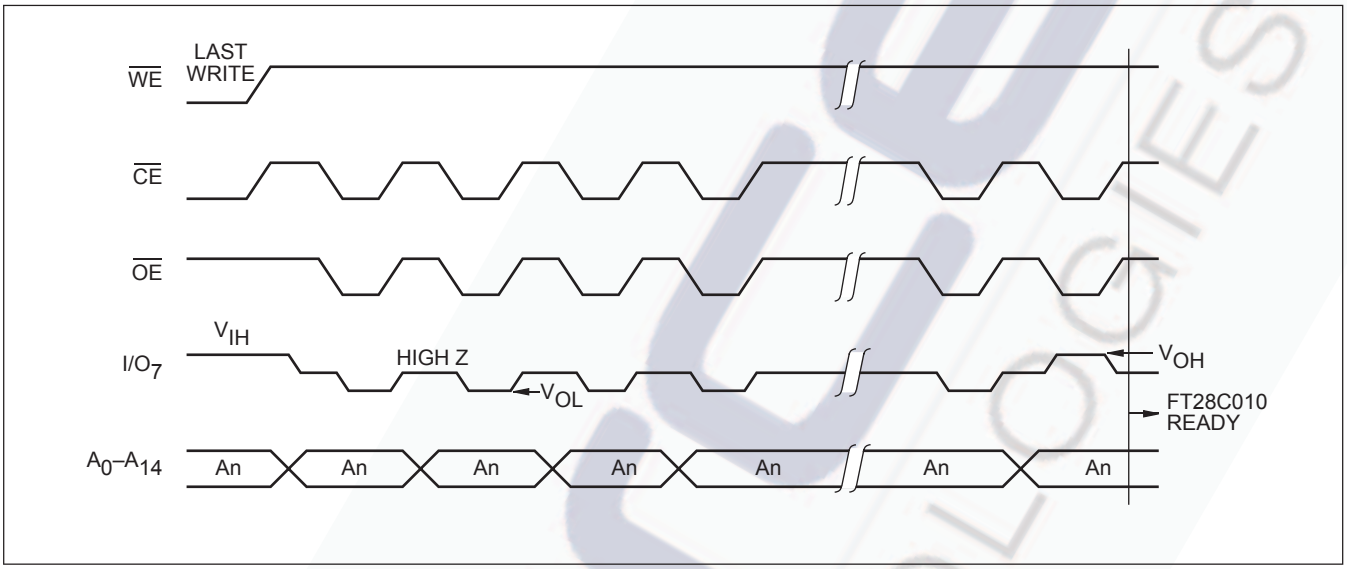
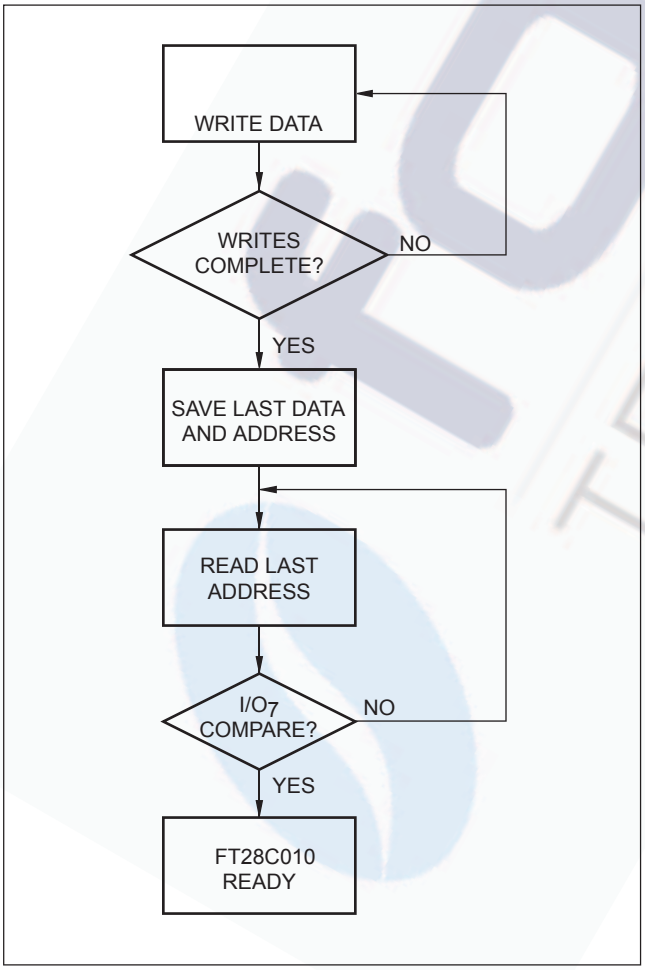


Figure 3. $\overline{DATA}$ Polling Software Flow



$\overline{DATA}$ Polling can effectively halve the time for writing to the
FT28C010. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

The Toggle Bit I/O_6

Figure 4. Toggle Bit Bus Sequence

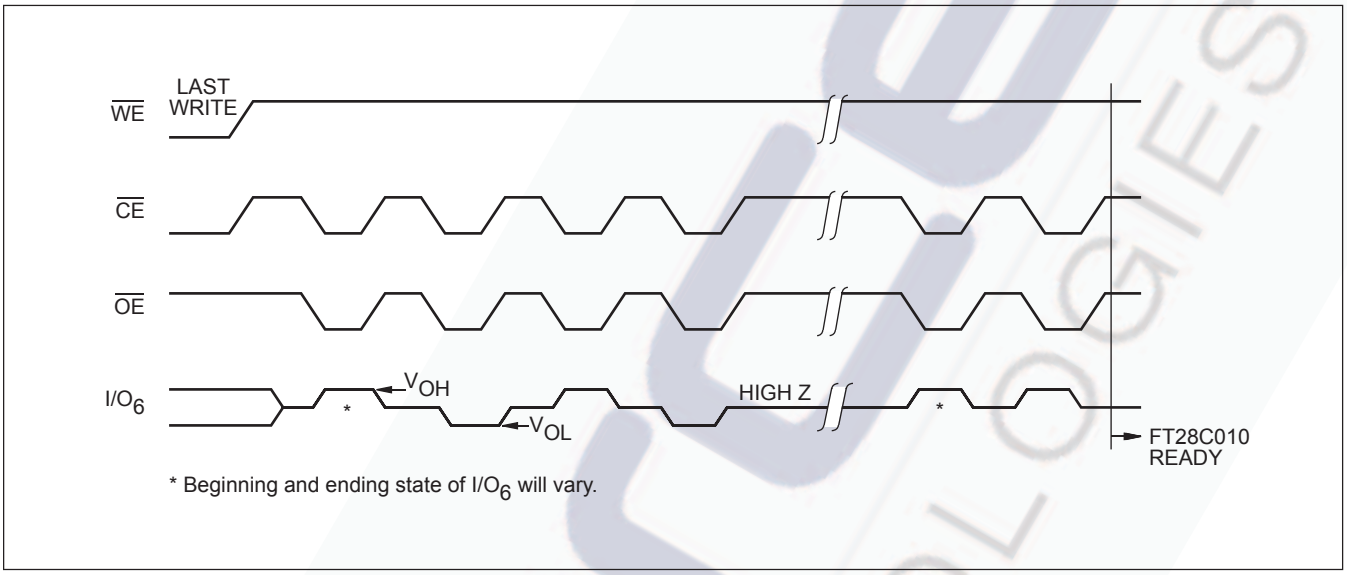
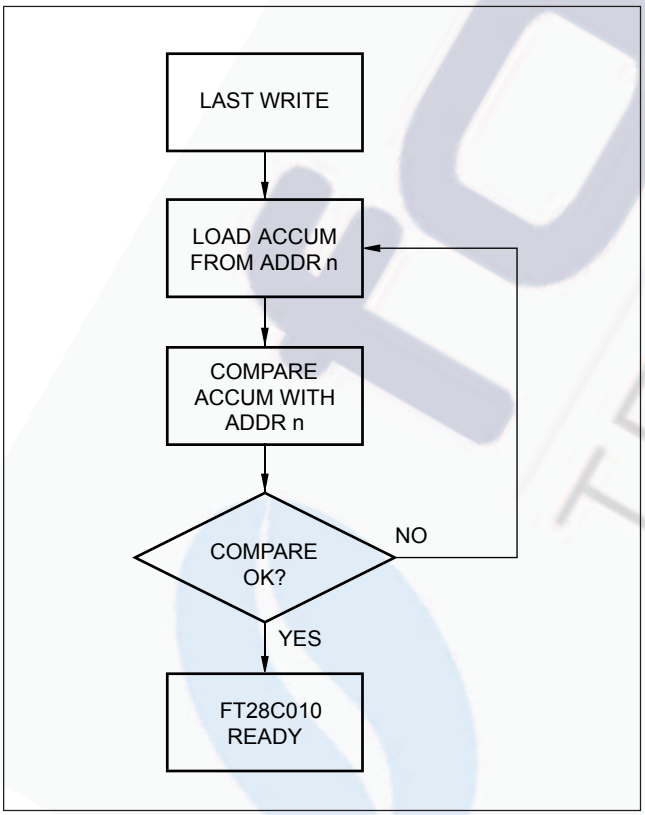


Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple FT28C010 memories that is frequently updated. Toggle Bit Polling can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for polling the Toggle Bit.

HARDWARE DATA PROTECTION

The FT28C010 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse less than 10ns will not initiate a write cycle.
- Default V_{CC} Sense—All functions are inhibited when V_{CC} is ≤3.5V.
- Write inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity.

SOFTWARE DATA PROTECTION

The FT28C010 offers a software controlled data protection feature. The FT28C010 is shipped from Force with the software data protection NOT ENABLED: that is the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The FT28C010 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilising the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the FT28C010 is also protected from inadvertent and accidental writes in the powered-up state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figures 6 and 7 for the sequence. The three byte sequence opens the page write window enabling the host to write from one to two hundred fifty-six bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Software Data Protection

Figure 6. Timing Sequence—Byte or Page Write

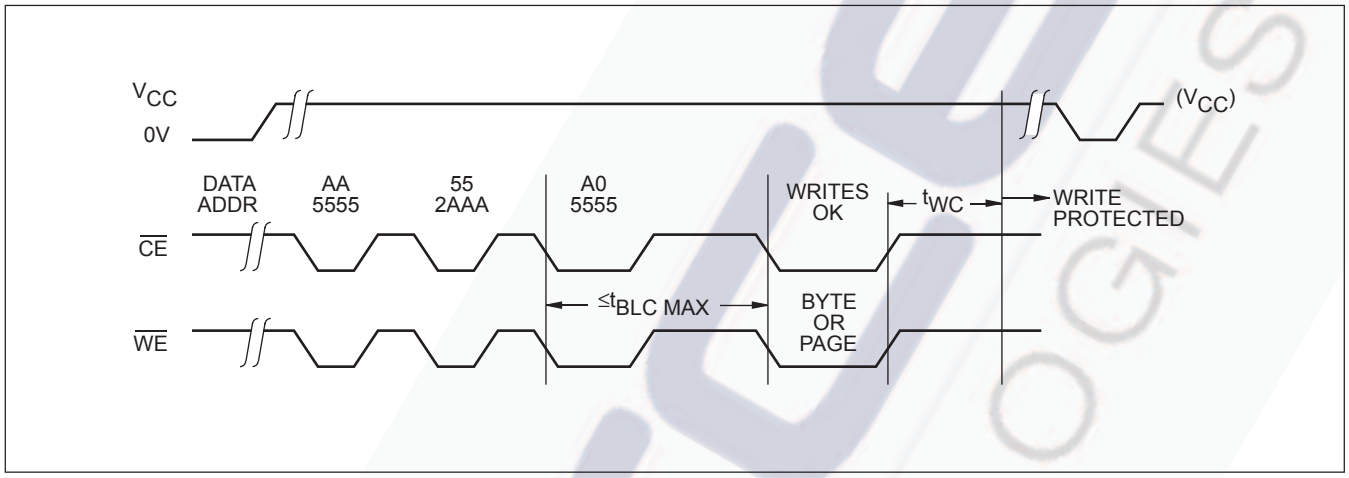
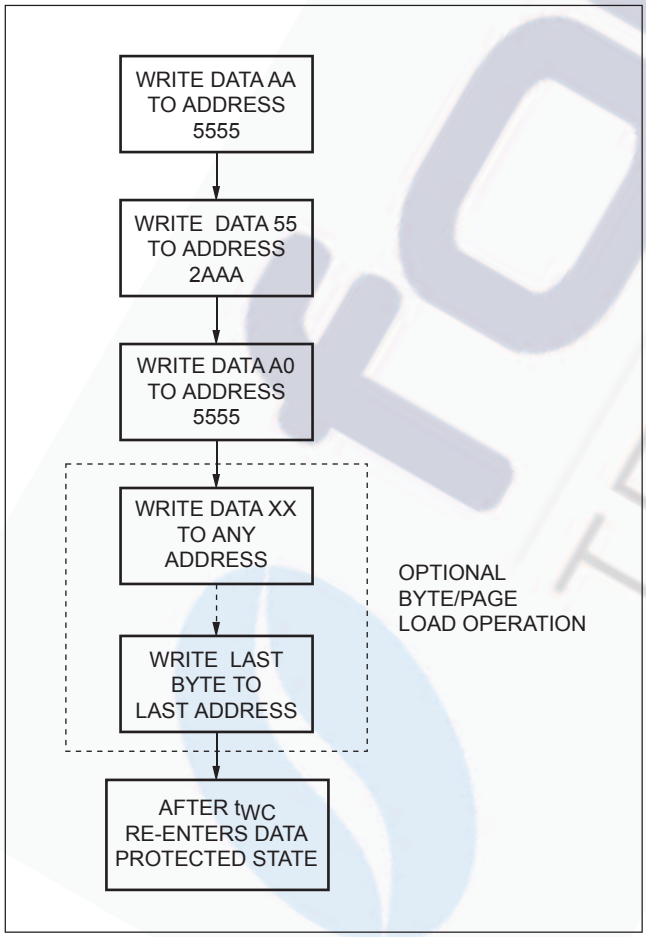


Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the FT28C010 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the FT28C010 will be write protected during power-down and after any subsequent power-up. The state of A_{15} and A_{16} while executing the algorithm is don't care.

Note: Once initiated, the sequence of write operations should not be interrupted.

Resetting Software Data Protection

Figure 8. Reset Software Data Protection Timing Sequence

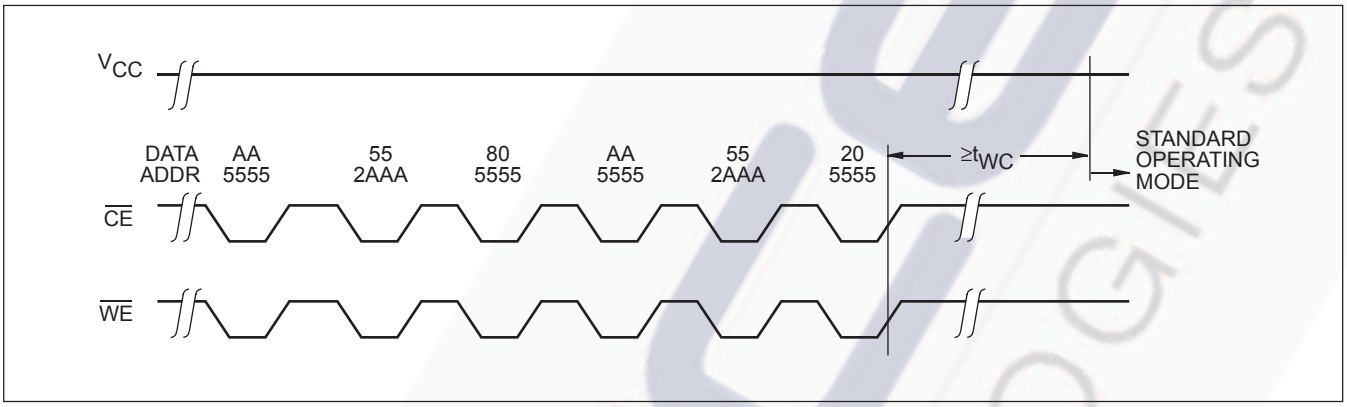
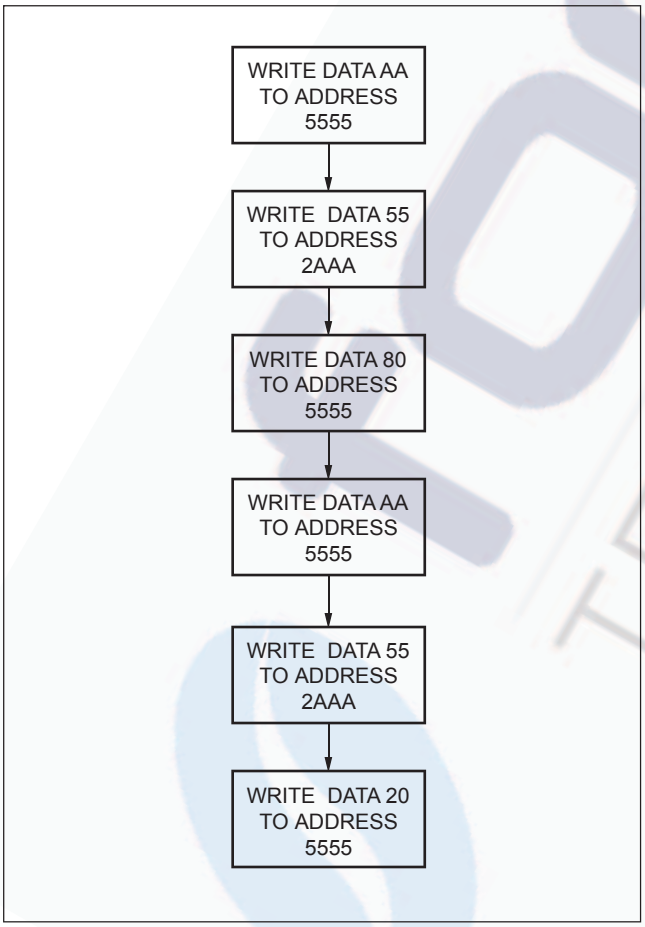


Figure 9. Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E^{2}PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the FT28C010 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

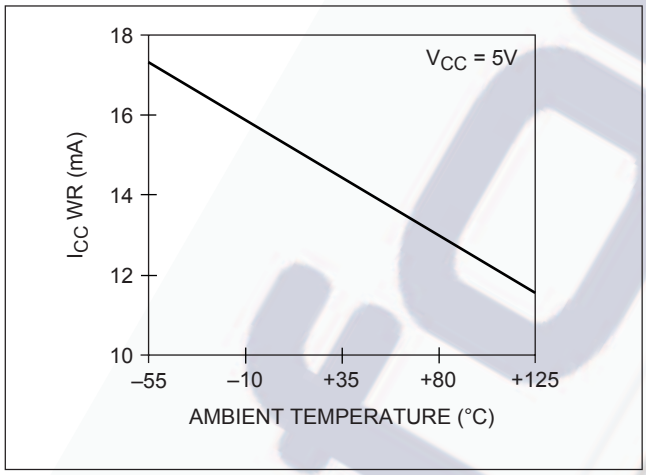
Because the FT28C010 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

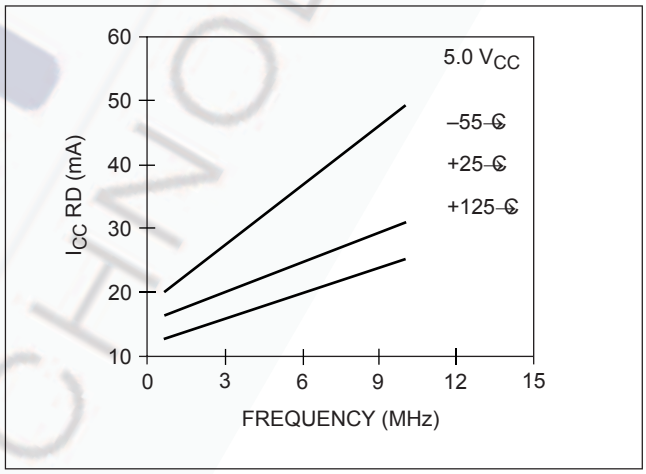
Because the FT28C010 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 µF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7µF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

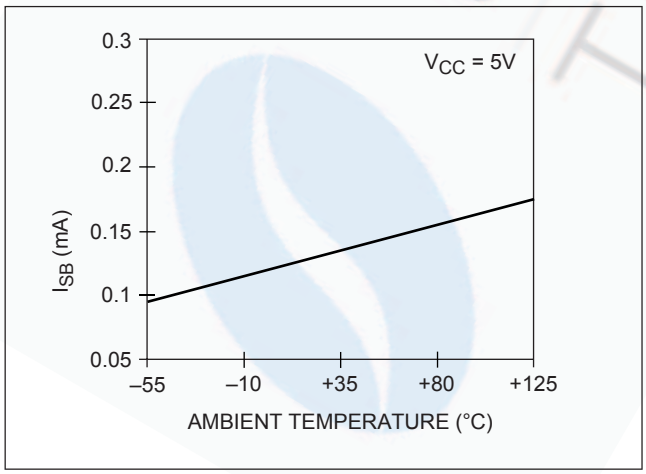
Active Supply Current vs. Ambient Temperature



I_{CC} (RD) by Temperature over Frequency



Standby Supply Current vs. Ambient Temperature



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
- FT28C010 ..... –10° C to +85°C
- FT28C010I ..... –65° C to +135°C
- FT28C010M ..... –65° C to +135°C

Storage Temperature ..... –65° C to +150°C

Voltage on any Pin with
- Respect to V_{SS} ..... –1V to +7V

D.C. Output Current 5mA

Lead Temperature
- (Soldering, 10 seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMEND OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

Supply Voltage	Limits
FT28C010	5V±10%

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active) (TTL Inputs)		50	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = Open, Address Inputs = .4V/2.4V Levels @ f = 5MHz
I_{SB1}	V_{CC} Current (Standby) (TTL Inputs)		3	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{IH}
I_{SB2}	V_{CC} Current (Standby) (CMOS Inputs)		500	µA	$\overline{CE}$ = V_{CC} – 0.3V, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{CC}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(1)	Input LOW Voltage	–1	0.8	V	
V_{IH}(1)	Input HIGH Voltage	2	V_{CC} + 1	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –400µA

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(2)	Power-up to Read Operation	100	µs
t_{PUW}(2)	Power-up to Write Operation	5	ms

CAPACITANCE T_A = +25° C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	10	pF	V_{IN} = 0V

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units
Endurance	10,000		Cycles Per Byte
Endurance	100,000		Cycles Per Page
Data Retention	100		Years

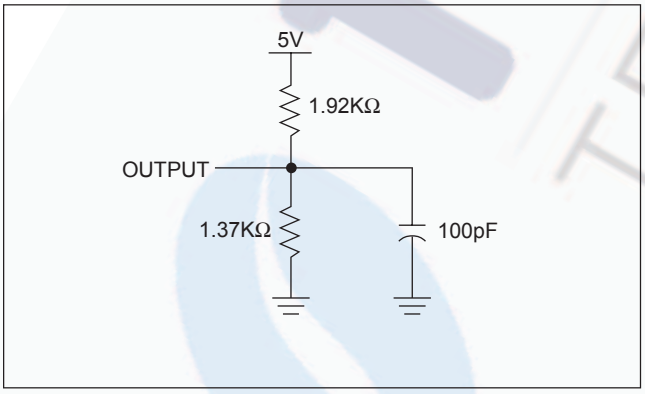
A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

MODE SELECTION

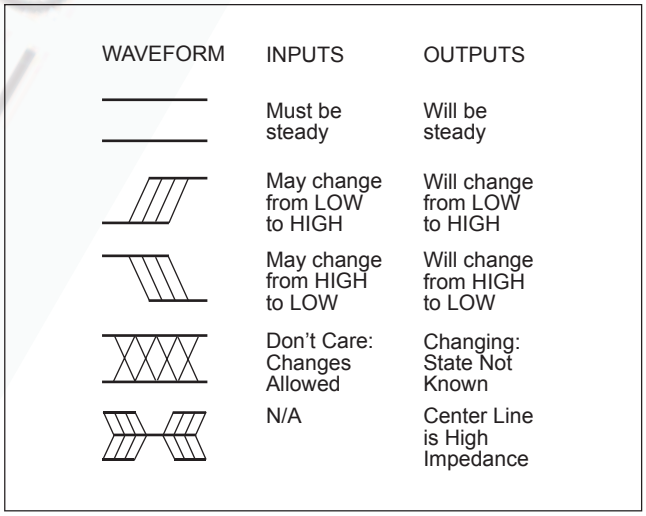
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

EQUIVALENT A.C. LOAD CIRCUIT



Note: (2) This parameter is periodically sampled and not 100% tested.

SYMBOL TABLE

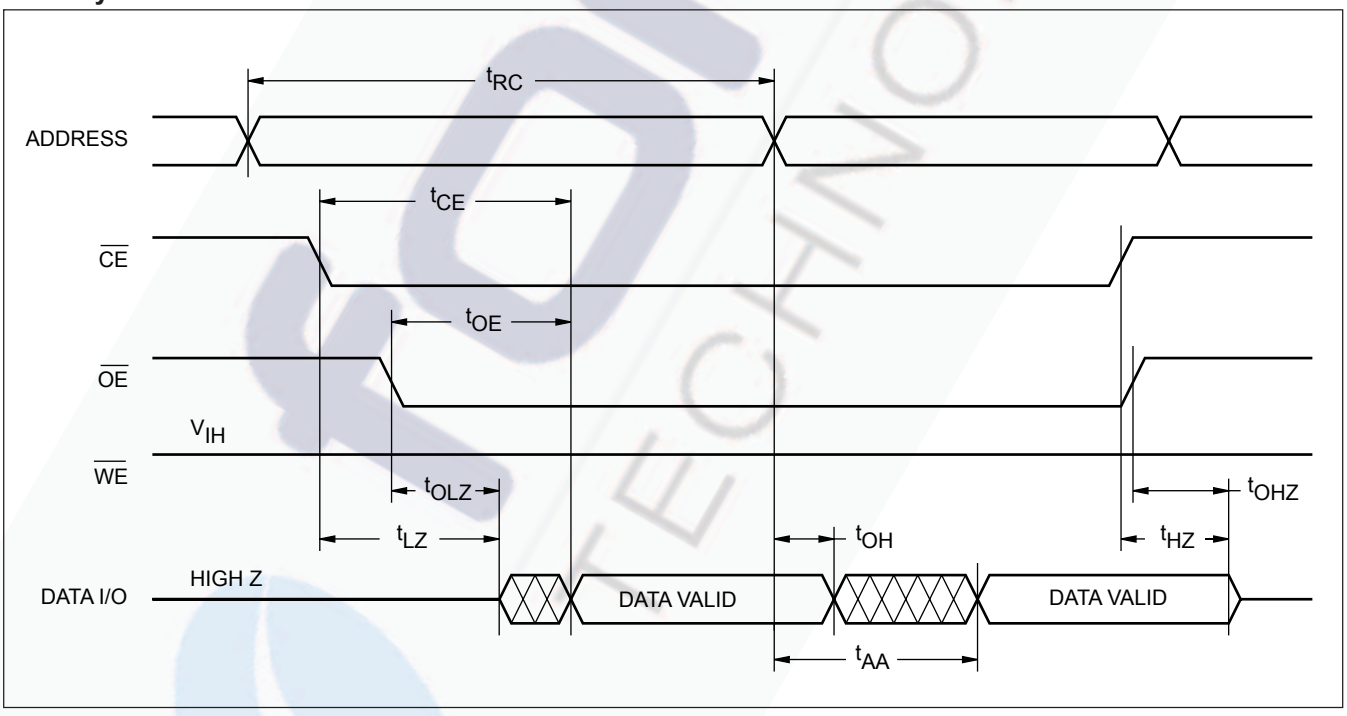


A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Read Cycle Limits

Symbol	Parameter	FT28C010-12		FT28C010-15		FT28C010-20		FT28C010-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	120		150		200		250		ns
t_{CE}	Chip Enable Access Time		120		150		200		250	ns
t_{AA}	Address Access Time		120		150		200		250	ns
t_{OE}	Output Enable Access Time		50		50		50		50	ns
t_{LZ}(3)	$\overline{CE}$ LOW to Active Output	0		0		0		0		ns
t_{OLZ}(3)	$\overline{OE}$ LOW to Active Output	0		0		0		0		ns
t_{HZ}(3)	$\overline{CE}$ HIGH to High Z Output		50		50		50		50	ns
t_{OHZ}(3)	$\overline{OE}$ HIGH to High Z Output		50		50		50		50	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

Read Cycle

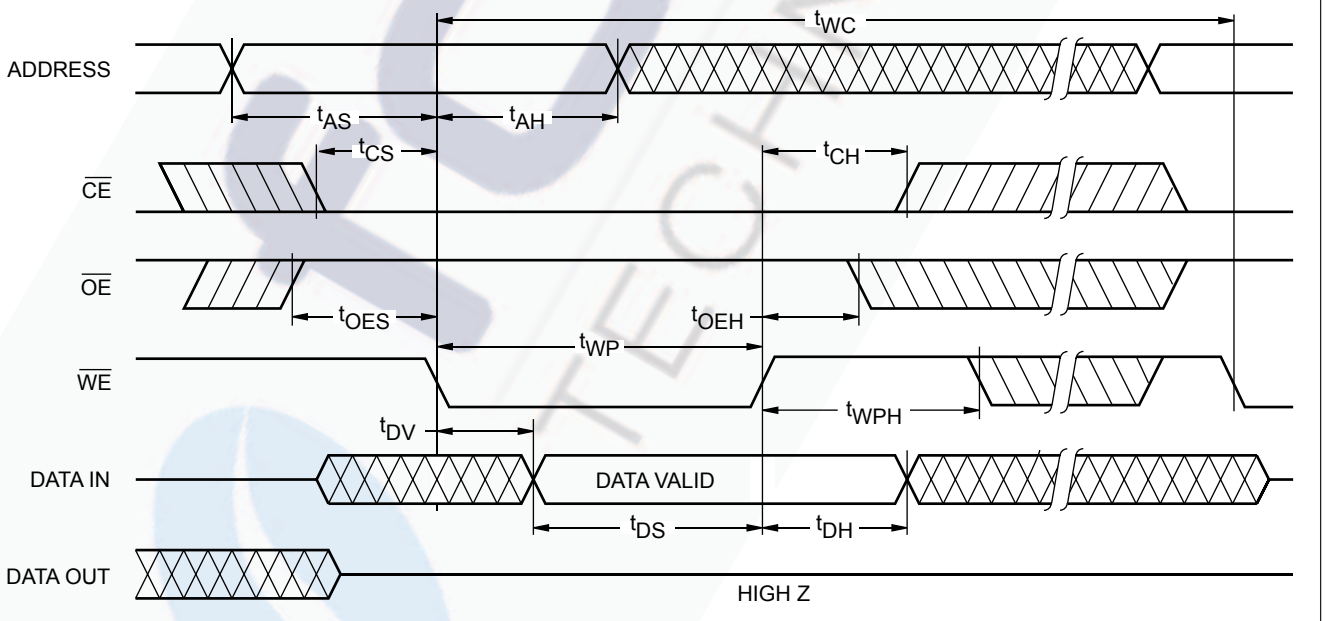


Note: (3) t_{LZ} min.,t_{HZ}, t_{OLZ} min., and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured, with C_L = 5pF, from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

Write Cycle Limits

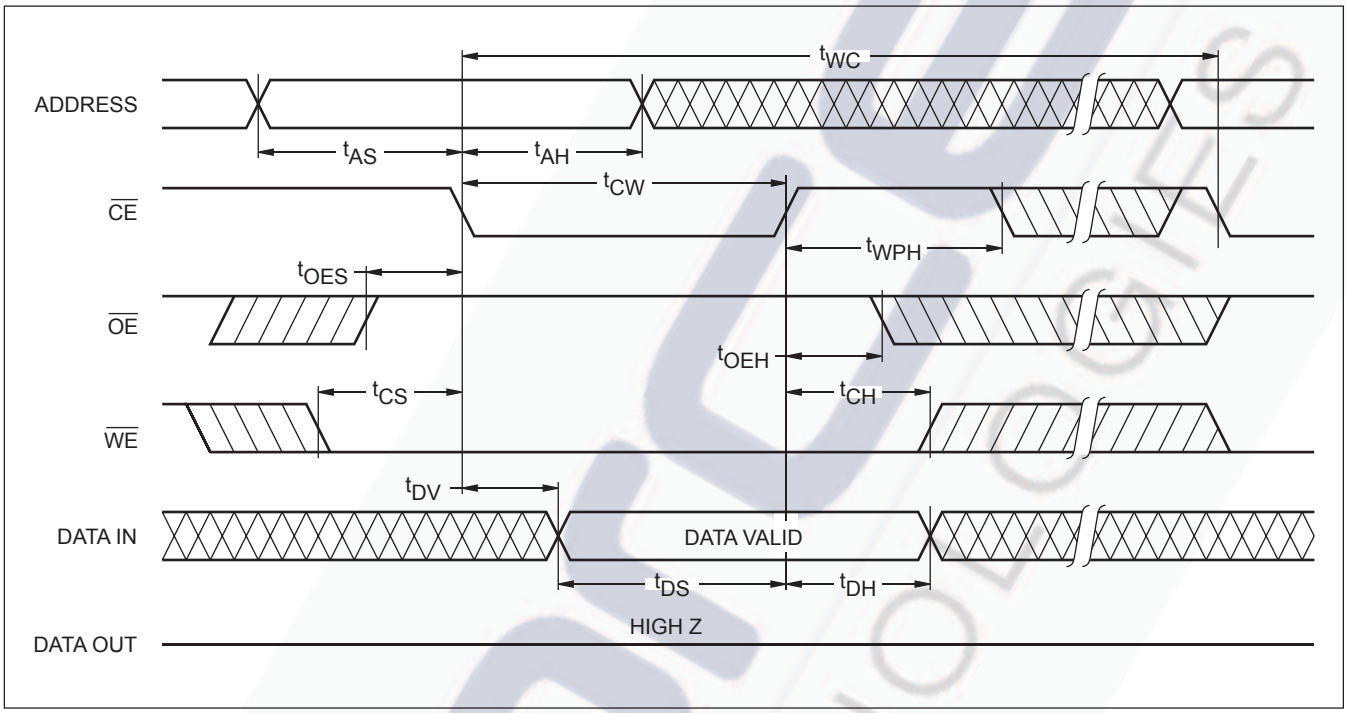
Symbol	Parameter	Min.	Max.	Units
t_{WC}(4)	Write Cycle Time		10	ms
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	$\overline{CE}$ Pulse Width	100		ns
t_{OES}	$\overline{OE}$ HIGH Setup Time	10		ns
t_{OEH}	$\overline{OE}$ HIGH Hold Time	10		ns
t_{WP}	$\overline{WE}$ Pulse Width	100		ns
t_{WPH}	$\overline{WE}$ HIGH Recovery	100		ns
t_{DV}	Data Valid		1	µs
t_{DS}	Data Setup	50		ns
t_{DH}	Data Hold	0		ns
t_{DW}	Delay to Next Write	10		µs
t_{BLC}	Byte Load Cycle	0.2	100	µs

$\overline{WE}$ Controlled Write Cycle

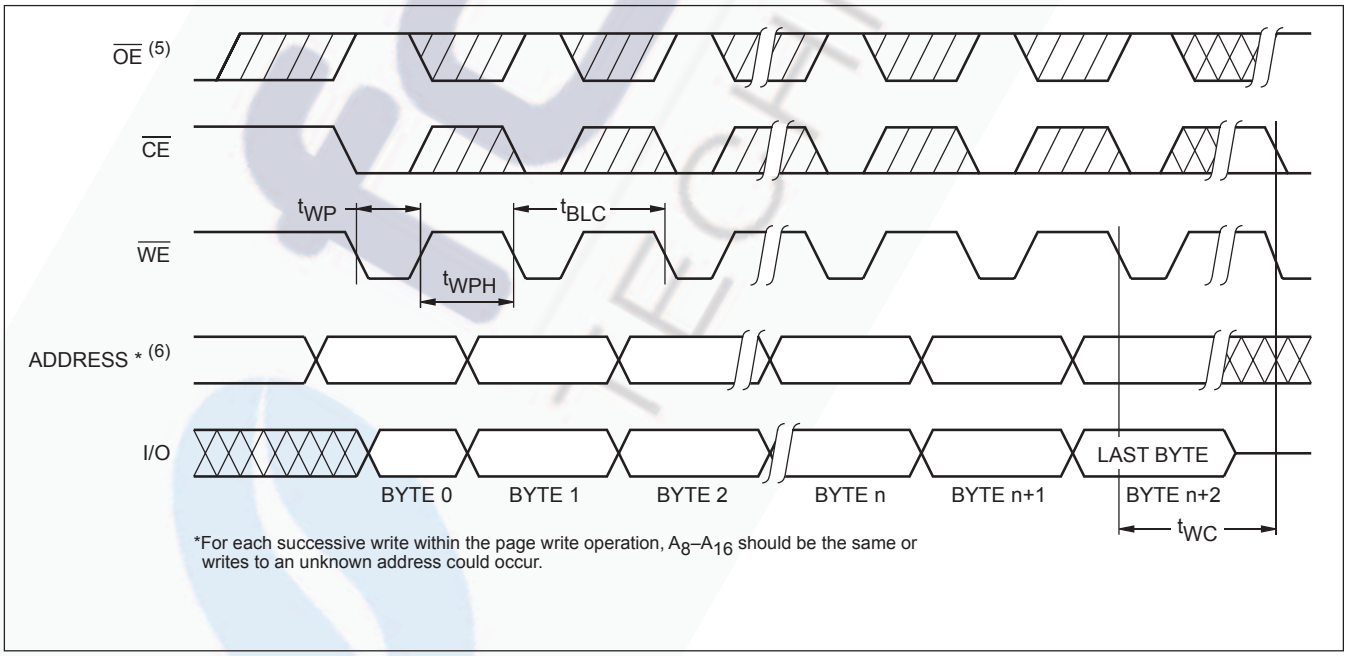


Notes: (4) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to complete internal write operation.

$\overline{CE}$ Controlled Write Cycle



Page Write Cycle

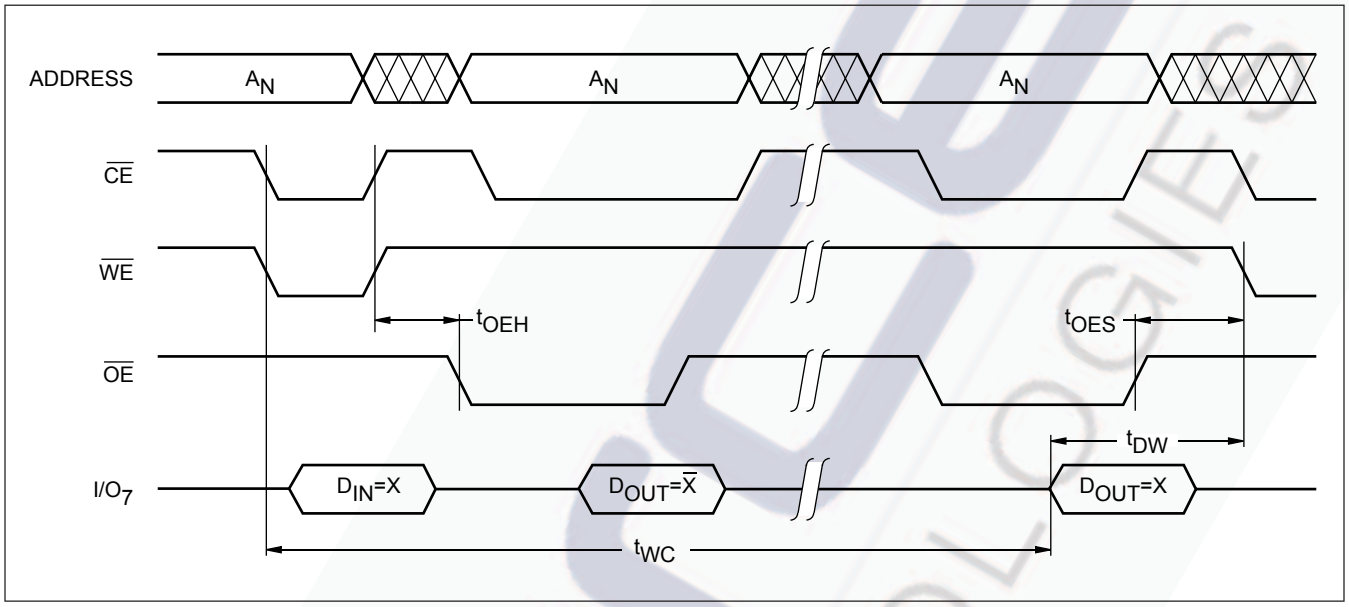


*For each successive write within the page write operation, A_8–A_{16} should be the same or writes to an unknown address could occur.

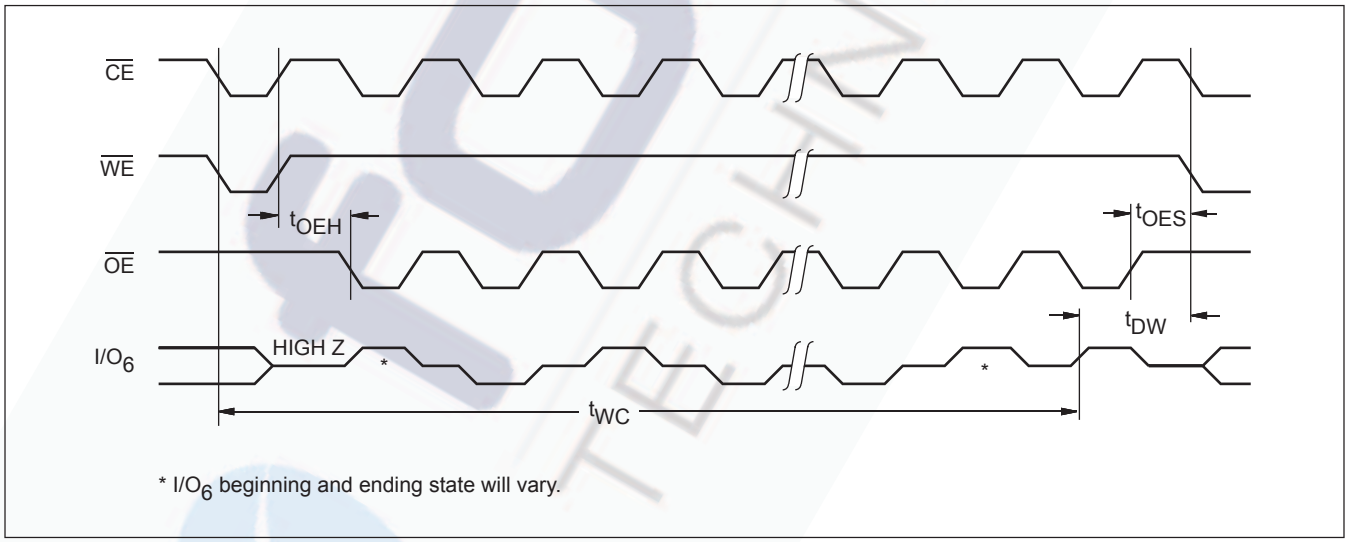
Notes: (5) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(6) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{DATA}$ Polling Timing Diagram(7)



Toggle Bit Timing Diagram

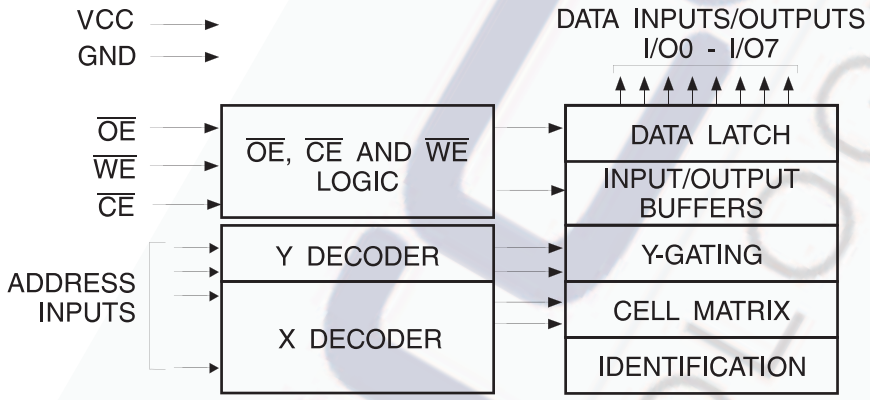


Note: (7) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

The FT28C010 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128-bytes simultaneously. During a write cycle, the address and 1 to 128-bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ POLLING of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Force's 28C010 has additional features to ensure high quality and manufacturability. The device utilises internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 128-bytes of EEPROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration

Pin Name	Function
A0 - A16	Addresses
CE	Chip Enable
OE	Output Enable
WE	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

Device Operation

READ: The FT28C010 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the FT28C010 allows 1 to 128-bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 127 additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the FT28C010 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A7 - A16 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A7 - A16 must be the same.

The A0 to A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The FT28C010 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the FT28C010 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Force has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the FT28C010 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a write: (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the FT28C010. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the FT28C010 is shipped from Force with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the 3-byte command sequence and after t_{WC} the entire FT28C010 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the FT28C010. This is done by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the FT28C010 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 128-bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 1FF80H to 1FFFFH the bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE: The entire device can be erased using a 6-byte software code. Please see Software Chip Erase application note for details.

DC and AC Operating Range (Commercial/Industrial)

		FT28C010-12	FT28C010-15	FT28C010-20
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

DC and AC Operating Range (Military)

		FT28C010-12	FT28C010-15	FT28C010-20	FT28C010-25
Operating Temperature (Case)	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes (Commercial/Industrial/Military)

Mode	CE	OE	WE	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be VIL or VIH.
2. Refer to AC Programming Waveforms

DC Characteristics (Commercial/Industrial)

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V		200	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V		3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		40	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2		V

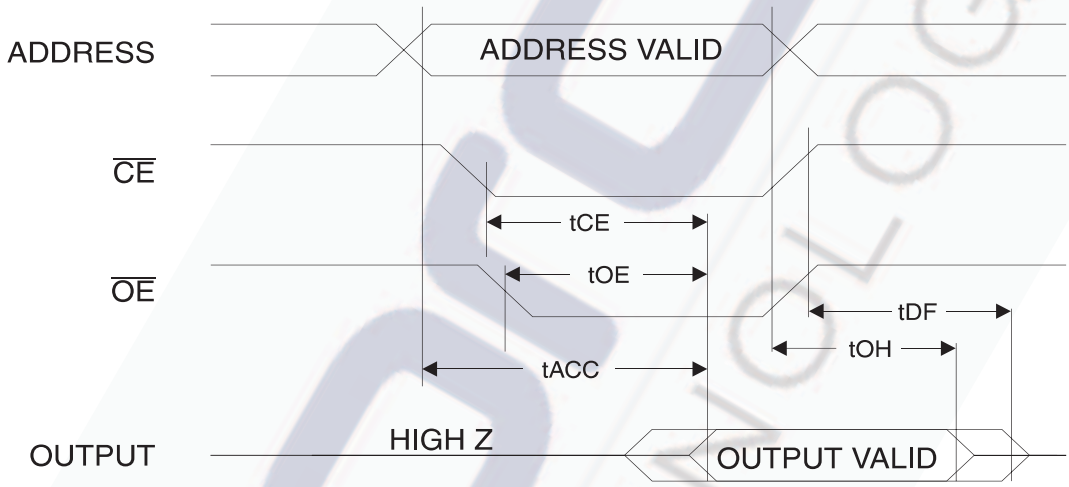
DC Characteristics (Military)

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V		3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		80	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V	4,2		V

AC Read Characteristics (Commercial/Industrial/Military)

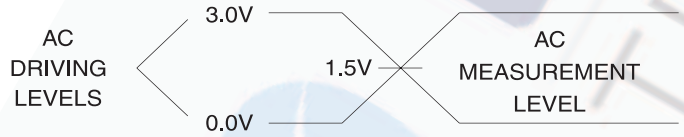
Symbol	Parameter	FT28C010-12		FT28C010-15		FT28C010-20		FT28C010-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		120		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ o utput Delay D	0	50	0	55	0	55	0	55	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ o Output loat F	0	50	0	55	0	55	0	55	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

AC Read Waveforms(1)(2)(3)(4)

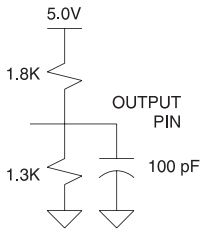


Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact in t_{ACC}.
3. t_{DF} is specified from OE or CE wichever occurs first (CL = 5 pF).
4. This parameter is characterised and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C(1)

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

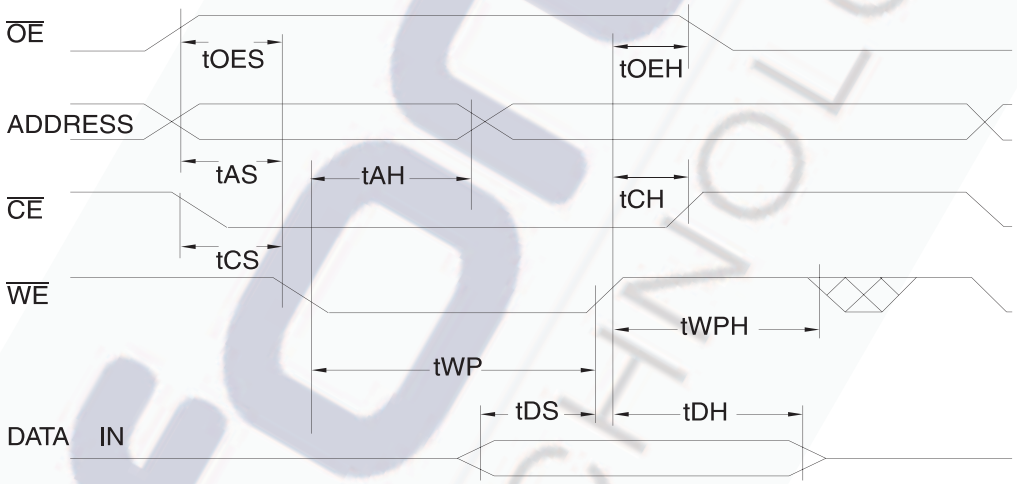
Note: 1. This parameter is 100% characterised and is not 100% tested.

AC Write Characteristics (Commercial/Industrial/Military)

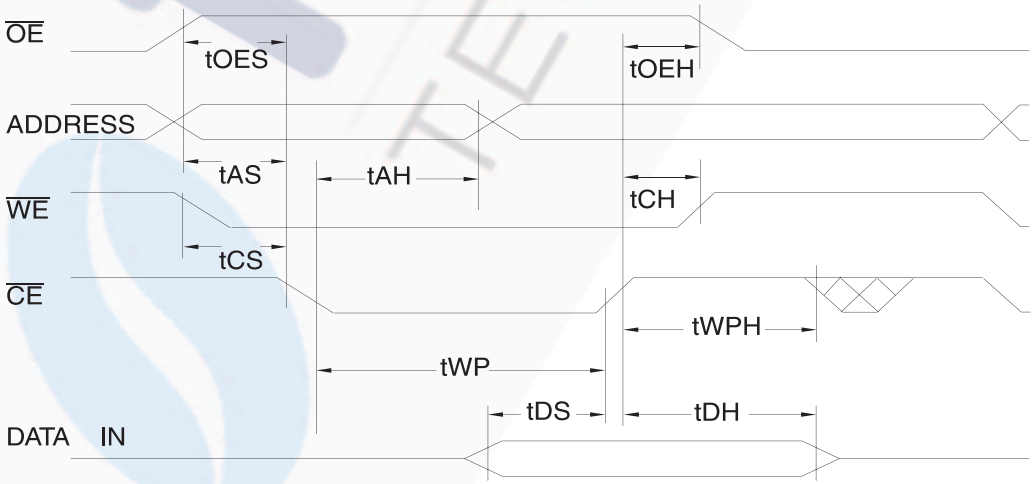
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

AC Write Waveforms

$\overline{WE}$ Controlled



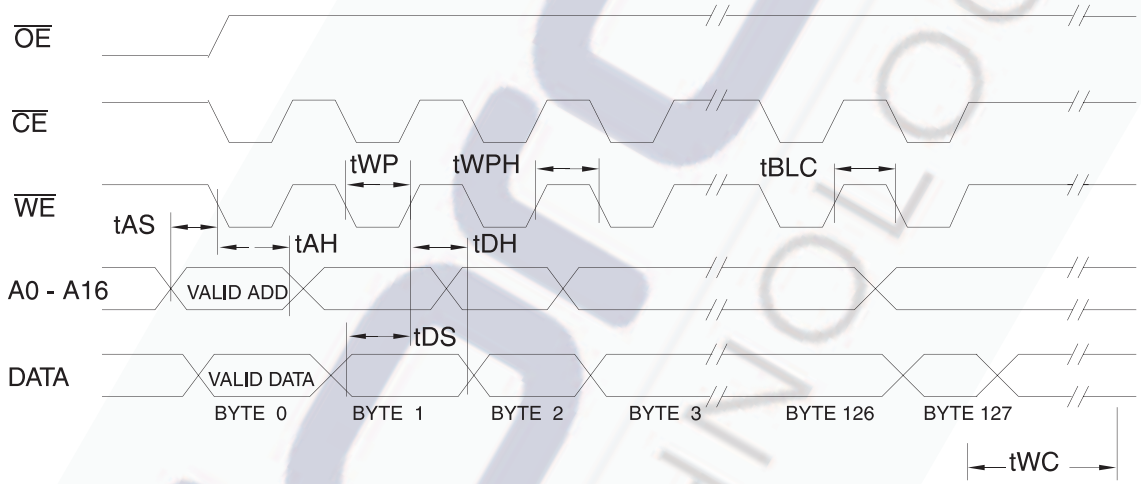
$\overline{CE}$ Controlled



Page Mode Characteristics (Commercial/Industrial/Military)

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns

Page Mode Write Waveforms (1)(2)

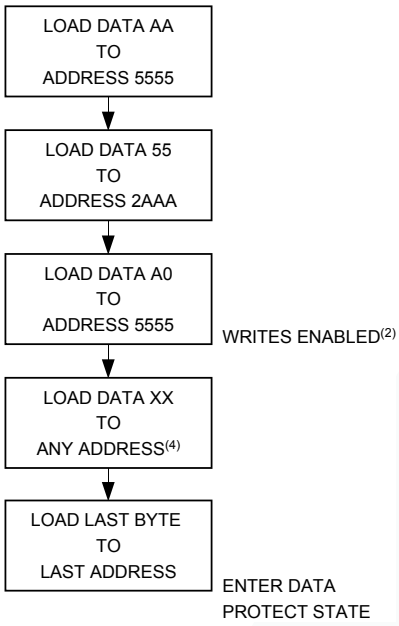


Notes: 1. A7 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

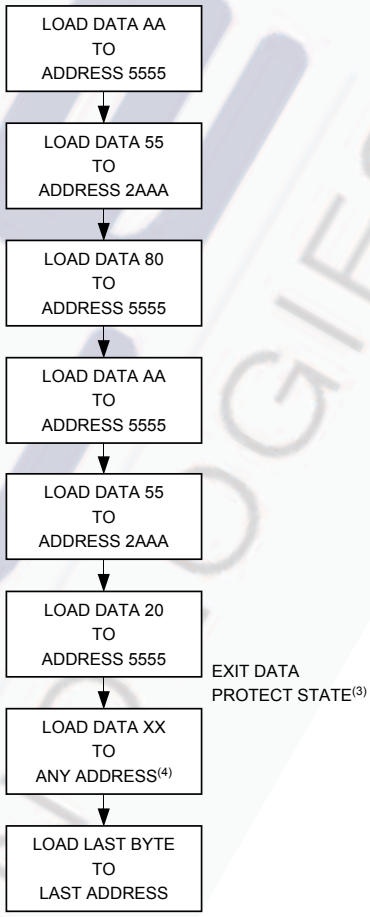
Chip Erase Waveforms

t_S = 5 msec (min.)
$t_W = t_H$ = 10 msec (min.)
V_H = 12.0V ± 0.5V

Software Data Protection Enable Algorithm(1)

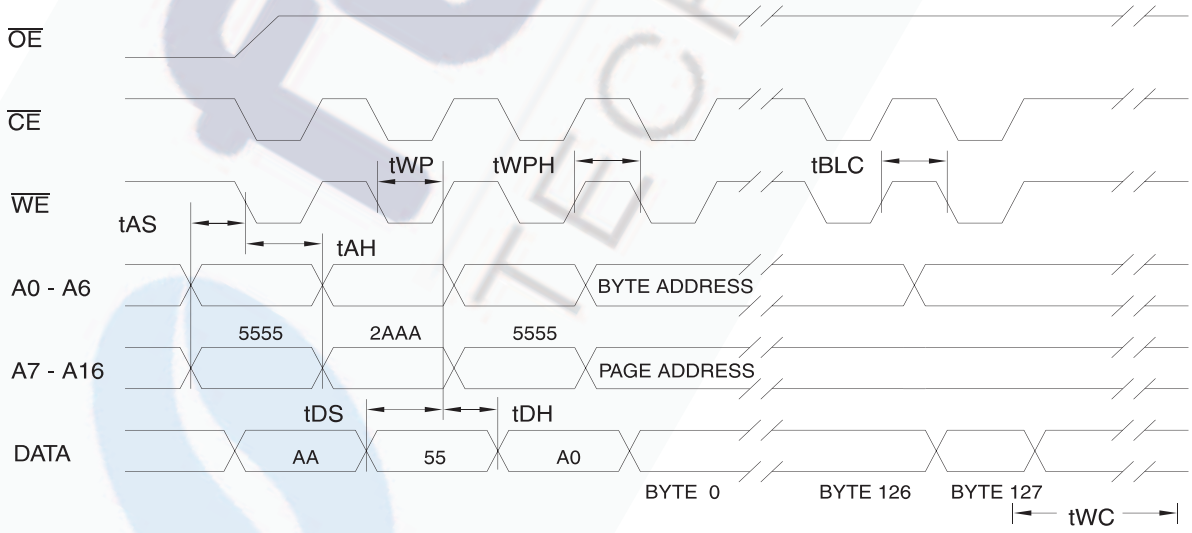


Software Data Protection Disable Algorithm(1)



Notes:
1. Data Format: I/O7 - I/O0 (Hex); Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data if loaded.
4. 1 to 128 bytes of data are loaded.

Software Protected Program Cycle Waveform(1)(2)(3)



Notes:
1. A0 - A14 must conform to the addressing sequence for the first 3 bytes as shown above.
2. After the command sequence has been issued and a page write operation follows, the page address inputs (A7 - A16) must be the same for each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characterstics (Commercial/Industrial/Military)(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterised and not 100% tested.
2. See AC Read Characteristics.

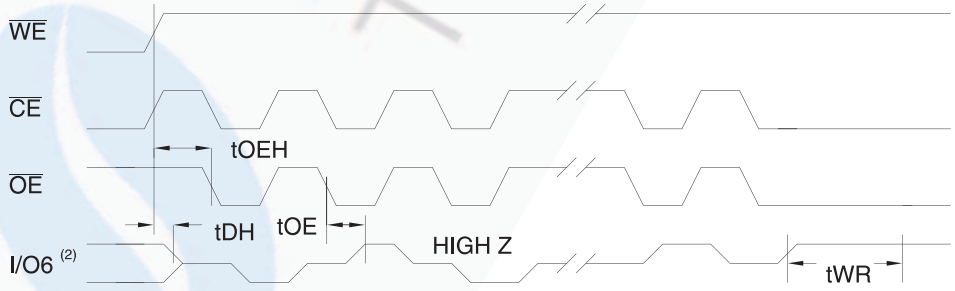
$\overline{\text{Data}}$ Polling Waveforms

Toggle Bit Characteristics (Commercial/Industrial/Military)(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterised and not 100% tested.
2. See AC Read Characteristics.

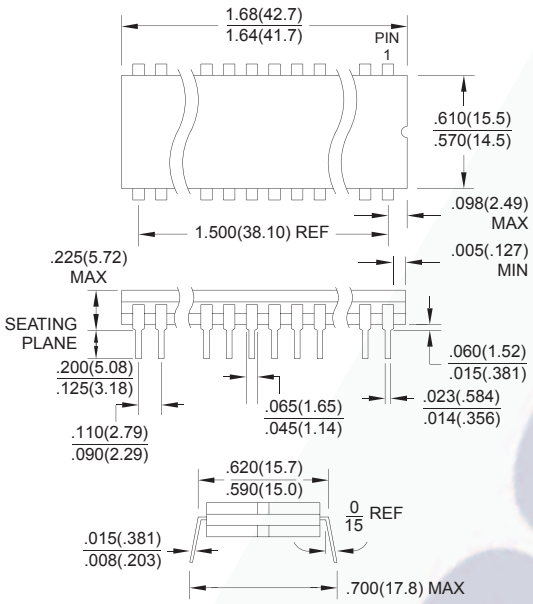
Toggle Bit Waveforms(1)(2)(3)



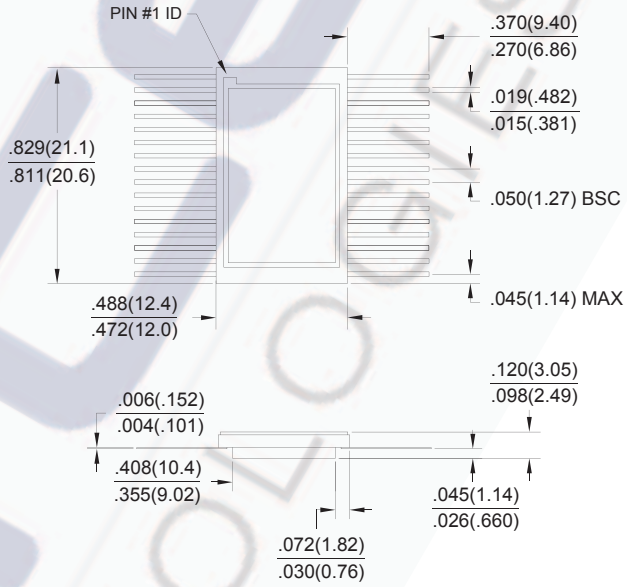
Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any addres location may be used but the address should not vary.

Packaging Information

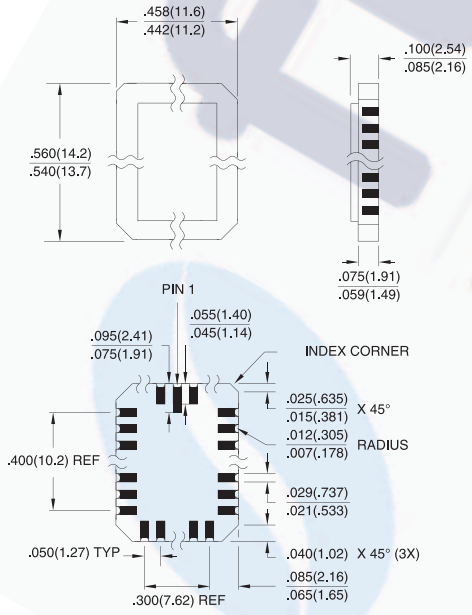
D 32-Lead, 0.600" Wide, Non-Windowed, Ceramic Dual inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-16 CONFIG A



F 32-Lead, Non-Windowed, Ceramic Bottom Brazed Flat Package (Flatpack)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 F-18 CONFIG B
JEDEC OUTLINE MO-115

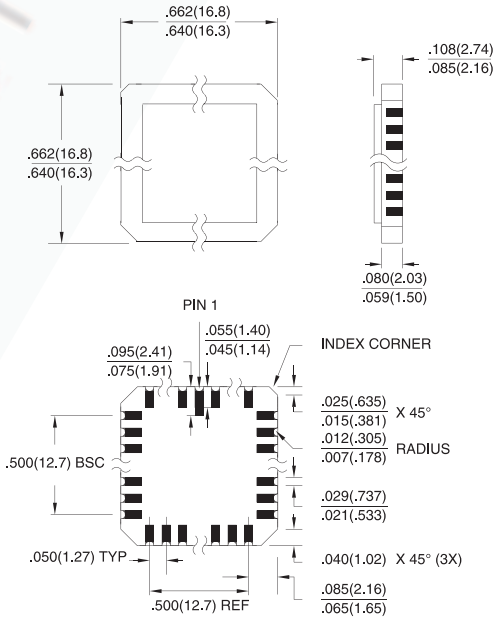


E 32-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)*
MIL-STD-1835 C-12



*Controlling dimension: millimeters

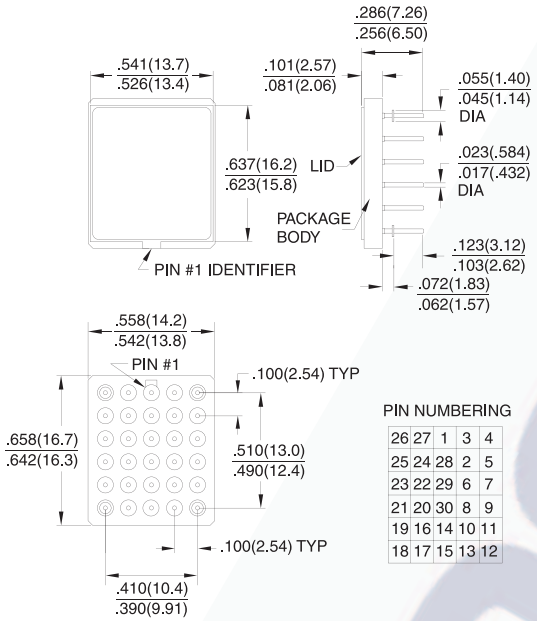
L 44-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)*
MIL-STD-1835 C-5



*Controlling dimension: millimeters

Packaging Information

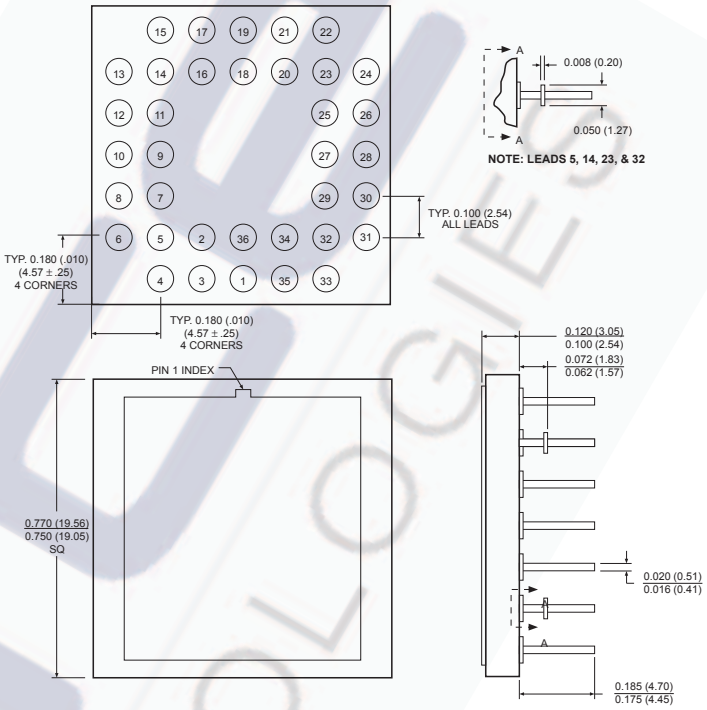
U 30-Pin, Ceramic Pin Grid Array (PGA)
Dimensions in Inches and (Millimeters)



PIN NUMBERING

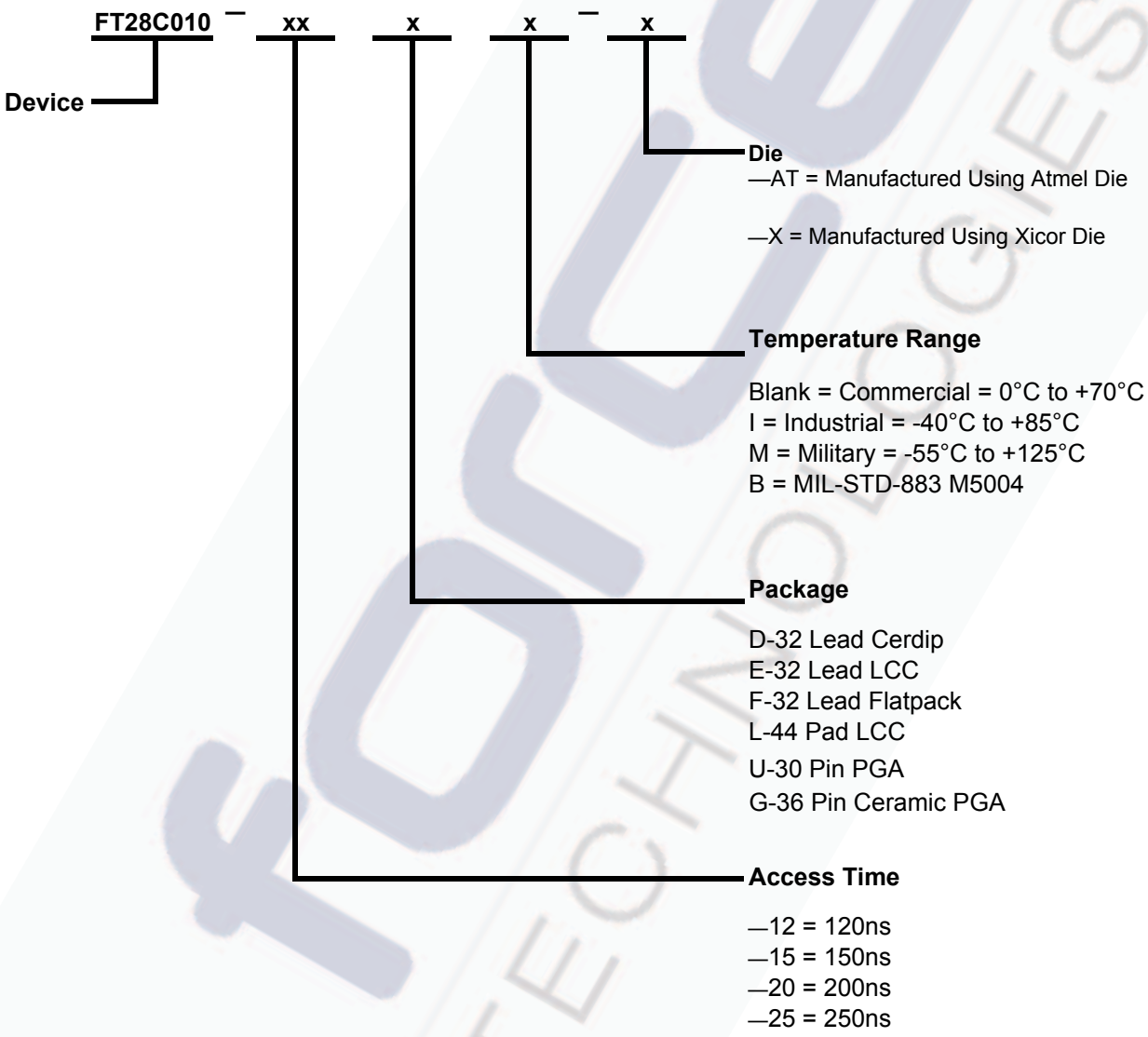
26	27	1	3	4
25	24	28	2	5
23	22	29	6	7
21	20	30	8	9
19	16	14	10	11
18	17	15	13	12

G 36-Lead Ceramic Pin Grid Array Package Typ



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Ordering Information



force TECHNOLOGIES

Monolithic Devices-Product Flow Matrix

The device shall be screened as specified in the table below. NON-COMPLIANT but in accordance with Mil-Std-883.
Manufactured batches shall have Lots tests carried out in accordance with Mil-Std-883 (Mil-M-38510)
All manufacturing is carried out at DSCC approved facilities.

Screening	Method	**/C**	**/I**	**/B** (5004)	**/B05** (5005)	QA test condition	UpScreen only
Visual Inspection Kit	Incoming and Outgoing Inspection Procedures	100%	100%	100%	100%		100%
Temperature Cycling				100%	100%	1010, test condition C	-
Centrifuge					100%	2001E	-
Constant acceleration				100%	100%	2001, test condition E (min)Y1 orientation	-
Seal a. Fine b. Gross			100%	100%	100%	1014 Cond A or B Cond C	-
Visual inspection				100%	100%	FT WIP documentation	100%
Interim (pre-BI)Electrical	In accordance with applicable device specification. or as defined in QM p4.1.1			100%	100%		100%
Burn-in test	Dynamic			100%	100%	1015, 160 hours at 125°C minimum	-
Percentage defective allowable (PDA) calculation	Review			5%	QCI		-
Final GrpA Electrical Tests A)Static Tests: 25oC (subgrp.1) Max.& Min. subgrp 2,3) B) Dynamic (Linear devices) 25oC (subgrp.4) Max.& Min. subgrp 5,6) C)Functional 25oC (subgrp.7) Max.& Min. subgrp 8) D) Switching (Digital devices) 25oC (subgrp.9) Max.& Min. subgrp 10,11)	In accordance with applicable device specification. or as defined in QM p4.1.1	100%	100% -40oC +85oC	100% -55oC +125oC	100% -55oC +125oC	5005 p2	100% Tmin Tmax
External Visual			100%	100%	100%	2009	100%
Group B				-	100%	2015/2003/2011	-
Group C				-	100%	1005	-
Group D				-	100%	2016/2004/1014/1011/ 1010/1004/2002/2007/ 2001/1009/1018/2025/2024	-
Marking & Inspect	As FT WIP documentation	100%		100%	100%		100%
Data Preparation	As FT QA documentation	100%		100%	100%		100%
Dry Bake store/ship	As FT WIP documentation	100%		100%	100%	JEDEC	100%

Note.
Suffix code

/C = Parts are assembled and tested to Commercial temperature 0oC to +70oC
/I = Parts are assembled and tested to Extended temperature -40oC to +85oC
/B = Parts are Based on METHOD 5004 screening procedures and Mil-Std-883F Test methods.
/B5 = Parts are Based on Control Procedures for :
GroupA (Electrical)
GroupB (Enviromental)
GroupC (Die related)
GroupD (Package related) Tests.
It is based on METHOD 5005 Conformance procedures and Mil-Std-883F Test methods

Revision History

Rev. 1	First Draft	12/01/11
Rev 1.1	Added 36 Lead Ceramic PGA (G)	02/03/11