P-CHANNEL ENHANCEMENT MODE POWER MOSFET

MEP4435Q8

Description

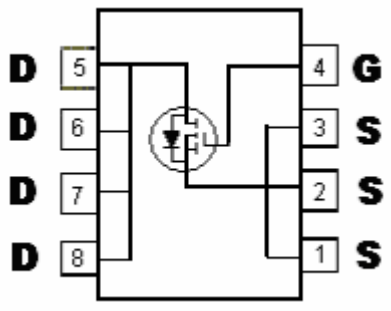
The MEP4435Q8 is a P-channel enhancement-mode MOSFET, providing the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness. The SOP-8 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

Features

- $R_{DS(ON)}$=20mΩ@V_{GS}=-10V, I_D=-10A
  $R_{DS(ON)}$=35mΩ@V_{GS}=-5V, I_D=-7A
- Simple drive requirement
- Low on-resistance
- Fast switching speed
- Pb-free package

Equivalent Circuit

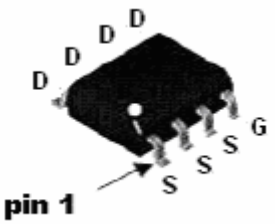
MEP4435Q8



G：Gate
S：Source
D：Drain

Outline

SOP-8



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	-30	V
Gate-Source Voltage	V_{GS}	±25	V
Continuous Drain Current @T_A=25 °C	I_D	-10	A
Continuous Drain Current @T_A=100 °C	I_D	-8	A
Pulsed Drain Current (Note 1)	I_{DM}	-40	A
Total Power Dissipation @ T_A=25 °C (Note 2)	Pd	2.5	W
Linear Derating Factor		0.02	W / °C
Operating Junction Temperature	Tj	-55~+150	°C
Storage Temperature	Tstg	-55~+150	°C
Thermal Resistance, Junction-to-Ambient (Note 2)	Rth,j-a	50	°C/W

Note : 1.Pulse width limited by maximum junction temperature.
2. Surface mounted on 1 in² copper pad of FR-4 board; 125 °C/W when mounted on minimum copper pad

Electrical Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	-30	-	-	V	V_{GS}=0, I_D=-250μA
$\Delta V_{DSS}/\Delta Tj$	-	-0.037	-	V/°C	Reference to 25°C, I_D=-1mA
$V_{GS(th)}$	-1	-	-3	V	V_{DS}=V_{GS}, I_D=-250μA
I_{GSS}	-	-	±100	nA	V_{GS}=±25V, V_{DS}=0
I_{DSS}	-	-	-1	μA	V_{DS}=-24V, V_{GS}=0
I_{DSS}	-	-	-10	μA	V_{DS}=-20V, V_{GS}=0, Tj=125°C
$I_{D(ON)}$	40	-	-	A	V_{DS}=-5V, V_{GS}=-10V
*$R_{DS(ON)}$	-	15	20	mΩ	I_D=-10A, V_{GS}=-10V
	-	25	35		I_D=-7A, V_{GS}=-5V
*G_{FS}	-	24	-	S	V_{DS}=-5V, I_D=-10A
Dynamic					
Ciss	-	2815	-	pF	V_{DS}=-15V, V_{GS}=0, f=1MHz
Coss	-	1060	-		
Crss	-	955	-		
$t_{d(ON)}$	-	12	-	ns	V_{DD}=-15V, I_D=-1A, V_{GS}=-10V, R_G=2.7Ω
t_r	-	10	-		
$t_{d(OFF)}$	-	35	-		
t_f	-	7	-		
Qg	-	25	-	nC	V_{DS}=-15V, I_D=-10A, V_{GS}=-10V,
Qgs	-	7	-		
Qgd	-	9	-		
Rg	-	4	-	Ω	V_{GS}=15mV, V_{DS}=0, f=1MHz

Electrical Characteristics(Cont.) (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Source-Drain Diode					
I_S	-	-	-3	A	$V_D=V_G=0$, $V_S=-1.2V$
I_{SM}	-	-	-12		$V_{GS}=0V$, $I_{SD}=-2.1A$
*V_{SD}	-	-	-1.3	V	$I_F=I_S$, $V_{GS}=0V$
*trr	-	32	-	ns	$I_F=I_S$, $dI_F/dt=100A/\mu s$
*Qrr	-	26	-	nC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Characteristic Curves

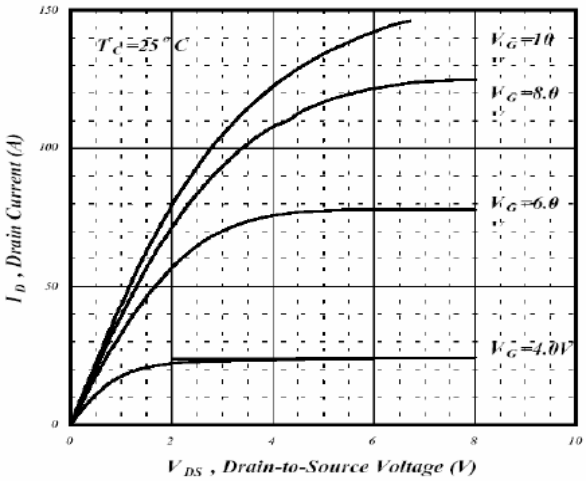


Fig 1. Typical Output Characteristics

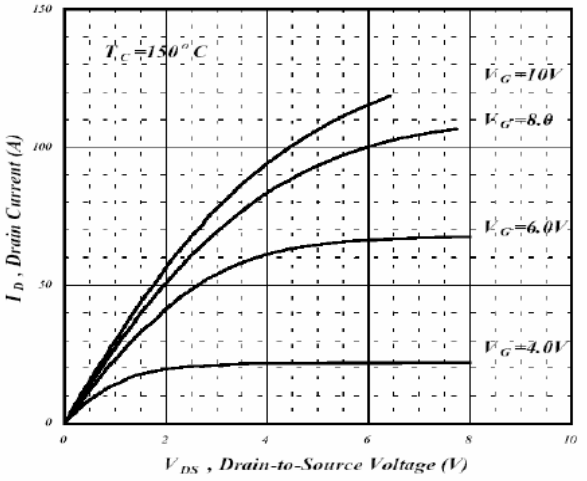


Fig 2. Typical Output Characteristics

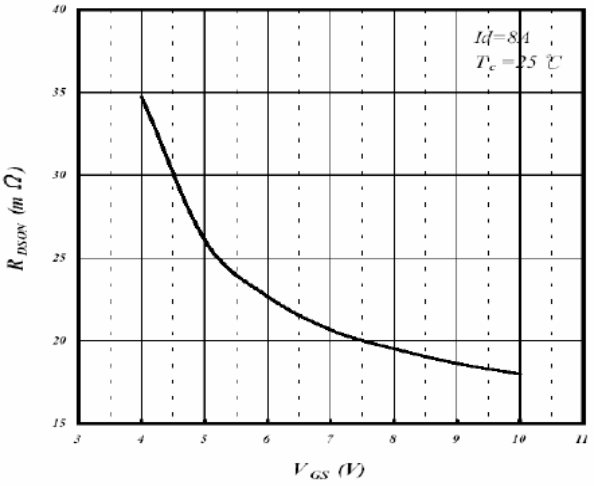


Fig 3. On-Resistance v.s. Gate Voltage

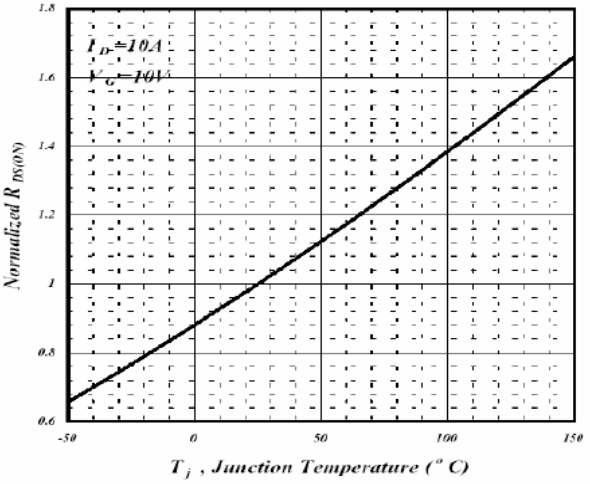


Fig 4. Normalized On-Resistance v.s. Junction Temperature

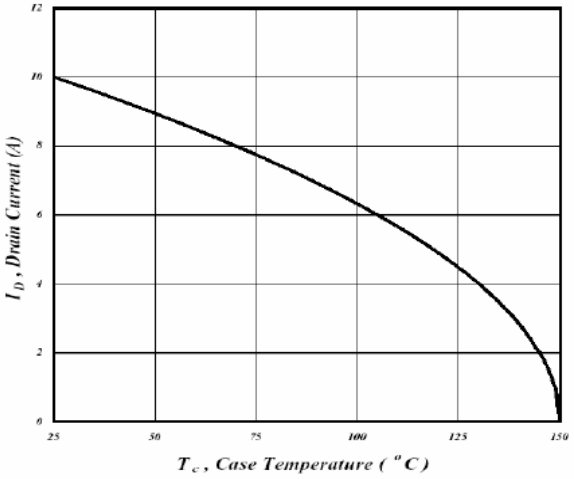


Fig 5. Maximum Drain Current v.s. Case Temperature

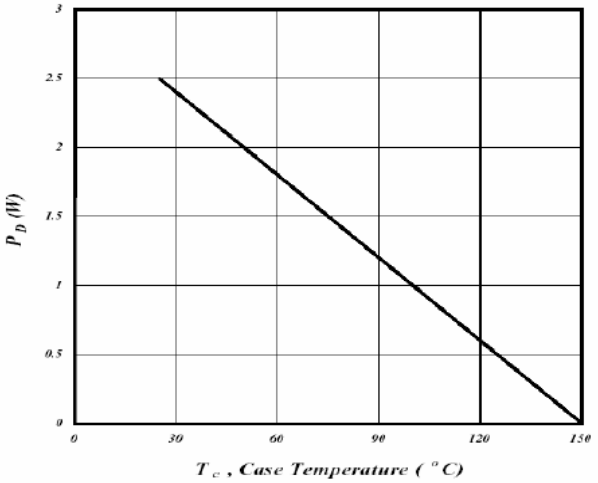


Fig 6. Type Power Dissipation

Characteristic Curves(Cont.)

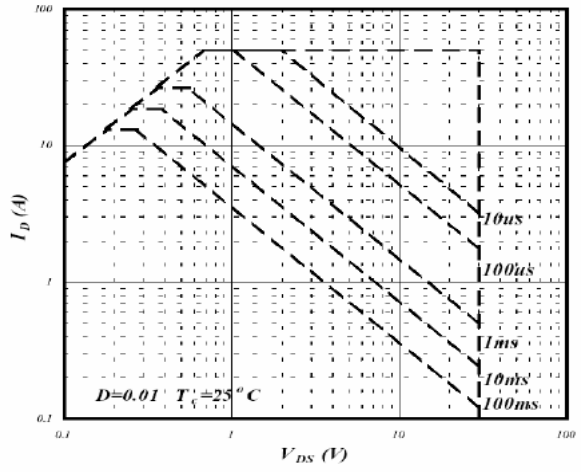


Fig 7. Maximum Safe Operating Area

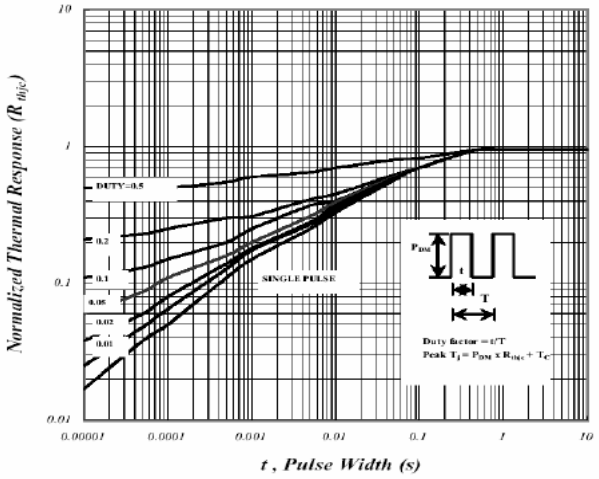


Fig 8. Effective Transient Thermal Impedance

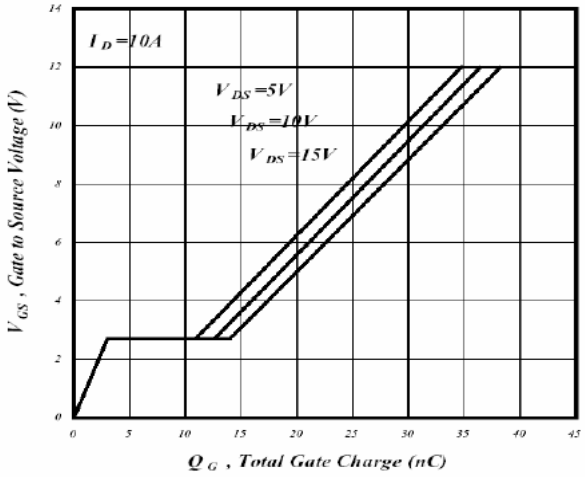


Fig 9. Gate Charge Characteristics

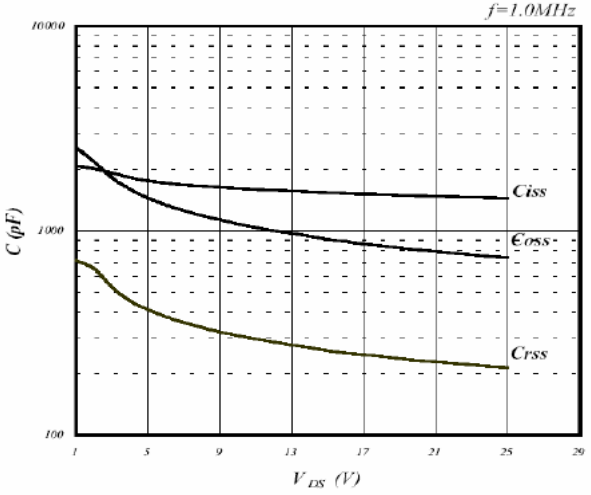


Fig 10. Typical Capacitance Characteristics

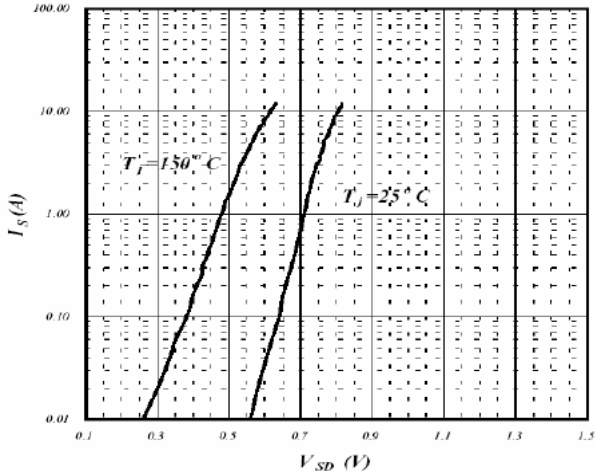


Fig 11. Forward Characteristics of Reverse Diode

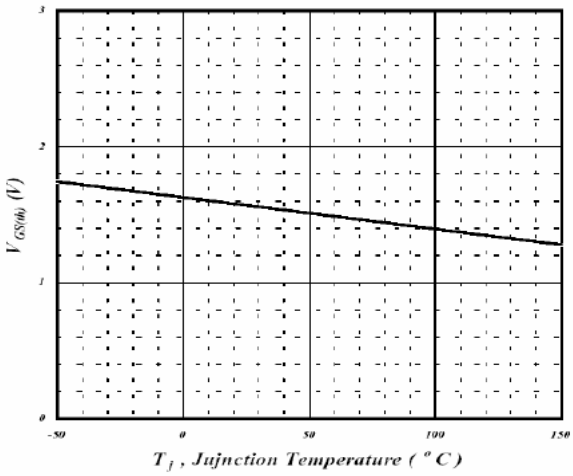


Fig 12. Gate Threshold Voltage v.s. Junction Temperature

Characteristic Curves(Cont.)

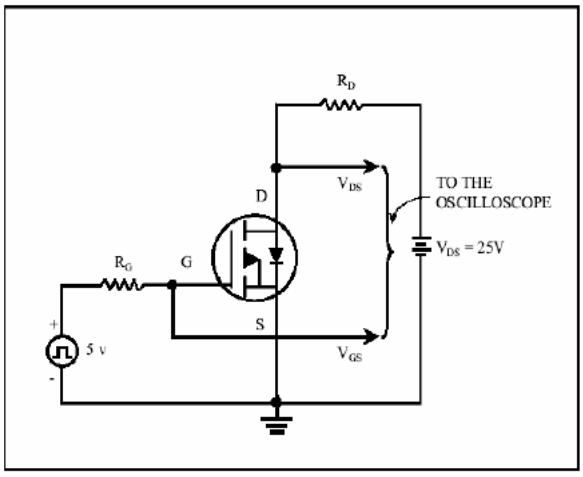


Fig 13. Switching Time Circuit

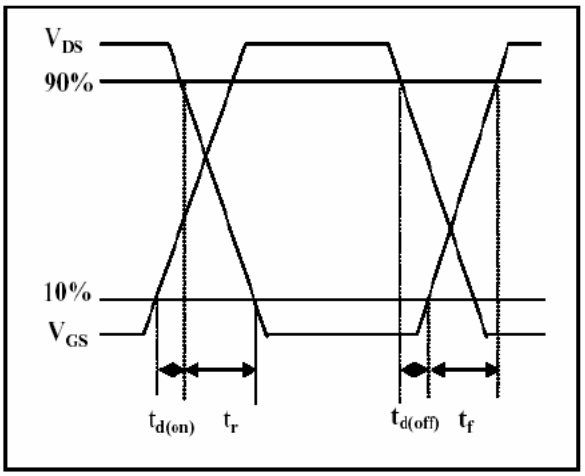


Fig 14. Switching Time Waveform

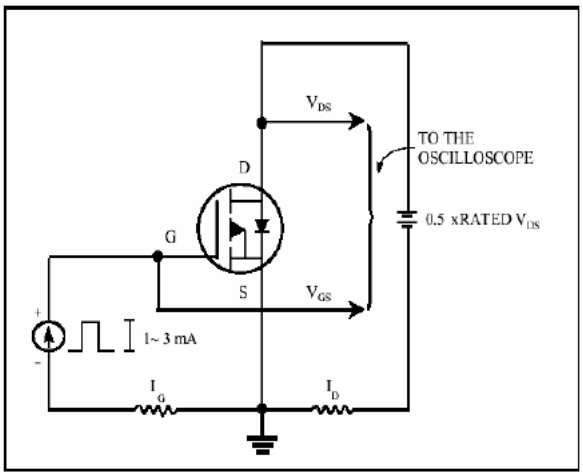


Fig 15. Gate Charge Circuit

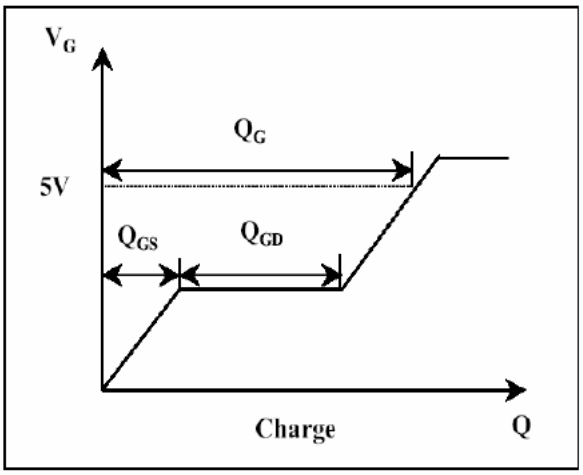
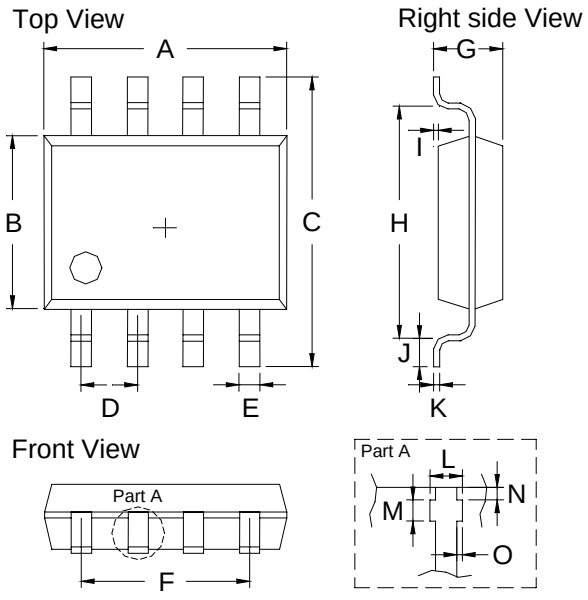
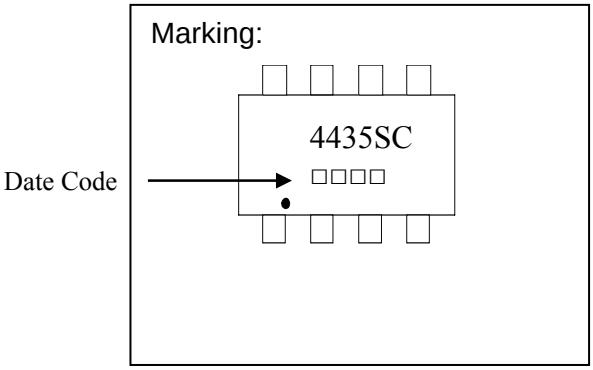


Fig 16. Gate Charge Waveform

SOP-8 Dimension





8-Lead SOP-8 Plastic Package
CYStek Package Code: Q8

*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1909	0.2007	4.85	5.10	I	0.0019	0.0078	0.05	0.20
B	0.1515	0.1555	3.85	3.95	J	0.0118	0.0275	0.30	0.70
C	0.2283	0.2441	5.80	6.20	K	0.0074	0.0098	0.19	0.25
D	0.0480	0.0519	1.22	1.32	L	0.0145	0.0204	0.37	0.52
E	0.0145	0.0185	0.37	0.47	M	0.0118	0.0197	0.30	0.50
F	0.1472	0.1527	3.74	3.88	N	0.0031	0.0051	0.08	0.13
G	0.0570	0.0649	1.45	1.65	O	0.0000	0.0059	0.00	0.15
H	0.1889	0.2007	4.80	5.10					

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Tin plating
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0