SN8P2743 Series

USER'S MANUAL

Version 2.0

SN8P2743
SN8P2742
SN8P27411

SONiX 8-Bit Micro-Controller

AMENDENT HISTORY

Version	Date	Description
VER 0.1	Oct. 2009	First issue.
VER 0.2	Mar. 2010	1. Fix typing errors of feature table. 2. Fix typing errors of bit definition of system registers. 3. Fix typing errors of I/O shared pin table. 4. Add P0 application notices. 5. Modify P0.1 to write only type. 6. Modify TC0 pulse width table. 7. Add TC0ENB control notice in comparator 1 special function. 8. Modify OP-amp pin definition. 9. Add development tools description. 10. Modify electrical characteristic section.
VER 0.3	Apr. 2010	1. Modify the pin assignments of SN8P2742P and SN8P2742S. 2. Modify PROGRAMMING PIN MAPPING table for SN8P2742P and SN8P2742S. 3. Modify DEVELOPMENT TOOL for SN8P2742.
VER 0.4	Jun. 2010	1. Modify EV-Kit version from “A” to “V1.0”. 2. Modify EV2740 EV-KIT schematic / outline. 3. Modify DEVELOPMENT TOOL chapter.
VER 1.0	May. 2011	1. Version update. 2. Modify “DEVELOPMENT TOOL” description 3. Modify “Chapter 16.3 CHARACTERISTIC GRAPHS”
VER 1.1	May. 2011	1. Modify “Chapter 10.4 COMPARATOR MODE REGISTER” CMDB0 register bit3 CM1D3 >> CM0D3. 2. Modify “Chapter 13.1 OVERVIEW” description : It is necessary to set P4 as input mode with pull-up resistor by program >> It is necessary to set P4 as input mode without pull-up resistor by program
VER 1.2	Sep. 2011	1. Add SN8P2741 pin assignment and modify some Chapters
VER 1.3	Dec. 2011	1. Delete SN8P2741 pin assignment and the others. 2. Add SN8P27411 pin assignment and the others.
VER 1.4	May. 2012	1. Modify SN8P27411 pin assignment.
VER 1.5	Oct. 2012	Modify SN8P27411 pin assignment.
VER 1.6	Nov. 2012	Modify “Electrical Characteristic” with “OP AMP CHARACTERISTIC”.
VER 1.7	Jun. 2013	Modify Package Information: SK-DIP24 content.
VER 1.8	Aug. 2013	1. Modify “Electrical Characteristic” with “OP AMP CHARACTERISTIC” with offset range. 2. Modify “ANALOG COMPARATOR 0~2” chapters description and others.
VER 1.9	Jul. 2015	Add “To support MUL / DAA instruction” description.
VER 2.0	Mar. 2016	Modify operating temperature from 0~70℃ to -20~70℃ and others.

Table of Content

1 PRODUCT OVERVIEW

1.1 FEATURES

- **Memory configuration**
  ROM size: 4K * 16 bits.
  RAM size: 128 * 8 bits.

- **8 levels stack buffer.**
- **7 interrupt sources**
  6 internal interrupts: T0, TC0, ADC, CM0, CM1, CM2
  1 external interrupt: INT0

- **I/O pin configuration**
  Bi-directional: P0, P1, P4.
  Wakeup: P0, P1 level change.
  Pull-up resisters: P0, P1, P4.
  Op-amp/Comparator pins: P1, P4.
  ADC input pin: P4.0~P4.7.

- **Fcpu (Instruction cycle)**
  Fcpu = Fosc/4, Fosc/8, Fosc/16.

- **3-Level LVD**
  2.0V/2.4V/3.6V

- **Powerful instructions**
  Instruction's length is one word.
  Most of instructions are one cycle only.
  All ROM area JMP/CALL instruction.
  All ROM area lookup table function (MOVC).
  To support MUL / DAA instruction

- **One 8-bit basic timer. (T0).**
- **One 8-bit timer with PWM and pulse generator (TC0).**
- **One 2K/4K programmable buzzer output.**
- **8-channel 12-bit SAR ADC.**
- **1-set rail-to-rail OP-amp.**
- **3-set comparators.**
- **On chip watchdog timer and clock source is Internal low clock RC type (16KHz @3V, 32KHz @5V).**

- **4 system clocks**
  External high clock: RC type up to 10 MHz
  External high clock: Crystal type up to 16 MHz
  Internal high clock: RC type 16MHz
  Internal low clock: RC type 16KHz(3V), 32KHz(5V)

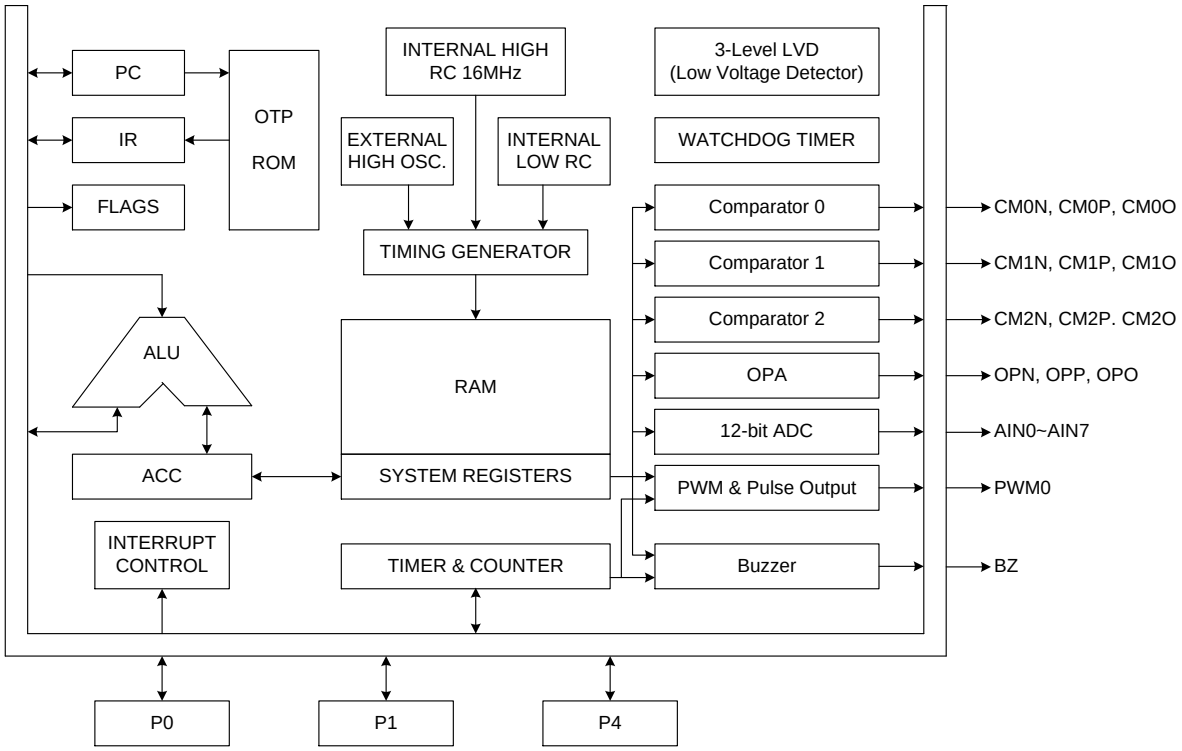
- **4 operating modes**
  Normal mode: Both high and low clock active
  Slow mode: Low clock only.
  Sleep mode: Both high and low clock stop
  Green mode: Periodical wakeup by timer

- **Package (Chip form support)**
  SKDIP 24 pin
  PDIP 20 pin
  SOP 24 pin
  SOP 20 pin
  PDIP 16 pin
  SOP 16 pin

☞ **Features Selection Table**

CHIP	ROM	RAM	Stack	Timer		PWM	Pulse Generator	Buzzer	Ext. Int	I/O	ADC	OP-amp	Comp-arator	Package
				T0	TC0									
SN8P2743	4K*16	128*8	8	V	V	1	1	1	1	22	8-ch	1	3	SKDIP24 SOP24
SN8P2742	4K*16	128*8	8	V	V	1	1	1	-	18	6-ch	1	3	PDIP20 SOP20
SN8P27411	4K*16	128*8	8	V	V	1	1	1	-	14	6-ch	1	3	PDIP16 SOP16

1.2 SYSTEM BLOCK DIAGRAM



1.3 PIN ASSIGNMENT

SN8P2743K (SKDIP 24 pin)
SN8P2743S (SOP 24 pin)

VSS	1	U	24	VDD
XIN/P0.6	2		23	P4.7/AIN7
XOUT/P0.5/BZ	3		22	P4.6/AIN6
RST/VPP/P0.4	4		21	P4.5/AIN5
P0.0/INT0	5		20	P4.4/AIN4
P0.1/PWM0	6		19	P4.3/AIN3/CM0O
P0.2/CM0P	7		18	P4.2/AIN2/CM1O
P0.3/CM0N	8		17	P4.1/AIN1/CM2O
P1.6/CM1P	9		16	P4.0/AIN0/AVREFH
P1.5/CM1N	10		15	P1.0/OPN
P1.4/CM2P	11		14	P1.1/OPP
P1.3/CM2N	12		13	P1.2/OPO

SN8P2742P (DIP 20 pin)
SN8P2742S (SOP 20 pin)

VSS	1	U	20	VDD
XIN/P0.6	2		19	P4.5/AIN5
XOUT/P0.5/BZ	3		18	P4.4/AIN4
RST/VPP/P0.4/ P0.1/PWM0	4		17	P4.3/AIN3/CM0O
P0.2/CM0P	5		16	P4.2/AIN2/CM1O
P0.3/CM0N	6		15	P4.1/AIN1/CM2O
P1.6/CM1P	7		14	P4.0/AIN0/AVREFH
P1.5/CM1N	8		13	P1.0/OPN
P1.4/CM2P	9		12	P1.1/OPP
P1.3/CM2N	10		11	P1.2/OPO

SN8P27411P (DIP 16 pin)

VDD	1	U	16	P4.7/AIN7
XOUT/P0.5/BZ	2		15	P4.6/AIN6
RST/VPP/P0.4/ P0.1/PWM0	3		14	P4.4/AIN4
P0.2/CM0P	4		13	VSS
P0.3/CM0N	5		12	P4.2/AIN2/CM1O
P1.5/CM1N	6		11	P4.1/AIN1/CM2O
P1.3/CM2N	7		10	P4.0/AIN0/AVREFH
P4.3/OPO	8		9	P1.0/OPN

✸ **OPP (OPA's positive pin) pin connects to ground.**

SN8P27411S (SOP 16 pin)

VDD	1	U	16	VSS
XOUT/P0.5/BZ	2		15	P4.7/AIN7
RST/VPP/P0.4/ P0.1/PWM0	3		14	P4.6/AIN6
P0.2/CM0P	4		13	P4.4/AIN4
P0.3/CM0N	5		12	P4.2/AIN2/CM1O
P1.5/CM1N	6		11	P4.1/AIN1/CM2O
P1.3/CM2N	7		10	P4.0/AIN0/AVREFH
P4.3/OPO	8		9	P1.0/OPN

✸ **OPP (OPA's positive pin) pin connects to ground.**

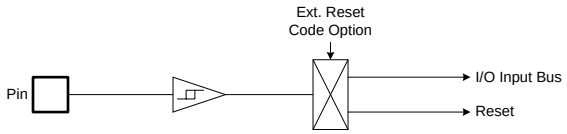
1.4 PIN DESCRIPTIONS

PIN NAME	TYPE	DESCRIPTION
VDD, VSS	P	Power supply input pins for digital and analog circuit.
P0.4/RST/VPP	I, P	RST: System external reset input pin. Schmitt trigger structure, active "low", normal stay to "high".
		VPP: OTP 12.3V power input pin in programming mode.
		P0.4: Input only pin with Schmitt trigger structure and no pull-up resistor. Level change wake-up.
XIN/P0.6	I/O	XIN: Oscillator input pin while external oscillator enable (crystal and RC).
		P0.6: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
XOUT/P0.5/BZ	I/O	XOUT: Oscillator output pin while external crystal enable.
		P0.5: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
		BZ: 2K/4K programmable buzzer output pin.
P0.0/INT0	I/O	P0.0: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
		INT0: External interrupt 0 input pin.
P0.1/PWM0	I/O	P0.1: Output pin with open-drain structure.
		PWM0: PWM output pin and pulse output pin.
P0.2/CM0P	I/O	P0.2: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
		CM0P: The positive input pin of comparator.
P0.2/CM0N	I/O	P0.3: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
		CM0N: The negative input pin of comparator.
P1.0/OPN	I/O	P1.0: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
		OPN: The negative input pin of OP amp.
P1.1/OPP	I/O	P1.1: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
		OPP: The positive input pin of OP amp.
P1.2/OPO	I/O	P1.2: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
		OPO: The output pin of OP amp.

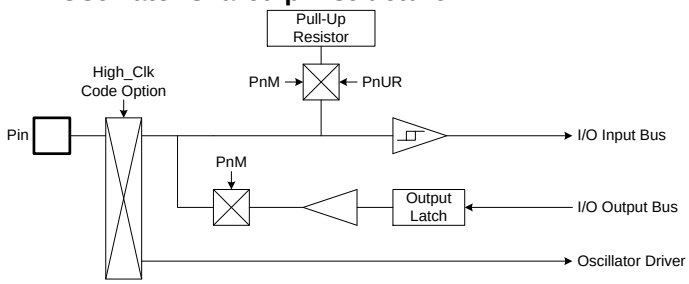
P1.3/CM2N	I/O	P1.3: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
		CM2N: The negative input pin of comparator.
P1.4/CM2P	I/O	P1.4: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
		CM2P: The positive input pin of comparator.
P1.5/CM1N	I/O	P1.5: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
		CM1N: The negative input pin of comparator.
P1.6/CM1P	I/O	P1.6: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters. Level change wake-up.
		CM1P: The positive input pin of comparator.
P4.0/AIN0/AVREFH	I/O	P4.0: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
		AIN0: ADC analog input pin.
		AVREFH: ADC reference high voltage input pin.
P4.1/AIN1/CM2O	I/O	P4.1: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
		AIN1: ADC analog input pin.
		CM2O: The output pin of comparator.
P4.2/AIN2/CM1O	I/O	P4.2: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
		AIN2: ADC analog input pin.
		CM1O: The output pin of comparator.
P4.3/AIN3/CM0O	I/O	P4.3: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
		AIN3: ADC analog input pin.
		CM0O: The output pin of comparator.
P4.4/AIN4	I/O	P4.4: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
		AIN4: ADC analog input pin.
P4.5/AIN5	I/O	P4.5: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
		AIN5: ADC analog input pin.
P4.6/AIN6	I/O	P4.6: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
		AIN6: ADC analog input pin.
P4.7/AIN7	I/O	P4.7: Bi-direction pin. Schmitt trigger structure as input mode. Built-in pull-up resisters.
		AIN7: ADC analog input pin. Refer to ADC section.

1.5 PIN CIRCUIT DIAGRAMS

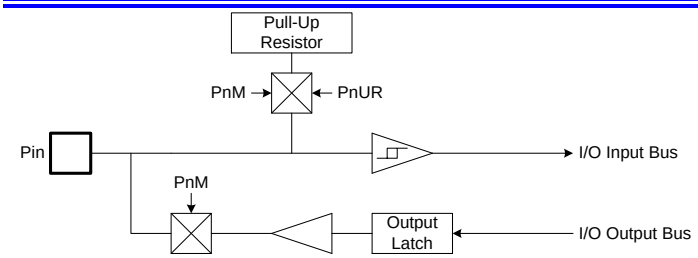
- **Reset shared pin structure:**



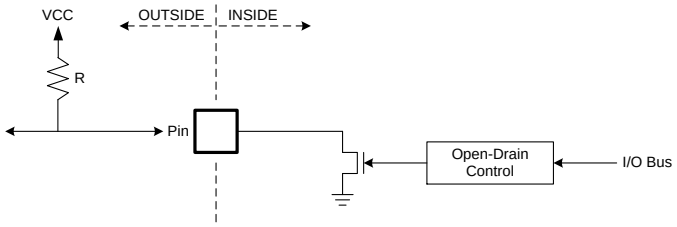
- **Oscillator shared pin structure:**



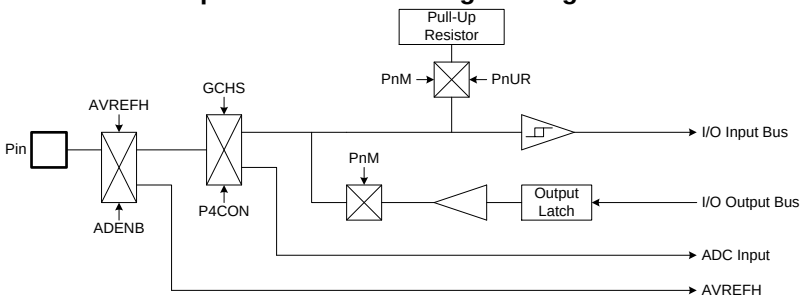
- **GPIO structure:**



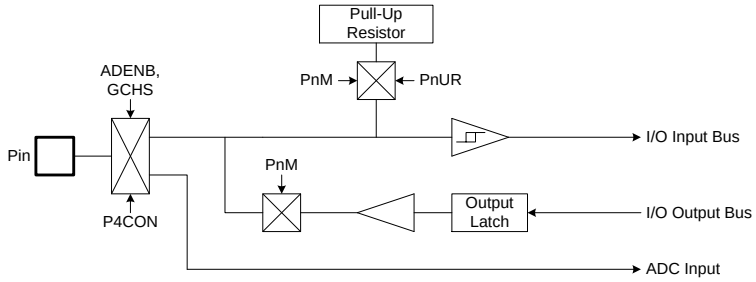
- **P0.1: Open-drain shared pin, output only I/O:**



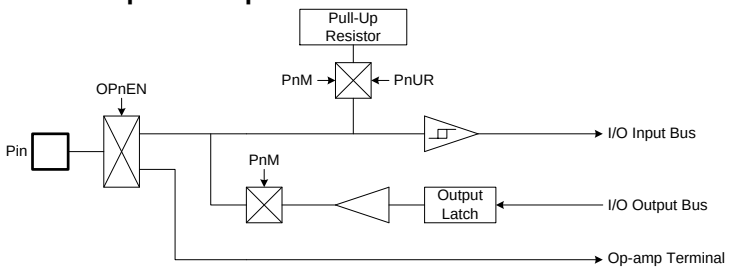
- **ADC shared pin with reference high voltage structure:**



- **ADC shared pin structure:**

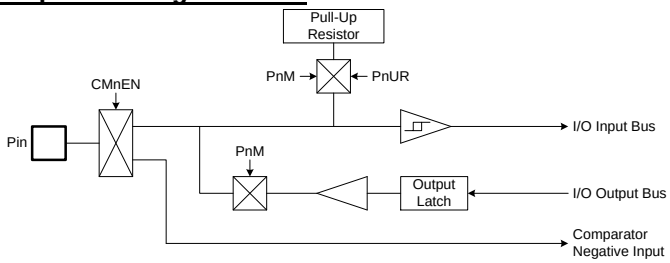


- **OP-amp shared pins structure:**

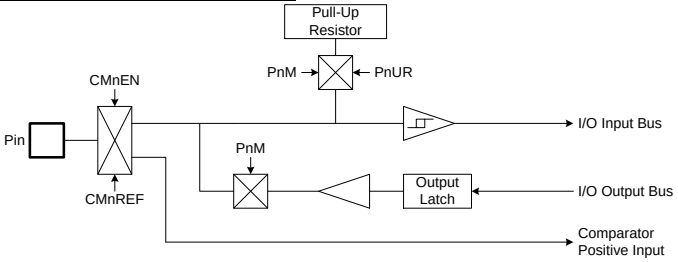


- **Comparator shared pins structure:**

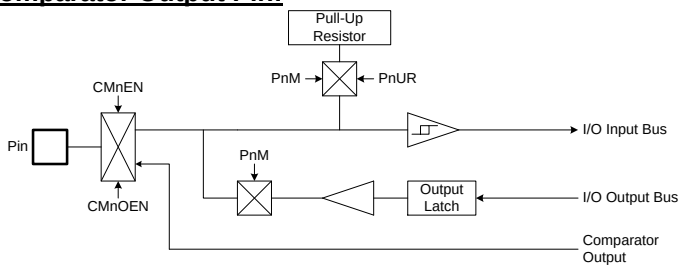
Comparator Negative Pin:



Comparator Positive Pin:



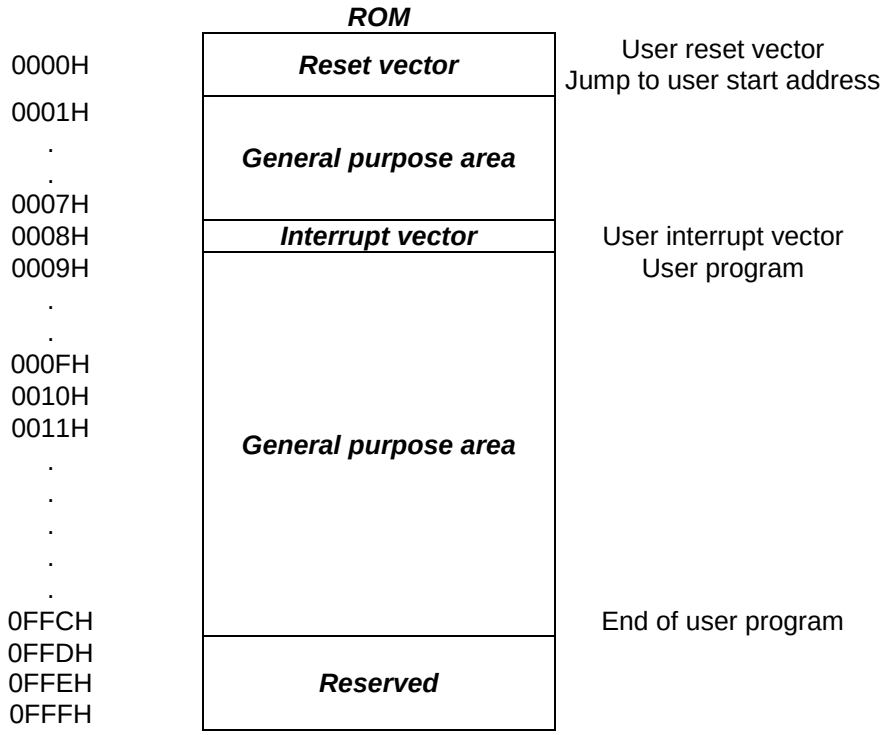
Comparator Output Pin:



2 CENTRAL PROCESSOR UNIT (CPU)

2.1 PROGRAM MEMORY (ROM)

☞ ***4K words ROM***



The ROM includes Reset vector, Interrupt vector, General purpose area and Reserved area. The Reset vector is program beginning address. The Interrupt vector is the head of interrupt service routine when any interrupt occurring. The General purpose area is main program area including main loop, sub-routines and data table.

2.1.1 RESET VECTOR (0000H)

A one-word vector address area is used to execute system reset.

- ☞ **Power On Reset (NT0=1, NPD=0).**
- ☞ **Watchdog Reset (NT0=0, NPD=0).**
- ☞ **External Reset (NT0=1, NPD=1).**

After power on reset, external reset or watchdog timer overflow reset, then the chip will restart the program from address 0000h and all system registers will be set as default values. It is easy to know reset status from NT0, NPD flags of PFLAG register. The following example shows the way to define the reset vector in the program memory.

➢ **Example: Defining Reset Vector**

```
                ORG     0           ; 0000H
                JMP     START       ; Jump to user program address.
                …

                ORG     10H
START:                              ; 0010H, The head of user program.
                …                   ; User program
                …


                ENDP                ; End of program
```

2.1.2 INTERRUPT VECTOR (0008H)

A 1-word vector address area is used to execute interrupt request. If any interrupt service executes, the program counter (PC) value is stored in stack buffer and jump to 0008h of program memory to execute the vectored interrupt. Users have to define the interrupt vector. The following example shows the way to define the interrupt vector in the program memory.

✸ ***Note: "PUSH", "POP" instructions save and load ACC/PFLAG without (NT0, NPD). PUSH/POP buffer is a unique buffer and only one level.***

➢ **Example: Defining Interrupt Vector. The interrupt service routine is following ORG 8.**

```
.CODE
                ORG     0               ; 0000H
                JMP     START           ; Jump to user program address.
                …

                ORG     8               ; Interrupt vector.
                PUSH                    ; Save ACC and PFLAG register to buffers.
                …
                …
                POP                     ; Load ACC and PFLAG register from buffers.
                RETI                    ; End of interrupt service routine
                …

START:                                  ; The head of user program.
                …                       ; User program
                …
                JMP     START           ; End of user program
                …

                ENDP                    ; End of program
```

➢ **Example: Defining Interrupt Vector. The interrupt service routine is following user program.**

```
.CODE
        ORG     0           ; 0000H
        JMP     START       ; Jump to user program address.
        …
        ORG     8           ; Interrupt vector.
        JMP     MY_IRQ      ; 0008H, Jump to interrupt service routine address.

        ORG     10H
START:                      ; 0010H, The head of user program.
        …                   ; User program.
        …
        …
        JMP     START       ; End of user program.
        …
MY_IRQ:                     ;The head of interrupt service routine.
        PUSH                ; Save ACC and PFLAG register to buffers.
        …
        …
        POP                 ; Load ACC and PFLAG register from buffers.
        RETI                ; End of interrupt service routine.
        …

        ENDP                ; End of program.
```

✸ ***Note: It is easy to understand the rules of SONIX program from demo programs given above. These points are as following:***

1. ***The address 0000H is a "JMP" instruction to make the program starts from the beginning.***
2. ***The address 0008H is interrupt vector.***
3. ***User's program is a loop routine for main purpose application.***

2.1.3 LOOK-UP TABLE DESCRIPTION

In the ROM's data lookup function, Y register is pointed to middle byte address (bit 8~bit 15) and Z register is pointed to low byte address (bit 0~bit 7) of ROM. After MOVC instruction executed, the low-byte data will be stored in ACC and high-byte data stored in R register.

➢ **Example: To look up the ROM data located "TABLE1".**

```
                B0MOV   Y, #TABLE1$M    ; To set lookup table1's middle address
                B0MOV   Z, #TABLE1$L    ; To set lookup table1's low address.
                MOVC                    ; To lookup data, R = 00H, ACC = 35H
                                        ; Increment the index address for next address.
                INCMS   Z               ; Z+1
                JMP     @F              ; Z is not overflow.
                INCMS   Y               ; Z overflow (FFH → 00), → Y=Y+1
                NOP                     ;
                                        ;
@@:             MOVC                    ; To lookup data, R = 51H, ACC = 05H.
                …                       ;
TABLE1:         DW      0035H           ; To define a word (16 bits) data.
                DW      5105H
                DW      2012H
                …
```

✷ ***Note: The Y register will not increase automatically when Z register crosses boundary from 0xFF to 0x00. Therefore, user must be take care such situation to avoid look-up table errors. If Z register is overflow, Y register must be added one. The following INC_YZ macro shows a simple method to process Y and Z registers automatically.***

➢ **Example: INC_YZ macro.**

```
INC_YZ          MACRO
                INCMS   Z               ; Z+1
                JMP     @F              ; Not overflow

                INCMS   Y               ; Y+1
                NOP                     ; Not overflow
@@:
                ENDM
```

➢ **Example: Modify above example by "INC_YZ" macro.**

```
                B0MOV     Y, #TABLE1$M    ; To set lookup table1's middle address
                B0MOV     Z, #TABLE1$L    ; To set lookup table1's low address.
                MOVC                      ; To lookup data, R = 00H, ACC = 35H

                INC_YZ                    ; Increment the index address for next address.
                                          ;
@@:             MOVC                      ; To lookup data, R = 51H, ACC = 05H.
                …                         ;
TABLE1:         DW        0035H           ; To define a word (16 bits) data.
                DW        5105H
                DW        2012H
                …
```

The other example of look-up table is to add Y or Z index register by accumulator. Please be careful if "carry" happen.

➢ **Example: Increase Y and Z register by B0ADD/ADD instruction.**

```
                B0MOV     Y, #TABLE1$M    ; To set lookup table's middle address.
                B0MOV     Z, #TABLE1$L    ; To set lookup table's low address.

                B0MOV     A, BUF          ; Z = Z + BUF.
                B0ADD     Z, A

                B0BTS1    FC              ; Check the carry flag.
                JMP       GETDATA         ; FC = 0
                INCMS     Y               ; FC = 1. Y+1.
                NOP
GETDATA:                                  ;
                MOVC                      ; To lookup data. If BUF = 0, data is 0x0035
                                          ; If BUF = 1, data is 0x5105
                                          ; If BUF = 2, data is 0x2012
                …
TABLE1:         DW        0035H           ; To define a word (16 bits) data.
                DW        5105H
                DW        2012H
                …
```

2.1.4 JUMP TABLE DESCRIPTION

The jump table operation is one of multi-address jumping function. Add low-byte program counter (PCL) and ACC value to get one new PCL. If PCL is overflow after PCL+ACC, PCH adds one automatically. The new program counter (PC) points to a series jump instructions as a listing table. It is easy to make a multi-jump program depends on the value of the accumulator (A).

✸ ***Note: PCH only support PC up counting result and doesn't support PC down counting. When PCL is carry after PCL+ACC, PCH adds one automatically. If PCL borrow after PCL–ACC, PCH keeps value and not change.***

➢ **Example: Jump table.**

```
        ORG     0X0100          ; The jump table is from the head of the ROM boundary

        B0ADD   PCL, A          ; PCL = PCL + ACC, PCH + 1 when PCL overflow occurs.
        JMP     A0POINT         ; ACC = 0, jump to A0POINT
        JMP     A1POINT         ; ACC = 1, jump to A1POINT
        JMP     A2POINT         ; ACC = 2, jump to A2POINT
        JMP     A3POINT         ; ACC = 3, jump to A3POINT
```

SONIX provides a macro for safe jump table function. This macro will check the ROM boundary and move the jump table to the right position automatically. The side effect of this macro maybe wastes some ROM size.

➢ **Example: If "jump table" crosses over ROM boundary will cause errors.**

```
@JMP_A  MACRO   VAL
        IF      (($+1) !& 0XFF00) !!= (($+(VAL)) !& 0XFF00)
        JMP     ($ | 0XFF)
        ORG     ($ | 0XFF)
        ENDIF
        B0ADD   PCL, A
        ENDM
```

✸ ***Note: "VAL" is the number of the jump table listing number.***

➢ **Example: "@JMP_A" application in SONIX macro file called "MACRO3.H".**

```
        B0MOV   A, BUF0         ; "BUF0" is from 0 to 4.
        @JMP_A  5               ; The number of the jump table listing is five.
        JMP     A0POINT         ; ACC = 0, jump to A0POINT
        JMP     A1POINT         ; ACC = 1, jump to A1POINT
        JMP     A2POINT         ; ACC = 2, jump to A2POINT
        JMP     A3POINT         ; ACC = 3, jump to A3POINT
        JMP     A4POINT         ; ACC = 4, jump to A4POINT
```

If the jump table position is across a ROM boundary (0x00FF~0x0100), the "@JMP_A" macro will adjust the jump table routine begin from next RAM boundary (0x0100).

➢ **Example: "@JMP_A" operation.**

; Before compiling program.

```
ROM address
            B0MOV     A, BUF0       ; "BUF0" is from 0 to 4.
            @JMP_A    5             ; The number of the jump table listing is five.
0X00FD      JMP       A0POINT       ; ACC = 0, jump to A0POINT
0X00FE      JMP       A1POINT       ; ACC = 1, jump to A1POINT
0X00FF      JMP       A2POINT       ; ACC = 2, jump to A2POINT
0X0100      JMP       A3POINT       ; ACC = 3, jump to A3POINT
0X0101      JMP       A4POINT       ; ACC = 4, jump to A4POINT
```

; After compiling program.

```
ROM address
            B0MOV     A, BUF0       ; "BUF0" is from 0 to 4.
            @JMP_A    5             ; The number of the jump table listing is five.
0X0100      JMP       A0POINT       ; ACC = 0, jump to A0POINT
0X0101      JMP       A1POINT       ; ACC = 1, jump to A1POINT
0X0102      JMP       A2POINT       ; ACC = 2, jump to A2POINT
0X0103      JMP       A3POINT       ; ACC = 3, jump to A3POINT
0X0104      JMP       A4POINT       ; ACC = 4, jump to A4POINT
```

2.1.5 CHECKSUM CALCULATION

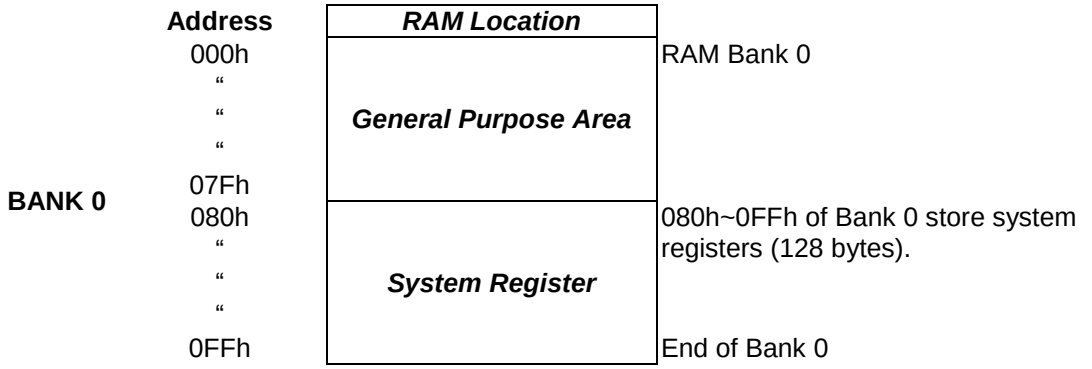
The last ROM address are reserved area. User should avoid these addresses (last address) when calculate the Checksum value.

➢ **Example: The demo program shows how to calculated Checksum from 00H to the end of user's code.**

```
                MOV     A,#END_USER_CODE$L
                B0MOV   END_ADDR1, A        ; Save low end address to end_addr1
                MOV     A,#END_USER_CODE$M
                B0MOV   END_ADDR2, A        ; Save middle end address to end_addr2
                CLR     Y                   ; Set Y to 00H
                CLR     Z                   ; Set Z to 00H
@@:
                MOVC
                B0BSET  FC                  ; Clear C flag
                ADD     DATA1, A            ; Add A to Data1
                MOV     A, R
                ADC     DATA2, A            ; Add R to Data2
                JMP     END_CHECK           ; Check if the YZ address =    the end of code
AAA:
                INCMS   Z                   ; Z=Z+1
                JMP     @B                  ; If Z != 00H calculate to next address
                JMP     Y_ADD_1             ; If Z = 00H increase Y
END_CHECK:
                MOV     A, END_ADDR1
                CMPRS   A, Z                ; Check if Z = low end address
                JMP     AAA                 ; If Not jump to checksum calculate
                MOV     A, END_ADDR2
                CMPRS   A, Y                ; If Yes, check if Y = middle end address
                JMP     AAA                 ; If Not jump to checksum calculate
                JMP     CHECKSUM_END        ; If Yes checksum calculated is done.

Y_ADD_1:
                INCMS   Y                   ; Increase Y
                NOP
                JMP     @B                  ; Jump to checksum calculate
CHECKSUM_END:
                …
                …
END_USER_CODE:                              ; Label of program end
```

2.2 DATA MEMORY (RAM)

☞ ***128 X 8-bit RAM***



The 128-byte general purpose RAM is in Bank 0. Sonix provides “Bank 0” type instructions (e.g. b0mov, b0add, b0bts1, b0bset…) to control Bank 0 RAM in non-zero RAM bank condition directly.

2.2.1 SYSTEM REGISTER

2.2.1.1 SYSTEM REGISTER TABLE

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
8	L	H	R	Z	Y	-	PFLAG	-	-	-	-	-	-	-	-	-
9	-	-	-	-	-	-	-	-	-	-	CMDB0	CMDB1	CM0M	CM1M	CM2M	OPM
A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	P4CON	-
B	-	ADM	ADB	ADR	ADT	-	-	-	P0M	-	-	-	-	-	-	PEDGE
C	P1W	P1M	-	-	P4M	-	-	-	INTRQ	INTEN	OSCM	-	WDTR	TC0R	PCL	PCH
D	P0	P1	-	-	P4	-	-	-	T0M	T0C	TC0M	TC0C	BZM	-	-	STKP
E	P0UR	P1UR	-	-	P4UR	-	@HL	@YZ	TC0D	-	-	-	-	-	-	-
F	STK7L	STK7H	STK6L	STK6H	STK5L	STK5H	STK4L	STK4H	STK3L	STK3H	STK2L	STK2H	STK1L	STK1H	STK0L	STK0H

2.2.1.2 SYSTEM REGISTER DESCRIPTION

H, L = Working, @HL addressing register.
R = Working register and ROM look-up data buffer.
CMDB0 = Comparator output de-bounce control register 0.
CM0M = Comparator 0 mode register.
CM2M = Comparator 2 mode register.
P4CON = P4 configuration register.
ADB = ADC data buffer.
ADT = ADC offset calibration register.
INTRQ = Interrupt request register.
OSCM = Oscillator mode register.
PnM = Port n input/output mode register.
PnUR = Port n pull-up resister control register.
T0M = T0 mode register.
TC0M = TC0 mode register.
TC0R = TC0 auto-reload data buffer.
BZM = 2K/4K buzzer mode register.
@YZ = RAM YZ indirect addressing index pointer.
STK0~STK7 = Stack 0 ~ stack 7 buffer.
Y, Z = Working, @YZ and ROM addressing register.
PFLAG = Special flag register.
CMDB1 = Comparator output de-bounce control register 1.
CM1M = Comparator 1 mode register.
OPM = OP amp 0~2 mode register.
ADM = ADC mode register.
ADR = ADC resolution select register.
PEDGE = P0.0, P0.1, P0.2 edge direction register.
INTEN = Interrupt enable register.
WDTR = Watchdog timer clear register.
Pn = Port n data buffer.
PCH, PCL = Program counter.
T0C = T0 counting register.
TC0C = TC0 counting register.
TC0D = TC0 duty control register.
@HL = RAM HL indirect addressing index pointer.
STKP = Stack pointer buffer.

2.2.1.3 BIT DEFINITION of SYSTEM REGISTER

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
080H	LBIT7	LBIT6	LBIT5	LBIT4	LBIT3	LBIT2	LBIT1	LBIT0	R/W	L
081H	HBIT7	HBIT6	HBIT5	HBIT4	HBIT3	HBIT2	HBIT1	HBIT0	R/W	H
082H	RBIT7	RBIT6	RBIT5	RBIT4	RBIT3	RBIT2	RBIT1	RBIT0	R/W	R
083H	ZBIT7	ZBIT6	ZBIT5	ZBIT4	ZBIT3	ZBIT2	ZBIT1	ZBIT0	R/W	Z
084H	YBIT7	YBIT6	YBIT5	YBIT4	YBIT3	YBIT2	YBIT1	YBIT0	R/W	Y
086H	NT0	NPD	LVD36	LVD24		C	DC	Z	R/W	PFLAG
09AH	CM1D3	CM1D2	CM1D1	CM1D0	CM0D3	CM0D2	CM0D1	CM0D0	R/W	CMDB0
09BH					CM2D3	CM2D2	CM2D1	CM2D0	R/W	CMDB1
09CH	CM0EN	CM0OEN	CM0OUT	CM0SF	CM0G				R/W	CM0M
09DH	CM1EN	CM1OEN	CM1OUT	CM1SF	CM1G	CM2RS2	CM2RS1	CM2RS0	R/W	CM1M
09EH	CM2EN	CM2OEN	CM2OUT	CM2SF	CM2G	CM2RS2	CM2RS1	CM2RS0	R/W	CM2M
09FH								OPEN	R/W	OPM
0AEH	P4CON7	P4CON6	P4CON5	P4CON4	P4CON3	P4CON2	P4CON1	P4CON0	W	P4CON
0B1H	ADENB	ADS	EOC	GCHS	AVREFH	CHS2	CHS1	CHS0	R/W	ADM
0B2H	ADB11	ADB10	ADB9	ADB8	ADB7	ADB6	ADB5	ADB4	R	ADB
0B3H		ADCKS1	ADLEN	ADCKS0	ADB3	ADB2	ADB1	ADB0	R/W	ADR
0B4H	ADTS1	ADTS0		ADT4	ADT3	ADT2	ADT1	ADT0	R/W	ADT
0B8H		P06M	P05M	-	P03M	P02M	-	P00M	R/W	P0M
0BFH							P00G1	P00G0	R/W	PEDGE
0C0H		P16W	P15W	P14W	P13W	P12W	P11W	P10W	W	P1W
0C1H		P16M	P15M	P14M	P13M	P12M	P11M	P10M	R/W	P1M
0C4H	P47M	P46M	P45M	P44M	P43M	P42M	P41M	P40M	R/W	P4M
0C8H	ADCIRQ		TC0IRQ	T0IRQ	CM2IRQ	CM1IRQ	CM0IRQ	P00IRQ	R/W	INTRQ
0C9H	ADCIEN		TC0IEN	T0IEN	CM2IEN	CM1IEN	CM0IEN	P00IEN	R/W	INTEN
0CAH				CPUM1	CPUM0	CLKMD	STPHX		R/W	OSCM
0CCH	WDTR7	WDTR6	WDTR5	WDTR4	WDTR3	WDTR2	WDTR1	WDTR0	W	WDTR
0CDH	TC0R7	TC0R6	TC0R5	TC0R4	TC0R3	TC0R2	TC0R1	TC0R0	W	TC0R
0CEH	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	R/W	PCL
0CFH					PC11	PC10	PC9	PC8	R/W	PCH
0D0H		P06	P05	P04	P03	P02	P01	P00	R/W	P0
0D1H		P16	P15	P14	P13	P12	P11	P10	R/W	P1
0D4H	P47	P46	P45	P44	P43	P42	P41	P40	R/W	P4
0D8H	T0ENB	T0rate2	T0rate1	T0rate0					R/W	T0M
0D9H	T0C7	T0C6	T0C5	T0C4	T0C3	T0C2	T0C1	T0C0	R/W	T0C
0DAH	TC0ENB	TC0rate2	TC0rate1	TC0rate0	TC0CKS	TC0DIR	TC0PO	PWM0OUT	R/W	TC0M
0DBH	TC0C7	TC0C6	TC0C5	TC0C4	TC0C3	TC0C2	TC0C1	TC0C0	R/W	TC0C
0DCH	BZEN	BZRate1	BZrate0						R/W	BZM
0DFH	GIE					STKPB2	STKPB1	STKPB0	R/W	STKP
0E0H		P06R	P05R	-	P03R	P02R	-	P00R	W	P0UR
0E1H		P16R	P15R	P14R	P13R	P12R	P11R	P10R	W	P1UR
0E4H	P47R	P46R	P45R	P44R	P43R	P42R	P41R	P40R	W	P4UR
0E6H	@HL7	@HL6	@HL5	@HL4	@HL3	@HL2	@HL1	@HL0	R/W	@HL
0E7H	@YZ7	@YZ6	@YZ5	@YZ4	@YZ3	@YZ2	@YZ1	@YZ0	R/W	@YZ
0E8H	TC0D7	TC0D6	TC0D5	TC0D4	TC0D3	TC0D2	TC0D1	TC0D0	R/W	TC0D
0F0H	S7PC7	S7PC6	S7PC5	S7PC4	S7PC3	S7PC2	S7PC1	S7PC0	R/W	STK7L
0F1H					S7PC11	S7PC10	S7PC9	S7PC8	R/W	STK7H
0F2H	S6PC7	S6PC6	S6PC5	S6PC4	S6PC3	S6PC2	S6PC1	S6PC0	R/W	STK6L
0F3H					S6PC11	S6PC10	S6PC9	S6PC8	R/W	STK6H
0F4H	S5PC7	S5PC6	S5PC5	S5PC4	S5PC3	S5PC2	S5PC1	S5PC0	R/W	STK5L
0F5H					S5PC11	S5PC10	S5PC9	S5PC8	R/W	STK5H
0F6H	S4PC7	S4PC6	S4PC5	S4PC4	S4PC3	S4PC2	S4PC1	S4PC0	R/W	STK4L
0F7H					S4PC11	S4PC10	S4PC9	S4PC8	R/W	STK4H
0F8H	S3PC7	S3PC6	S3PC5	S3PC4	S3PC3	S3PC2	S3PC1	S3PC0	R/W	STK3L
0F9H					S3PC11	S3PC10	S3PC9	S3PC8	R/W	STK3H
0FAH	S2PC7	S2PC6	S2PC5	S2PC4	S2PC3	S2PC2	S2PC1	S2PC0	R/W	STK2L
0FBH					S2PC11	S2PC10	S2PC9	S2PC8	R/W	STK2H
0FCH	S1PC7	S1PC6	S1PC5	S1PC4	S1PC3	S1PC2	S1PC1	S1PC0	R/W	STK1L
0FDH					S1PC11	S1PC10	S1PC9	S1PC8	R/W	STK1H

0FEH	S0PC7	S0PC6	S0PC5	S0PC4	S0PC3	S0PC2	S0PC1	S0PC0	R/W	STK0L
0FFH					S0PC11	S0PC10	S0PC9	S0PC8	R/W	STK0H

✸ ***Note:***

1. ***To avoid system error, make sure to put all the "0" and "1" as it indicates in the above table.***
2. ***All of register names had been declared in SN8ASM assembler.***
3. ***One-bit name had been declared in SN8ASM assembler with "F" prefix code.***
4. ***"b0bset", "b0bclr", "bset", "bclr" instructions are only available to the "R/W" registers.***

2.2.2 ACCUMULATOR

The ACC is an 8-bit data register responsible for transferring or manipulating data between ALU and data memory. If the result of operating is zero (Z) or there is carry (C or DC) occurrence, then these flags will be set to PFLAG register. ACC is not in data memory (RAM), so ACC can't be access by "B0MOV" instruction during the instant addressing mode.

➢ **Example: Read and write ACC value.**

```
; Read ACC data and store in BUF data memory.
                MOV         BUF, A

; Write a immediate data into ACC.
                MOV         A, #0FH

; Write ACC data from BUF data memory.
                MOV         A, BUF
; or
                B0MOV       A, BUF
```

The system doesn't store ACC and PFLAG value when interrupt executed. ACC and PFLAG data must be saved to other data memories. "PUSH", "POP" save and load ACC, PFLAG data into buffers.

➢ **Example: Protect ACC and working registers.**

```
INT_SERVICE:
                PUSH                ; Save ACC and PFLAG to buffers.
                …
                …
                POP                 ; Load ACC and PFLAG from buffers.

                RETI                ; Exit interrupt service vector
```

2.2.3 PROGRAM FLAG

The PFLAG register contains the arithmetic status of ALU operation, system reset status and LVD detecting status. NT0, NPD bits indicate system reset status including power on reset, LVD reset, reset by external pin active and watchdog reset. C, DC, Z bits indicate the result status of ALU operation. LVD24, LVD36 bits indicate LVD detecting power voltage status.

086H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PFLAG	NT0	NPD	LVD36	LVD24	-	C	DC	Z
Read/Write	R/W	R/W	R	R	-	R/W	R/W	R/W
After reset	-	-	0	0	-	0	0	0

Bit [7:6] **NT0, NPD:** Reset status flag.

NT0	NPD	Reset Status
0	0	Watch-dog time out
0	1	Reserved
1	0	Reset by LVD
1	1	Reset by external Reset Pin

Bit 5 **LVD36:** LVD 3.6V operating flag and only support LVD code option is LVD_H.
0 = Inactive (VDD > 3.6V).
1 = Active (VDD ≦ 3.6V).

Bit 4 **LVD24:** LVD 2.4V operating flag and only support LVD code option is LVD_M.
0 = Inactive (VDD > 2.4V).
1 = Active (VDD ≦ 2.4V).

Bit 2 **C:** Carry flag
1 = Addition with carry, subtraction without borrowing, rotation with shifting out logic “1”, comparison result ≧ 0.
0 = Addition without carry, subtraction with borrowing signal, rotation with shifting out logic “0”, comparison result < 0.

Bit 1 **DC:** Decimal carry flag
1 = Addition with carry from low nibble, subtraction without borrow from high nibble.
0 = Addition without carry from low nibble, subtraction with borrow from high nibble.

Bit 0 **Z:** Zero flag
1 = The result of an arithmetic/logic/branch operation is zero.
0 = The result of an arithmetic/logic/branch operation is not zero.

✸ ***Note: Refer to instruction set table for detailed information of C, DC and Z flags.***

2.2.4 PROGRAM COUNTER

The program counter (PC) is a 12-bit binary counter separated into the high-byte 4 and the low-byte 8 bits. This counter is responsible for pointing a location in order to fetch an instruction for kernel circuit. Normally, the program counter is automatically incremented with each instruction during program execution.

Besides, it can be replaced with specific address by executing CALL or JMP instruction. When JMP or CALL instruction is executed, the destination address will be inserted to bit 0 ~ bit 11.

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC	-	-	-	-	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
After reset	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0	0
	PCH								PCL							

☞ **ONE ADDRESS SKIPPING**

There are nine instructions (CMPRS, INCS, INCMS, DECS, DECMS, BTS0, BTS1, B0BTS0, B0BTS1) with one address skipping function. If the result of these instructions is true, the PC will add 2 steps to skip next instruction.

If the condition of bit test instruction is true, the PC will add 2 steps to skip next instruction.

```
            B0BTS1    FC          ; To skip, if Carry_flag = 1
            JMP       C0STEP      ; Else jump to C0STEP.
            …
            …
C0STEP:     NOP

            B0MOV     A, BUF0     ; Move BUF0 value to ACC.
            B0BTS0    FZ          ; To skip, if Zero flag = 0.
            JMP       C1STEP      ; Else jump to C1STEP.
            …
            …
C1STEP:     NOP
```

If the ACC is equal to the immediate data or memory, the PC will add 2 steps to skip next instruction.

```
            CMPRS     A, #12H     ; To skip, if ACC = 12H.
            JMP       C0STEP      ; Else jump to C0STEP.
            …
            …
C0STEP:     NOP
```

If the destination increased by 1, which results overflow of 0xFF to 0x00, the PC will add 2 steps to skip next instruction.

INCS instruction:

```
        INCS    BUF0
        JMP     C0STEP      ; Jump to C0STEP if ACC is not zero.
        …
        …
C0STEP: NOP
```

INCMS instruction:

```
        INCMS   BUF0
        JMP     C0STEP      ; Jump to C0STEP if BUF0 is not zero.
        …
        …
C0STEP: NOP
```

If the destination decreased by 1, which results underflow of 0x01 to 0x00, the PC will add 2 steps to skip next instruction.

DECS instruction:

```
        DECS    BUF0
        JMP     C0STEP      ; Jump to C0STEP if ACC is not zero.
        …
        …
C0STEP: NOP
```

DECMS instruction:

```
        DECMS   BUF0
        JMP     C0STEP      ; Jump to C0STEP if BUF0 is not zero.
        …
        …
C0STEP: NOP
```

☞ **MULTI-ADDRESS JUMPING**

Users can jump around the multi-address by either JMP instruction or ADD M, A instruction (M = PCL) to activate multi-address jumping function. Program Counter supports **"ADD M,A"**, **"ADC M,A"** and **"B0ADD M,A"** instructions for carry to PCH when PCL overflow automatically. For jump table or others applications, users can calculate PC value by the three instructions and don't care PCL overflow problem.

✸ ***Note: PCH only support PC up counting result and doesn't support PC down counting. When PCL is carry after PCL+ACC, PCH adds one automatically. If PCL borrow after PCL–ACC, PCH keeps value and not change.***

➢ **Example: If PC = 0323H (PCH = 03H, PCL = 23H)**

```
; PC = 0323H
                MOV     A, #28H
                B0MOV   PCL, A          ; Jump to address 0328H
                …

; PC = 0328H
                MOV     A, #00H
                B0MOV   PCL, A          ; Jump to address 0300H
                …
```

➢ **Example: If PC = 0323H (PCH = 03H, PCL = 23H)**

```
; PC = 0323H
                B0ADD   PCL, A          ; PCL = PCL + ACC, the PCH cannot be changed.
                JMP     A0POINT         ; If ACC = 0, jump to A0POINT
                JMP     A1POINT         ; ACC = 1, jump to A1POINT
                JMP     A2POINT         ; ACC = 2, jump to A2POINT
                JMP     A3POINT         ; ACC = 3, jump to A3POINT
                …
                …
```

2.2.5 H, L REGISTERS

The H and L registers are the 8-bit buffers. There are two major functions of these registers.

- Can be used as general working registers
- Can be used as RAM data pointers with @HL register

081H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H	HBIT7	HBIT6	HBIT5	HBIT4	HBIT3	HBIT2	HBIT1	HBIT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	-	-	-	-	-	-	-	-

080H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
L	LBIT7	LBIT6	LBIT5	LBIT4	LBIT3	LBIT2	LBIT1	LBIT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	-	-	-	-	-	-	-	-

➢ **Example: If want to read a data from RAM address 20H of bank_0, it can use indirectly addressing mode to access data as following.**

```
B0MOV   H, #00H     ; To set RAM bank 0 for H register
B0MOV   L, #20H     ; To set location 20H for L register
B0MOV   A, @HL      ; To read a data into ACC
```

➢ **Example: Clear general-purpose data memory area of bank 0 using @HL register.**

```
        CLR     H           ; H = 0, bank 0
        B0MOV   L, #07FH    ; L = 7FH, the last address of the data memory area
CLR_HL_BUF:
        CLR     @HL         ; Clear @HL to be zero
        DECMS   L           ; L – 1, if L = 0, finish the routine
        JMP     CLR_HL_BUF  ; Not zero

        CLR     @HL
END_CLR:                    ; End of clear general purpose data memory area of bank 0
        …
        …
```

2.2.6 Y, Z REGISTERS

The Y and Z registers are the 8-bit buffers. There are three major functions of these registers.

- Can be used as general working registers
- Can be used as RAM data pointers with @YZ register
- Can be used as ROM data pointer with the MOVC instruction for look-up table

084H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Y	YBIT7	YBIT6	YBIT5	YBIT4	YBIT3	YBIT2	YBIT1	YBIT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	-	-	-	-	-	-	-	-

083H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Z	ZBIT7	ZBIT6	ZBIT5	ZBIT4	ZBIT3	ZBIT2	ZBIT1	ZBIT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	-	-	-	-	-	-	-	-

➢ **Example: Uses Y, Z register as the data pointer to access data in the RAM address 025H of bank0.**

```
B0MOV   Y, #00H     ; To set RAM bank 0 for Y register
B0MOV   Z, #25H     ; To set location 25H for Z register
B0MOV   A, @YZ      ; To read a data into ACC
```

➢ **Example: Uses the Y, Z register as data pointer to clear the RAM data.**

```
        B0MOV   Y, #0           ; Y = 0, bank 0
        B0MOV   Z, #07FH        ; Z = 7FH, the last address of the data memory area
CLR_YZ_BUF:
        CLR     @YZ             ; Clear @YZ to be zero
        DECMS   Z               ; Z – 1, if Z= 0, finish the routine
        JMP     CLR_YZ_BUF      ; Not zero
        CLR     @YZ
END_CLR:                        ; End of clear general purpose data memory area of bank 0
        …
```

2.2.7 R REGISTER

R register is an 8-bit buffer. There are two major functions of the register.

- Can be used as working register
- For store high-byte data of look-up table
  (MOVC instruction executed, the high-byte data of specified ROM address will be stored in R register and the low-byte data will be stored in ACC).

082H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	RBIT7	RBIT6	RBIT5	RBIT4	RBIT3	RBIT2	RBIT1	RBIT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	-	-	-	-	-	-	-	-

✸ ***Note: Please refer to the "LOOK-UP TABLE DESCRIPTION" about R register look-up table application.***

2.3 ADDRESSING MODE

2.3.1 IMMEDIATE ADDRESSING MODE

The immediate addressing mode uses an immediate data to set up the location in ACC or specific RAM.

- **Example: Move the immediate data 12H to ACC.**

```
MOV     A, #12H         ; To set an immediate data 12H into ACC.
```

- **Example: Move the immediate data 12H to R register.**

```
B0MOV   R, #12H         ; To set an immediate data 12H into R register.
```

✷ ***Note: In immediate addressing mode application, the specific RAM must be 0x80~0x87 working register.***

2.3.2 DIRECTLY ADDRESSING MODE

The directly addressing mode moves the content of RAM location in or out of ACC.

- **Example: Move 0x12 RAM location data into ACC.**

```
B0MOV   A, 12H          ; To get a content of RAM location 0x12 of bank 0 and save in
                        ACC.
```

- **Example: Move ACC data into 0x12 RAM location.**

```
B0MOV   12H, A          ; To get a content of ACC and save in RAM location 12H of
                        bank 0.
```

2.3.3 INDIRECTLY ADDRESSING MODE

The indirectly addressing mode is to access the memory by the data pointer registers (H/L, Y/Z).

- **Example: Indirectly addressing mode with @HL register**

```
B0MOV   H, #0           ; To clear H register to access RAM bank 0.
B0MOV   L, #12H         ; To set an immediate data 12H into L register.
B0MOV   A, @HL          ; Use data pointer @HL reads a data from RAM location
                        ; 012H into ACC.
```

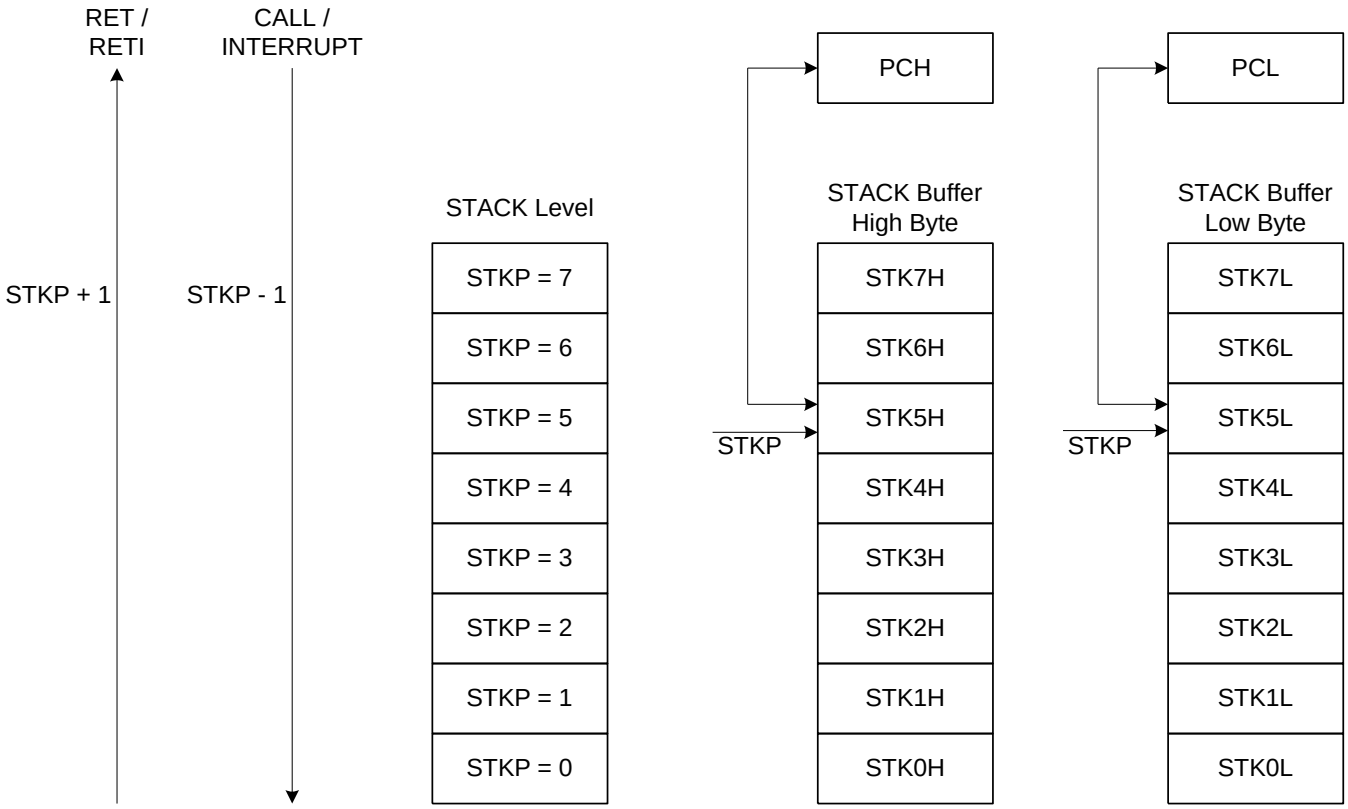
- **Example: Indirectly addressing mode with @YZ register**

```
B0MOV   Y, #0           ; To clear Y register to access RAM bank 0.
B0MOV   Z, #12H         ; To set an immediate data 12H into Z register.
B0MOV   A, @YZ          ; Use data pointer @YZ reads a data from RAM location
                        ; 012H into ACC.
```

2.4 STACK OPERATION

2.4.1 OVERVIEW

The stack buffer has 8-level. These buffers are designed to push and pop up program counter's (PC) data when interrupt service routine and "CALL" instruction are executed. The STKP register is a pointer designed to point active level in order to push or pop up data from stack buffer. The STKnH and STKnL are the stack buffers to store program counter (PC) data.



2.4.2 STACK REGISTERS

The stack pointer (STKP) is a 3-bit register to store the address used to access the stack buffer, 13-bit data memory (STKnH and STKnL) set aside for temporary storage of stack addresses.

The two stack operations are writing to the top of the stack (push) and reading from the top of stack (pop). Push operation decrements the STKP and the pop operation increments each time. That makes the STKP always point to the top address of stack buffer and write the last program counter value (PC) into the stack buffer.

The program counter (PC) value is stored in the stack buffer before a CALL instruction executed or during interrupt service routine. Stack operation is a LIFO type (Last in and first out). The stack pointer (STKP) and stack buffer (STKnH and STKnL) are located in the system register area bank 0.

0DFH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STKP	GIE	-	-	-	-	STKPB2	STKPB1	STKPB0
Read/Write	R/W	-	-	-	-	R/W	R/W	R/W
After reset	0	-	-	-	-	1	1	1

Bit[2:0] **STKPBn:** Stack pointer (n = 0 ~ 2)

Bit 7 **GIE:** Global interrupt control bit.
0 = Disable.
1 = Enable. Please refer to the interrupt chapter.

➢ **Example: Stack pointer (STKP) reset, we strongly recommended to clear the stack pointers in the beginning of the program.**

```
MOV     A, #00000111B
B0MOV   STKP, A
```

0F0H~0FFH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STKnH	-	-	-	SnPC12	SnPC11	SnPC10	SnPC9	SnPC8
Read/Write	-	-	-	R/W	R/W	R/W	R/W	R/W
After reset	-	-	-	0	0	0	0	0

0F0H~0FFH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STKnL	SnPC7	SnPC6	SnPC5	SnPC4	SnPC3	SnPC2	SnPC1	SnPC0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

STKn = STKnH , STKnL (n = 7 ~ 0)

2.4.3 STACK OPERATION EXAMPLE

The two kinds of Stack-Save operations refer to the stack pointer (STKP) and write the content of program counter (PC) to the stack buffer are CALL instruction and interrupt service. Under each condition, the STKP decreases and points to the next available stack location. The stack buffer stores the program counter about the op-code address. The Stack-Save operation is as the following table.

Stack Level	*STKP Register*			*Stack Buffer*		*Description*
	STKPB2	**STKPB1**	**STKPB0**	**High Byte**	**Low Byte**	
0	1	1	1	Free	Free	-
1	1	1	0	STK0H	STK0L	-
2	1	0	1	STK1H	STK1L	-
3	1	0	0	STK2H	STK2L	-
4	0	1	1	STK3H	STK3L	-
5	0	1	0	STK4H	STK4L	-
6	0	0	1	STK5H	STK5L	-
7	0	0	0	STK6H	STK6L	-
8	1	1	1	STK7H	STK7L	-
> 8	1	1	0	-	-	**Stack Over, error**

There are Stack-Restore operations correspond to each push operation to restore the program counter (PC). The RETI instruction uses for interrupt service routine. The RET instruction is for CALL instruction. When a pop operation occurs, the STKP is incremented and points to the next free stack location. The stack buffer restores the last program counter (PC) to the program counter registers. The Stack-Restore operation is as the following table.

Stack Level	*STKP Register*			*Stack Buffer*		*Description*
	STKPB2	**STKPB1**	**STKPB0**	**High Byte**	**Low Byte**	
8	1	1	1	STK7H	STK7L	-
7	0	0	0	STK6H	STK6L	-
6	0	0	1	STK5H	STK5L	-
5	0	1	0	STK4H	STK4L	-
4	0	1	1	STK3H	STK3L	-
3	1	0	0	STK2H	STK2L	-
2	1	0	1	STK1H	STK1L	-
1	1	1	0	STK0H	STK0L	-
0	1	1	1	Free	Free	-

2.5 CODE OPTION TABLE

The code option is the system hardware configurations including oscillator type, watchdog timer operation, LVD option, reset pin option and OTP ROM security control. The code option items are as following table:

Code Option	Content	Function Description
High_Clk	IHRC_16M	High speed internal 16MHz RC. XIN/XOUT pins are bi-direction GPIO mode.
	RC	Low cost RC for external high clock oscillator. XIN pin is connected to RC oscillator. XOUT pin is bi-direction GPIO mode.
	32K X'tal	Low frequency, power saving crystal (e.g. 32.768KHz) for external high clock oscillator.
	12M X'tal	High speed crystal /resonator (e.g. 12MHz) for external high clock oscillator.
	4M X'tal	Standard crystal /resonator (e.g. 4M) for external high clock oscillator.
Fcpu	Fhosc/4	Instruction cycle is 4 oscillator clocks.
	Fhosc/8	Instruction cycle is 8 oscillator clocks.
	Fhosc/16	Instruction cycle is 16 oscillator clocks.
Watch_Dog	Always_On	Watchdog timer is always on enable even in power down and green mode.
	Enable	Enable watchdog timer. Watchdog timer stops in power down mode and green mode.
	Disable	Disable Watchdog function.
Reset_Pin	Reset	Enable External reset pin.
	P04	Enable P0.4 input only without pull-up resister.
Security	Enable	Enable ROM code Security function.
	Disable	Disable ROM code Security function.
LVD	LVD_L	LVD will reset chip if VDD is below 2.0V
	LVD_M	LVD will reset chip if VDD is below 2.0V Enable LVD24 bit of PFLAG register for 2.4V low voltage indicator.
	LVD_H	LVD will reset chip if VDD is below 2.4V Enable LVD36 bit of PFLAG register for 3.6V low voltage indicator.
	LVD_MAX	LVD will reset chip if VDD is below 3.6V

2.5.1 Fcpu code option

Fcpu means instruction cycle of normal mode (high clock). In slow mode, the system clock source is internal low speed RC oscillator. The Fcpu of slow mode isn't controlled by Fcpu code option and fixed Flosc/4 (16KHz/4 @3V, 32KHz/4 @5V).

2.5.2 Reset_Pin code option

The reset pin is shared with general input only pin controlled by code option.

- **Reset:** The reset pin is external reset function. When falling edge trigger occurring, the system will be reset.
- **P04:** Set reset pin to general input only pin (P0.4). The external reset function is disabled and the pin is input pin.

2.5.3 Security code option

Security code option is OTP ROM protection. When enable security code option, the ROM code is secured and not dumped complete ROM contents.

3 RESET

3.1 OVERVIEW

The system would be reset in three conditions as following.

- Power on reset
- Watchdog reset
- Brown out reset
- External reset (only supports external reset pin enable situation)

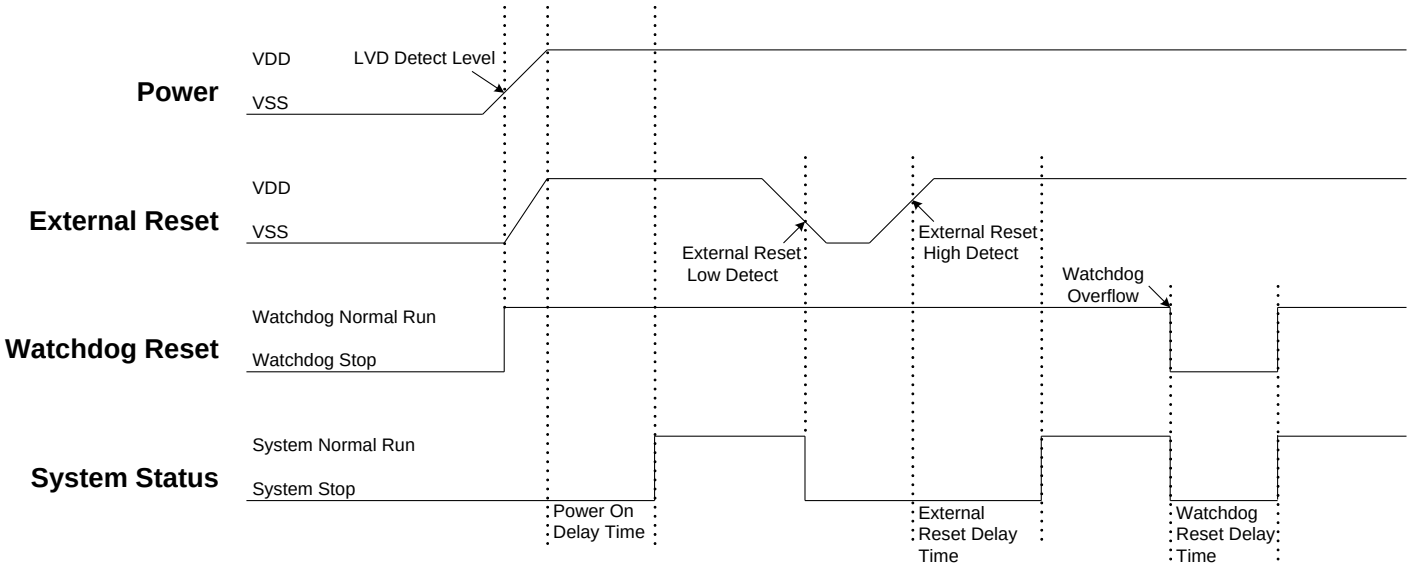
When any reset condition occurs, all system registers keep initial status, program stops and program counter is cleared. After reset status released, the system boots up and program starts to execute from ORG 0. The NT0, NPD flags indicate system reset status. The system can depend on NT0, NPD status and go to different paths by program.

086H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PFLAG	NT0	NPD	LVD36	LVD24	-	C	DC	Z
Read/Write	R/W	R/W	R	R	-	R/W	R/W	R/W
After reset	-	-	0	0	-	0	0	0

Bit [7:6] **NT0, NPD:** Reset status flag.

NT0	NPD	Condition	Description
0	0	Watchdog reset	Watchdog timer overflow.
0	1	Reserved	-
1	0	Power on reset and LVD reset.	Power voltage is lower than LVD detecting level.
1	1	External reset	External reset pin detect low level status.

Finishing any reset sequence needs some time. The system provides complete procedures to make the power on reset successful. For different oscillator types, the reset time is different. That causes the VDD rise rate and start-up time of different oscillator is not fixed. RC type oscillator's start-up time is very short, but the crystal type is longer. Under client terminal application, users have to take care the power on reset time for the master terminal requirement. The reset timing diagram is as following.



3.2 POWER ON RESET

The power on reset depend no LVD operation for most power-up situations. The power supplying to system is a rising curve and needs some time to achieve the normal voltage. Power on reset sequence is as following.

- **Power-up:** System detects the power voltage up and waits for power stable.
- **External reset (only external reset pin enable):** System checks external reset pin status. If external reset pin is not high level, the system keeps reset status and waits external reset pin released.
- **System initialization:** All system registers is set as initial conditions and system is ready.
- **Oscillator warm up:** Oscillator operation is successfully and supply to system clock.
- **Program executing:** Power on sequence is finished and program executes from ORG 0.

3.3 WATCHDOG RESET

Watchdog reset is a system protection. In normal condition, system works well and clears watchdog timer by program. Under error condition, system is in unknown situation and watchdog can't be clear by program before watchdog timer overflow. Watchdog timer overflow occurs and the system is reset. After watchdog reset, the system restarts and returns normal mode. Watchdog reset sequence is as following.

- **Watchdog timer status:** System checks watchdog timer overflow status. If watchdog timer overflow occurs, the system is reset.
- **System initialization:** All system registers is set as initial conditions and system is ready.
- **Oscillator warm up:** Oscillator operation is successfully and supply to system clock.
- **Program executing:** Power on sequence is finished and program executes from ORG 0.

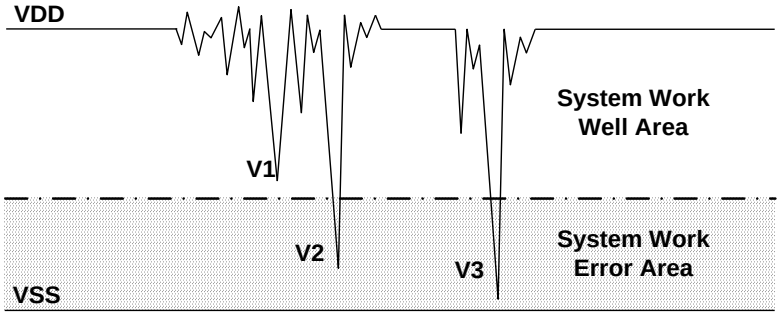
Watchdog timer application note is as following.

- Before clearing watchdog timer, check I/O status and check RAM contents can improve system error.
- Don't clear watchdog timer in interrupt vector and interrupt service routine. That can improve main routine fail.
- Clearing watchdog timer program is only at one part of the program. This way is the best structure to enhance the watchdog timer function.

✸ ***Note: Please refer to the "WATCHDOG TIMER" about watchdog timer detail information.***

3.4 BROWN OUT RESET

The brown out reset is a power dropping condition. The power drops from normal voltage to low voltage by external factors (e.g. EFT interference or external loading changed). The brown out reset would make the system not work well or executing program error.



Brown Out Reset Diagram

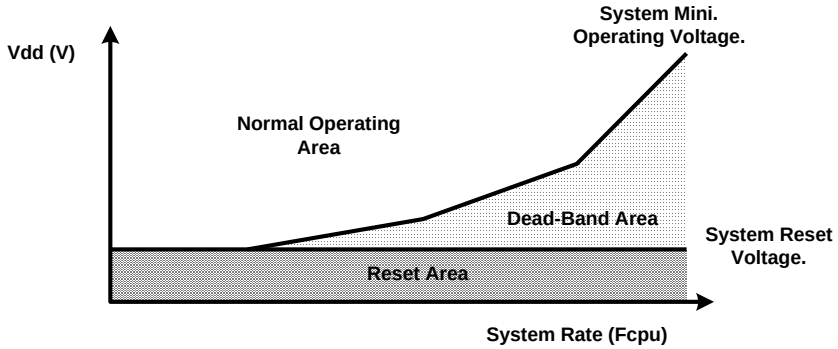
The power dropping might through the voltage range that's the system dead-band. The dead-band means the power range can't offer the system minimum operation power requirement. The above diagram is a typical brown out reset diagram. There is a serious noise under the VDD, and VDD voltage drops very deep. There is a dotted line to separate the system working area. The above area is the system work well area. The below area is the system work error area called dead-band. V1 doesn't touch the below area and not effect the system operation. But the V2 and V3 is under the below area and may induce the system error occurrence. Let system under dead-band includes some conditions.

DC application:
The power source of DC application is usually using battery. When low battery condition and MCU drive any loading, the power drops and keeps in dead-band. Under the situation, the power won't drop deeper and not touch the system reset voltage. That makes the system under dead-band.

AC application:
In AC power application, the DC power is regulated from AC power source. This kind of power usually couples with AC noise that makes the DC power dirty. Or the external loading is very heavy, e.g. driving motor. The loading operating induces noise and overlaps with the DC power. VDD drops by the noise, and the system works under unstable power situation.
The power on duration and power down duration are longer in AC application. The system power on sequence protects the power on successful, but the power down situation is like DC low battery condition. When turn off the AC power, the VDD drops slowly and through the dead-band for a while.

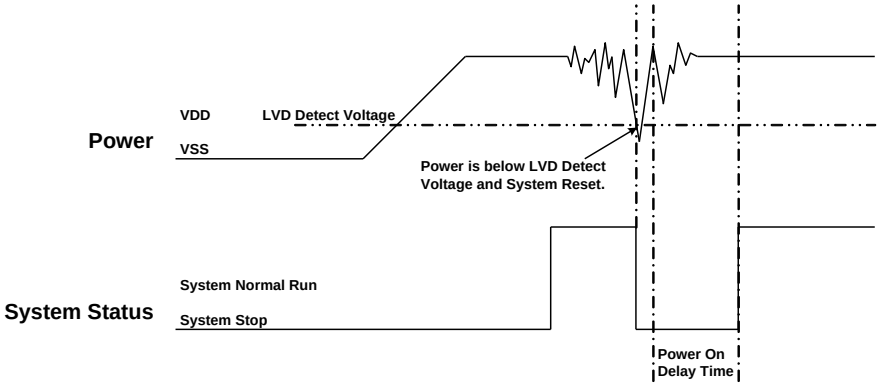
3.5 THE SYSTEM OPERATING VOLTAGE

To improve the brown out reset needs to know the system minimum operating voltage which is depend on the system executing rate and power level. Different system executing rates have different system minimum operating voltage. The electrical characteristic section shows the system voltage to executing rate relationship.



Normally the system operation voltage area is higher than the system reset voltage to VDD, and the reset voltage is decided by LVD detect level. The system minimum operating voltage rises when the system executing rate upper even higher than system reset voltage. The dead-band definition is the system minimum operating voltage above the system reset voltage.

3.6 LOW VOLTAGE DETECTOR (LVD)



The LVD (low voltage detector) is built-in Sonix 8-bit MCU to be brown out reset protection. When the VDD drops and is below LVD detect voltage, the LVD would be triggered, and the system is reset. The LVD detect level is different by each MCU. The LVD voltage level is a point of voltage and not easy to cover all dead-band range. Using LVD to improve brown out reset is depend on application requirement and environment. If the power variation is very deep, violent and trigger the LVD, the LVD can be the protection. If the power variation can touch the LVD detect level and make system work error, the LVD can't be the protection and need to other reset methods. More detail LVD information is in the electrical characteristic section.
The LVD is three levels design (2.0V/2.4V/3.6V) and controlled by LVD code option. The 2.0V LVD is always enable for power on reset and Brown Out reset. The 2.4V LVD includes LVD reset function and flag function to indicate VDD status function. The 3.6V includes flag function to indicate VDD status. LVD flag function can be an **easy low battery detector**. LVD24, LVD36 flags indicate VDD voltage level. For low battery detect application, only checking LVD24, LVD36 status to be battery status. This is a cheap and easy solution.

086H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PFLAG	NT0	NPD	LVD36	LVD24	-	C	DC	Z
Read/Write	R/W	R/W	R	R	-	R/W	R/W	R/W
After reset	-	-	0	0	-	0	0	0

Bit 5 **LVD36:** LVD 3.6V operating flag and only support LVD code option is LVD_H.
0 = Inactive (VDD > 3.6V).
1 = Active (VDD ≦ 3.6V).

Bit 4 **LVD24:** LVD 2.4V operating flag and only support LVD code option is LVD_M.
0 = Inactive (VDD > 2.4V).
1 = Active (VDD ≦ 2.4V).

LVD	LVD Code Option			
	LVD_L	LVD_M	LVD_H	LVD_MAX
2.0V Reset	Available	Available	Available	Available
2.4V Flag	-	Available	-	-
2.4V Reset	-	-	Available	-
3.6V Flag	-	-	Available	-
3.6V Reset	-	-	-	Available

LVD_L
If VDD < 2.0V, system will be reset.
Disable LVD24 and LVD36 bit of PFLAG register.
LVD_M
If VDD < 2.0V, system will be reset.
Enable LVD24 bit of PFLAG register. If VDD > 2.4V, LVD24 is "0". If VDD ≦2.4V, LVD24 flag is "1".
Disable LVD36 bit of PFLAG register.
LVD_H
If VDD < 2.4V, system will be reset.
Enable LVD24 bit of PFLAG register. If VDD > 2.4V, LVD24 is "0". If VDD ≦2.4V, LVD24 flag is "1".
Enable LVD36 bit of PFLAG register. If VDD > 3.6V, LVD36 is "0". If VDD ≦3.6V, LVD36 flag is "1".
LVD_MAX
If VDD < 3.6V, system will be reset.

✷ ***Note:***
1. ***After any LVD reset, LVD24, LVD36 flags are cleared.***
2. ***The voltage level of LVD 2.4V or 3.6V is for design reference only. Don't use the LVD indicator as precision VDD measurement.***

3.7 BROWN OUT RESET IMPROVEMENT

How to improve the brown reset condition? There are some methods to improve brown out reset as following.

- **LVD reset**
- **Watchdog reset**
- **Reduce the system executing rate**
- **External reset circuit. (Zener diode reset circuit, Voltage bias reset circuit, External reset IC)**

✸ ***Note:***

1. ***The " Zener diode reset circuit", "Voltage bias reset circuit" and "External reset IC" can completely improve the brown out reset, DC low battery and AC slow power down conditions.***
2. ***For AC power application and enhance EFT performance, the system clock is 4MHz/4 (1 mips) and use external reset (" Zener diode reset circuit", "Voltage bias reset circuit", "External reset IC"). The structure can improve noise effective and get good EFT characteristic.***

Watchdog reset:
The watchdog timer is a protection to make sure the system executes well. Normally the watchdog timer would be clear at one point of program. Don't clear the watchdog timer in several addresses. The system executes normally and the watchdog won't reset system. When the system is under dead-band and the execution error, the watchdog timer can't be clear by program. The watchdog is continuously counting until overflow occurrence. The overflow signal of watchdog timer triggers the system to reset, and the system return to normal mode after reset sequence. This method also can improve brown out reset condition and make sure the system to return normal mode.
If the system reset by watchdog and the power is still in dead-band, the system reset sequence won't be successful and the system stays in reset status until the power return to normal range. Watchdog timer application note is as following.

Reduce the system executing rate:
If the system rate is fast and the dead-band exists, to reduce the system executing rate can improve the dead-band. The lower system rate is with lower minimum operating voltage. Select the power voltage that's no dead-band issue and find out the mapping system rate. Adjust the system rate to the value and the system exits the dead-band issue. This way needs to modify whole program timing to fit the application requirement.

External reset circuit:
The external reset methods also can improve brown out reset and is the complete solution. There are three external reset circuits to improve brown out reset including "Zener diode reset circuit", "Voltage bias reset circuit" and "External reset IC". These three reset structures use external reset signal and control to make sure the MCU be reset under power dropping and under dead-band. The external reset information is described in the next section.

3.8 EXTERNAL RESET

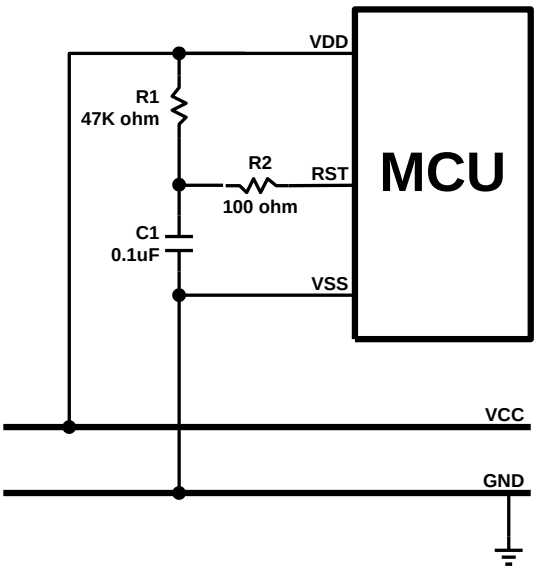
External reset function is controlled by “Reset_Pin” code option. Set the code option as “Reset” option to enable external reset function. External reset pin is Schmitt Trigger structure and low level active. The system is running when reset pin is high level voltage input. The reset pin receives the low voltage and the system is reset. The external reset operation actives in power on and normal running mode. During system power-up, the external reset pin must be high level input, or the system keeps in reset status. External reset sequence is as following.

- **External reset (only external reset pin enable):** System checks external reset pin status. If external reset pin is not high level, the system keeps reset status and waits external reset pin released.
- **System initialization:** All system registers is set as initial conditions and system is ready.
- **Oscillator warm up:** Oscillator operation is successfully and supply to system clock.
- **Program executing:** Power on sequence is finished and program executes from ORG 0.

The external reset can reset the system during power on duration, and good external reset circuit can protect the system to avoid working at unusual power condition, e.g. brown out reset in AC power application…

3.9 EXTERNAL RESET CIRCUIT

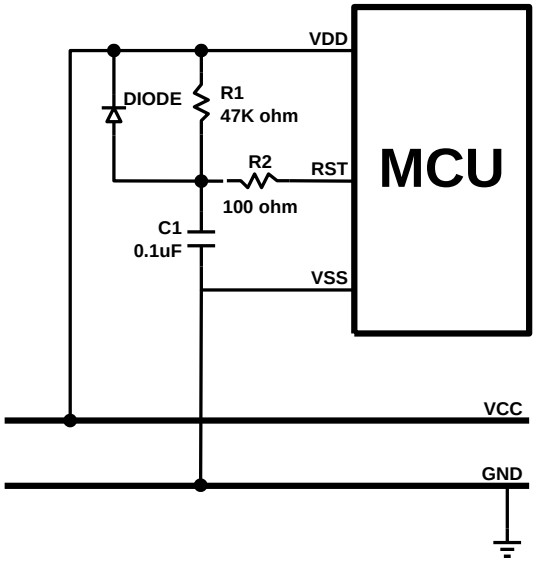
3.9.1 Simply RC Reset Circuit



This is the basic reset circuit, and only includes R1 and C1. The RC circuit operation makes a slow rising signal into reset pin as power up. The reset signal is slower than VDD power up timing, and system occurs a power on signal from the timing difference.

✸ ***Note: The reset circuit is no any protection against unusual power or brown out reset.***

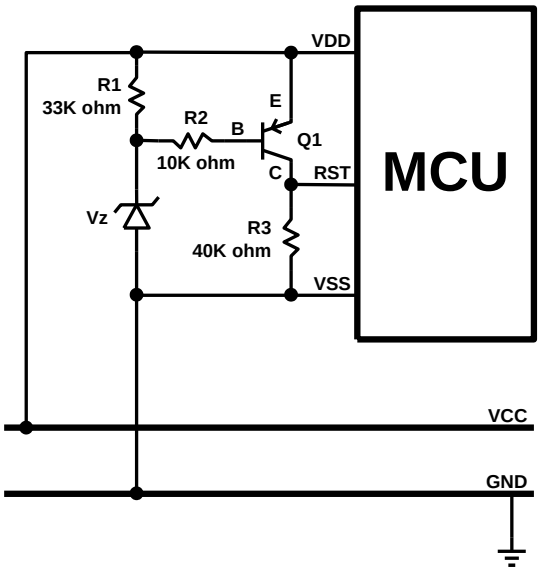
3.9.2 Diode & RC Reset Circuit



This is the better reset circuit. The R1 and C1 circuit operation is like the simply reset circuit to make a power on signal. The reset circuit has a simply protection against unusual power. The diode offers a power positive path to conduct higher power to VDD. It is can make reset pin voltage level to synchronize with VDD voltage. The structure can improve slight brown out reset condition.

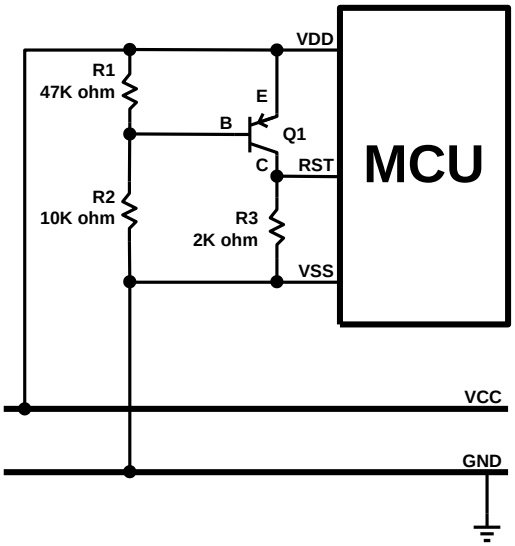
✷ ***Note: The R2 100 ohm resistor of "Simply reset circuit" and "Diode & RC reset circuit" is necessary to limit any current flowing into reset pin from external capacitor C in the event of reset pin breakdown due to Electrostatic Discharge (ESD) or Electrical Over-stress (EOS).***

3.9.3 Zener Diode Reset Circuit



The zener diode reset circuit is a simple low voltage detector and can **improve brown out reset condition completely**. Use zener voltage to be the active level. When VDD voltage level is above "Vz + 0.7V", the C terminal of the PNP transistor outputs high voltage and MCU operates normally. When VDD is below "Vz + 0.7V", the C terminal of the PNP transistor outputs low voltage and MCU is in reset mode. Decide the reset detect voltage by zener specification. Select the right zener voltage to conform the application.

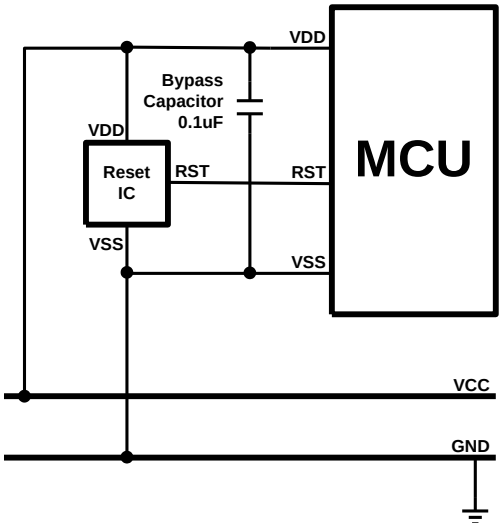
3.9.4 Voltage Bias Reset Circuit



The voltage bias reset circuit is a low cost voltage detector and can **improve brown out reset condition completely**. The operating voltage is not accurate as zener diode reset circuit. Use R1, R2 bias voltage to be the active level. When VDD voltage level is above or equal to "0.7V x (R1 + R2) / R1", the C terminal of the PNP transistor outputs high voltage and MCU operates normally. When VDD is below "0.7V x (R1 + R2) / R1", the C terminal of the PNP transistor outputs low voltage and MCU is in reset mode.
Decide the reset detect voltage by R1, R2 resistances. Select the right R1, R2 value to conform the application. In the circuit diagram condition, the MCU's reset pin level varies with VDD voltage variation, and the differential voltage is 0.7V. If the VDD drops and the voltage lower than reset pin detect level, the system would be reset. If want to make the reset active earlier, set the R2 > R1 and the cap between VDD and C terminal voltage is larger than 0.7V. The external reset circuit is with a stable current through R1 and R2. For power consumption issue application, e.g. DC power system, the current must be considered to whole system power consumption.

✸ ***Note: Under unstable power condition as brown out reset, "Zener diode rest circuit" and "Voltage bias reset circuit" can protects system no any error occurrence as power dropping. When power drops below the reset detect voltage, the system reset would be triggered, and then system executes reset sequence. That makes sure the system work well under unstable power situation.***

3.9.5 External Reset IC



The external reset circuit also use external reset IC to enhance MCU reset performance. This is a high cost and good effect solution. By different application and system requirement to select suitable reset IC. The reset circuit can improve all power variation.

4 SYSTEM CLOCK

4.1 OVERVIEW

The micro-controller is a dual clock system including high-speed and low-speed clocks. The high-speed clock includes internal high-speed oscillator and external oscillators selected by “High_CLK” code option. The low-speed clock is from internal low-speed oscillator controlled by “CLKMD” bit of OSCM register. Both high-speed clock and low-speed clock can be system clock source through a divider to decide the system clock rate.

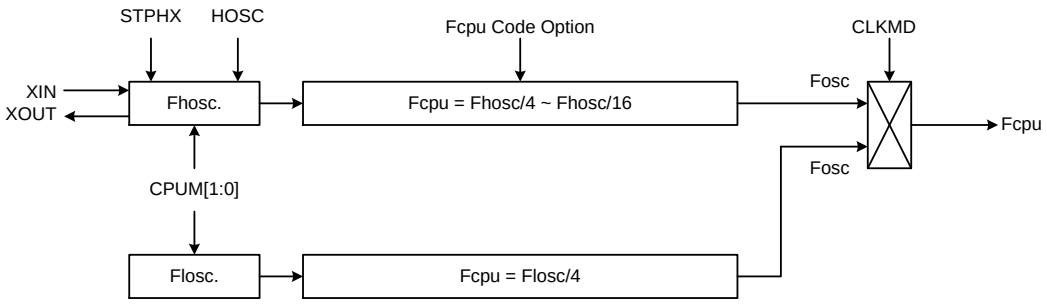
- **High-speed oscillator**

Internal high-speed oscillator is 16MHz RC type called “**IHRC**”.
External high-speed oscillator includes crystal/ceramic (4MHz, 12MHz, 32KHz) and RC type.

- **Low-speed oscillator**

Internal low-speed oscillator is 16KHz @3V, 32KHz @5V RC type called “**ILRC**”.

- **System clock block diagram**



- HOSC: High_Clk code option.
- Fhosc: External high-speed clock / Internal high-speed RC clock.
- Flosc: Internal low-speed RC clock (about 16KHz@3V and @5V).
- Fosc: System clock source.
- Fcpu: Instruction cycle.

4.2 FCPU (INSTRUCTION CYCLE)

The system clock rate is instruction cycle called “**Fcpu**” which is divided from the system clock source and decides the system operating rate. Fcpu rate is selected by Fcpu code option and the range is **Fhosc/4~Fhosc/16** under system normal mode. If the system high clock source is external 4MHz crystal, and the Fcpu code option is Fhosc/4, the Fcpu frequency is 4MHz/4 = 1MHz. Under system slow mode, the Fcpu is fixed Flosc/4, 16KHz/4=4KHz @3V, 32KHz/4=8KHz @5V.

4.3 SYSTEM HIGH-SPEED CLOCK

The system high-speed clock has internal and external two-type. The external high-speed clock includes 4MHz, 12MHz, 32KHz crystal/ceramic and RC type. These high-speed oscillators are selected by “**High_CLK**” code option.

4.3.1 HIGH_CLK CODE OPTION

For difference clock functions, Sonix provides multi-type system high clock options controlled by "High_CLK" code option. The High_CLK code option defines the system oscillator types including IHRC_16M, RC, 32K X'tal, 12M X'tal and 4M X'tal. These oscillator options support different bandwidth oscillator.

- **IHRC_16M:** The system high-speed clock source is internal high-speed 16MHz RC type oscillator. In the mode, XIN and XOUT pins are bi-direction GPIO mode, and not to connect any external oscillator device.
- **RC:** The system high-speed clock source is external low cost RC type oscillator. The RC oscillator circuit only connects to XIN pin, and the XOUT pin is bi-direction GPIO mode.
- **32K X'tal:** The system high-speed clock source is external low-speed 32768Hz crystal. The option only supports 32768Hz crystal and the RTC function is workable.
- **12M X'tal:** The system high-speed clock source is external high-speed crystal/ceramic. The oscillator bandwidth is 10MHz~16MHz.
- **4M X'tal:** The system high-speed clock source is external high-speed crystal/resonator. The oscillator bandwidth is 1MHz~10MHz.

4.3.2 INTERNAL HIGH-SPEED OSCILLATOR RC TYPE (IHRC)

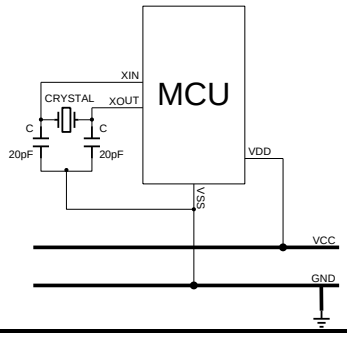
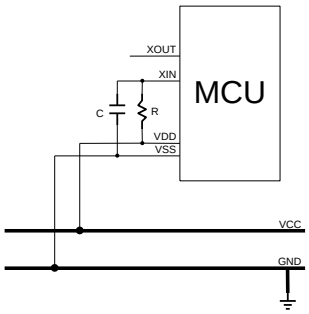
The internal high-speed oscillator is 16MHz RC type. The accuracy is ±2% under commercial condition. When the "High_CLK" code option is "IHRC_16M", the internal high-speed oscillator is enabled.

- **IHRC_16M:** The system high-speed clock is internal 16MHz oscillator RC type. XIN/XOUT pins are general purpose I/O pins.

4.3.3 EXTERNAL HIGH-SPEED OSCILLATOR

The external high-speed oscillator includes 4MHz, 12MHz, 32KHz and RC type. The 4MHz, 12MHz and 32KHz oscillators support crystal and ceramic types connected to XIN/XOUT pins with 20pF capacitors to ground. The RC type is a low cost RC circuit only connected to XIN pin. The capacitance is not below 100pF, and use the resistance to decide the frequency.

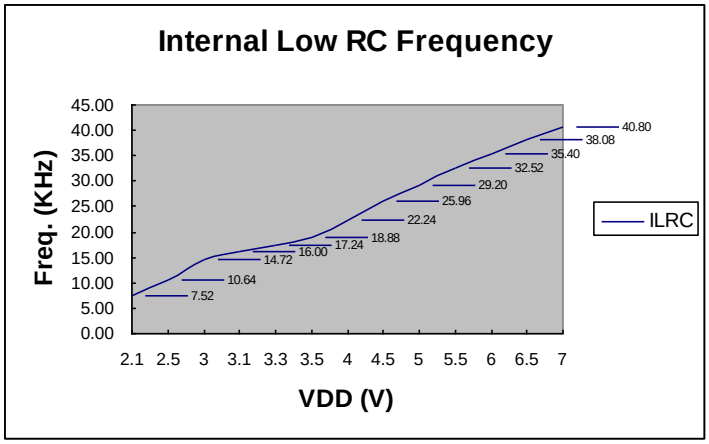
4.3.4 EXTERNAL OSCILLATOR APPLICATION CIRCUIT

CRYSTAL/CERAMIC	RC Type
	

✷ ***Note: Connect the Crystal/Ceramic and C as near as possible to the XIN/XOUT/VSS pins of micro-controller. Connect the R and C as near as possible to the VDD pin of micro-controller.***

4.4 SYSTEM LOW-SPEED CLOCK

The system low clock source is the internal low-speed oscillator built in the micro-controller. The low-speed oscillator uses RC type oscillator circuit. The frequency is affected by the voltage and temperature of the system. In common condition, the frequency of the RC oscillator is about 16KHz at 3V and 32KHz at 5V. The relation between the RC frequency and voltage is as the following figure.



The internal low RC supports watchdog clock source and system slow mode controlled by “CLKMD” bit of OSCM register.

- ***Flosc = Internal low RC oscillator (about 16KHz @3V, 32KHz @5V).***
- ***Slow mode Fcpu = Flosc / 4***

There are two conditions to stop internal low RC. One is power down mode, and the other is green mode of 32K mode and watchdog disable. If system is in 32K mode and watchdog disable, only 32K oscillator actives and system is under low power consumption.

➢ **Example: Stop internal low-speed oscillator by power down mode.**

```
B0BSET      FCPUM0          ; To stop external high-speed oscillator and internal low-speed
                            ; oscillator called power down mode (sleep mode).
```

✸ ***Note: The internal low-speed clock can’t be turned off individually. It is controlled by CPUM0, CPUM1 (32K, watchdog disable) bits of OSCM register.***

4.5 OSCM REGISTER

The OSCM register is an oscillator control register. It controls oscillator status, system mode.

095H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OSCM	0	0	0	CPUM1	CPUM0	CLKMD	STPHX	0
Read/Write	-	-	-	R/W	R/W	R/W	R/W	-
After reset	-	-	-	0	0	0	0	-

Bit 1 **STPHX:** External high-speed oscillator control bit.
0 = External high-speed oscillator free run.
1 = External high-speed oscillator free run stop. Internal low-speed RC oscillator is still running.

Bit 2 **CLKMD:** System high/Low clock mode control bit.
0 = Normal (dual) mode. System clock is high clock.
1 = Slow mode. System clock is internal low clock.

Bit[4:3] **CPUM[1:0]:** CPU operating mode control bits.
00 = normal.
01 = sleep (power down) mode.
10 = green mode.
11 = reserved.

"STPHX" bit controls internal high speed RC type oscillator and external oscillator operations. When "STPHX=0", the external oscillator or internal high speed RC type oscillator active. When "STPHX=1", the external oscillator or internal high speed RC type oscillator are disabled. The STPHX function is depend on different high clock options to do different controls.

- **IHRC_16M: "STPHX=1" disables internal high speed RC type oscillator.**
- **RC, 4M, 12M, 32K: "STPHX=1" disables external oscillator.**

4.6 SYSTEM CLOCK MEASUREMENT

Under design period, the users can measure system clock speed by software instruction cycle (Fcpu). This way is useful in RC mode.

➢ **Example: Fcpu instruction cycle of external oscillator.**

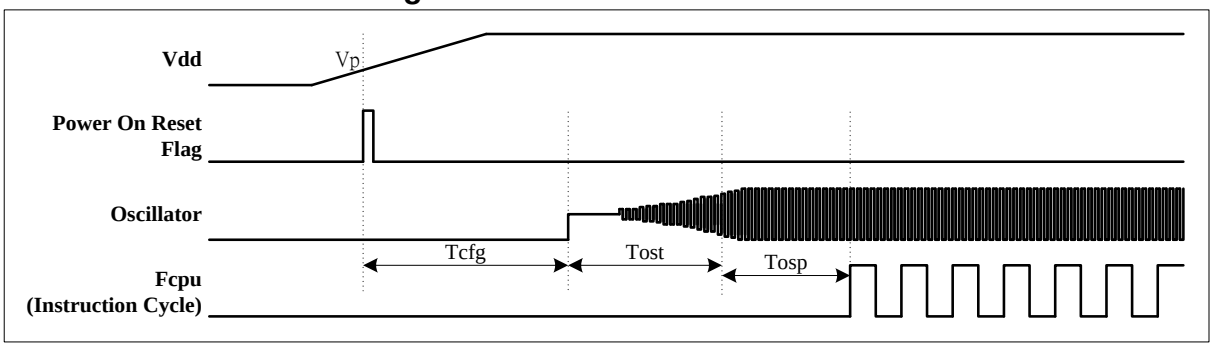
```
        B0BSET    P0M.0     ; Set P0.0 to be output mode for outputting Fcpu toggle signal.
@@:
        B0BSET    P0.0      ; Output Fcpu toggle signal in low-speed clock mode.
        B0BCLR    P0.0      ; Measure the Fcpu frequency by oscilloscope.
        JMP       @B
```

✸ ***Note: Do not measure the RC frequency directly from XIN; the probe impendence will affect the RC frequency.***

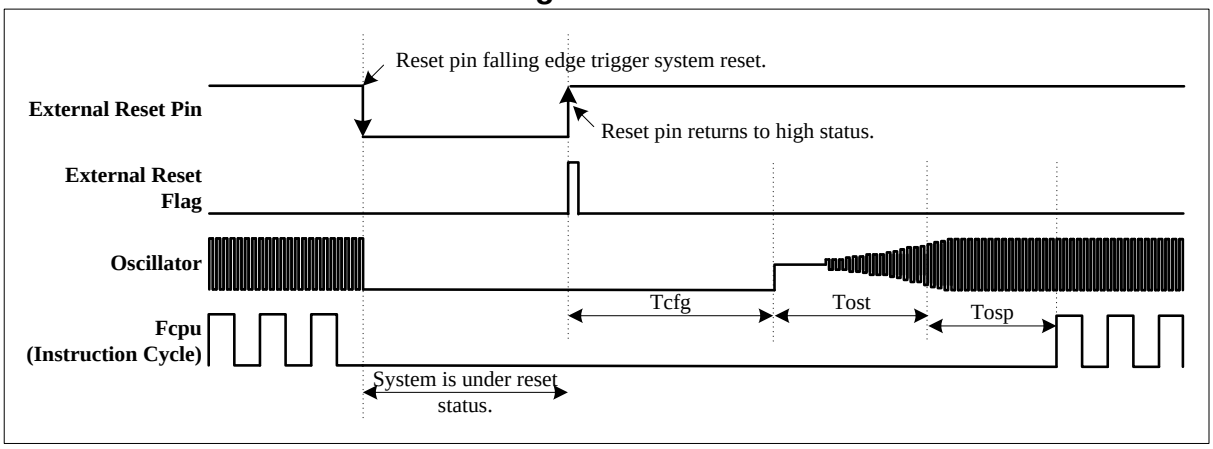
4.7 SYSTEM CLOCK TIMING

Parameter	Symbol	Description	Typical
Hardware configuration time	Tcfg	2048*F_{ILRC}	64ms @ F_{ILRC} = 32KHz 128ms @ F_{ILRC} = 16KHz
Oscillator start up time	Tost	The start-up time is depended on oscillator's material, factory and architecture. Normally, the low-speed oscillator's start-up time is lower than high-speed oscillator. The RC type oscillator's start-up time is faster than crystal type oscillator.	-
Oscillator warm-up time	Tosp	Oscillator warm-up time of reset condition. 2048*F_{hosc} (Power on reset, LVD reset, watchdog reset, external reset pin active.)	64ms @ F_{hosc} = 32KHz 512us @ F_{hosc} = 4MHz 128us @ F_{hosc} = 16MHz
		Oscillator warm-up time of power down mode wake-up condition. 2048*F_{hosc} ……Crystal/resonator type oscillator, e.g. 32768Hz crystal, 4MHz crystal, 16MHz crystal… 32*F_{hosc}……RC type oscillator, e.g. external RC type oscillator, internal high-speed RC type oscillator.	X'tal: 64ms @ F_{hosc} = 32KHz 512us @ F_{hosc} = 4MHz 128us @ F_{hosc} = 16MHz RC: 8us @ F_{hosc} = 4MHz 2us @ F_{hosc} = 16MHz

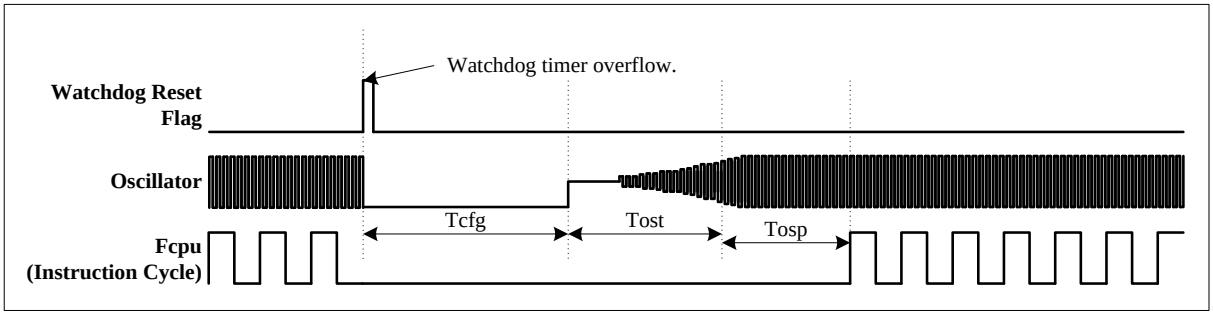
- **Power On Reset Timing**



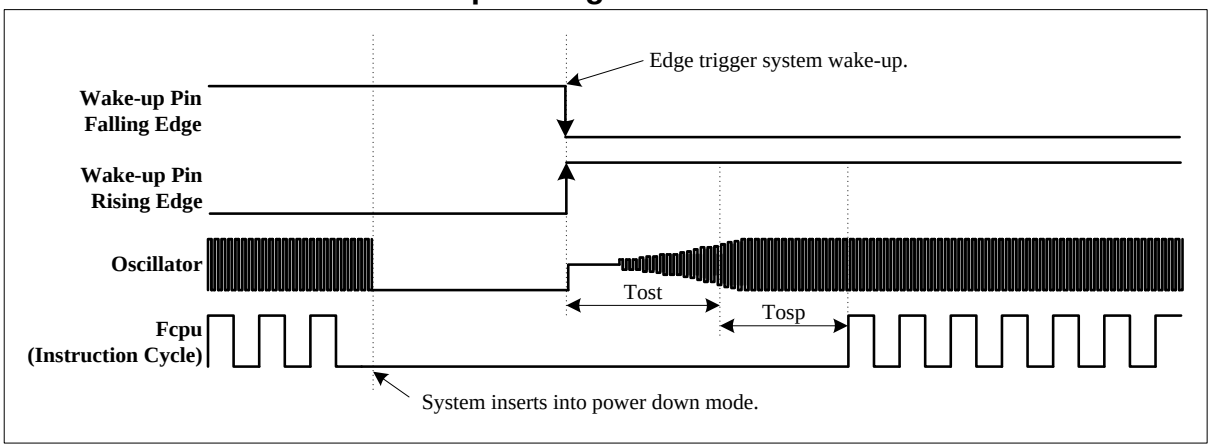
- **External Reset Pin Reset Timing**



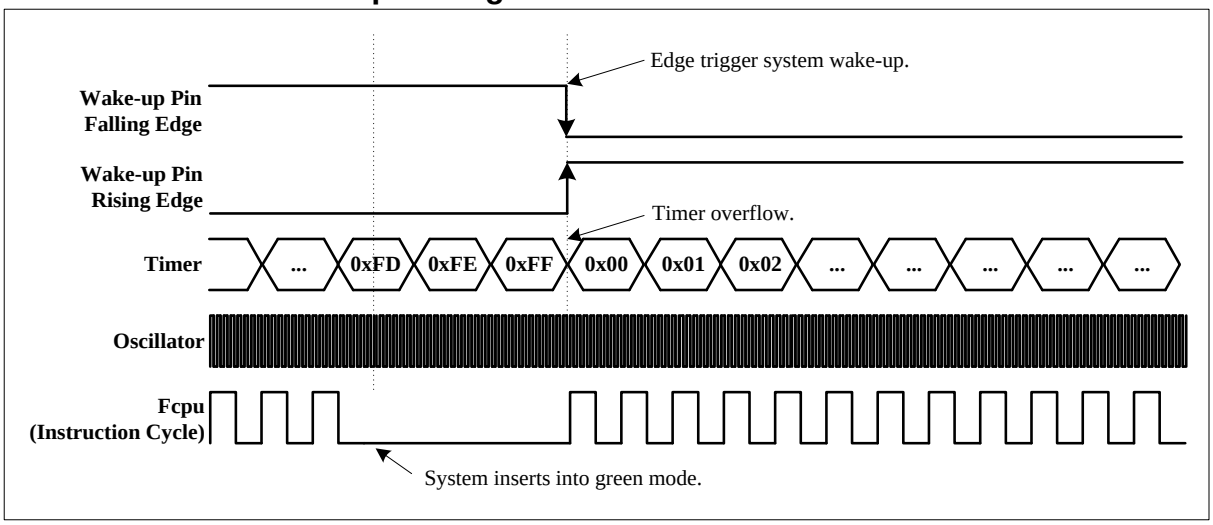
Watchdog Reset Timing



Power Down Mode Wake-up Timing

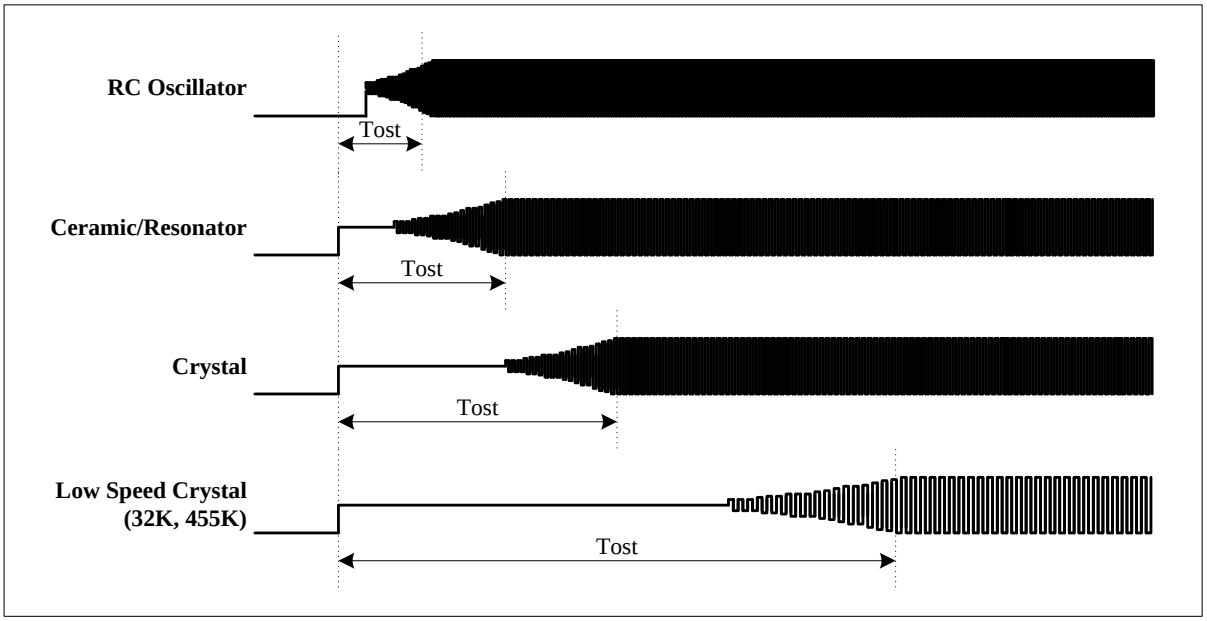


Green Mode Wake-up Timing



Oscillator Start-up Time

The start-up time is depended on oscillator's material, factory and architecture. Normally, the low-speed oscillator's start-up time is lower than high-speed oscillator. The RC type oscillator's start-up time is faster than crystal type oscillator.



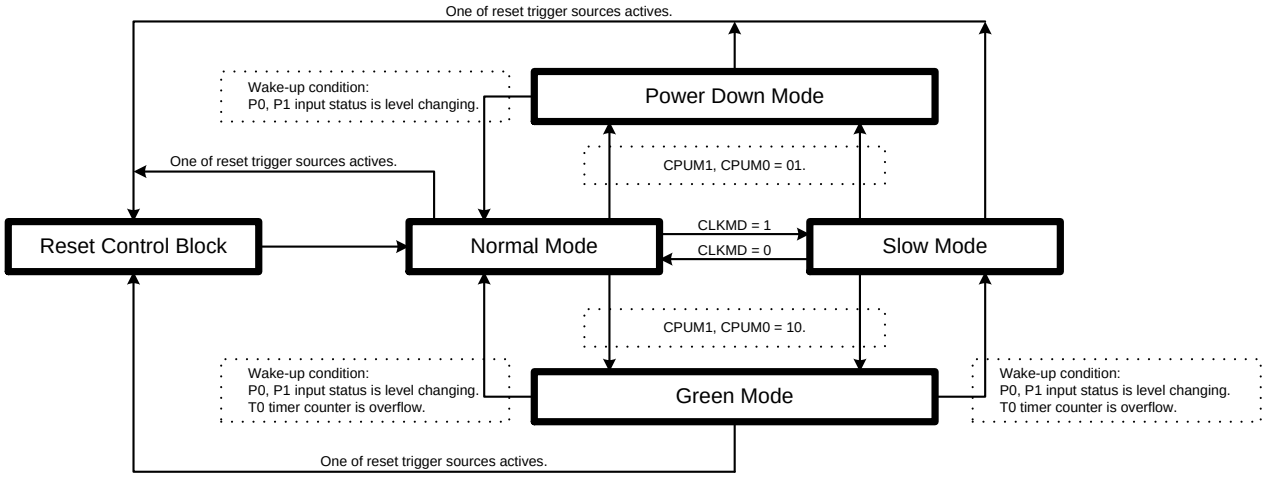
5 SYSTEM OPERATION MODE

5.1 OVERVIEW

The chip builds in four operating mode for difference clock rate and power saving reason. These modes control oscillators, op-code operation and analog peripheral devices' operation.

- Normal mode: System high-speed operating mode.
- Slow mode: System low-speed operating mode.
- Power down mode: System power saving mode (Sleep mode).
- Green mode: System ideal mode.

Operating Mode Control Block



Operating Mode Clock Control Table

Operating Mode	Normal Mode	Slow Mode	Green Mode	Power Down Mode
EHOSC	Running	By STPHX	By STPHX	Stop
IHRC	Running	By STPHX	By STPHX	Stop
ILRC	Running	Running	Running	Stop
CPU instruction	Executing	Executing	Stop	Stop
T0 timer	By T0ENB	By T0ENB	By T0ENB	Inactive
TC0 timer	By TC0ENB	By TC0ENB	By TC0ENB (PWM active)	Inactive
Watchdog timer	By Watch_Dog Code option	By Watch_Dog Code option	By Watch_Dog Code option	By Watch_Dog Code option
Internal interrupt	All active	All active	T0	All inactive
External interrupt	All active	All active	All active	All inactive
Wakeup source	-	-	P0, P1, T0 Reset	P0, P1 Reset

- **EHOSC:** External high-speed oscillator (XIN/XOUT).
- **IHRC:** Internal high-speed oscillator RC type.
- **ILRC:** Internal low-speed oscillator RC type.

5.2 NORMAL MODE

The Normal Mode is system high clock operating mode. The system clock source is from high speed oscillator. The program is executed. After power on and any reset trigger released, the system inserts into normal mode to execute program. When the system is wake-up from power down mode, the system also inserts into normal mode. In normal mode, the high speed oscillator actives, and the power consumption is largest of all operating modes.

- The program is executed, and full functions are controllable.
- The system rate is high speed.
- The high speed oscillator and internal low speed RC type oscillator active.
- Normal mode can be switched to other operating modes through OSCM register.
- Power down mode is wake-up to normal mode.
- Slow mode is switched to normal mode.
- Green mode from normal mode is wake-up to normal mode.

5.3 SLOW MODE

The slow mode is system low clock operating mode. The system clock source is from internal low speed RC type oscillator. The slow mode is controlled by CLKMD bit of OSCM register. When CLKMD=0, the system is in normal mode. When CLKMD=1, the system inserts into slow mode. The high speed oscillator won't be disabled automatically after switching to slow mode, and must be disabled by SPTHX bit to reduce power consumption. In slow mode, the system rate is fixed Flosc/4 (Flosc is internal low speed RC type oscillator frequency).

- The program is executed, and full functions are controllable.
- The system rate is low speed (Flosc/4).
- The internal low speed RC type oscillator actives, and the high speed oscillator is controlled by STPHX=1. In slow mode, to stop high speed oscillator is strongly recommendation.
- Slow mode can be switched to other operating modes through OSCM register.
- Power down mode from slow mode is wake-up to normal mode.
- Normal mode is switched to slow mode.
- Green mode from slow mode is wake-up to slow mode.

5.4 POWER DOWN MODE

The power down mode is the system ideal status. No program execution and oscillator operation. Whole chip is under low power consumption status under 1uA. The power down mode is waked up by P0, P1 hardware level change trigger. P1 wake-up function is controlled by P1W register. Any operating modes into power down mode, the system is waked up to normal mode. Inserting power down mode is controlled by CPUM0 bit of OSCM register. When CPUM0=1, the system inserts into power down mode. After system wake-up from power down mode, the CPUM0 bit is disabled (zero status) automatically.

- The program stops executing, and full functions are disabled.
- All oscillators including external high speed oscillator, internal high speed oscillator and internal low speed oscillator stop.
- The power consumption is under 1uA.
- The system inserts into normal mode after wake-up from power down mode.
- The power down mode wake-up source is P0 and P1 level change trigger.

✷ ***Note: If the system is in normal mode, to set STPHX=1 to disable the high clock oscillator. The system is under no system clock condition. This condition makes the system stay as power down mode, and can be wake-up by P0, P1 level change trigger.***

5.5 GREEN MODE

The green mode is another system ideal status not like power down mode. In power down mode, all functions and hardware devices are disabled. But in green mode, the system clock source keeps running, so the power consumption of green mode is larger than power down mode. In green mode, the program isn't executed, but the timer with wake-up function actives as enabled, and the timer clock source is the non-stop system clock. The green mode has 2 wake-up sources. One is the P0, P1 level change trigger wake-up. The other one is internal timer with wake-up function occurring overflow. That's mean users can setup one fix period to timer, and the system is waked up until the time out. Inserting green mode is controlled by CPUM1 bit of OSCM register. When CPUM1=1, the system inserts into green mode. After system wake-up from green mode, the CPUM1 bit is disabled (zero status) automatically.

- The program stops executing, and full functions are disabled.
- Only the timer with wake-up function actives.
- The oscillator to be the system clock source keeps running, and the other oscillators operation is depend on system operation mode configuration.
- If inserting green mode from normal mode, the system insets to normal mode after wake-up.
- If inserting green mode from slow mode, the system insets to slow mode after wake-up.
- The green mode wake-up sources are P0, P1 level change trigger and unique time overflow.
- PWM output functions active in green mode, but the timer can't wake-up the system as overflow.

✸ ***Note: Sonix provides "GreenMode" macro to control green mode operation. It is necessary to use "GreenMode" macro to control system inserting green mode.***
The macro includes three instructions. Please take care the macro length as using BRANCH type instructions, e.g. bts0, bts1, b0bts0, b0bts1, ins, incms, decs, decms, cmprs, jmp, or the routine would be error.

5.6 OPERATING MODE CONTROL MACRO

Sonix provides operating mode control macros to switch system operating mode easily.

Macro	Length	Description
SleepMode	1-word	The system insets into Sleep Mode (Power Down Mode).
GreenMode	3-word	The system inserts into Green Mode.
SlowMode	2-word	The system inserts into Slow Mode and stops high speed oscillator.
Slow2Normal	5-word	The system returns to Normal Mode from Slow Mode. The macro includes operating mode switch, enable high speed oscillator, high speed oscillator warm-up delay time.

- **Example: Switch normal/slow mode to power down (sleep) mode.**

```
SleepMode                    ; Declare “SleepMode” macro directly.
```

- **Example: Switch normal mode to slow mode.**

```
SlowMode                     ; Declare “SlowMode” macro directly.
```

- **Example: Switch slow mode to normal mode (The external high-speed oscillator stops).**

```
Slow2Normal                  ; Declare “Slow2Normal” macro directly.
```

- **Example: Switch normal/slow mode to green mode.**

```
GreenMode                    ; Declare “GreenMode” macro directly.
```

- **Example: Switch normal/slow mode to green mode and enable T0 wake-up function.**

```
; Set T0 timer wakeup function.
        B0BCLR      FT0IEN      ; To disable T0 interrupt service
        B0BCLR      FT0ENB      ; To disable T0 timer
        MOV         A,#20H      ;
        B0MOV       T0M,A       ; To set T0 clock = Fcpu / 64
        MOV         A,#74H
        B0MOV       T0C,A       ; To set T0C initial value = 74H (To set T0 interval = 10 ms)
        B0BCLR      FT0IEN      ; To disable T0 interrupt service
        B0BCLR      FT0IRQ      ; To clear T0 interrupt request
        B0BSET      FT0ENB      ; To enable T0 timer

; Go into green mode
        GreenMode               ; Declare “GreenMode” macro directly.
```

5.7 WAKEUP

5.7.1 OVERVIEW

Under power down mode (sleep mode) or green mode, program doesn't execute. The wakeup trigger can wake the system up to normal mode or slow mode. The wakeup trigger sources are external trigger (P0/P1 level change) and internal trigger (T0 timer overflow). The wakeup function builds in interrupt operation issued IRQ flag and trigger system executing interrupt service routine as system wakeup occurrence.

- Power down mode is waked up to normal mode. The wakeup trigger is only external trigger (P0/P1 level change)
- Green mode is waked up to last mode (normal mode or slow mode). The wakeup triggers are external trigger (P0/P1 level change) and internal trigger (T0 timer overflow).
- Wakeup interrupt function issues WAKEIRQ as system wakeup from power down mode or green mode. If WAKEIEN is "1" meaning enable, the wakeup event triggers program counter point to interrupt vector (ORG 8) executing interrupt service routine.

✸ ***Note: If wake-up source is external interrupt source, the WAKE bit won't be set, and external interrupt IRQ bit is set. The system issues external interrupt request and executes interrupt service routine.***

5.7.2 WAKEUP TIME

When the system is in power down mode (sleep mode), the high clock oscillator stops. When waked up from power down mode, MCU waits for 2048 external high-speed oscillator clocks and 32 internal high-speed oscillator clocks as the wakeup time to stable the oscillator circuit. After the wakeup time, the system goes into the normal mode.

✸ ***Note: Wakeup from green mode is no wakeup time because the clock doesn't stop in green mode.***

The value of the external high clock oscillator wakeup time is as the following.

The Wakeup time = 1/Fosc * 2048 (sec) + high clock start-up time

➢ **Example: In power down mode (sleep mode), the system is waked up. After the wakeup time, the system goes into normal mode. The wakeup time is as the following.**

The wakeup time = 1/Fosc * 2048 = 0.512 ms (Fosc = 4MHz)
The total wakeup time = 0.512 ms + oscillator start-up time

The value of the internal high clock oscillator RC type wakeup time is as the following.

The Wakeup time = 1/Fosc * 32 (sec) + high clock start-up time

➢ **Example: In power down mode (sleep mode), the system is waked up. After the wakeup time, the system goes into normal mode. The wakeup time is as the following.**

The wakeup time = 1/Fosc * 32 = 2 us (Fhosc = 16MHz)

✸ ***Note: The high clock start-up time is depended on the VDD and oscillator type of high clock.***

5.7.3 P1W WAKEUP CONTROL REGISTER

Under power down mode (sleep mode) and green mode, the I/O ports with wakeup function are able to wake the system up to normal mode. The wake-up trigger edge is level changing. When wake-up pin occurs rising edge or falling edge, the system is waked up by the trigger edge. The Port 0 and Port 1 have wakeup function. Port 0 wakeup function always enables, but the Port 1 is controlled by the P1W register.

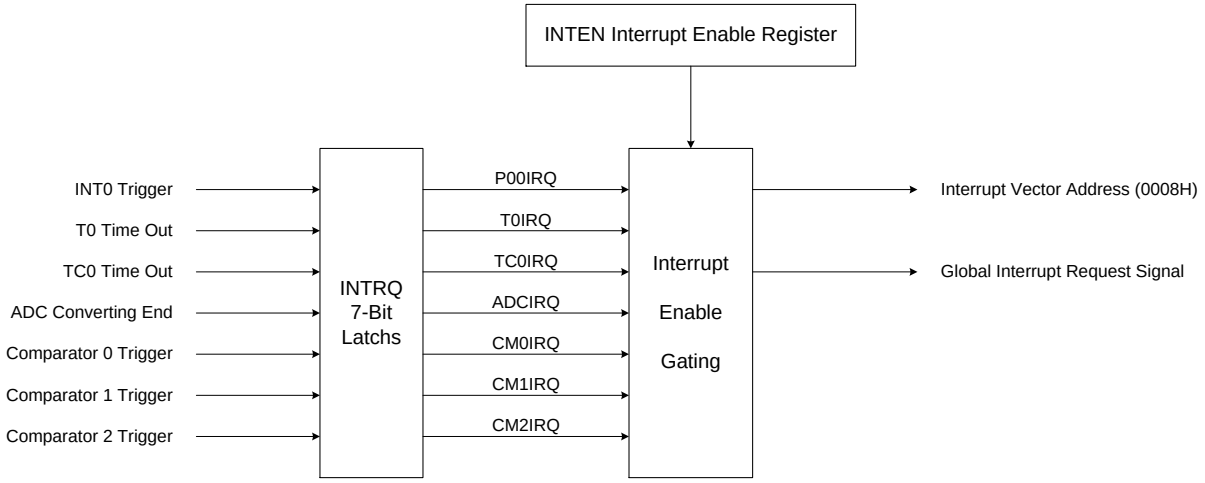
0C0H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1W	-	P16W	P15W	P14W	P13W	P12W	P11W	P10W
Read/Write	-	W	W	W	W	W	W	W
After reset	-	0	0	0	0	0	0	0

Bit[6:0] **P10W~P16W:** Port 1 wakeup function control bits.
0 = Disable P1n wakeup function.
1 = Enable P1n wakeup function.

6 INTERRUPT

6.1 OVERVIEW

This MCU provides 7 interrupt sources, including 6 internal interrupt (T0/TC0/CM0/CM1/CM2/ADC) and 1 external interrupt (INT0). The external interrupt can wakeup the chip while the system is switched from power down mode to high-speed normal mode, and interrupt request is latched until return to normal mode. Once interrupt service is executed, the GIE bit in STKP register will clear to “0” for stopping other interrupt request. On the contrast, when interrupt service exits, the GIE bit will set to “1” to accept the next interrupts’ request. Most of the interrupt request signals are stored in INTRQ register.



✷ ***Note: The GIE bit must enable during all interrupt operation.***

6.2 INTEN INTERRUPT ENABLE REGISTER

INTEN is the interrupt request control register including four internal interrupts, three external interrupts enable control bits. One of the register to be set “1” is to enable the interrupt request function. Once of the interrupt occur, the stack is incremented and program jump to ORG 8 to execute interrupt service routines. The program exits the interrupt service routine when the returning interrupt service routine instruction (RETI) is executed.

0C9H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTEN	ADCIEN	-	TC0IEN	T0IEN	CM2IEN	CM1IEN	CM0IEN	P00IEN
Read/Write	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	-	0	0	0	0	0	0

Bit 0 **P00IEN:** External P0.0 interrupt (INT0) control bit.
0 = Disable INT0 interrupt function.
1 = Enable INT0 interrupt function.

Bit 1 **CM0IEN:** Comparator 0 interrupt control bit.
0 = Disable comparator 0 interrupt function.
1 = Enable comparator 0 interrupt function.

Bit 2 **CM1IEN:** Comparator 1 interrupt control bit.
0 = Disable comparator 1 interrupt function.
1 = Enable comparator 1 interrupt function.

Bit 3 **CM2IEN:** Comparator 2 interrupt control bit.
0 = Disable comparator 2 interrupt function.
1 = Enable comparator 2 interrupt function.

Bit 4 **T0IEN:** T0 timer interrupt control bit.
0 = Disable T0 interrupt function.
1 = Enable T0 interrupt function.

Bit 5 **TC0IEN:** TC0 timer interrupt control bit.
0 = Disable TC0 interrupt function.
1 = Enable TC0 interrupt function.

Bit 7 **ADCIEN:** ADC interrupt control bit.
0 = Disable ADC interrupt function.
1 = Enable ADC interrupt function.

6.3 INTRQ INTERRUPT REQUEST REGISTER

INTRQ is the interrupt request flag register. The register includes all interrupt request indication flags. Each one of the interrupt requests occurs, the bit of the INTRQ register would be set “1”. The INTRQ value needs to be clear by programming after detecting the flag. In the interrupt vector of program, users know the any interrupt requests occurring by the register and do the routine corresponding of the interrupt request.

0C8H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTRQ	ADCIRQ	-	TC0IRQ	T0IRQ	CM2IRQ	CM1IRQ	CM0IRQ	P00IRQ
Read/Write	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	-	0	0	0	0	0	0

Bit 0 **P00IRQ:** External P0.0 interrupt (INT0) request flag.
0 = None INT0 interrupt request.
1 = INT0 interrupt request.

Bit 1 **CM0IRQ:** Comparator 0 interrupt request flag.
0 = None comparator 0 interrupt request.
1 = Comparator 0 interrupt request.

Bit 2 **CM1IRQ:** Comparator 1 interrupt request flag.
0 = None comparator 1 interrupt request.
1 = Comparator 1 interrupt request.

Bit 3 **CM2IRQ:** Comparator 2 interrupt request flag.
0 = None comparator 2 interrupt request.
1 = Comparator 2 interrupt request.

Bit 4 **T0IRQ:** T0 timer interrupt request flag.
0 = None T0 interrupt request.
1 = T0 interrupt request.

Bit 5 **TC0IRQ:** TC0 timer interrupt request flag.
0 = None TC0 interrupt request.
1 = TC0 interrupt request.

Bit 7 **ADCIRQ:** ADC interrupt request flag.
0 = None ADC interrupt request.
1 = ADC interrupt request.

6.4 GIE GLOBAL INTERRUPT OPERATION

GIE is the global interrupt control bit. All interrupts start work after the GIE = 1 It is necessary for interrupt service request. One of the interrupt requests occurs, and the program counter (PC) points to the interrupt vector (ORG 8) and the stack add 1 level.

0DFH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STKP	GIE	-	-	-	-	STKPB2	STKPB1	STKPB0
Read/Write	R/W	-	-	-	-	R/W	R/W	R/W
After reset	0	-	-	-	-	1	1	1

Bit 7 **GIE:** Global interrupt control bit.
0 = Disable global interrupt.
1 = Enable global interrupt.

➢ **Example: Set global interrupt control bit (GIE).**

```
B0BSET      FGIE            ; Enable GIE
```

✸ ***Note: The GIE bit must enable during all interrupt operation.***

6.5 PUSH, POP ROUTINE

When any interrupt occurs, system will jump to ORG 8 and execute interrupt service routine. It is necessary to save ACC, PFLAG data. The chip includes “PUSH”, “POP” for in/out interrupt service routine. The two instructions save and load **ACC**, **PFLAG** data into buffers and avoid main routine error after interrupt service routine finishing.

✷ ***Note: ”PUSH”, “POP” instructions save and load ACC/PFLAG without (NT0, NPD). PUSH/POP buffer is an unique buffer and only one level.***

➢ **Example: Store ACC and PAFLG data by PUSH, POP instructions when interrupt service routine executed.**

```
                ORG     0
                JMP     START

                ORG     8
                JMP     INT_SERVICE

                ORG     10H
START:
                …

INT_SERVICE:
                PUSH                    ; Save ACC and PFLAG to buffers.
                …
                …
                POP                     ; Load ACC and PFLAG from buffers.

                RETI                    ; Exit interrupt service vector
                …
                ENDP
```

6.6 EXTERNAL INTERRUPT OPERATION (INT0)

Sonix provides 1 external interrupt sources in the micro-controller. INT0 is external interrupt trigger sources and build in edge trigger configuration function. When the external edge trigger occurs, the external interrupt request flag will be set to “1” when the external interrupt control bit enabled. If the external interrupt control bit is disabled, the external interrupt request flag won’t active when external edge trigger occurrence. When external interrupt control bit is enabled and external interrupt edge trigger is occurring, the program counter will jump to the interrupt vector (ORG 8) and execute interrupt service routine.

The external interrupt builds in wake-up latch function. That means when the system is triggered wake-up from power down mode, the wake-up source is external interrupt source (P0.0), and the trigger edge direction matches interrupt edge configuration, the trigger edge will be latched, and the system executes interrupt service routine fist after wake-up.

0BFH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PEDGE	-	-	-	-	-	-	P00G1	P00G0
Read/Write	-	-	-	-	-	-	R/W	R/W
After reset	-	-	-	-	-	-	0	0

Bit[1:0] **P00G[1:0]:** INT0 edge trigger select bits.
00 = reserved,
01 = rising edge,
10 = falling edge,
11 = rising/falling bi-direction.

➢ **Example: Setup INT0 interrupt request and bi-direction edge trigger.**

```
        MOV     A, #03H
        B0MOV   PEDGE, A        ; Set INT0 interrupt trigger as bi-direction edge.

        B0BSET  FP00IEN         ; Enable INT0 interrupt service
        B0BCLR  FP00IRQ         ; Clear INT0 interrupt request flag
        B0BSET  FGIE            ; Enable GIE
```

➢ **Example: INT0 interrupt service routine.**

```
        ORG     8               ; Interrupt vector
        JMP     INT_SERVICE
INT_SERVICE:
        …                       ; Push routine to save ACC and PFLAG to buffers.

        B0BTS1  FP00IRQ         ; Check P00IRQ
        JMP     EXIT_INT        ; P00IRQ = 0, exit interrupt vector

        B0BCLR  FP00IRQ         ; Reset P00IRQ
        …                       ; INT0 interrupt service routine
EXIT_INT:
        …                       ; Pop routine to load ACC and PFLAG from buffers.
        RETI                    ; Exit interrupt vector
```

6.7 T0 INTERRUPT OPERATION

When the T0C counter occurs overflow, the T0IRQ will be set to “1” however the T0IEN is enable or disable. If the T0IEN = 1, the trigger event will make the T0IRQ to be “1” and the system enter interrupt vector. If the T0IEN = 0, the trigger event will make the T0IRQ to be “1” but the system will not enter interrupt vector. Users need to care for the operation under multi-interrupt situation.

➢ **Example: T0 interrupt request setup. Fcpu = 4MHz / 4.**

```
        B0BCLR      FT0IEN      ; Disable T0 interrupt service
        B0BCLR      FT0ENB      ; Disable T0 timer
        MOV         A, #20H     ;
        B0MOV       T0M, A      ; Set T0 clock = Fcpu / 64
        MOV         A, #64H     ; Set T0C initial value = 64H
        B0MOV       T0C, A      ; Set T0 interval = 10 ms

        B0BSET      FT0IEN      ; Enable T0 interrupt service
        B0BCLR      FT0IRQ      ; Clear T0 interrupt request flag
        B0BSET      FT0ENB      ; Enable T0 timer

        B0BSET      FGIE        ; Enable GIE
```

➢ **Example: T0 interrupt service routine.**

```
        ORG         8           ; Interrupt vector
        JMP         INT_SERVICE
INT_SERVICE:

        …                       ; Push routine to save ACC and PFLAG to buffers.

        B0BTS1      FT0IRQ      ; Check T0IRQ
        JMP         EXIT_INT    ; T0IRQ = 0, exit interrupt vector

        B0BCLR      FT0IRQ      ; Reset T0IRQ
        MOV         A, #64H
        B0MOV       T0C, A      ; Reset T0C.
        …                       ; T0 interrupt service routine
        …
EXIT_INT:
        …                       ; Pop routine to load ACC and PFLAG from buffers.


        RETI                    ; Exit interrupt vector
```

6.8 TC0 INTERRUPT OPERATION

When the TC0C counter overflows, the TC0IRQ will be set to "1" no matter the TC0IEN is enable or disable. If the TC0IEN and the trigger event TC0IRQ is set to be "1". As the result, the system will execute the interrupt vector. If the TC0IEN = 0, the trigger event TC0IRQ is still set to be "1". Moreover, the system won't execute interrupt vector even when the TC0IEN is set to be "1". Users need to be cautious with the operation under multi-interrupt situation.

➢ **Example: TC0 interrupt request setup. Fcpu = 16MHz / 16.**

```
        B0BCLR      FTC0IEN         ; Disable TC0 interrupt service
        B0BCLR      FTC0ENB         ; Disable TC0 timer
        MOV         A, #20H         ;
        B0MOV       TC0M, A         ; Set TC0 clock = Fcpu / 64
        MOV         A, #64H         ; Set TC0C initial value = 64H
        B0MOV       TC0C, A         ; Set TC0 interval = 10 ms

        B0BSET      FTC0IEN         ; Enable TC0 interrupt service
        B0BCLR      FTC0IRQ         ; Clear TC0 interrupt request flag
        B0BSET      FTC0ENB         ; Enable TC0 timer

        B0BSET      FGIE            ; Enable GIE
```

➢ **Example: TC0 interrupt service routine.**

```
        ORG         8               ; Interrupt vector
        JMP         INT_SERVICE
INT_SERVICE:

        …                           ; Push routine to save ACC and PFLAG to buffers.

        B0BTS1      FTC0IRQ         ; Check TC0IRQ
        JMP         EXIT_INT        ; TC0IRQ = 0, exit interrupt vector

        B0BCLR      FTC0IRQ         ; Reset TC0IRQ
        MOV         A, #64H
        B0MOV       TC0C, A         ; Reset TC0C.
        …                           ; TC0 interrupt service routine
        …
EXIT_INT:
        …                           ; Pop routine to load ACC and PFLAG from buffers.

        RETI                        ; Exit interrupt vector
```

6.9 ADC INTERRUPT OPERATION

When the ADC converting successfully, the ADCIRQ will be set to “1” no matter the ADCIEN is enable or disable. If the ADCIEN and the trigger event ADCIRQ is set to be “1”. As the result, the system will execute the interrupt vector. If the ADCIEN = 0, the trigger event ADCIRQ is still set to be “1”. Moreover, the system won’t execute interrupt vector even when the ADCIEN is set to be “1”. Users need to be cautious with the operation under multi-interrupt situation.

➢ **Example: ADC interrupt request setup.**

```
        B0BCLR      FADCIEN         ; Disable ADC interrupt service

        MOV         A, #10110000B   ;
        B0MOV       ADM, A          ; Enable P4.0 ADC input and ADC function.
        MOV         A, #00000000B   ; Set ADC converting rate = Fcpu/16
        B0MOV       ADR, A

        B0BSET      FADCIEN         ; Enable ADC interrupt service
        B0BCLR      FADCIRQ         ; Clear ADC interrupt request flag
        B0BSET      FGIE            ; Enable GIE

        B0BSET      FADS            ; Start ADC transformation
```

➢ **Example: ADC interrupt service routine.**

```
        ORG         8               ; Interrupt vector
        JMP         INT_SERVICE
INT_SERVICE:

        …                           ; Push routine to save ACC and PFLAG to buffers.

        B0BTS1      FADCIRQ         ; Check ADCIRQ
        JMP         EXIT_INT        ; ADCIRQ = 0, exit interrupt vector

        B0BCLR      FADCIRQ         ; Reset ADCIRQ
        …                           ; ADC interrupt service routine
        …
EXIT_INT:
        …                           ; Pop routine to load ACC and PFLAG from buffers.

        RETI                        ; Exit interrupt vector
```

6.10 COMPARATOR INTERRUPT OPERATION (CMP0~CMP2)

Sonix provides 3 sets comparator with interrupt function in the micro-controller. The comparator interrupt trigger edge direction is controlled by comparator register. CM0G of CM0M is control comparator 0 interrupt trigger edge direction. CM1G of CM1M is control comparator 1 interrupt trigger edge direction. CM2G of CM2M is control comparator 2 interrupt trigger edge direction. When the comparator output status transition occurs, the comparator interrupt request flag will be set to "1" no matter the comparator interrupt control bit status. The comparator interrupt flag doesn't active only when comparator control bit is disabled. When comparator interrupt control bit is enabled and comparator interrupt edge trigger is occurring, the program counter will jump to the interrupt vector (ORG 8) and execute interrupt service routine.

09CH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CM0M	CM0EN	CM0OEN	CM0OUT	CM0SF	CM0G	-	-	-
Read/Write	R/W	R/W	R/W	R/W	R/W	-	-	-
After Reset	0	0	0	0	0	-	-	-

Bit 3 **CM0G:** Comparator 0 interrupt trigger direction control bit.
0 = Falling edge trigger. Comparator output status is from high to low as CM0P < CM0N.
1 = Rising edge trigger. Comparator output status is from low to high as CM0P > CM0N.

09DH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CM1M	CM1EN	CM1OEN	CM1OUT	CM1SF	CM1G	CM1RS2	CM1RS1	CM1RS0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After Reset	0	0	0	0	0	0	0	0

Bit 3 **CM1G:** Comparator 1 output trigger direction control bit.
0 = Falling edge trigger. Comparator output status is from high to low as CM1P < CM1N.
1 = Rising edge trigger. Comparator output status is from low to high as CM1P > CM1N.

09EH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CM2M	CM2EN	CM2OEN	CM2OUT	CM2SF	CM2G	CM2RS2	CM2RS1	CM2RS0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After Reset	0	0	0	0	0	0	0	0

Bit 3 **CM2G:** Comparator 2 output trigger direction control bit.
0 = Falling edge trigger. Comparator output status is from high to low as CM2P < CM2N.
1 = Rising edge trigger. Comparator output status is from low to high as CM2P > CM2N.

➢ **Example: Setup comparator 0 interrupt request and falling edge trigger.**

```
        MOV     A, #00H
        B0MOV   CM0M, A         ; Set comparator 0 interrupt trigger as bi-direction edge.

        B0BSET  FCM0IEN         ; Enable comparator 0 interrupt service
        B0BCLR  FCM0IRQ         ; Clear comparator 0 interrupt request flag
        B0BSET  FCM0EN          ; Enable comparator 0.
        B0BSET  FGIE            ; Enable GIE
```

➢ **Example: Comparator 0 interrupt service routine.**

```
        ORG     8               ; Interrupt vector
        JMP     INT_SERVICE
INT_SERVICE:
        …                       ; Push routine to save ACC and PFLAG to buffers.

        B0BTS1  FCM0IRQ         ; Check CM0IRQ
        JMP     EXIT_INT        ; CM0IRQ = 0, exit interrupt vector

        B0BCLR  FCM0IRQ         ; Reset CM0IRQ
        …                       ; Comparator 0 interrupt service routine
EXIT_INT:
        …                       ; Pop routine to load ACC and PFLAG from buffers.
        RETI                    ; Exit interrupt vector
```

6.11 MULTI-INTERRUPT OPERATION

Under certain condition, the software designer uses more than one interrupt requests. Processing multi-interrupt request requires setting the priority of the interrupt requests. The IRQ flags of interrupts are controlled by the interrupt event. Nevertheless, the IRQ flag "1" doesn't mean the system will execute the interrupt vector. In addition, which means the IRQ flags can be set "1" by the events without enable the interrupt. Once the event occurs, the IRQ will be logic "1". The IRQ and its trigger event relationship is as the below table.

Interrupt Name	*Trigger Event Description*
P00IRQ	P0.0 trigger controlled by PEDGE
T0IRQ	T0C overflow
TC0IRQ	TC0C overflow
ADCIRQ	ADC converting end.
CM0IRQ	Comparator 0 output level transition.
CM1IRQ	Comparator 1 output level transition.
CM2IRQ	Comparator 2 output level transition.

For multi-interrupt conditions, two things need to be taking care of. One is to set the priority for these interrupt requests. Two is using IEN and IRQ flags to decide which interrupt to be executed. Users have to check interrupt control bit and interrupt request flag in interrupt routine.

➢ **Example: Check the interrupt request under multi-interrupt operation**

```
                ORG         8               ; Interrupt vector
                JMP         INT_SERVICE
INT_SERVICE:
                …                           ; Push routine to save ACC and PFLAG to buffers.
INTP00CHK:                                  ; Check INT0 interrupt request
                B0BTS1      FP00IEN         ; Check P00IEN
                JMP         INTT0CHK        ; Jump check to next interrupt
                B0BTS0      FP00IRQ         ; Check P00IRQ
                JMP         INTP00
INTT0CHK:                                   ; Check T0 interrupt request
                B0BTS1      FT0IEN          ; Check T0IEN
                JMP         INTTC0CHK       ; Jump check to next interrupt
                B0BTS0      FT0IRQ          ; Check T0IRQ
                JMP         INTT0           ; Jump to T0 interrupt service routine
INTTC0CHK:                                  ; Check TC0 interrupt request
                B0BTS1      FTC0IEN         ; Check TC0IEN
                JMP         INTADCHK        ; Jump check to next interrupt
                B0BTS0      FTC0IRQ         ; Check TC0IRQ
                JMP         INTTC0          ; Jump to TC0 interrupt service routine
INTADCHK:                                   ; Check ADC interrupt request
                B0BTS1      FADCIEN         ; Check ADCIEN
                JMP         …               ; Jump check to next interrupt
                B0BTS0      FADCIRQ         ; Check ADCIRQ
                JMP         INTADC          ; Jump to ADC interrupt service routine
                …
                …
INT_EXIT:
                …                           ; Pop routine to load ACC and PFLAG from buffers.

                RETI                        ; Exit interrupt vector
```

7 I/O PORT

7.1 OVERVIEW

The micro-controller builds in 22 pin I/O. Most of the I/O pins are mixed with analog pins and special function pins. The I/O shared pin list is as following.

I/O Pin		Shared Pin		Shared Pin Control Condition
Name	Type	Name	Type	
P0.0	I/O	INT0	DC	P00IEN=1
P0.1	O	PWM0	DC	PWM0OUT=1.
P0.2	I/O	CM0P	AC	CM0EN=1
P0.3	I/O	CM0N	AC	CM0EN=1
P0.4	I	RST	DC	Reset_Pin code option = Reset
		VPP	HV	OTP Programming
P0.5	I/O	XOUT	AC	High_CLK code option = 32K, 4M, 12M
		BZ	DC	BZEN=1
P0.6	I/O	XIN	AC	High_CLK code option = RC, 32K, 4M, 12M
P1.0	I/O	OPN	AC	OPEN=1
P1.1	I/O	OPP	AC	OPEN=1
P1.2	I/O	OPO	AC	OPEN=1
P1.3	I/O	CM2N	AC	CM2EN=1
P1.4	I/O	CM2P	AC	CM2EN=1, CM2RS[2:0]=000b
P1.5	I/O	CM1N	AC	CM1EN=1
P1.6	I/O	CM1P	AC	CM1EN=1, CM1RS[2:0]=000b
P4.0	I/O	AIN0	AC	ADENB=1, GCHS=1, CHS[2:0] = 000b
		AVREFH	AC	ADENB=1, AVREFH=1
P4[7:1]	I/O	AIN[7:1]	AC	ADENB=1, GCHS=1, CHS[2:0] = 001b~111b

*** DC: Digital Characteristic. AC: Analog Characteristic. HV: High Voltage Characteristic.**

7.2 I/O PORT MODE

The port direction is programmed by PnM register. When the bit of PnM register is “0”, the pin is input mode. When the bit of PnM register is “1”, the pin is output mode.

0B8H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0M	-	P06M	P05M	-	P03M	P02M	-	P00M
Read/Write	-	R/W	R/W	-	R/W	R/W	-	R/W
After reset	-	0	0	-	0	0	-	0

0C1H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1M	-	P16M	P15M	P14M	P13M	P12M	P11M	P10M
Read/Write	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	-	0	0	0	0	0	0	0

0C4H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P4M	P47M	P46M	P45M	P44M	P43M	P42M	P41M	P40M
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit[7:0] **PnM[7:0]:** Pn mode control bits. (n = 0~4).
0 = Pn is input mode.
1 = Pn is output mode.

✸ ***Note:***
1. ***Users can program them by bit control instructions (B0BSET, B0BCLR).***
2. ***P0.4 input pin only, and the P0M.4 is undefined***

➢ **Example: I/O mode selecting**

```
CLR     P0M             ; Set all ports to be input mode.
CLR     P4M

MOV     A, #0FFH        ; Set all ports to be output mode.
B0MOV   P0M, A
B0MOV   P4M,A

B0BCLR  P4M.0           ; Set P4.0 to be input mode.

B0BSET  P4M.0           ; Set P4.0 to be output mode.
```

7.3 I/O PULL UP REGISTER

The I/O pins build in internal pull-up resistors and only support I/O input mode. The port internal pull-up resistor is programmed by PnUR register. When the bit of PnUR register is "0", the I/O pin's pull-up is disabled. When the bit of PnUR register is "1", the I/O pin's pull-up is enabled.

0E0H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0UR	-	P06R	P05R	-	P03R	P02R	-	P00R
Read/Write	-	W	W	-	W	W	-	W
After reset	-	0	0	-	0	0	-	0

0E1H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1UR	-	P16R	P15R	P14R	P14R	P12R	P11R	P10R
Read/Write	-	W	W	W	W	W	W	W
After reset	-	0	0	0	0	0	0	0

0E4H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P4UR	P47R	P46R	P45R	P44R	P43R	P42R	P41R	P40R
Read/Write	W	W	W	W	W	W	W	W
After reset	0	0	0	0	0	0	0	0

✸ ***Note:P0.4 is input only pin and without pull-up resister. The P0UR.4 is undefined.***

➢ **Example: I/O Pull up Register**

```
MOV     A, #0FFH        ; Enable Port0, 4 Pull-up register,
B0MOV   P0UR, A         ;
B0MOV   P4UR,A
```

7.4 I/O PORT DATA REGISTER

0D0H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0	-	P06	P05	P04	P03	P02	P01	P00
Read/Write	-	R/W	R/W	R	R/W	R/W	W	R/W
After reset	-	0	0	0	0	0	0	0

0D1H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1	-	P16	P15	P14	P13	P12	P11	P10
Read/Write	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	-	0	0	0	0	0	0	0

0D4H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P4	P47	P46	P45	P44	P43	P42	P41	P40
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

✸ ***Note:***

1. ***The P04 keeps "1" when external reset enable by code option.***
2. ***If set one bit of P0 register (P0.n bit), recommend using "MOV" or "B0MOV" instructions to control the bit, not use "read & modify write" type instructions (e.g. bset, bclr, b0bset, b0bclr…), or the write only type bit (P0.1) is modified after executing instruction.***

➢ **Example: Read data from input port.**

```
B0MOV   A, P0       ; Read data from Port 0
B0MOV   A, P4       ; Read data from Port 4
```

➢ **Example: Write data to output port.**

```
MOV     A, #0FFH    ; Write data FFH to all Port.
B0MOV   P0, A
B0MOV   P4, A
```

➢ **Example: Write one bit data to output port.**

```
B0BSET  P4.0        ; Set P4.0 to be "1".
B0BCLR  P4.0        ; Set P4.0 to be "0".
```

7.5 PORT 4 ADC SHARE PIN

The Port 4 is shared with ADC input function and no Schmitt trigger structure. Only one pin of port 4 can be configured as ADC input in the same time by ADM register. The other pins of port 4 are digital I/O pins. Connect an analog signal to COMS digital input pin, especially the analog signal level is about 1/2 VDD will cause extra current leakage. In the power down mode, the above leakage current will be a big problem. Unfortunately, if users connect more than one analog input signal to port 4 will encounter above current leakage situation. P4CON is Port4 Configuration register. Write "1" into P4CON.n will configure related port 4 pin as pure analog input pin to avoid current leakage.

0AEH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P4CON	P4CON7	P4CON6	P4CON5	P4CON4	P4CON3	P4CON2	P4CON1	P4CON0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit[4:0] **P4CON[7:0]:** P4.n configuration control bits.
0 = P4.n can be an analog input (ADC input) or digital I/O pins.
1 = P4.n is pure analog input, can't be a digital I/O pin.

✸ ***Note: When Port 4.n is general I/O port not ADC channel, P4CON.n must set to "0" or the Port 4.n digital I/O signal would be isolated.***

Port 4 ADC analog input is controlled by GCHS and CHSn bits of ADM register. If GCHS = 0, P4.n is general purpose bi-direction I/O port. If GCHS = 1, P4.n pointed by CHSn is ADC analog signal input pin.

0B1H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADM	ADENB	ADS	EOC	GCHS	AVREFH	CHS2	CHS1	CHS0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit 4 **GCHS:** Global channel select bit.
0 = Disable AIN channel.
1 = Enable AIN channel.

Bit 3 **AVREFH:** ADC external high reference voltage input pin control bit.
0 = ADC high reference voltage is from internal Vdd. P4.0 is GPIO or AIN0 pin.
1 = Enable ADC external high reference voltage input pin from P4.0.

Bit[2:0] **CHS[2:0]:** ADC input channels select bit.
000 = AIN0, 001 = AIN1, 010 = AIN2, 011 = AIN3, 100 = AIN4, 101 = AIN5, 110 = AIN6, 111 = AIN7.

✸ ***Note: For P4.n general purpose I/O function, users should make sure of P4.n's ADC channel is disabled, or P4.n is automatically set as ADC analog input when GCHS = 1 and CHS[2:0] point to P4.n.***

➢ **Example: Set P4.1 to be general purpose input mode. P4CON.1 must be set as "0".**

```
; Check GCHS and CHS[2:0] status.
        B0BCLR      FGCHS       ;If CHS[2:0] point to P4.1 (CHS[2:0] = 001B), set GCHS=0
                                ;If CHS[2:0] don't point to P4.1 (CHS[2:0] ≠ 001B), don't
                                care GCHS status.

; Clear P4CON.
        B0BCLR      P4CON.1     ; Enable P4.1 digital function.

; Enable P4.1 input mode.
        B0BCLR      P4M.1       ; Set P4.1 as input mode.
```

➢ **Example: Set P4.1 to be general purpose output. P4CON.1 must be set as "0".**

```
; Check GCHS and CHS[2:0] status.
        B0BCLR      FGCHS       ;If CHS[2:0] point to P4.1 (CHS[2:0] = 001B), set GCHS=0.
                                ;If CHS[2:0] don't point to P4.1 (CHS[2:0] ≠ 001B), don't
                                care GCHS status.

; Clear P4CON.
        B0BCLR      P4CON.1     ; Enable P4.1 digital function.

; Set P4.1 output buffer to avoid glitch.
        B0BSET      P4.1        ; Set P4.1 buffer as "1".
; or
        B0BCLR      P4.1        ; Set P4.1 buffer as "0".

; Enable P4.1 output mode.
        B0BSET      P4M.1       ; Set P4.1 as input mode.
```

P4.0 is shared with general purpose I/O, ADC input (AIN0) and ADC external high reference voltage input. AVREFH flag of ADM register is external ADC high reference voltage input control bit. If AVREFH is enabled, P4.0 general purpose I/O and ADC analog input (AIN0) functions are disabled. P4.0 pin is connected to ADC high reference voltage directly.

✸ ***Note: For P4.0 general purpose I/O and AIN0 functions, AVREFH must be set as "0".***

➢ **Example: Set P4.0 to be general purpose input mode. AVREFH and P4CON.0 bits must be set as "0".**

```
; Check AVREFH status.
        B0BTS0      FAVREFH     ; Check AVREFH = 0.
        B0BCLR      FAVREFH     ; AVREFH = 1, clear it to disable external ADC high
                                reference input.
                                ; AVREFH = 0, execute next routine.

; Check GCHS and CHS[2:0] status.
        B0BCLR      FGCHS       ;If CHS[2:0] point to P4.0 (CHS[2:0] = 000B), set GCHS=0
                                ;If CHS[2:0] don't point to P4.0 (CHS[2:0] ≠ 000B), don't
                                care GCHS status.

; Clear P4CON.
        B0BCLR      P4CON.0     ; Enable P4.0 digital function.

; Enable P4.0 input mode.
        B0BCLR      P4M.0       ; Set P4.0 as input mode.
```

➢ **Example: Set P4.0 to be general purpose output. EVHENB and P4CON.0 bits must be set as "0".**

```
; Check AVREFH status.
        B0BTS0      FAVREFH     ; Check AVREFH = 0.
        B0BCLR      FAVREFH     ; AVREFH = 1, clear it to disable external ADC high reference input.
                                ; AVREFH = 0, execute next routine.

; Check GCHS and CHS[2:0] status.
        B0BCLR      FGCHS       ;If CHS[2:0] point to P4.0 (CHS[2:0] = 000B), set GCHS=0
                                ;If CHS[2:0] don't point to P4.0 (CHS[2:0] ≠ 000B), don't care GCHS status.

; Clear P4CON.
        B0BCLR      P4CON.0     ; Enable P4.0 digital function.

; Set P4.0 output buffer to avoid glitch.
        B0BSET      P4.0        ; Set P4.0 buffer as "1".
; or
        B0BCLR      P4.0        ; Set P4.0 buffer as "0".

; Enable P4.0 output mode.
        B0BSET      P4M.0       ; Set P4.0 as input mode.
```

8 TIMERS

8.1 WATCHDOG TIMER

The watchdog timer (WDT) is a binary up counter designed for monitoring program execution. If the program goes into the unknown status by noise interference, WDT overflow signal raises and resets MCU. Watchdog clock controlled by code option and the clock source is internal low-speed oscillator.

Watchdog overflow time = 8192 / Internal Low-Speed oscillator (sec).

VDD	*Internal Low RC Freq.*	*Watchdog Overflow Time*
3V	16KHz	512ms
5V	32KHz	256ms

The watchdog timer has three operating options controlled "WatchDog" code option.

- **Disable:** Disable watchdog timer function.
- **Enable:** Enable watchdog timer function. Watchdog timer actives in normal mode and slow mode. In power down mode and green mode, the watchdog timer stops.
- **Always_On:** Enable watchdog timer function. The watchdog timer actives and not stop in power down mode and green mode.

In high noisy environment, the "Always_On" option of watchdog operations is the strongly recommendation to make the system reset under error situations and re-start again.

Watchdog clear is controlled by WDTR register. Moving **0x5A** data into WDTR is to reset watchdog timer.

0CCH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTR	WDTR7	WDTR6	WDTR5	WDTR4	WDTR3	WDTR2	WDTR1	WDTR0
Read/Write	W	W	W	W	W	W	W	W
After reset	0	0	0	0	0	0	0	0

➢ **Example: An operation of watchdog timer is as following. To clear the watchdog timer counter in the top of the main routine of the program.**

```
Main:
        MOV     A, #5AH         ; Clear the watchdog timer.
        B0MOV   WDTR, A
        …
        CALL    SUB1
        CALL    SUB2
        …
        JMP     MAIN
```

➢ **Example: Clear watchdog timer by "@RST_WDT" macro of Sonix IDE.**

```
Main:
        @RST_WDT                ; Clear the watchdog timer.
        …
        CALL    SUB1
        CALL    SUB2
        …
        JMP     MAIN
```

Watchdog timer application note is as following.

- Before clearing watchdog timer, check I/O status and check RAM contents can improve system error.
- Don't clear watchdog timer in interrupt vector and interrupt service routine. That can improve main routine fail.
- Clearing watchdog timer program is only at one part of the program. This way is the best structure to enhance the watchdog timer function.

➢ **Example: An operation of watchdog timer is as following. To clear the watchdog timer counter in the top of the main routine of the program.**

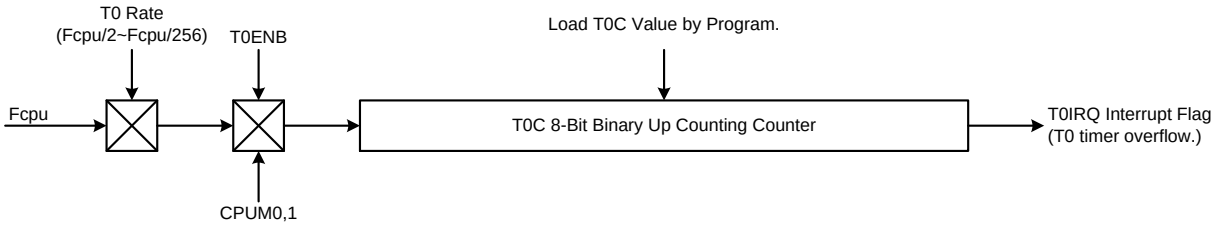
```
Main:
                …                               ; Check I/O.
                …                               ; Check RAM
Err:            JMP $                           ; I/O or RAM error. Program jump here and don't
                                                ; clear watchdog. Wait watchdog timer overflow to reset IC.

Correct:                                        ; I/O and RAM are correct. Clear watchdog timer and
                                                ; execute program.
                MOV         A, #5AH             ; Clear the watchdog timer.
                B0MOV       WDTR, A
                …
                CALL        SUB1
                CALL        SUB2
                …
                …
                …
                JMP         MAIN
```

8.2 T0 8-BIT BASIC TIMER

8.2.1 OVERVIEW

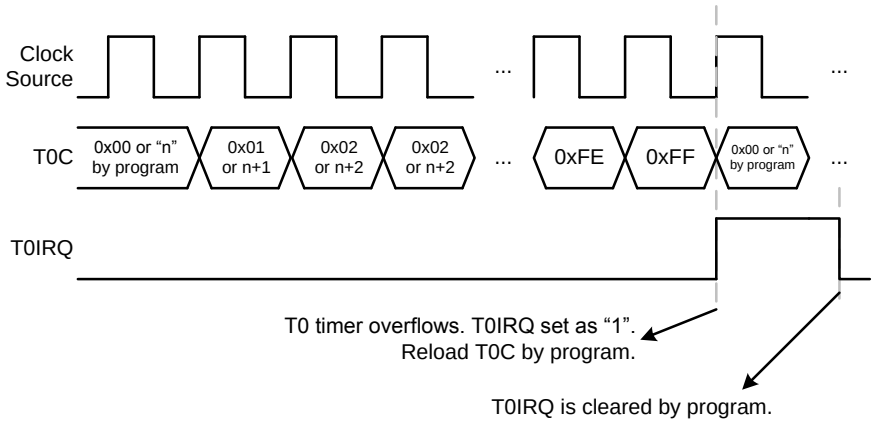
The T0 timer is an 8-bit binary up timer with basic timer function. The basic timer function supports flag indicator (T0IRQ bit) and interrupt operation (interrupt vector). The interval time is programmable through T0M, T0C registers. The T0 builds in green mode wake-up function. When T0 timer overflow occurs under green mode, the system will be waked-up to last operating mode.

- ☞ **8-bit programmable up counting timer:** Generate time-out at specific time intervals based on the selected clock frequency.
- ☞ **Interrupt function:** T0 timer function supports interrupt function. When T0 timer occurs overflow, the T0IRQ actives and the system points program counter to interrupt vector to do interrupt sequence.
- ☞ **Green mode function:** T0 timer keeps running in green mode and wakes up system when T0 timer overflows.



8.2.2 T0 TIMER OPERATION

T0 timer is controlled by T0ENB bit. When T0ENB=0, T0 timer stops. When T0ENB=1, T0 timer starts to count. T0C increases “1” by timer clock source. When T0 overflow event occurs, T0IRQ flag is set as ”1” to indicate overflow and cleared by program. The overflow condition is T0C count from full scale (0xFF) to zero scale (0x00). T0 doesn’t build in double buffer, so load T0C by program when T0 timer overflows to fix the correct interval time. If T0 timer interrupt function is enabled (T0IEN=1), the system will execute interrupt procedure. The interrupt procedure is system program counter points to interrupt vector (ORG 8) and executes interrupt service routine after T0 overflow occurrence. Clear T0IRQ by program is necessary in interrupt procedure. T0 timer can works in normal mode, slow mode and green mode. In green mode, T0 keeps counting, set T0IRQ and wakes up system when T0 timer overflows.



T0 clock source is Fcpu (instruction cycle) through T0rate[2:0] pre-scaler to decide Fcpu/2~Fcpu/256. T0 length is 8-bit (256 steps), and the one count period is each cycle of input clock.

T0rate[2:0]	T0 Clock	T0 Interval Time			
		Fhosc=16MHz, Fcpu=Fhosc/4		Fhosc=16MHz, Fcpu=Fhosc/16	
		max. (ms)	Unit (us)	max. (ms)	Unit (us)
000b	Fcpu/256	16.384	64	65.536	256
001b	Fcpu/128	8.192	32	32.768	128
010b	Fcpu/64	4.096	16	16.384	64
011b	Fcpu/32	2.048	8	8.192	32
100b	Fcpu/16	1.024	4	4.096	16
101b	Fcpu/8	0.512	2	2.048	8
110b	Fcpu/4	0.256	1	1.024	4
111b	Fcpu/2	0.128	0.5	0.512	2

8.2.3 T0M MODE REGISTER

T0M is T0 timer mode control register to configure T0 operating mode including T0 pre-scaler, clock source…These configurations must be setup completely before enabling T0 timer.

0D8H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T0M	T0ENB	T0rate2	T0rate1	T0rate0	-	-	-	-
Read/Write	R/W	R/W	R/W	R/W	-	-	-	-
After reset	0	0	0	0	-	-	-	-

Bit [6:4] **T0RATE[2:0]:** T0 timer clock source select bits.
000 = Fcpu/256, 001 = Fcpu/128, 010 = Fcpu/64, 011 = Fcpu/32, 100 = Fcpu/16, 101 = Fcpu/8, 110 = Fcpu/4,111 = Fcpu/2.

Bit 7 **T0ENB:** T0 counter control bit.
0 = Disable T0 timer.
1 = Enable T0 timer.

8.2.4 T0C COUNTING REGISTER

T0C is T0 8-bit counter. When T0C overflow occurs, the T0IRQ flag is set as “1” and cleared by program. The T0C decides T0 interval time through below equation to calculate a correct value. It is necessary to write the correct value to T0C register, and then enable T0 timer to make sure the fist cycle correct. After one T0 overflow occurs, the T0C register is loaded a correct value by program.

0D9H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T0C	T0C7	T0C6	T0C5	T0C4	T0C3	T0C2	T0C1	T0C0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

The equation of T0C initial value is as following.

T0C initial value = 256 - (T0 interrupt interval time * T0 clock rate)

- **Example: To calculation T0C to obtain 10ms T0 interval time. T0 clock source is Fcpu = 16MHz/16 = 1MHz. Select T0RATE=001 (Fcpu/128).**
  T0 interval time = 10ms. T0 clock rate = 16MHz/16/128

*T0C initial value = 256 - (T0 interval time * input clock)*
*= 256 - (10ms * 16MHz / 16 / 128)*
*= 256 - (10^{-2} * 16MHz / 16 / 128)*
= B2H

8.2.5 T0 TIMER OPERATION EXPLAME

- **T0 TIMER CONFIGURATION:**

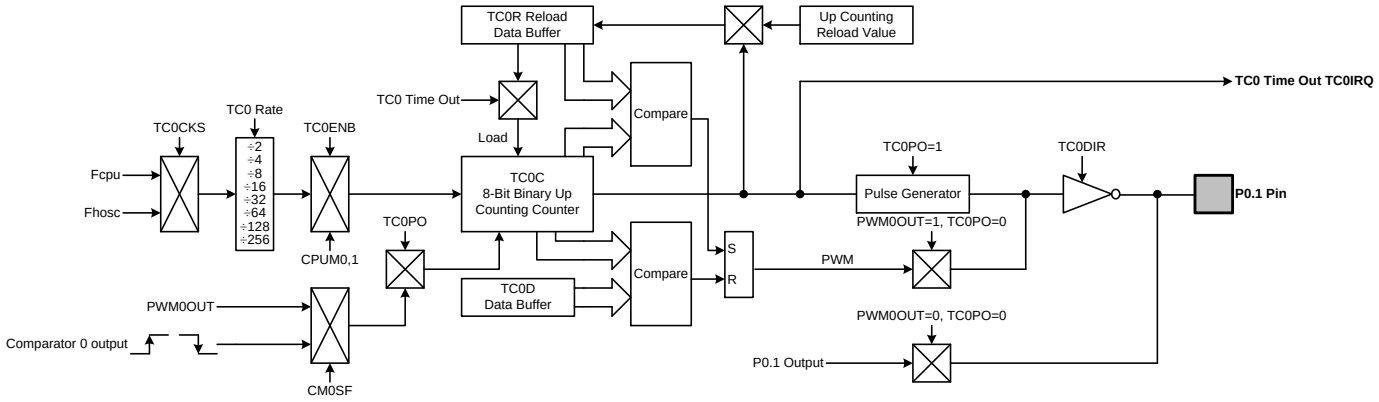
```
; Reset T0 timer.
        CLR     T0M             ; Clear T0M register.

; Set T0 clock source and T0 rate.
        MOV     A, #0nnn00000b
        B0MOV   T0M, A

; Set T0C register for T0 Interval time.
        MOV     A, #value
        B0MOV   T0C, A

; Clear T0IRQ
        B0BCLR  FT0IRQ

; Enable T0 timer and interrupt function.
        B0BSET  FT0IEN          ; Enable T0 interrupt function.
        B0BSET  FT0ENB          ; Enable T0 timer.
```

8.3 TC0 8-BIT TIMER/COUNTER

8.3.1 OVERVIEW

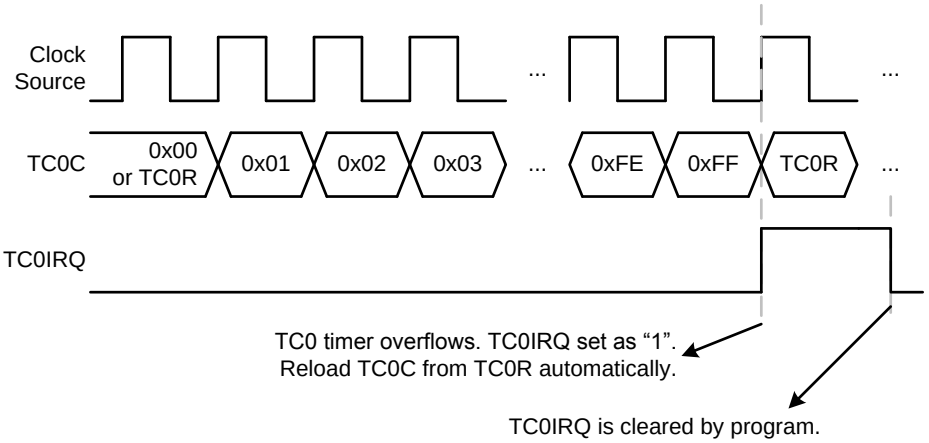
The TC0 timer is an 8-bit binary up timer with basic timer, PWM function and pulse generator. The basic timer function supports flag indicator (TC0IRQ bit) and interrupt operation (interrupt vector). The interval time is programmable through TC0M, TC0C, TC0R registers. TC0 builds in duty/cycle programmable PWM. The PWM cycle and resolution are controlled by TC0 timer clock rate, TC0R and TC0D registers, so the PWM with good flexibility to implement IR carry signal, motor control and brightness adjuster…TC0 timer also builds in pulse generator function. The pulse generator function is one cycle PWM format as start trigger occurrence. The pulse output trigger source has TC0PO control bit and comparator 0 output edge controlled by register. TC0 counter supports auto-reload function which always enabled. When TC0 timer overflow occurs, the TC0C will be reloaded from TC0R automatically. The auto-reload function is always enabled. The TC0 doesn't build in green mode wake-up function. The main purposes of the TC0 timer are as following.

- **8-bit programmable up counting timer:** Generate time-out at specific time intervals based on the selected clock frequency.
- **Interrupt function:** TC0 timer function supports interrupt function. When TC0 timer occurs overflow, the TC0IRQ actives and the system points program counter to interrupt vector to do interrupt sequence.
- **Duty/cycle programmable PWM:** The PWM is duty/cycle programmable controlled by TC0R and TC0D registers.
- **Pulse generator:** The pulse generator function is one cycle PWM format as start trigger occurrence. The pulse output trigger source has TC0PO control bit and comparator 0 output edge controlled by register. When TC0PO = 1, CM0SF = 0, the pulse generator trigger is PWM0OUT bit. When TC0PO = 1, CM0SF = 1, the pulse generator trigger is comparator 0 output edge.
- **Green mode function:** All TC0 functions (timer, PWM, pulse generator) keeps running in green mode, but no wake-up function. Timer IRQ actives as any IRQ trigger occurrence, e.g. timer overflow…



8.3.2 TC0 TIMER OPERATION

TC0 timer is controlled by TC0ENB bit. When TC0ENB=0, TC0 timer stops. When TC0ENB=1, TC0 timer starts to count. Before enabling TC0 timer, setup TC0 timer's configurations to select timer function modes, e.g. basic timer, interrupt function…TC0C increases "1" by timer clock source. When TC0 overflow event occurs, TC0IRQ flag is set as "1" to indicate overflow and cleared by program. The overflow condition is TC0C count from full scale (0xFF) to zero scale (0x00). In difference function modes, TC0C value relates to operation. If TC0C value changing effects operation, the transition of operations would make timer function error. So TC0 builds in double buffer to avoid these situations happen. The double buffer concept is to flash TC0C during TC0 counting, to set the new value to TC0R (reload buffer), and the new value will be loaded from TC0R to TC0C after TC0 overflow occurrence automatically. In the next cycle, the TC0 timer runs under new conditions, and no any transitions occur. The auto-reload function is no any control interface and always actives as TC0 enables. If TC0 timer interrupt function is enabled (TC0IEN=1), the system will execute interrupt procedure. The interrupt procedure is system program counter points to interrupt vector (ORG 0008H) and executes interrupt service routine after TC0 overflow occurrence. Clear TC0IRQ by program is necessary in interrupt procedure. TC0 timer can works in normal mode, slow mode and green mode. But in green mode, TC0 keep counting, set TC0IRQ and outputs PWM, but can't wake-up system.

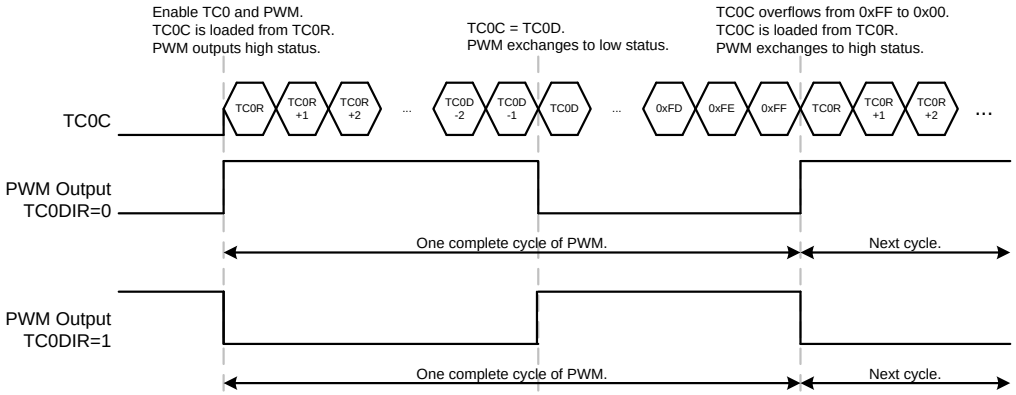


TC0 provides different clock sources to implement different applications and configurations. TC0 clock source includes Fcpu (instruction cycle) and Fhosc (high speed oscillator) controlled by TC0CKS bit. TC0CKS bit selects the clock source is from Fcpu or Fhosc. If TC0CKS=0, TC0 clock source is Fcpu through TC0rate[2:0] pre-scalar to decide Fcpu/2~Fcpu/256. If TC0CKS=1, TC0 clock source is Fhosc through TC0rate[2:0] pre-scalar to decide Fhosc/2~Fhosc/256. TC0 length is 8-bit (256 steps), and the one count period is each cycle of input clock.

TC0CKS	TC0rate[2:0]	TC0 Clock	TC0 Interval Time			
			Fhosc=16MHz, Fcpu=Fhosc/4		Fhosc=4MHz, Fcpu=Fhosc/4	
			max. (ms)	Unit (us)	max. (ms)	Unit (us)
0	000b	Fcpu/256	16.384	64	65.536	256
0	001b	Fcpu/128	8.192	32	32.768	128
0	010b	Fcpu/64	4.096	16	16.384	64
0	011b	Fcpu/32	2.048	8	8.192	32
0	100b	Fcpu/16	1.024	4	4.096	16
0	101b	Fcpu/8	0.512	2	2.048	8
0	110b	Fcpu/4	0.256	1	1.024	4
0	111b	Fcpu/2	0.128	0.5	0.512	2
1	000b	Fhosc/256	4.096	16	16.384	64
1	001b	Fhosc/128	2.048	8	8.192	32
1	010b	Fhosc/64	1.024	4	4.096	16
1	011b	Fhosc/32	0.512	2	2.048	8
1	100b	Fhosc/16	0.256	1	1.024	4
1	101b	Fhosc/8	0.128	0.5	0.512	2
1	110b	Fhosc/4	0.064	0.25	0.256	1
1	111b	Fhosc/2	0.032	0.125	0.128	0.5

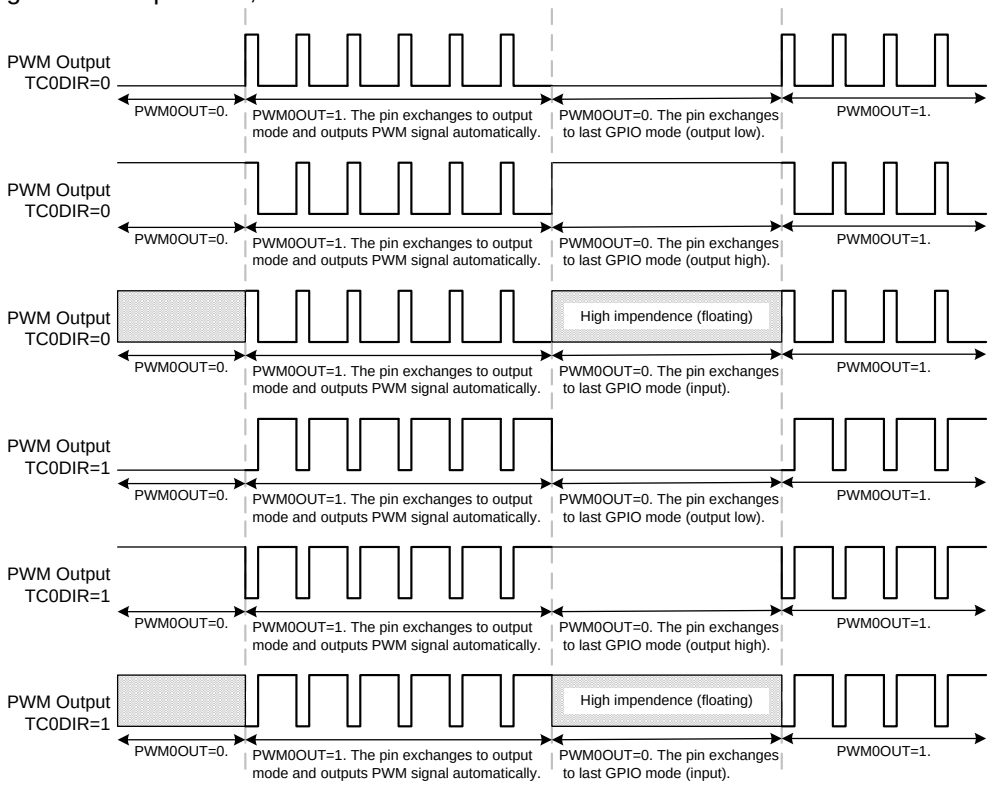
8.3.3 PULSE WIDTH MODULATION (PWM)

TC0 timer builds in PWM function controlled by PWM0OUT bit. PWM output pin is shared with GPIO. When PWM0OUT=1, the PWM function is enabled and GPIO pin is switched from GPIO to PWM output status. When PWM0OUT=0, PWM output pin returns to GPIO last status. PWM signal is generated from the result of TC0C, TC0R and TC0D comparison. When PWM0OUT=1 or TC0C counts from 0xFF to 0x00 (overflow), the PWM outputs high status which is the PWM initial status. TC0C is loaded new data from TC0R register to decide PWM cycle and resolution. TC0C keeps counting, and the system compares TC0C and TC0D. When TC0C=TC0D, the PWM output status exchanges to low. TC0C keeps counting. When TC0 timer overflow occurs, and one cycle of PWM signal finishes. TC0C is reloaded from TC0R automatically, and PWM output status exchanges to high for next cycle. TC0D decides the high duty duration, and TC0R decides the resolution and cycle of PWM. TC0R can't be larger than TC0D, or the PWM signal is error. The PWM output phase can be selected through TC0DIR bit. When TC0DIR = 0, PWM's phase is high pulse and low idle status. When TC0DIR = 1, PWM's phase is low pulse and high idle status.



The resolution of PWM is decided by TC0R. TC0R range is from 0x00~0xFF. If TC0R = 0x00, PWM's resolution is 1/256. If TC0R = 0x80, PWM's resolution is 1/128. TC0D controls the high pulse width of PWM for PWM's duty. When TC0C = TC0D, PWM output exchanges to low status. TC0D must be greater than TC0R, or the PWM signal keeps low status. When PWM outputs, TC0IRQ still actives as TC0 overflows, and TC0 interrupt function actives as TC0IEN = 1. But strongly recommend be careful to use PWM and TC0 timer together, and make sure both functions work well.

The PWM output pin is shared with GPIO and switch to output PWM signal as PWM0OUT=1 automatically. If PWM0OUT bit is cleared to disable PWM, the output pin exchanges to last GPIO mode automatically. It easily to implement carry signal on/off operation, not to control TC0ENB bit.



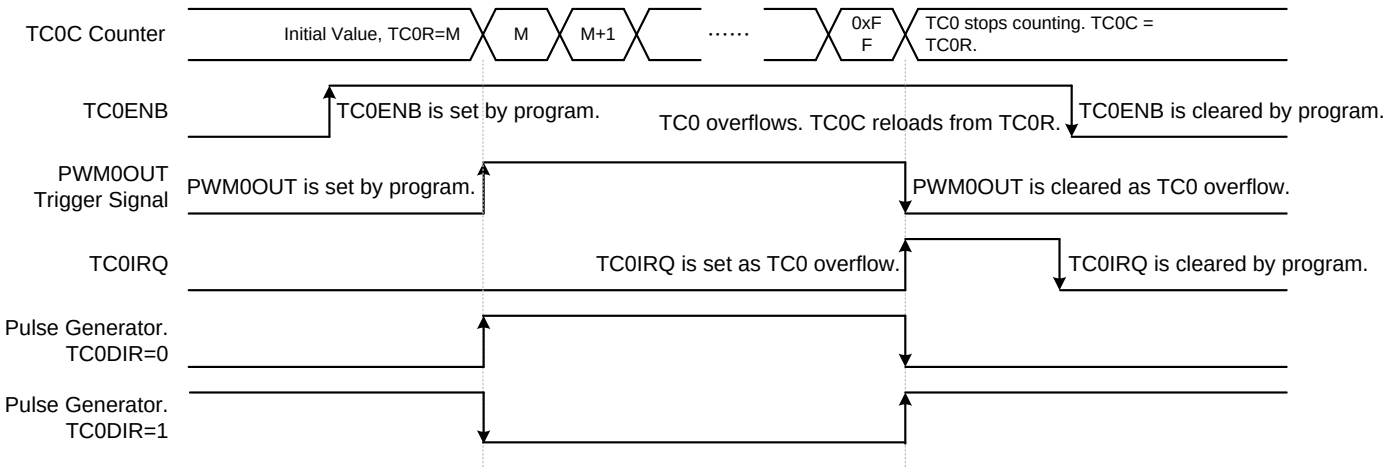
8.3.4 TC0 Pulse Generator Function

TC0 timer builds in pulse generator function. The pulse generator outputs a pulse, and the pulse width is decided by TC0 timer's interval time. The pulse generator is controlled by TC0PO bit. When TC0PO = 0, TC0 is normal timer mode or PWM function mode. When TC0PO = 1, TC0 is pulse generator mode. The pulse generator needs a start trigger signal to control TC0 counter and pulse signal output. When TC0PO is set as "1", TC0 counter keeps stopping, and TC0C/TC0R registers' value is set by program. TC0C value decides the pulse width. When the trigger event occurs, TC0 counter starts to count, and pulse output pin outputs pulse status controlled TC0DIR. When TC0 counter overflows, pulse signal finishes and changes to idle status. The TC0C stops counting and reloads new value through TC0R register. In pulse generator mode, the TC0IRQ is issued as TC0 counter overflow. During pulse generator operating, to change pulse width is through TC0R, not TC0C, or the pulse width would be error.

The pulse output control signal includes two trigger sources, and CM0SF bit controls TC0 pulse generator trigger source. One is PWM0OUT bit (CM0SF=0), and the other is comparator 0 output edge (CM0SF=1). If the trigger source is PWM0OUT bit, set PWM0OUT bit to output pulse signal by program, and PWM0OUT bit is cleared as TC0 counter overflow. To output next pulse is to set PWM0OUT bit by program again.

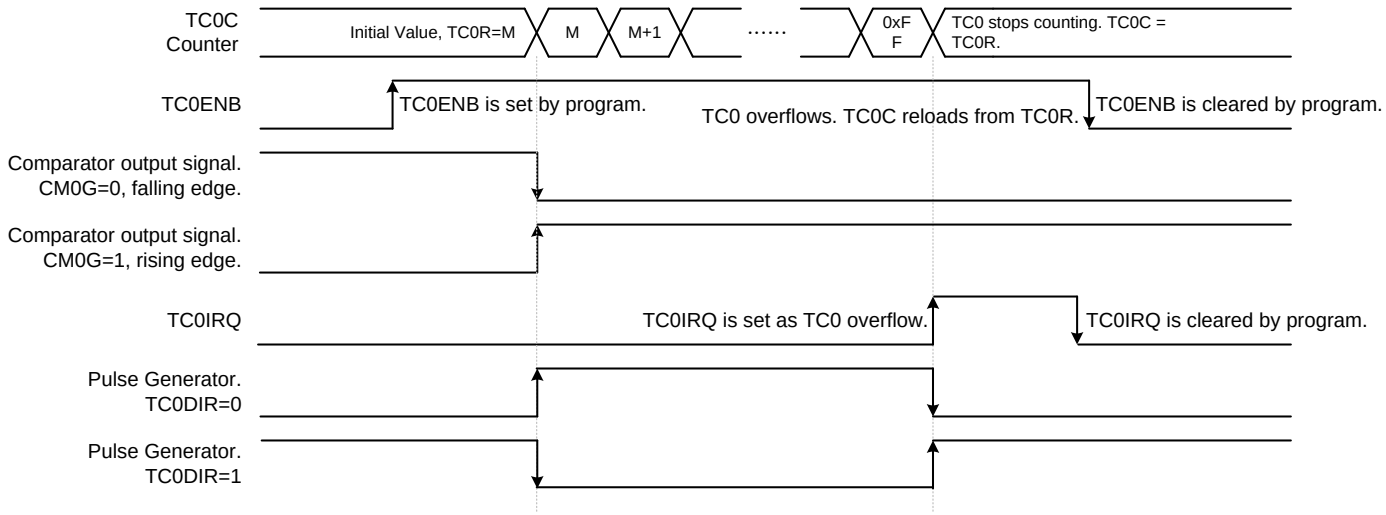
TC0 Rate=Fhosc/2=8MHz @Fhosc=16MHz					
TC0C/TC0R	0x00	0x01	…	0xFE	0xFF
Pulse Width (ns)	31875	31750	…	125	0
TC0 Rate=Fhosc/4=4KHz @Fhosc=16MHz					
TC0C/TC0R	0x00	0x01	…	0xFE	0xFF
Pulse Width (us)	63750	63500	…	250	0
TC0 Rate=Fhosc/256=62.5KHz @Fhosc=16MHz					
TC0C/TC0R	0x00	0x01	…	0xFE	0xFF
Pulse Width (us)	4080	4064	…	16	0
TC0 Rate=Fcpu/2=0.5MHz @Fcpu=Fhosc/16=16MHz/16=1MHz					
TC0C/TC0R	0x00	0x01	…	0xFE	0xFF
Pulse Width (us)	510	508	…	2	0
TC0 Rate=Fcpu/256=3.90625KHz @Fcpu=Fhosc/16=16MHz/16=1MHz					
TC0C/TC0R	0x00	0x01	…	0xFE	0xFF
Pulse Width (us)	65280	65024	…	256	0

- **TC0PO=1, CM0SF=0: TC0ENB must be set as "1". TC0 8-bit binary up counter is controlled by PWM0OUT bit. If PWM0OUT bit is set as "1" by program, TC0 starts to count. If TC0 overflows, TC0 stops counting, PWM0OUT bit is cleared automatically, TC0IRQ is issued, and TC0C reloads new value from TC0R. It is necessary to set PWM0OUT = 1 by program making TC0 counts again.**



If the trigger is comparator 0 output edge (rising edge and falling edge controlled by comparator control register's CM0G bit), pulse starts to output as trigger edge condition occurrence. When TC0 overflows, pulse output pin returns to idle status.

- **TC0PO=1, CM0SF=1: TC0ENB must be set as "1". TC0 8-bit binary up counter is controlled by comparator 0 output edge condition. The trigger edge can be selected through CM0G bit. If comparator output edge occurs, TC0 starts to count. If TC0 overflows, TC0 stops counting, TC0IRQ is issued, and TC0C reloads new value from TC0R.**



8.3.5 TC0M MODE REGISTER

TC0M is TC0 timer mode control register to configure TC0 operating mode including TC0 pre-scalar, clock source, PWM function…These configurations must be setup completely before enabling TC0 timer.

0B4H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC0M	TC0ENB	TC0rate2	TC0rate1	TC0rate0	TC0CKS	TC0DIR	TC0PO	PWM0OUT
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit 0 **PWM0OUT:** PWM0 output and pulse generator output control bit.
TC0PO = 0:
0 = Disable PWM0 output function, and P0.1 is GPIO mode.
1 = Enable PWM0 output function, and PWM0 signal outputs through P0.1 pin.
TC0PO = 1:
0 = Stop pulse output, or the end of pulse output cleared automatically.
1 = Enable pulse output.

Bit 1 **TC0PO:** TC0 pulse output function control bit.
0 = Disable.
1 = Enable TC0 pulse output function through P0.1 pin. \

Bit 2 **TC0DIR:** PWM0 and Pulse generator output phase select bit.
0 = Normal phase. High pulse and low idle status.
1 = Inverse phase. Low pulse and high idle status.

Bit 3 **TC0CKS:** TC0 clock source select bit.
0 = TC0 clock source is internal system clock (Fcpu).
1 = TC0 clock source is high clock source (Fhosc).

Bit [6:4] **TC0RATE [2:0]:** TC0 timer clock source select bits.
TC0CKS = 0:
000 = Fcpu/256, 001 = Fcpu/128, 010 = Fcpu/64, 011 = Fcpu/32, 100 = Fcpu/16, 101 = Fcpu/8, 110 = Fcpu/4, 111 = Fcpu/2.
TC0CKS = 1:
000 = Fhosc/256, 001 = Fhosc /128, 010 = Fhosc /64, 011 = Fhosc /32, 100 = Fhosc /16, 101 = Fhosc /8, 110 = Fhosc /4, 111 = Fhosc /2.

Bit 7 **TC0ENB:** TC0 timer control bit.
0 = Disable.
1 = Enable.

8.3.6 TC0C COUNTING REGISTER

TC0C is TC0 8-bit counter. When TC0C overflow occurs, the TC0IRQ flag is set as “1” and cleared by program. The TC0C decides TC0 interval time through below equation to calculate a correct value. It is necessary to write the correct value to TC0C register and TC0R register first time, and then enable TC0 timer to make sure the fist cycle correct. After one TC0 overflow occurs, the TC0C register is loaded a correct value from TC0R register automatically, not program.

0B5H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC0C	TC0C7	TC0C6	TC0C5	TC0C4	TC0C3	TC0C2	TC0C1	TC0C0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

The equation of TC0C initial value is as following.

TC0C initial value = 256 - (TC0 interrupt interval time * TC0 clock rate)

8.3.7 TC0R AUTO-RELOAD REGISTER

TC0 timer builds in auto-reload function, and TC0R register stores reload data. When TC0C overflow occurs, TC0C register is loaded data from TC0R register automatically. Under TC0 timer counting status, to modify TC0 interval time is to modify TC0R register, not TC0C register. New TC0C data of TC0 interval time will be updated after TC0 timer overflow occurrence, TC0R loads new value to TC0C register. But at the first time to setup TC0M, TC0C and TC0R must be set the same value before enabling TC0 timer. TC0 is double buffer design. If new TC0R value is set by program, the new value is stored in 1st buffer. Until TC0 overflow occurs, the new value moves to real TC0R buffer. This way can avoid any transitional condition to affect the correctness of TC0 interval time and PWM output signal.

0B6H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC0R	TC0R7	TC0R6	TC0R5	TC0R4	TC0R3	TC0R2	TC0R1	TC0R0
Read/Write	W	W	W	W	W	W	W	W
After reset	0	0	0	0	0	0	0	0

The equation of TC0R initial value is as following.

TC0R initial value = 256 - (TC0 interrupt interval time * TC0 clock rate)

- **Example: To calculation TC0C and TC0R value to obtain 10ms TC0 interval time. TC0 clock source is Fcpu = 16MHz/16 = 1MHz. Select TC0RATE=000 (Fcpu/128).**
  TC0 interval time = 10ms. TC0 clock rate = 16MHz/16/128

  *TC0C/TC0R initial value = 256 - (TC0 interval time * input clock)*
  *= 256 - (10ms * 16MHz / 16 / 128)*
  *= 256 - (10^{-2} * 16 * 10^{6} / 16 / 128)*
  = B2H

8.3.8 TC0D PWM DUTY REGISTER

TC0D register's purpose is to decide PWM duty. In PWM mode, TC0R controls PWM's cycle, and TC0D controls the duty of PWM. The operation is base on timer counter value. When TC0C = TC0D, the PWM high duty finished and exchange to low level. It is easy to configure TC0D to choose the right PWM's duty for application.

0B7H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC0D	TC0D7	TC0D6	TC0D5	TC0D4	TC0D3	TC0D2	TC0D1	TC0D0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After Reset	0	0	0	0	0	0	0	0

The equation of TC0D initial value is as following.

TC0D initial value = TC0R + (PWM high pulse width period / TC0 clock rate)

- **Example: To calculate TC0D value to obtain 1/3 duty PWM signal. The TC0 clock source is Fcpu = 16MHz/16= 1MHz. Select TC0RATE=000 (Fcpu/128). TC0R = B2H. TC0 interval time = 10ms. So the PWM cycle is 100Hz. In 1/3 duty condition, the high pulse width is about 3.33ms.**

  TC0D initial value = B2H + (PWM high pulse width period / TC0 clock rate)
  *= B2H + (3.33ms * 16MHz / 16 / 128)*
  = B2H + 1AH
  = CCH

8.3.9 TC0 TIMER OPERATION EXPLAME

- **TC0 TIMER CONFIGURATION:**

```
; Reset TC0 timer.
        CLR     TC0M            ; Clear TC0M register.

; Set TC0 rate.
        MOV     A, #0nnn0000b
        B0MOV   TC0M, A

; Set TC0 clock source.
        B0BCLR  FTC0CKS         ; TC0 clock source is Fcpu.
; or
        B0BSET  FTC0CKS         ; TC0 clock source is Fhosc.

; Set TC0C and TC0R register for TC0 Interval time.
        MOV     A, #value       ; TC0C must be equal to TC0R.
        B0MOV   TC0C, A
        B0MOV   TC0R, A

; Clear TC0IRQ
        B0BCLR  FTC0IRQ

; Enable TC0 timer and interrupt function.
        B0BSET  FTC0IEN         ; Enable TC0 interrupt function.
        B0BSET  FTC0ENB         ; Enable TC0 timer.
```

- **TC0 PWM CONFIGURATION:**

```
; Reset TC0 timer.
        CLR     TC0M            ; Clear TC0M register.

; Set TC0 rate.
        MOV     A, #0nnn0000b
        B0MOV   TC0M, A

; Set TC0 clock source.
        B0BCLR  FTC0CKS         ; TC0 clock source is Fcpu.
; or
        B0BSET  FTC0CKS         ; TC0 clock source is Fhosc.

; Set TC0C and TC0R register for PWM cycle.
        MOV     A, #value1      ; TC0C must be equal to TC0R.
        B0MOV   TC0C, A
        B0MOV   TC0R, A

; Set TC0D register for PWM duty.
        MOV     A, #value2      ; TC0D must be greater than TC0R.
        B0MOV   TC0D, A

; Set PWM output phase.
        B0BCLR  FTC0DIR         ; High pulse and low idle status.
; or
        B0BSET  FTC0DIR         ; Low pulse and high idle status.

; Enable PWM and TC0 timer.
        B0BSET  FPWM0OUT        ; Enable PWM.
        B0BSET  FTC0ENB         ; Enable TC0 timer.
```

- **TC0 PULSE GENERATOR CONFIGURATION:**

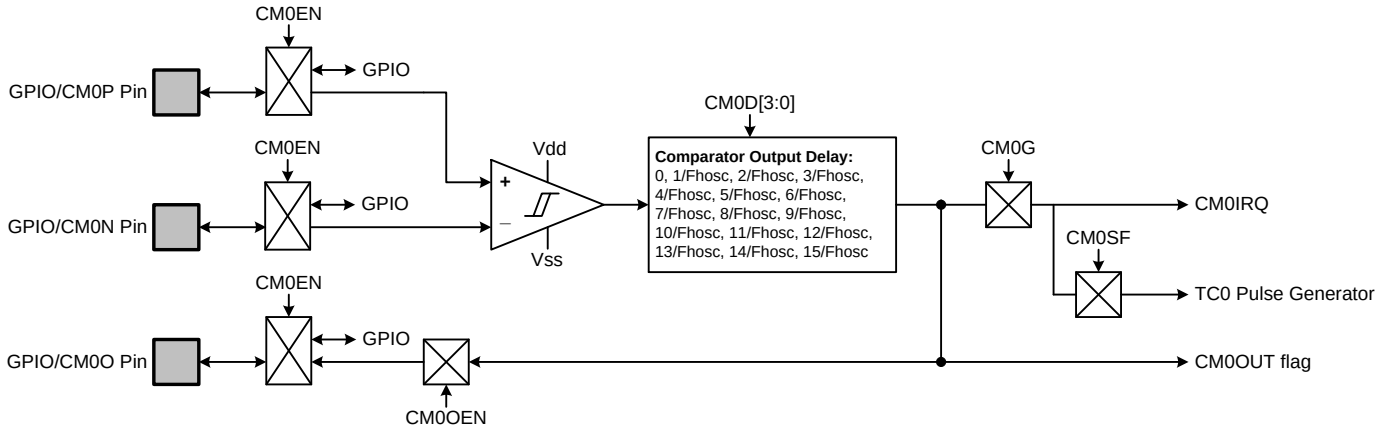
```
; Reset TC0 timer.
        CLR     TC0M            ; Clear TC0M register.

; Set TC0 rate.
        MOV     A, #0nnn0000b
        B0MOV   TC0M, A

; Set TC0 clock source.
        B0BCLR  FTC0CKS         ; TC0 clock source is Fcpu.
; or
        B0BSET  FTC0CKS         ; TC0 clock source is Fhosc.

; Set TC0C and TC0R register for pulse width.
        MOV     A, #value1      ; TC0C must be equal to TC0R.
        B0MOV   TC0C, A
        B0MOV   TC0R, A

; Set pulse output phase.
        B0BCLR  FTC0DIR         ; High pulse and low idle status.
; or
        B0BSET  FTC0DIR         ; Low pulse and high idle status.

; Set pulse output trigger source.
        B0BCLR  FCM0SF          ; Pulse output trigger source is PWM0OUT bit.
; or
        B0BSET  FCM0SF          ; Pulse output trigger source is comparator 0 output edge.

; Enable pulse output and TC0 timer.
        B0BSET  FTC0PO          ; Enable pulse output function.
        B0BSET  FTC0ENB         ; Enable TC0 timer.
```

9 ANALOG COMPARAOTR 0

9.1 OVERVIEW

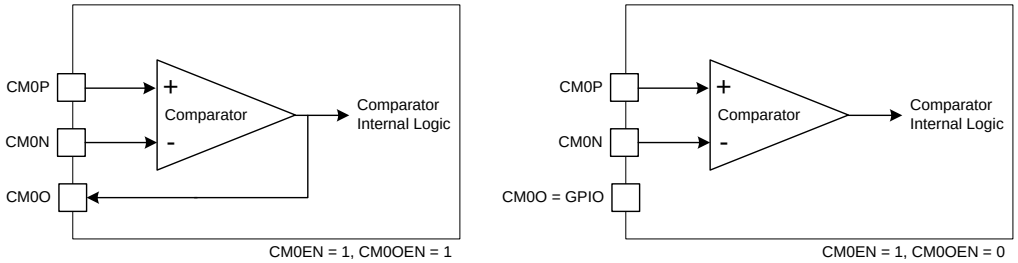
The micro-controller builds in one comparator with TC0 pulse generator trigger function. The comparator has normal comparator mode and TC0 pulse output trigger source. The comparator is not Rail-to-Rail structure. That means the input voltage is not real from Vdd~Vss (Reference to “Electrical characteristics” chapter). When the positive input voltage is greater than the negative input voltage, the comparator output is high. When the positive input voltage is smaller than the negative input voltage, the comparator output is low. The main purposes of comparator 0 are as following.

- **Normal comparator function:** General comparator mode compares the two tensions of positive input terminal and negative input terminal.
- **Interrupt function:** Comparator 0 supports interrupt function. When comparator 0 output edge direction equals to edge selection, the CM0IRQ actives and the system points program counter to interrupt vector to do interrupt sequence.
- **TC0 pulse generator trigger source:** Comparator 0 can be TC0 pulse generator trigger source controlled by CM0SF bit. When TC0PO = 1 and CM0SF = 1, comparator 0 output status triggers TC0 pulse generator to outputs pulse signal.
- **Green mode function:** Comparator 0 still actives in green mode, but no wake-up function. CM0IRQ can be latched as trigger event occurrence until system wakes up. After system wakes up, the comparator 0 interrupt service routine is executed by program.



9.2 NORMAL COMPARATOR MODE

Comparator pins are shared with GPIO controlled by CM0EN bit. When CM0EN=1, CM0N pin is enabled connected to comparator negative terminal, and CM0P pin is enabled connected to comparator positive terminal. CM0OEN controls comparator output connected to GPIO or not. When CM0OEN=1, comparator output terminal is connected to CM0O pin and isolate GPIO function. When CM0OEN=0, comparator output status can be read through CM0OUT flag and CM0O pin is GPIO mode.

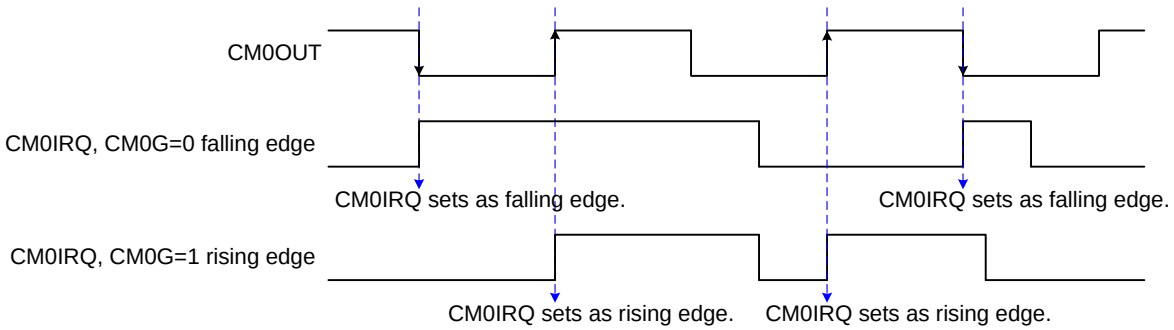


✸ ***Note: The comparator enable condition is fixed CM0EN=1, or the comparator pins are GPIO mode and comparator is disabled.***

The CM0OUT and CM0IRQ bits indicate the comparator result. The CM0OUT shows the comparator result immediately, but the CM0IRQ only indicates the event of the comparator result. The event condition is controlled by register and includes rising edge (CM0OUT changes from low to high) and falling edge (CM0OUT changes from high to low) controlled by CM0G bit. When CM0G = 0, the comparator 0 interrupt trigger direction is falling edge. When CM0G = 1, the comparator 0 interrupt trigger direction is rising edge.

✸ ***Note: CM0OUT is comparator raw output without latch. It varies depend on the comparator process result. But the CM0IRQ is latch comparator output result. It must be cleared by program.***

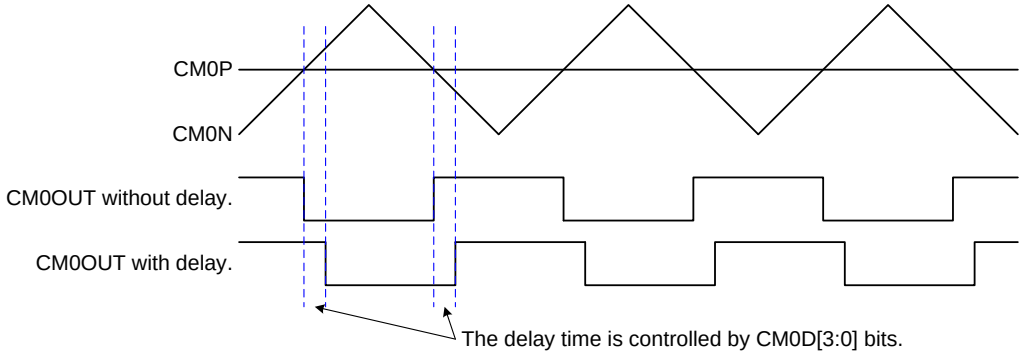
Comparator supports interrupt function. The interrupt trigger condition can be selected through CM0G bit including rising edge and falling edge. If CM0G = 0, comparator output trigger edge is falling edge. If CM0G = 1, comparator output trigger edge is rising edge. The edge detection is from comparator output signal through delay processor. When comparator output edge event occurs and equal CM0G condition, CM0IRQ flag is issued. If CM0IEN = 1, program counter points to interrupt vector to execute interrupt service routine.



***. CM0IRQ is cleared by program.**

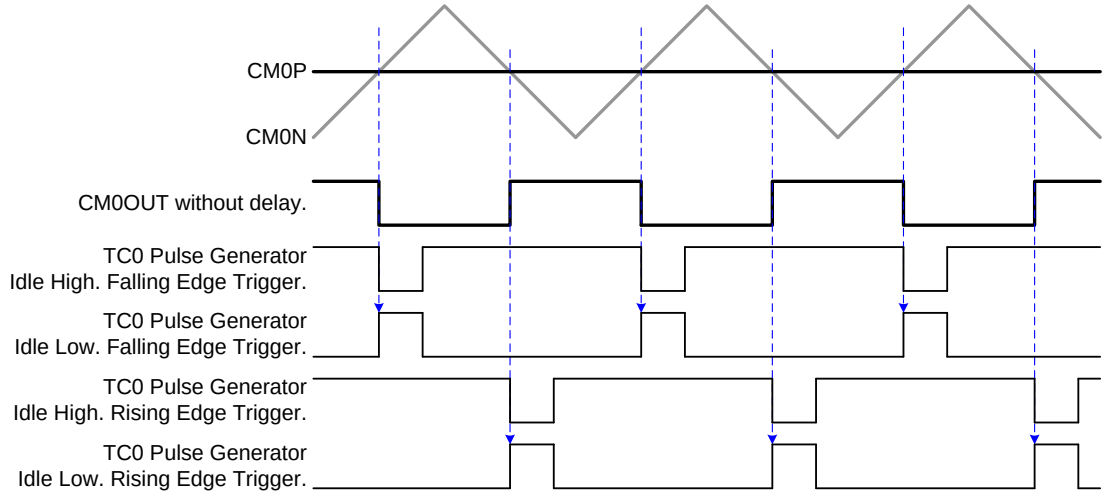
Comparator 0 compares positive terminal's voltage and negative terminal's voltage, and then output result to output pin. When V+ > V-, comparator outputs high status. When V+ < V-, comparator outputs low status. Comparator output terminal builds in delay control block to achieve output hysteresis to filter output transition condition. The delay option has 16-step including no delay, 1/Fhosc, 2/Fhosc, 3/Fhosc, 4/Fhosc, 5/Fhosc, 6/Fhosc, 7/Fhosc, 8/Fhosc, 9/Fhosc, 10/Fhosc, 11/Fhosc, 12/Fhosc, 13/Fhosc, 14/Fhosc, 15/Fhosc controlled by CM0D[3:0] bits.

CM0D[3:0]	**0000b**	**0001b**	**0010b**	**0011b**	**0100b**	**0101b**	**0110b**	**0111b**
	No	1/Fhosc	2/Fhosc	3/Fhosc	4/Fhosc	5/Fhosc	6/Fhosc	7/Fhosc
Delay time (us) Fhosc=16MHz	0	0.0625	0.125	0.1875	0.25	0.3125	0.375	0.4375
Delay time (us) Fhosc=4MHz	0	0.25	0.5	0.75	1	1.25	1.5	1.75
CM0D[3:0]	**1000b**	**1001b**	**1010b**	**1011b**	**1100b**	**1101b**	**1110b**	**1111b**
	8/Fhosc	9/Fhosc	10/Fhosc	11/Fhosc	12/Fhosc	13/Fhosc	14/Fhosc	15/Fhosc
Delay time (us) Fhosc=16MHz	0.5	0.5625	0.625	0.6875	0.75	0.8125	0.875	0.9375
Delay time (us) Fhosc=4MHz	2	2.25	2.5	2.75	3	3.25	3.5	3.75

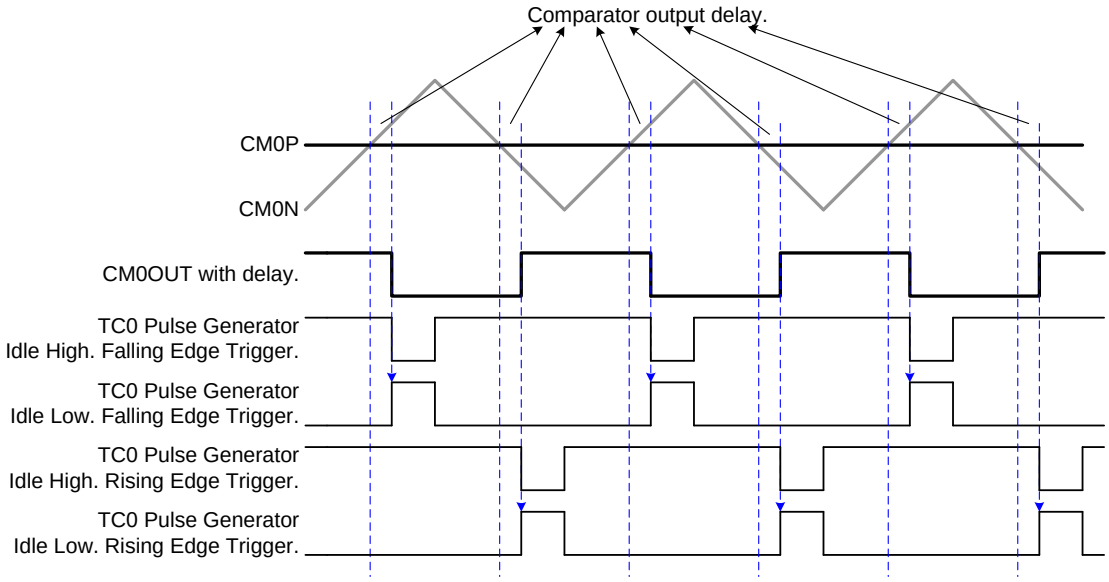


9.3 COMPARATOR 0 SPECIAL FUCNITON

Besides normal comparator function, comparator 0 builds in a special mode to trigger TC0 pulse generator through comparator output edge and controlled by CM0SF bit. When CM0SF=1, comparator 0 special mode is enabled. If comparator 0 output trigger condition occurs, TC0 pulse generator is triggered to output a pulse signal, and comparator interrupt function actives. More detail operation is referred to TC0 pulse generator contents.



TC0 pulse generator output signal without delay.



TC0 pulse generator output signal with delay.

9.4 COMPARATOR MODE REGISTER

09CH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CM0M	CM0EN	CM0OEN	CM0OUT	CM0SF	CM0G	-	-	-
Read/Write	R/W	R/W	R	R/W	R/W	-	-	-
After Reset	0	0	0	0	0	-	-	-

Bit 3 **CM0G:** Comparator output trigger direction control bit.
0 = Falling edge trigger. Comparator output status is from high to low as CM0P < CM0N.
1 = Rising edge trigger. Comparator output status is from low to high as CM0P > CM0N.

Bit 4 **CM0SF:** Comparator 0 special mode control bit.
0 = Disable. Comparator 0 is normal comparator function.
1 = Enable. Comparator 0 output edge triggers TC0 pulse generator.

Bit 5 **CM0OUT:** Comparator 0 output flag bit.
0 = CM0P voltage is less than CM0N voltage.
1 = CM0P voltage is larger than CM0N voltage.

Bit 6 **CM0OEN:** Comparator 0 output pin control bit.
0 = Disable. CM0O is GPIO mode.
1 = Enable. CM0O is comparator output pin and isolate GPIO function.

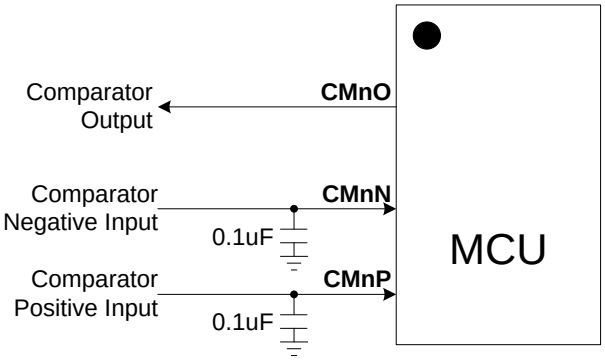
Bit 7 **CM0EN:** Comparator 0 control bit.
0 = Disable. Comparator pins are GPIO mode.
1 = Enable. CM0N and CM0P pins are comparator mode. CM0O is controlled by CM0OEN bit.

09AH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMDB0	CM1D3	CM1D2	CM1D1	CM1D0	CM0D3	CM0D2	CM0D1	CM0D0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After Reset	0	0	0	0	0	0	0	0

Bit [3:0] **CM0D[3:0]:** Comparator 0 de-bounce time control bit.
0000=No delay, 0001=1/Fhosc, 0010=2/Fhosc, 0011=3/Fhosc, 0100=4/Fhosc, 0101=5/Fhosc, 0110=6/Fhosc, 0111=7/Fhosc, 1000=8/Fhosc, 1001=9/Fhosc, 1010=10/Fhosc, 1011=11/Fhosc, 1100=12/Fhosc, 1101=13/Fhosc, 1110=14/Fhosc, 1111=15/Fhosc.

9.5 COMPARATOR APPLICATION NOTICE

The comparator is to compares the positive voltage and negative voltage to output result. The positive and negative sources are analog signal. In hardware application circuit, the comparator input pins must be connected a 0.1uF comparator to reduce power noise and make the input signal more stable. The application circuit is as following.



9.6 COMPARATOR 0 OPERATION EXPLAME

- **COMPARATOR 0 CONFIGURATION:**

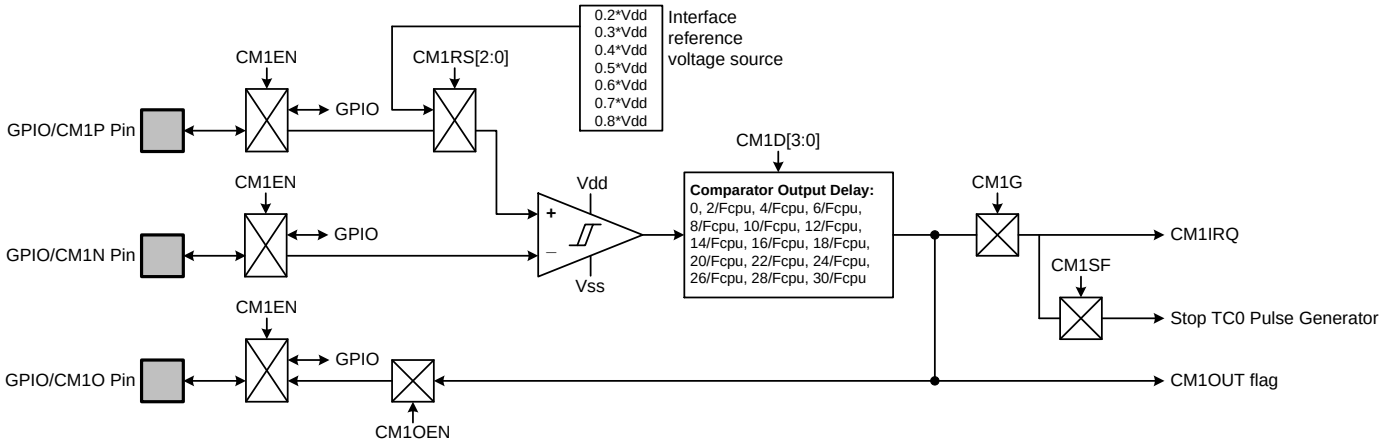
```
; Reset Comparator 0.
        CLR     CM0M            ; Clear CM0M register.

; Set Comparator 0 function mode.
        B0BCLR  FCM0SF          ; Normal comparator mode.
; or
        B0BSET  FCM0SF          ; Special function mode.

; Set Comparator 0 output pin.
        B0BCLR  FCM0OEN         ; Disable comparator 0 output pin.
; or
        B0BSET  FCM0OEN         ; Enable comparator 0 output pin.

; Set Comparator 0 interrupt trigger edge.
        B0BCLR  FCM0G           ; Falling edge.
; or
        B0BSET  FCM0G           ; Rising edge.

; Set Comparator 0 output de-bounce.
        B0MOV   A, CMDB0        ; Set CM0D[3:0] for comparator output de-bounce.
        AND     A, #1111 0000b
        OR      A, #0000 nnnnb
        B0MOV   CMDB0, A

; Clear CM0IRQ
        B0BCLR  FCM0IRQ

; Enable Comparator 0 and interrupt function.
        B0BSET  FCM0IEN         ; Enable Comparator 0 interrupt function.
        B0BSET  FCM0EN          ; Enable Comparator 0.
```

10 ANALOG COMPARAOTR 1

10.1 OVERVIEW

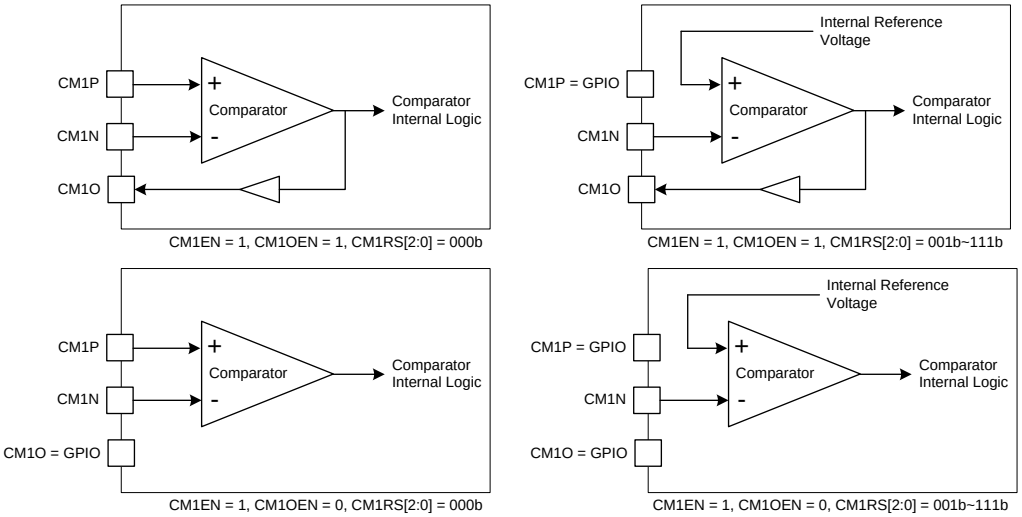
The micro-controller builds in one comparator with stopping TC0 pulse generator function. The comparator has normal comparator mode and stopping TC0 pulse output trigger source. The comparator is not Rail-to-Rail structure. That means the input voltage is not real from Vdd~Vss (Reference to “Electrical characteristics” chapter). When the positive input voltage is greater than the negative input voltage, the comparator output is high. When the positive input voltage is smaller than the negative input voltage, the comparator output is low. The comparator builds in internal reference voltage connected to comparator positive terminal, and comparator positive input pin can be GPIO mode as enabling internal reference voltage source. The main purposes of comparator 1 are as following.

- **Normal comparator function:** General comparator mode compares the two tensions of positive input terminal and negative input terminal.
- **Interrupt function:** Comparator 1 supports interrupt function. When comparator 1 output edge direction equals to edge selection, the CM1IRQ actives and the system points program counter to interrupt vector to do interrupt sequence.
- **TC0 pulse generator trigger stopping source:** Comparator 1 can be TC0 pulse generator stopping trigger source controlled by CM1SF bit. When TC0PO = 1 and CM1SF = 1, comparator 1 output status triggers TC0 pulse generator to stop outputting pulse signal.
- **Green mode function:** Comparator 1 still actives in green mode, but no wake-up function. CM1IRQ can be latched as trigger event occurrence until system wakes up. After system wakes up, the comparator 1 interrupt service routine is executed by program.



10.2 NORMAL COMPARATOR MODE

Comparator pins are shared with GPIO controlled by CM1EN bit. When CM1EN=1, CM1N pin is enabled connected to comparator negative terminal. Comparator positive terminal is controlled by CM1RS[2:0] bits. When CM1RS[2:0]=000b, comparator positive terminal is from CM1P pin, and GPIO function is isolated. When CM1RS[2:0]=001b~111b, comparator positive terminal is connected to internal reference voltage source including 7-level which are 0.2*Vdd, 0.3*Vdd, 0.4*Vdd, 0.5*Vdd, 0.6*Vdd, 0.7*Vdd, 0.8*Vdd, and CM1P pin is GPIO mode. CM1OEN controls comparator output connected to GPIO or not. When CM1OEN=1, comparator output terminal is connected to CM1O pin and isolate GPIO function. When CM1OEN=0, comparator output status can be read through CM1OUT flag and CM1O pin is GPIO mode.

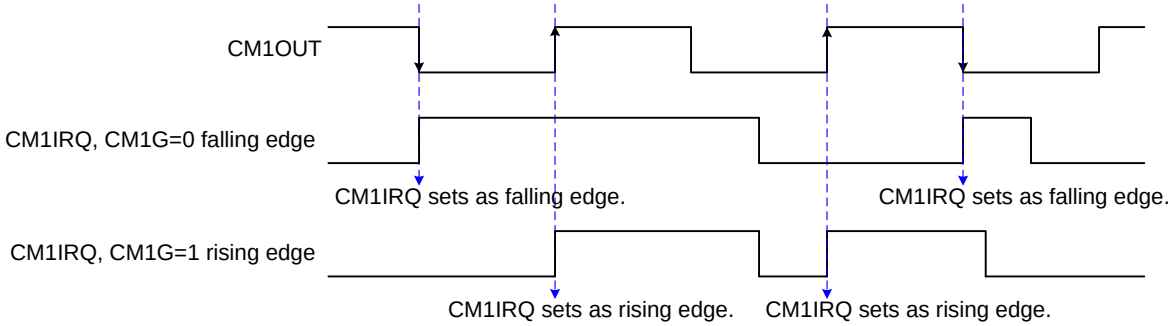


✸ ***Note: The comparator enable condition is fixed CM1EN=1, or the comparator pins are GPIO mode and comparator is disabled.***

The CM1OUT and CM1IRQ bits indicate the comparator result. The CM1OUT shows the comparator result immediately, but the CM1IRQ only indicates the event of the comparator result. The event condition is controlled by register and includes rising edge (CM1OUT changes from low to high) and falling edge (CM1OUT changes from high to low) controlled by CM1G bit. When CM1G = 0, the comparator 1 interrupt trigger direction is falling edge. When CM1G = 1, the comparator 1 interrupt trigger direction is rising edge.

✸ ***Note: CM1OUT is comparator raw output without latch. It varies depend on the comparator process result. But the CM1IRQ is latch comparator output result. It must be cleared by program.***

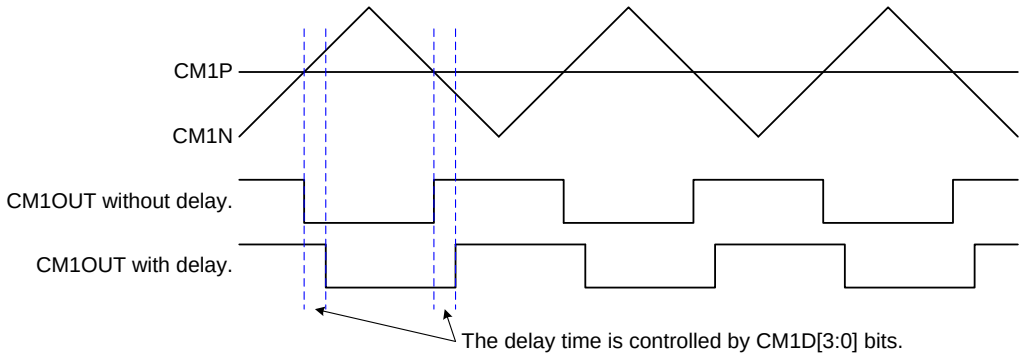
Comparator supports interrupt function. The interrupt trigger condition can be selected through CM1G bit including rising edge and falling edge. If CM1G = 0, comparator output trigger edge is falling edge. If CM1G = 1, comparator output trigger edge is rising edge. The edge detection is from comparator output signal through delay processor. When comparator output edge event occurs and equal CM1G condition, CM1IRQ flag is issued. If CM1IEN = 1, program counter points to interrupt vector to execute interrupt service routine.



***. CM1IRQ is cleared by program.**

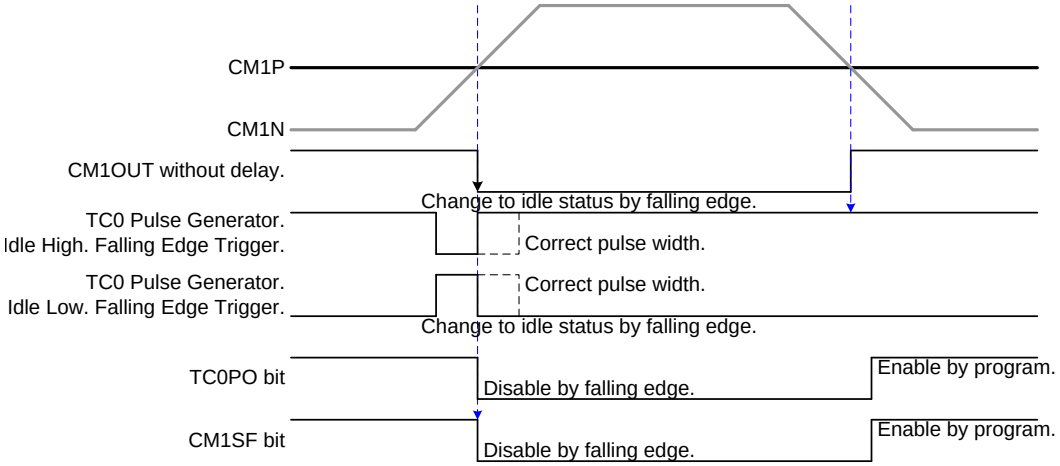
Comparator 1 compares positive terminal's voltage and negative terminal's voltage, and then output result to output pin. When V+ > V-, comparator outputs high status. When V+ < V-, comparator outputs low status. Comparator output terminal builds in delay control block to achieve output hysteresis to filter output transition condition. The delay option has 16-step including no delay, 2/Fcpu, 4/Fcpu, 6/Fcpu, 8/Fcpu, 10/Fcpu, 14/Fcpu, 16/Fcpu, 18/Fcpu, 20/Fcpu, 22/Fcpu, 24/Fcpu, 26/Fcpu, 28/Fcpu, 30/Fcpu controlled by CM1D[3:0] bits.

CM1D[2:0]	**0000b**	**0001b**	**0010b**	**0011b**	**0100b**	**0101b**	**0110b**	**0111b**
	No	2/Fcpu	4/Fcpu	6/Fcpu	8/Fcpu	10/Fcpu	12/Fcpu	14/Fcpu
Delay time (us) Fcpu=Fhosc/4 =16MHz/4=4MHz	0	0.5	1	1.5	2	2.5	3	3.5
Delay time (us) Fcpu=Fhosc/16 =16MHz/16=1MHz	0	2	4	6	8	10	12	14
CM1D[2:0]	**1000b**	**1001b**	**1010b**	**1011b**	**1100b**	**1101b**	**1110b**	**1111b**
	16/Fcpu	18/Fcpu	20/Fcpu	22/Fcpu	24/Fcpu	26/Fcpu	28/Fcpu	30/Fcpu
Delay time (us) Fcpu=Fhosc/4 =16MHz/4=4MHz	4	4.5	5	5.5	6	6.5	7	7.5
Delay time (us) Fcpu=Fhosc/16 =16MHz/16=1MHz	16	18	20	22	24	26	28	30

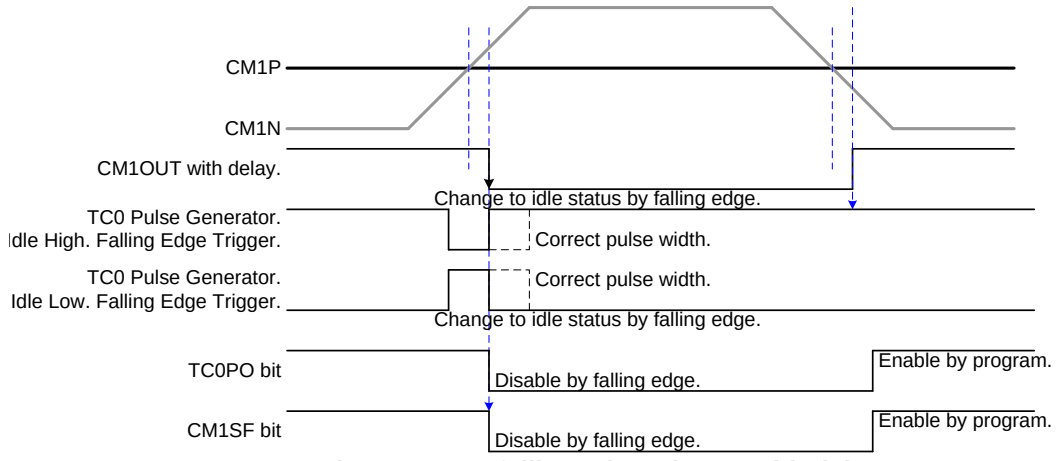


10.3 COMPARATOR 1 SPECIAL FUCNITON

Besides normal comparator function, comparator 1 builds in a special mode to stop TC0 pulse generator output signal. The special mode is to trigger TC0 pulse generator stopping output through comparator output edge and controlled by CM1SF bit. When CM1SF=1, comparator 1 special mode is enabled. If comparator 1 output trigger condition occurs, TC0 pulse generator function is disabled to turn off extern device. In this condition, TC0PO, TC0ENB and CM0SF bits are cleared to disable pulse output function automatically. Pulse output pin exchanges to GPIO mode and last status. CM1IRQ is issued to indicate surge event. It is necessary to enable pulse generator by program.



Stop TC0 pulse output @falling edge trigger, without delay.



Stop TC0 pulse output @falling edge trigger, with delay.

✸ ***Note: If TC0 pulse output is stopped by comparator 1 special mode trigger, the CM1SF and TC0PO bits are cleared automatically. It is necessary to set CM1SF, TC0PO and TC0ENB bits by program to recover TC0 pulse generator function.***

10.4 COMPARATOR MODE REGISTER

09DH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CM1M	CM1EN	CM1OEN	CM1OUT	CM1SF	CM1G	CM1RS2	CM1RS1	CM1RS0
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
After Reset	0	0	0	0	0	0	0	0

Bit [2:0] **CM1RS[2:0]:** Comparator positive terminal voltage source select bit.
000 = CM1P pin is comparator positive input pin, and GPIO function is isolated.
001 = Internal 0.2*Vdd. CM1P pin is GPIO mode.
010 = Internal 0.3*Vdd. CM1P pin is GPIO mode.
011 = Internal 0.4*Vdd. CM1P pin is GPIO mode.
100 = Internal 0.5*Vdd. CM1P pin is GPIO mode.
101 = Internal 0.6*Vdd. CM1P pin is GPIO mode.
110 = Internal 0.7*Vdd. CM1P pin is GPIO mode.
111 = Internal 0.8*Vdd. CM1P pin is GPIO mode.

Bit 3 **CM1G:** Comparator output trigger direction control bit.
0 = Falling edge trigger. Comparator output status is from high to low as CM1P < CM1N.
1 = Rising edge trigger. Comparator output status is from low to high as CM1P > CM1N.

Bit 4 **CM1SF:** Comparator 1 special mode control bit.
0 = Disable. Comparator 1 is normal comparator function.
1 = Enable. Comparator 1 output edge triggers TC0 pulse generator stopping.

Bit 5 **CM1OUT:** Comparator 1 output flag bit.
0 = CM1P voltage is less than CM1N voltage.
1 = CM1P voltage is larger than CM1N voltage.

Bit 6 **CM1OEN:** Comparator 1 output pin control bit.
0 = Disable. CM1O is GPIO mode.
1 = Enable. CM1O is comparator output pin and isolate GPIO function.

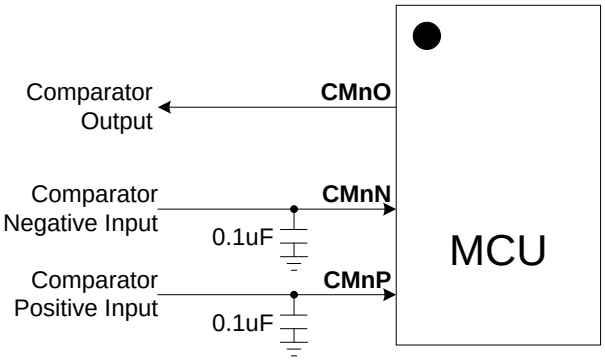
Bit 7 **CM1EN:** Comparator 1 control bit.
0 = Disable. Comparator pins are GPIO mode.
1 = Enable. CM1N pin is comparator mode. CM1O is controlled by CM1OEN bit. CM1P is controlled by CM1RS[2:0]bits.

09AH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMDB0	CM1D3	CM1D2	CM1D1	CM1D0	CM0D3	CM0D2	CM0D1	CM0D0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After Reset	0	0	0	0	0	0	0	0

Bit [7:4] **CM1D[3:0]:** Comparator 1 de-bounce time control bit.
0000=No delay, 0001=2/Fcpu, 0010=4/Fcpu, 0011=6/Fcpu, 0100=8/Fcpu, 0101=10/Fcpu, 0110=12/Fcpu,0111=14/Fcpu, 1000=16/Fcpu, 1001=18/Fcpu, 1010=20/Fcpu, 1011=22/Fcpu, 1100=24/Fcpu, 1101=26/Fcpu, 1110=28/Fcpu, 1111=30/Fcpu

10.5 COMPARATOR APPLICATION NOTICE

The comparator is to compares the positive voltage and negative voltage to output result. The positive and negative sources are analog signal. In hardware application circuit, the comparator input pins must be connected a 0.1uF comparator to reduce power noise and make the input signal more stable. The application circuit is as following.



10.6 COMPARATOR 1 OPERATION EXPLAME

- **COMPARATOR 1 CONFIGURATION:**

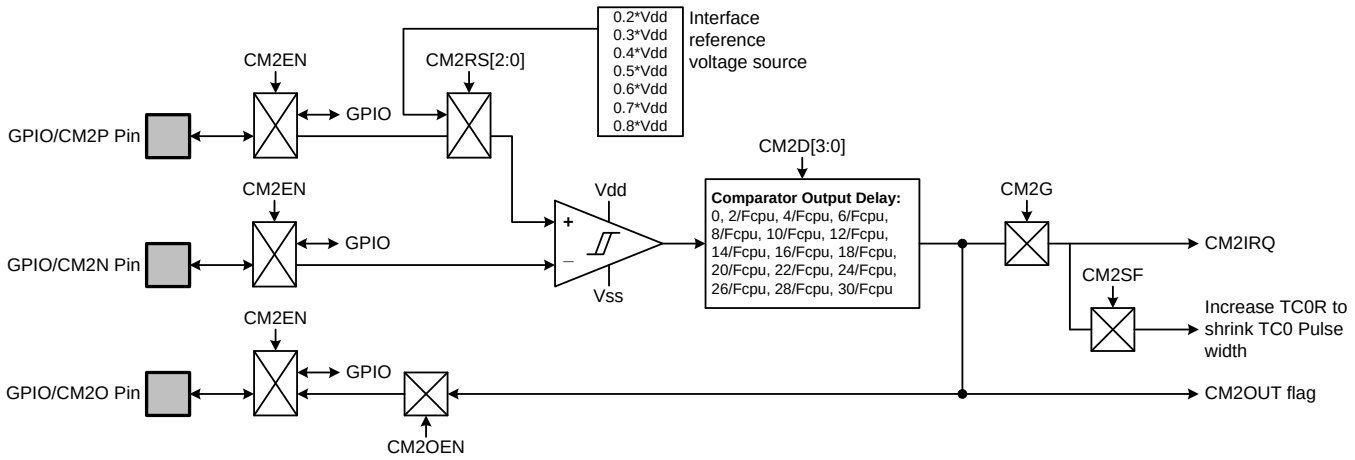
```
; Reset Comparator 1.
        CLR     CM1M            ; Clear CM1M register.

; Set Comparator 1 positive terminal.
        MOV     A, #00000nnnb   ; Set CM1RS[2:0] for comparator positive terminal.
        B0MOV   CM1M, A

; Set Comparator 1 function mode.
        B0BCLR  FCM1SF          ; Normal comparator mode.
; or
        B0BSET  FCM1SF          ; Special function mode.

; Set Comparator 1 output pin.
        B0BCLR  FCM1OEN         ; Disable comparator 1 output pin.
; or
        B0BSET  FCM1OEN         ; Enable comparator 1 output pin.

; Set Comparator 1 interrupt trigger edge.
        B0BCLR  FCM1G           ; Falling edge.
; or
        B0BSET  FCM1G           ; Rising edge.

; Set Comparator 1 output de-bounce.
        B0MOV   A, CMDB0        ; Set CM1D[3:0] for comparator output de-bounce.
        AND     A, #00001111b
        OR      A, #nnnn0000b
        B0MOV   CMDB0, A

; Clear CM1IRQ
        B0BCLR  FCM1IRQ

; Enable Comparator 1 and interrupt function.
        B0BSET  FCM1IEN         ; Enable Comparator 1 interrupt function.
        B0BSET  FCM1EN          ; Enable Comparator 1.
```

11 ANALOG COMPARAOTR 2

11.1 OVERVIEW

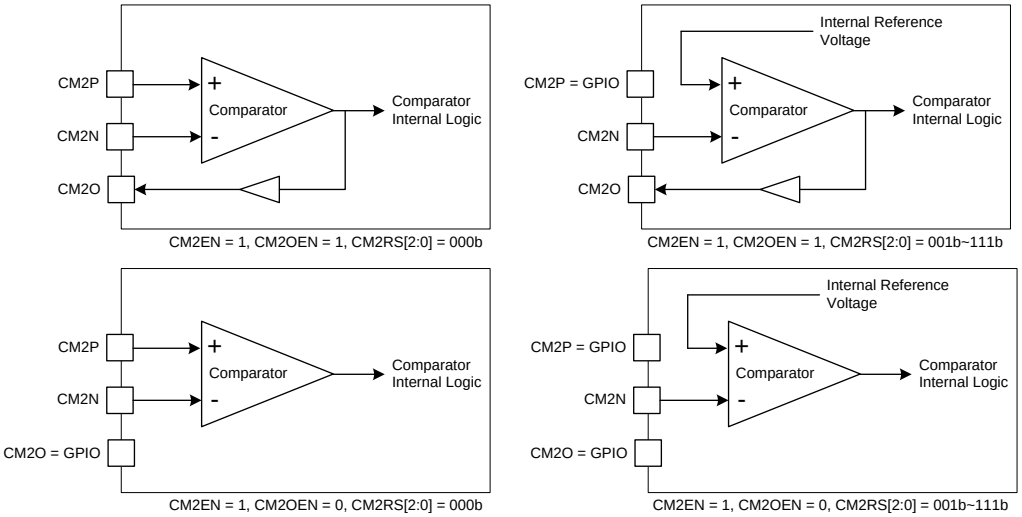
The micro-controller builds in one comparator with shrinking TC0 pulse width function. The comparator has normal comparator mode and shrinking TC0 pulse width trigger source. The comparator is not Rail-to-Rail structure. That means the input voltage is not real from Vdd~Vss (Reference to “Electrical characteristics” chapter). When the positive input voltage is greater than the negative input voltage, the comparator output is high. When the positive input voltage is smaller than the negative input voltage, the comparator output is low. The comparator builds in internal reference voltage connected to comparator positive terminal, and comparator positive input pin can be GPIO mode as enabling internal reference voltage source. The main purposes of comparator 2 are as following.

- **Normal comparator function:** General comparator mode compares the two tensions of positive input terminal and negative input terminal.
- **Interrupt function:** Comparator 2 supports interrupt function. When comparator 2 output edge direction equals to edge selection, the CM2IRQ actives and the system points program counter to interrupt vector to do interrupt sequence.
- **TC0 pulse width shrinking source:** Comparator 2 can be TC0 pulse width shrinking trigger source controlled by CM2SF bit. When TC0PO = 1 and CM2SF = 1, comparator 2 output status triggers to shrink TC0 pulse width through increasing TC0R register.
- **Green mode function:** Comparator 2 still actives in green mode, but no wake-up function. CM2IRQ can be latched as trigger event occurrence until system wakes up. After system wakes up, the comparator 2 interrupt service routine is executed by program.



11.2 NORMAL COMPARATOR MODE

Comparator pins are shared with GPIO controlled by CM2EN bit. When CM2EN=1, CM2N pin is enabled connected to comparator negative terminal. Comparator positive terminal is controlled by CM2RS[2:0] bits. When CM2RS[2:0]=000b, comparator positive terminal is from CM2P pin, and GPIO function is isolated. When CM2RS[2:0]=001b~111b, comparator positive terminal is connected to internal reference voltage source including 7-level which are 0.2*Vdd, 0.3*Vdd, 0.4*Vdd, 0.5*Vdd, 0.6*Vdd, 0.7*Vdd, 0.8*Vdd, and CM2P pin is GPIO mode. CM2OEN controls comparator output connected to GPIO or not. When CM2OEN=1, comparator output terminal is connected to CM2O pin and isolate GPIO function. When CM2OEN=0, comparator output status can be read through CM2OUT flag and CM2O pin is GPIO mode.

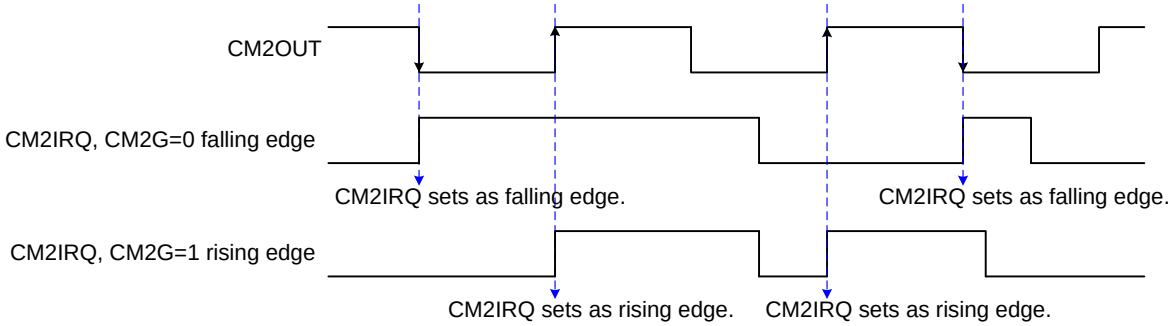


✸ ***Note: The comparator enable condition is fixed CM2EN=1, or the comparator pins are GPIO mode and comparator is disabled.***

The CM2OUT and CM2IRQ bits indicate the comparator result. The CM2OUT shows the comparator result immediately, but the CM2IRQ only indicates the event of the comparator result. The event condition is controlled by register and includes rising edge (CM2OUT changes from low to high) and falling edge (CM2OUT changes from high to low) controlled by CM2G bit. When CM2G = 0, the comparator 2 interrupt trigger direction is falling edge. When CM2G = 1, the comparator 2 interrupt trigger direction is rising edge.

✸ ***Note: CM2OUT is comparator raw output without latch. It varies depend on the comparator process result. But the CM2IRQ is latch comparator output result. It must be cleared by program.***

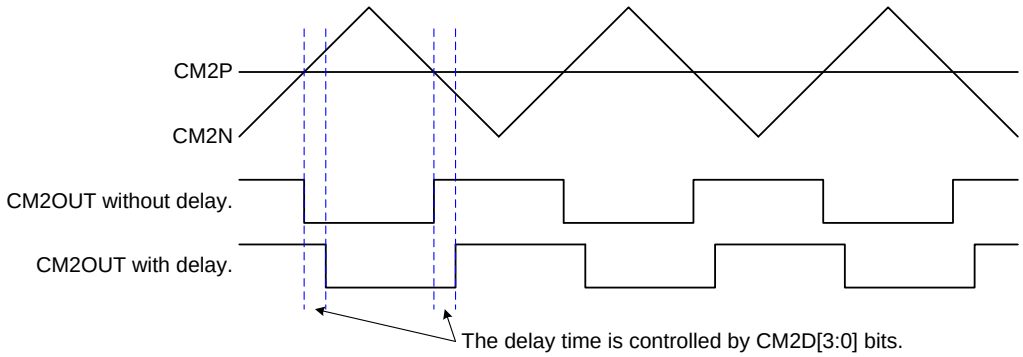
Comparator supports interrupt function. The interrupt trigger condition can be selected through CM2G bit including rising edge and falling edge. If CM2G = 0, comparator output trigger edge is falling edge. If CM2G = 1, comparator output trigger edge is rising edge. The edge detection is from comparator output signal through delay processor. When comparator output edge event occurs and equal CM2G condition, CM2IRQ flag is issued. If CM2IEN = 1, program counter points to interrupt vector to execute interrupt service routine.



***. CM2IRQ is cleared by program.**

Comparator 2 compares positive terminal's voltage and negative terminal's voltage, and then output result to output pin. When V+ > V-, comparator outputs high status. When V+ < V-, comparator outputs low status. Comparator output terminal builds in delay control block to achieve output hysteresis to filter output transition condition. The delay option has 16-step including no delay, 2/Fcpu, 4/Fcpu, 6/Fcpu, 8/Fcpu, 10/Fcpu, 14/Fcpu, 16/Fcpu, 18/Fcpu, 20/Fcpu, 22/Fcpu, 24/Fcpu, 26/Fcpu, 28/Fcpu, 30/Fcpu controlled by CM2D[3:0] bits.

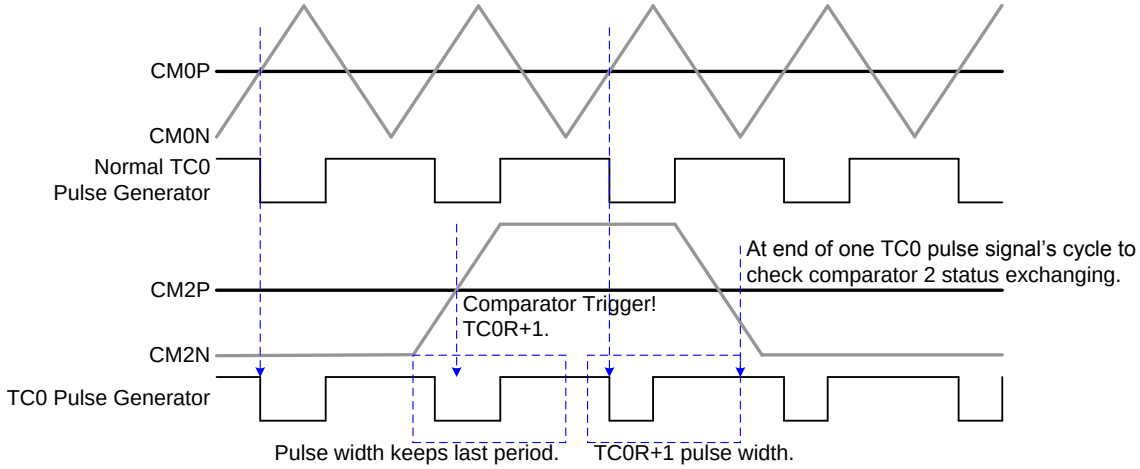
CM2D[2:0]	**0000b**	**0001b**	**0010b**	**0011b**	**0100b**	**0101b**	**0110b**	**0111b**
	No	2/Fcpu	4/Fcpu	6/Fcpu	8/Fcpu	10/Fcpu	12/Fcpu	14/Fcpu
Delay time (us) Fcpu=Fhosc/4 =16MHz/4=4MHz	0	0.5	1	1.5	2	2.5	3	3.5
Delay time (us) Fcpu=Fhosc/16 =16MHz/16=1MHz	0	2	4	6	8	10	12	14
CM2D[2:0]	**1000b**	**1001b**	**1010b**	**1011b**	**1100b**	**1101b**	**1110b**	**1111b**
	16/Fcpu	18/Fcpu	20/Fcpu	22/Fcpu	24/Fcpu	26/Fcpu	28/Fcpu	30/Fcpu
Delay time (us) Fcpu=Fhosc/4 =16MHz/4=4MHz	4	4.5	5	5.5	6	6.5	7	7.5
Delay time (us) Fcpu=Fhosc/16 =16MHz/16=1MHz	16	18	20	22	24	26	28	30



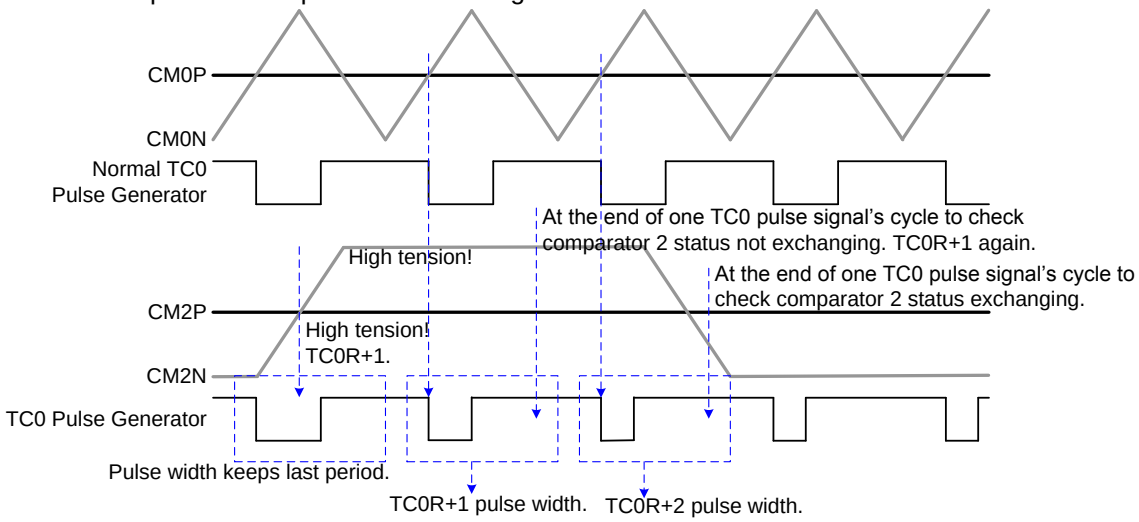
11.3 COMPARATOR 2 SPECIAL FUCNITON

Besides normal comparator function, comparator 2 builds in a special mode to shrink TC0 pulse width through increasing TC0R register. The special mode is to trigger increasing TC0R register and TC0 pulse width will be shrunk through comparator output edge and controlled by CM2SF bit. When CM2SF=1, comparator 2 special mode is enabled. If comparator 2 output trigger condition occurs, TC0R register increases 1 to shrink TC0 pulse width.

Step 1: When comparator 2 first trigger occurs, TC0R + 1 once to shrink TC0 pulse width. TC0 pulse width reduces a unit time automatically. The hardware checks comparator 2 high tension status at the end of one TC0 pulse signal's cycle. If the comparator output status exchanges, to expand TC0 pulse width through increasing TC0R register by program.



Step 2: If comparator output status doesn't exchange, TC0R + 1 at the end of one TC0 pulse signal's cycle and outputs the new pulse until comparator 2 output status exchanges.



✸ ***Note: If TC0R is increased to 0xFF, TC0R will keep 0xFF and not increase again, even the comparator output status never occurs exchanging.***

11.4 COMPARATOR MODE REGISTER

09EH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CM2M	CM2EN	CM2OEN	CM2OUT	CM2SF	CM2G	CM2RS2	CM2RS1	CM2RS0
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
After Reset	0	0	0	0	0	0	0	0

Bit [2:0] **CM2RS[2:0]:** Comparator positive terminal voltage source select bit.
000 = CM2P pin is comparator positive input pin, and GPIO function is isolated.
001 = Internal 0.2*Vdd. CM2P pin is GPIO mode.
010 = Internal 0.3*Vdd. CM2P pin is GPIO mode.
011 = Internal 0.4*Vdd. CM2P pin is GPIO mode.
100 = Internal 0.5*Vdd. CM2P pin is GPIO mode.
101 = Internal 0.6*Vdd. CM2P pin is GPIO mode.
110 = Internal 0.7*Vdd. CM2P pin is GPIO mode.
111 = Internal 0.8*Vdd. CM2P pin is GPIO mode.

Bit 3 **CM2G:** Comparator output trigger direction control bit.
0 = Falling edge trigger. Comparator output status is from high to low as CM2P < CM2N.
1 = Rising edge trigger. Comparator output status is from low to high as CM2P > CM2N.

Bit 4 **CM2SF:** Comparator 2 special mode control bit.
0 = Disable. Comparator 2 is normal comparator function.
1 = Enable. Comparator 2 output edge triggers TC0 pulse generator stopping.

Bit 5 **CM2OUT:** Comparator 2 output flag bit.
0 = CM2P voltage is less than CM2N voltage.
1 = CM2P voltage is larger than CM2N voltage.

Bit 6 **CM2OEN:** Comparator 2 output pin control bit.
0 = Disable. CM2O is GPIO mode.
1 = Enable. CM2O is comparator output pin and isolate GPIO function.

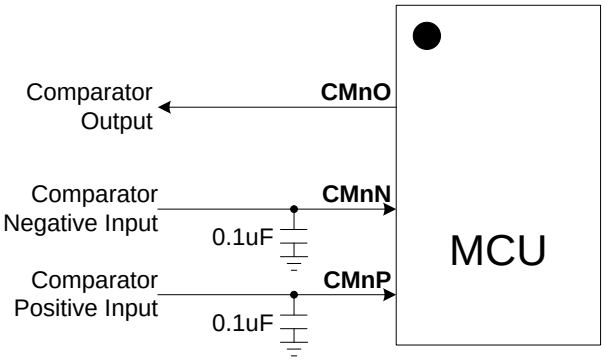
Bit 7 **CM2EN:** Comparator 2 control bit.
0 = Disable. Comparator pins are GPIO mode.
1 = Enable. CM2N pin is comparator mode. CM2O is controlled by CM2OEN bit. CM2P is controlled by CM2RS[2:0]bits.

09BH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMDB1	-	-	-	-	CM2D3	CM2D2	CM2D1	CM2D0
Read/Write	-	-	-	-	R/W	R/W	R/W	R/W
After Reset	-	-	-	-	0	0	0	0

Bit [7:4] **CM2D[3:0]:** Comparator 2 de-bounce time control bit.
0000=No delay, 0001=2/Fcpu, 0010=4/Fcpu, 0011=6/Fcpu, 0100=8/Fcpu, 0101=10/Fcpu, 0110=12/Fcpu,0111=14/Fcpu, 1000=16/Fcpu, 1001=18/Fcpu, 1010=20/Fcpu, 1011=22/Fcpu, 1100=24/Fcpu, 1101=26/Fcpu, 1110=28/Fcpu, 1111=30/Fcpu

11.5 COMPARATOR APPLICATION NOTICE

The comparator is to compares the positive voltage and negative voltage to output result. The positive and negative sources are analog signal. In hardware application circuit, the comparator input pins must be connected a 0.1uF comparator to reduce power noise and make the input signal more stable. The application circuit is as following.



11.6 COMPARATOR 2 OPERATION EXPLAME

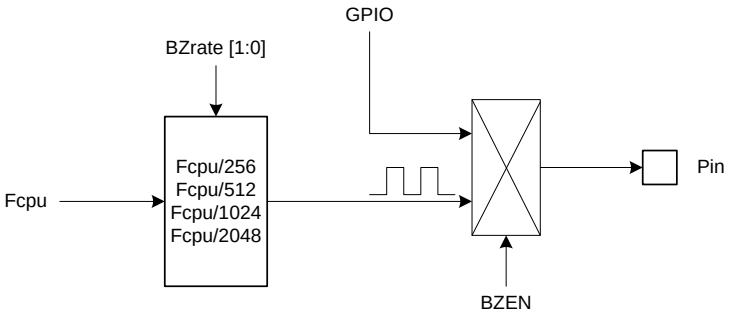
- **COMPARATOR 2 CONFIGURATION:**

```
; Reset Comparator 2.
        CLR     CM2M            ; Clear CM2M register.

; Set Comparator 2 positive terminal.
        MOV     A, #00000nnnb   ; Set CM2RS[2:0] for comparator positive terminal.
        B0MOV   CM2M, A

; Set Comparator 2 function mode.
        B0BCLR  FCM2SF          ; Normal comparator mode.
; or
        B0BSET  FCM2SF          ; Special function mode.

; Set Comparator 2 output pin.
        B0BCLR  FCM2OEN         ; Disable comparator 2 output pin.
; or
        B0BSET  FCM2OEN         ; Enable comparator 2 output pin.

; Set Comparator 2 interrupt trigger edge.
        B0BCLR  FCM2G           ; Falling edge.
; or
        B0BSET  FCM2G           ; Rising edge.

; Set Comparator 2 output de-bounce.
        MOV     A, #0000nnnnb   ; Set CM2D[3:0] for comparator output de-bounce.
        B0MOV   CMDB1, A

; Clear CM2IRQ
        B0BCLR  FCM2IRQ

; Enable Comparator 2 and interrupt function.
        B0BSET  FCM2IEN         ; Enable Comparator 2 interrupt function.
        B0BSET  FCM2EN          ; Enable Comparator 2.
```

12 2K/4K BUZZER GENERATOR

12.1 OVERVIEW

The MCU builds in Buzzer generator to drive external buzzer device. The buzzer generator purpose is to drive 2KHz or 4KHz buzzer. Adjusting buzzer output frequency is through BZM register. The buzzer output pin is shared with GPIO. When BZEN = 1, the pin outputs buzzer carry signal. When BZEN = 0, the pin returns to GPIO last condition (input mode, output high or output low status).



The buzzer frequency is divided from Fcpu (instruction cycle) controlled by BZrate bits, and Fcpu decides the buzzer frequency. The selection table is as following.

BZrate [1:0]	Buzzer Rate Division	Buzzer Rate		
		Fcpu = 1MHz	Fcpu = 2MHz	Fcpu = 4MHz
00	Fcpu/256	**4KHz**	8KHz	16KHz
01	Fcpu/512	**2KHz**	**4KHz**	8KHz
10	Fcpu/1024	1KHz	**2KHz**	**4KHz**
11	Fcpu/2048	0.5KHz	1KHz	**2KHz**

The buzzer target frequency is 2KHz and 4KHz. It is important to choice a good Fcpu rate to obtain the correct buzzer frequency. The above table shows 2KHz/4KHz buzzer frequency configurations.

12.2 BZM REGISTER

0DCH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BZM	BZEN	BZrate1	BZrate0	-	-	-	-	-
Read/Write	R/W	R/W	R/W	-	-	-	-	-
After reset	0	0	0	-	-	-	-	-

Bit 7 **BZEN:** Buzzer output control bit.
0 = Disable BZ output and BZ output pin transfers to I/O last status.
1 = Enable BZ output and disable GPIO function.

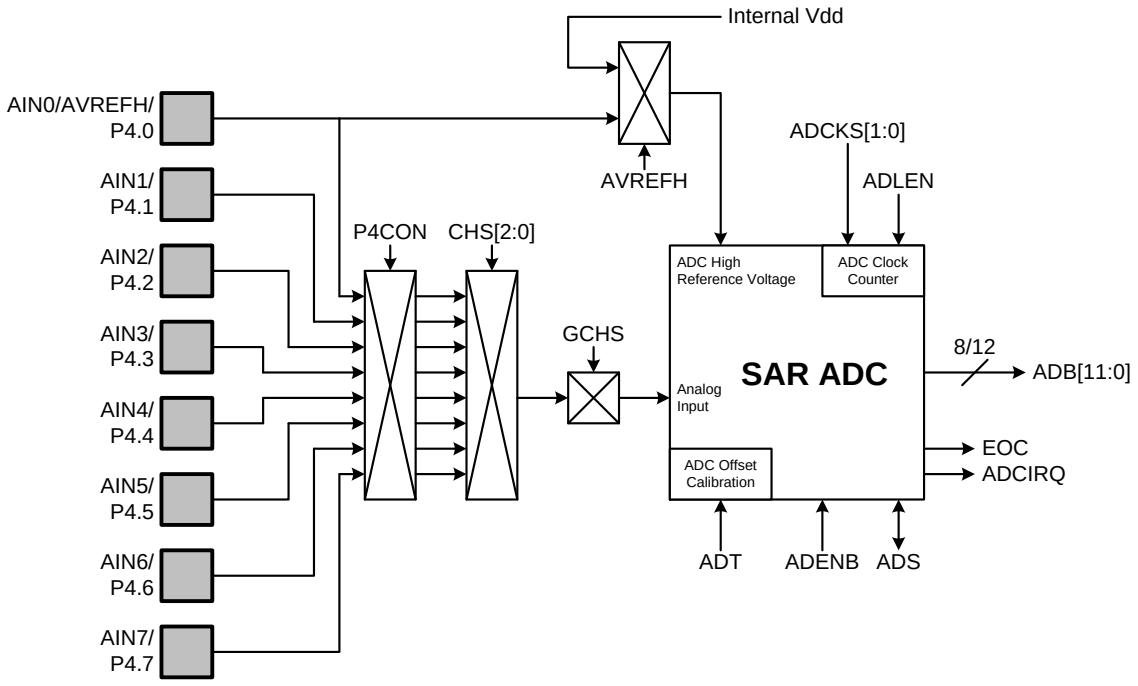
Bit[6:5] **BZrate[1:0]:** Buzzer rate control bits.
00 = Fcpu/256
01 = Fcpu/512
10 = Fcpu/1024
11 = Fcpu/2048

✷ ***Note:***
1. ***If BZEN=0, the buzzer output pin is GPIO mode and returns to last status after disabling buzzer output.***
2. ***If BZEN=1, the buzzer output pin is buzzer output function and isolates the GPIO function.***

13 8 CHANNEL ANALOG TO DIGITAL CONVERTER (ADC)

13.1 OVERVIEW

The analog to digital converter (ADC) is SAR structure with 8-input sources and up to 4096-step resolution to transfer analog signal into 12-bits digital buffers. The ADC builds in 8-channel input source (AIN0~AIN7) to measure 8 different analog signal sources controlled by CHS[2:0] and GCHS bits. The ADC resolution can be selected 8-bit and 12-bit resolutions through ADLEN bit. The ADC converting rate can be selected by ADCKS[1:0] bits to decide ADC converting time. The ADC reference high voltage includes two sources controlled by AVREFH bit. One is internal Vdd (AVREFH=0), and the other one is external reference voltage input pin from P4.0 pin (AVREFH=1). The ADC builds in P4CON register to set pure analog input pin. It is necessary to set P4 as input mode without pull-up resistor by program. After setup ADENB and ADS bits, the ADC starts to convert analog signal to digital data. When the conversion is complete, the ADC circuit will set EOC and ADCIRQ bits to “1” and the digital data outputs in ADB and ADR registers. If the ADCIEN = 1, the ADC interrupt request occurs and executes interrupt service routine when ADCIRQ = 1 after ADC converting. If ADC interrupt function is enabled (ADCIEN=1), the system will execute interrupt procedure. The interrupt procedure is system program counter points to interrupt vector (ORG 8) and executes interrupt service routine after finishing ADC converting. Clear ADCIRQ by program is necessary in interrupt procedure.



13.2 ADC MODE REGISTER

ADM is ADC mode control register to configure ADC configurations including ADC start, ADC channel selection, ADC high reference voltage source and ADC processing indicator…These configurations must be setup completely before starting ADC converting.

0B1H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADM	ADENB	ADS	EOC	GCHS	AVREFH	CHS2	CHS1	CHS0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After reset	0	0	0	0	0	0	0	0

Bit 7 **ADENB:** ADC control bit. **In power saving mode, disable ADC to reduce power consumption.**
0 = Disable ADC function.
1 = Enable ADC function.

Bit 6 **ADS:** ADC start control bit. **ADS bit is cleared after ADC processing automatically.**
0 = ADC converting stops.
1 = Start to execute ADC converting.

Bit 5 **EOC:** ADC status bit.
0 = ADC progressing.
1 = End of converting and reset ADS bit.

Bit 4 **GCHS:** ADC global channel select bit.
0 = Disable AIN channel.
1 = Enable AIN channel.

Bit 3 **AVREFH:** ADC high reference voltage source control bit.
0 = Internal Vdd. P4.0 is GPIO or AIN0 pin.
1 = Enable external reference voltage from P4.0.

Bit [2:0] **CHS[2:0]:** ADC input channel select bit.
000 = AIN0, 001 = AIN1, 010 = AIN2, 011 = AIN3, 100 = AIN4, 101 = AIN5, 110 = AIN6, 111 = AIN7

ADR register includes ADC mode control and ADC low-nibble data buffer. ADC configurations including ADC clock rate and ADC resolution. These configurations must be setup completely before starting ADC converting.

0B3H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADR	-	ADCKS1	ADLEN	ADCKS0	ADB3	ADB2	ADB1	ADB0
Read/Write	-	R/W	R/W	R/W	R	R	R	R
After reset	-	0	0	0	-	-	-	-

Bit 6,4 **ADCKS [1:0]:** ADC's clock rate select bit.
00 = Fcpu/16, 01 = Fcpu/8, 10 = Fcpu/1, 11 = Fcpu/2

Bit 5 **ADLEN:** ADC's resolution select bits.
0 = 8-bit.
1 = 12-bit.

13.3 ADC DATA BUFFER REGISTERS

ADC data buffer is 12-bit length to store ADC converter result. The high byte is ADB register, and the low-nibble is ADR[3:0] bits. The ADB register is only 8-bit register including bit 4~bit11 ADC data. To combine ADB register and the low-nibble of ADR will get full 12-bit ADC data buffer. The ADC data buffer is a read-only register and the initial status is unknown after system reset.

- **ADB[11:4]: In 8-bit ADC mode, the ADC data is stored in ADB register.**
- **ADB[11:0]: In 12-bit ADC mode, the ADC data is stored in ADB and ADR registers.**

0B2H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADB	ADB11	ADB10	ADB9	ADB8	ADB7	ADB6	ADB5	ADB4
Read/Write	R	R	R	R	R	R	R	R
After reset	-	-	-	-	-	-	-	-

Bit[7:0] **ADB[7:0]:** 8-bit ADC data buffer and the high-byte data buffer of 12-bit ADC.

0B3H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADR	-	ADCKS1	ADLEN	ADCKS0	ADB3	ADB2	ADB1	ADB0
Read/Write	-	R/W	R/W	R/W	R	R	R	R
After reset	-	0	0	0	-	-	-	-

Bit [3:0] **ADB [3:0]:** 12-bit low-nibble ADC data buffer.

The AIN input voltage v.s. ADB output data

AIN n	ADB11	ADB10	ADB9	ADB8	ADB7	ADB6	ADB5	ADB4	ADB3	ADB2	ADB1	ADB0
0/4096*VREFH	0	0	0	0	0	0	0	0	0	0	0	0
1/4096*VREFH	0	0	0	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
4094/4096*VREFH	1	1	1	1	1	1	1	1	1	1	1	0
4095/4096*VREFH	1	1	1	1	1	1	1	1	1	1	1	1

For different applications, users maybe need more than 8-bit resolution but less than 12-bit. To process the ADB and ADR data can make the job well. First, the ADC resolution must be set 12-bit mode and then to execute ADC converter routine. Then delete the LSB of ADC data and get the new resolution result. The table is as following.

ADC Resolution	ADB								ADR			
	ADB11	ADB10	ADB9	ADB8	ADB7	ADB6	ADB5	ADB4	ADB3	ADB2	ADB1	ADB0
8-bit	O	O	O	O	O	O	O	O	x	x	x	x
9-bit	O	O	O	O	O	O	O	O	O	x	x	x
10-bit	O	O	O	O	O	O	O	O	O	O	x	x
11-bit	O	O	O	O	O	O	O	O	O	O	O	x
12-bit	O	O	O	O	O	O	O	O	O	O	O	O
O = Selected, x = Useless												

✸ ***Note: The initial status of ADC data buffer including ADB register and ADR low-nibble after the system reset is unknown.***

13.4 ADC OPERATION DESCRIPTION AND NOTIC

13.4.1 ADC SIGNAL FORMAT

ADC sampling voltage range is limited by high/low reference voltage. The ADC low reference voltage is Vss and not changeable. The ADC high reference voltage includes internal Vdd and external reference voltage source from P4.0/AVREFH pin controlled by AVREFH bit. If AVREFH=0, ADC reference voltage is from internal Vdd (MCU power voltage). If AVREFH=1, ADC reference voltage is from external voltage source (P4.0/AVREFH). ADC reference voltage range limitation is **"(ADC high reference voltage – low reference voltage) ≧ 2V"**. ADC low reference voltage is Vss = 0V. So **ADC high reference voltage range is 2V~Vdd**. The range is ADC external high reference voltage range.

- **ADC Internal Low Reference Voltage = 0V.**
- **ADC Internal High Reference Voltage = Vdd. (AVREFH=0)**
- **ADC External High Reference Voltage = 2V~Vdd. (AVREFH=1)**

ADC sampled input signal voltage must be from ADC low reference voltage to ADC high reference. If the ADC input signal voltage is over the range, the ADC converting result is error (full scale or zero).

- **ADC Low Reference Voltage ≦ ADC Sampled Input Voltage ≦ ADC High Reference Voltage**

13.4.2 ADC CONVERTING TIME

The ADC converting time is from ADS=1 (Start to ADC convert) to EOC=1 (End of ADC convert). The converting time duration is depend on ADC resolution and ADC clock rate. 12-bit ADC's converting time is 1/(ADC clock /4)*16 sec, and the 8-bit ADC converting time is 1/(ADC clock /4)*12 sec. ADC clock source is Fcpu and includes Fcpu/1, Fcpu/2, Fcpu/8 and Fcpu/16 controlled by ADCKS[1:0] bits.
The ADC converting time affects ADC performance. If input high rate analog signal, it is necessary to select a high ADC converting rate. If the ADC converting time is slower than analog signal variation rate, the ADC result would be error. So to select a correct ADC clock rate and ADC resolution to decide a right ADC converting rate is very important.

12-bit ADC conversion time = 1/(ADC clock rate/4)*16 sec

ADLEN	ADCKS1, ADCKS0	ADC Clock Rate	Fcpu=4MHz		Fcpu=16MHz	
			ADC Converting time	ADC Converting Rate	ADC Converting time	ADC Converting Rate
1 (12-bit)	00	Fcpu/16	1/(4MHz/16/4)*16 = 256 us	3.906KHz	1/(16MHz/16/4)*16 = 64 us	15.625KHz
	01	Fcpu/8	1/(4MHz/8/4)*16 = 128 us	7.813KHz	1/(16MHz/8/4)*16 = 32 us	31.25KHz
	10	Fcpu	1/(4MHz/4)*16 = 16 us	62.5KHz	1/(16MHz/4)*16 = 4 us	250KHz
	11	Fcpu/2	1/(4MHz/2/4)*16 = 32 us	31.25KHz	1/(16MHz/2/4)*16 = 8 us	125KHz

8-bit ADC conversion time = 1/(ADC clock rate/4)*12 sec

ADLEN	ADCKS1, ADCKS0	ADC Clock Rate	Fcpu=4MHz		Fcpu=16MHz	
			ADC Converting time	ADC Converting Rate	ADC Converting time	ADC Converting Rate
0 (8-bit)	00	Fcpu/16	1/(4MHz/16/4)*12 = 192 us	5.208KHz	1/(16MHz/16/4)*12 = 48 us	20.833KHz
	01	Fcpu/8	1/(4MHz/8/4)*12 = 96 us	10.416KHz	1/(16MHz/8/4)*12 = 24 us	41.667KHz
	10	Fcpu	1/(4MHz/4)*12 = 12 us	83.333KHz	1/(16MHz/4)*12 = 3 us	333.333KHz
	11	Fcpu/2	1/(4MHz/2/4)*12 = 24 us	41.667KHz	1/(16MHz/2/4)*12 = 6 us	166.667KHz

13.4.3 ADC PIN CONFIGURATION

ADC input channels are shared with Port4. ADC channel selection is through ADCHS[2:0] bit. ADCHS[2:0] value points to the ADC input channel directly. ADCHS[2:0]=000 selects AIN0. ADCHS[2:0]=001 selects AIN1……Only one pin of port 4 can be configured as ADC input in the same time. The pins of Port4 configured as ADC input channel must be set input mode, disable internal pull-up and enable P4CON first by program. After selecting ADC input channel through ADCHS[2:0], set GCHS bit as "1" to enable ADC channel function.

- **The GPIO mode of ADC input channels must be set as input mode.**
- **The internal pull-up resistor of ADC input channels must be disabled.**
- **P4CON bits of ADC input channel must be set.**

The P4.0/AIN0 can be ADC external high reference voltage input pin when AVREFH=1. In the condition, P4.0 GPIO mode must be set as input mode and disable internal pull-up resistor.

- **The GPIO mode of ADC external high reference voltage input pin must be set as input mode.**
- **The internal pull-up resistor of ADC external high reference voltage input pin must be disabled.**

ADC input pins are shared with digital I/O pins. Connect an analog signal to COMS digital input pin, especially, the analog signal level is about 1/2 VDD will cause extra current leakage. In the power down mode, the above leakage current will be a big problem. Unfortunately, if users connect more than one analog input signal to port 4 will encounter above current leakage situation. P4CON is Port4 configuration register. Write "1" into P4CON [7:0] will configure related port 4 pin as pure analog input pin to avoid current leakage.

0AEH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P4CON	P4CON7	P4CON6	P4CON5	P4CON4	P4CON3	P4CON2	P4CON1	P4CON0
Read/Write	W	W	W	W	W	W	W	W
After reset	0	0	0	0	0	0	0	0

Bit[4:0] **P4CON[7:0]:** P4.n configuration control bits.
0 = P4.n can be an analog input (ADC input) or digital I/O pins.
1 = P4.n is pure analog input, can't be a digital I/O pin.

✷ ***Note: When Port 4.n is general I/O port not ADC channel, P4CON.n must set to "0" or the Port 4.n digital I/O signal would be isolated.***

13.5 ADC OPERATION EXAMLPE

- **ADC CONFIGURATION:**

```
; Reset ADC.
        CLR     ADM             ; Clear TC0M register.

; Set ADC clock rate and ADC resolution.
        MOV     A, #0nmn0000b   ; nn: ADCKS[1:0] for ADC clock rate.
        B0MOV   ADR, A          ; m: ADLEN for ADC reolution.

; Set ADC high reference voltage source.
        B0BCLR  FAVREFH         ; Internal Vdd.
or
        B0BSET  FAVREFH         ; External reference voltage.

; Set ADC input channel configuration.
        MOV     A, #value1      ; Set P4CON for ADC input channel.
        B0MOV   P4CON, A
        MOV     A, #value2      ; Set ADC input channel as input mode.
        B0MOV   P4M, A
        MOV     A, #value3      ; Disable ADC input channel's internal pull-up resistor.
        B0MOV   P4UR, A

; Enable ADC.
        B0BSET  FADCENB

; Execute ADC 100us warm-up time delay loop.
        CALL    100usDLY        ; 100us delay loop.

; Select ADC input channel.
        MOV     A, #value       ; Set ADCHS[2:0] for ADC input channel selection.
        OR      ADM, A

; Enable ADC input channel.
        B0BSET  FGCHS

; Enable ADC interrupt function.
        B0BCLR  FADCIRQ         ; Clear ADC interrupt flag.
        B0BSET  FADCIEN         ; Enable ADC interrupt function.

; Start to execute ADC converting.
        B0BSET  FADS
```

✸ ***Note:***

1. ***When ADENB is enabled, the system must be delay 100us to be the ADC warm-up time by program, and then set ADS to do ADC converting. The 100us delay time is necessary after ADENB setting (not ADS setting), or the ADC converting result would be error. Normally, the ADENB is set one time when the system under normal run condition, and do the delay time only one time.***
2. ***In power saving situation like power down mode and green mode, and not using ADC function, to disable ADC by program is necessary to reduce power consumption.***

- **ADC CONVERTING OPERATION:**

; ADC Interrupt disable mode.

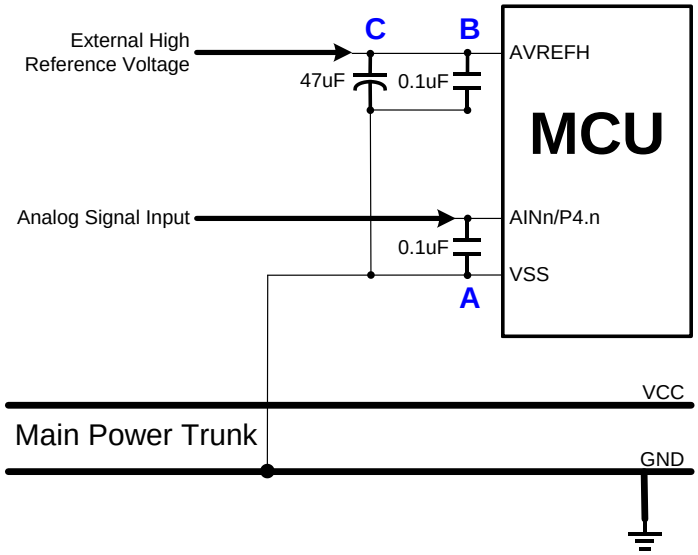
```
@@:
        B0BTS1      FEOC        ; Check ADC processing flag.
        JMP         @B          ; EOC=0: ADC is processing.
        B0MOV       A, ADB      ; EOC=1: End of ADC processing. Process ADC result.
        B0MOV       BUF1,A
        MOV         A, #00001111b
        AND         A, ADR
        B0MOV       BUF2,A
        …                       ; End of processing ADC result.
        CLR         FEOC        ; Clear ADC processing flag for next ADC converting.
```

; ADC Interrupt enable mode.

```
        ORG 8                   ; Interrupt vector.
INT_SR:                         ; Interrupt service routine.
        PUSH
        B0BTS1      FADCIRQ     ; Check ADC interrupt flag.
        JMP         EXIT_INT    ; ADCIRQ=0: Not ADC interrupt request.
        B0MOV       A, ADB      ; ADCIRQ=1: End of ADC processing. Process ADC result.
        B0MOV       BUF1,A
        MOV         A, #00001111b
        AND         A, ADR
        B0MOV       BUF2,A
        …                       ; End of processing ADC result.
        CLR         FEOC        ; Clear ADC processing flag for next ADC converting.
        JMP         INT_EXIT

INT_EXIT:
        POP
        RETI                    ; Exit interrupt service routine.
```

✸ ***Note: ADS is cleared when the end of ADC converting automatically. EOC bit indicates ADC processing status immediately and is cleared when ADS = 1. Users needn't to clear ADS bit by program.***

13.6 ADC APPLICATION CIRCUIT

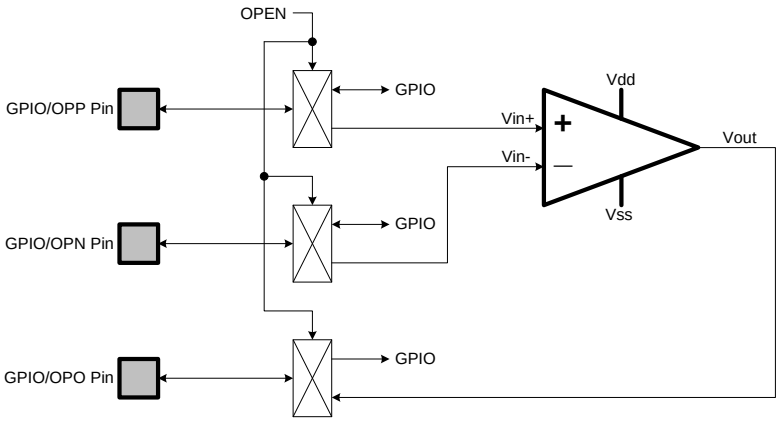


The analog signal is inputted to ADC input pin “AINn/P4.n”. The ADC input signal must be through a 0.1uF capacitor “A”. The 0.1uF capacitor is set between ADC input pin and VSS pin, and must be on the side of the ADC input pin as possible. Don’t connect the capacitor’s ground pin to ground plain directly, and must be through VSS pin. The capacitor can reduce the power noise effective coupled with the analog signal.

If the ADC high reference voltage is from external voltage source, the external high reference is connected to AVREFH pin (P4.0). The external high reference source must be through a 47uF ”C” capacitor first, and then 0.1uF capacitor “B”. These capacitors are set between AVREFH pin and VSS pin, and must be on the side of the AVREFH pin as possible. Don’t connect the capacitor’s ground pin to ground plain directly, and must be through VSS pin.

14 RAIL to RAIL OP AMPLIFER

14.1 OVERVIEW



The micro-controller builds in one OP AMP which is Rail-to-Rail structure. That means the input/output voltage is real from Vdd~Vss. The Rail-to-Rail OP AMP pins are shared with GPIO controlled by OPEN bit. When OPEN=0, OP AMP pins are GPIO mode. When OPEN=1, GPIO pins switch to OP AMP and isolate GPIO path. OP pins selection table is as following.

OP No.	OPEN	OP Positive Pin	OP Negative Pin	OP Output Pin
OP	OPEN=0	All pins are GPIO mode. OP amp is disabled.		
	OPEN=1	OPP (Vin+)	OPN (Vin-)	OPO (Vout)

✸ ***Note: If OP-amp disables, these pins exchange to GPIO mode and last status.***

14.2 OP AMP REGISTER

09FH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPM	-	-	-	-	-	-	-	OPEN
Read/Write	-	-	-	-	-	-	-	R/W
After Reset	-	-	-	-	-	-	-	0

Bit 0 **OPEN:** OP Amp control bit.
0 = Disable. P1.0, P1.1, P1.2 are GPIO mode.
1 = Enable. P1.0, P1.1, P1.2 are OP Amp pins.

15 INSTRUCTION TABLE

Field	Mnemonic		Description	C	DC	Z	Cycle
MOVE	MOV	A,M	A ← M	-	-	√	1
	MOV	M,A	M ← A	-	-	-	1
	B0MOV	A,M	A ← M (bank 0)	-	-	√	1
	B0MOV	M,A	M (bank 0) ← A	-	-	-	1
	MOV	A,I	A ← I	-	-	-	1
	B0MOV	M,I	M ← I, "M" only supports 0x80~0x87 registers (e.g. PFLAG,R,Y,Z…)	-	-	-	1
	XCH	A,M	A ←→M	-	-	-	1+N
	B0XCH	A,M	A ←→M (bank 0)	-	-	-	1+N
	MOVC		R, A ← ROM [Y,Z]	-	-	-	2
ARITHMETIC	ADC	A,M	A ← A + M + C, if occur carry, then C=1, else C=0	√	√	√	1
	ADC	M,A	M ← A + M + C, if occur carry, then C=1, else C=0	√	√	√	1+N
	ADD	A,M	A ← A + M, if occur carry, then C=1, else C=0	√	√	√	1
	ADD	M,A	M ← A + M, if occur carry, then C=1, else C=0	√	√	√	1+N
	B0ADD	M,A	M (bank 0) ← M (bank 0) + A, if occur carry, then C=1, else C=0	√	√	√	1+N
	ADD	A,I	A ← A + I, if occur carry, then C=1, else C=0	√	√	√	1
	SBC	A,M	A ← A - M - /C, if occur borrow, then C=0, else C=1	√	√	√	1
	SBC	M,A	M ← A - M - /C, if occur borrow, then C=0, else C=1	√	√	√	1+N
	SUB	A,M	A ← A - M, if occur borrow, then C=0, else C=1	√	√	√	1
	SUB	M,A	M ← A - M, if occur borrow, then C=0, else C=1	√	√	√	1+N
	SUB	A,I	A ← A - I, if occur borrow, then C=0, else C=1	√	√	√	1
	DAA		To adjust ACC's data format from HEX to DEC.	√	-	-	1
	MUL	A,M	R, A ← A * M, The LB of product stored in Acc and HB stored in R register. ZF affected by Acc.	-	-	√	2
LOGIC	AND	A,M	A ← A and M	-	-	√	1
	AND	M,A	M ← A and M	-	-	√	1+N
	AND	A,I	A ← A and I	-	-	√	1
	OR	A,M	A ← A or M	-	-	√	1
	OR	M,A	M ← A or M	-	-	√	1+N
	OR	A,I	A ← A or I	-	-	√	1
	XOR	A,M	A ← A xor M	-	-	√	1
	XOR	M,A	M ← A xor M	-	-	√	1+N
	XOR	A,I	A ← A xor I	-	-	√	1
PROCESS	SWAP	M	A (b3~b0, b7~b4) ←M(b7~b4, b3~b0)	-	-	-	1
	SWAPM	M	M(b3~b0, b7~b4) ← M(b7~b4, b3~b0)	-	-	-	1+N
	RRC	M	A ← RRC M	√	-	-	1
	RRCM	M	M ← RRC M	√	-	-	1+N
	RLC	M	A ← RLC M	√	-	-	1
	RLCM	M	M ← RLC M	√	-	-	1+N
	CLR	M	M ← 0	-	-	-	1
	BCLR	M.b	M.b ← 0	-	-	-	1+N
	BSET	M.b	M.b ← 1	-	-	-	1+N
	B0BCLR	M.b	M(bank 0).b ← 0	-	-	-	1+N
	B0BSET	M.b	M(bank 0).b ← 1	-	-	-	1+N
BRANCH	CMPRS	A,I	ZF,C ← A - I, If A = I, then skip next instruction	√	-	√	1 + S
	CMPRS	A,M	ZF,C ← A – M, If A = M, then skip next instruction	√	-	√	1 + S
	INCS	M	A ← M + 1, If A = 0, then skip next instruction	-	-	-	1+ S
	INCMS	M	M ← M + 1, If M = 0, then skip next instruction	-	-	-	1+N+S
	DECS	M	A ← M - 1, If A = 0, then skip next instruction	-	-	-	1+ S
	DECMS	M	M ← M - 1, If M = 0, then skip next instruction	-	-	-	1+N+S
	BTS0	M.b	If M.b = 0, then skip next instruction	-	-	-	1 + S
	BTS1	M.b	If M.b = 1, then skip next instruction	-	-	-	1 + S
	B0BTS0	M.b	If M(bank 0).b = 0, then skip next instruction	-	-	-	1 + S
	B0BTS1	M.b	If M(bank 0).b = 1, then skip next instruction	-	-	-	1 + S
	JMP	d	PC15/14 ← RomPages1/0, PC13~PC0 ← d	-	-	-	2
	CALL	d	Stack ← PC15~PC0, PC15/14 ← RomPages1/0, PC13~PC0 ← d	-	-	-	2
MISC	RET		PC ← Stack	-	-	-	2
	RETI		PC ← Stack, and to enable global interrupt	-	-	-	2
	PUSH		To push ACC and PFLAG (except NT0, NPD bit) into buffers.	-	-	-	1
	POP		To pop ACC and PFLAG (except NT0, NPD bit) from buffers.	√	√	√	1
	NOP		No operation	-	-	-	1

***Note:** 1. "M" is system register or RAM. If "M" is system registers then "N" = 0, otherwise "N" = 1.*
2. If branch condition is true then "S = 1", otherwise "S = 0".

16 ELECTRICAL CHARACTERISTIC

16.1 ABSOLUTE MAXIMUM RATING

Supply voltage (Vdd)..... - 0.3V ~ 6.0V
Input in voltage (Vin)..... Vss – 0.2V ~ Vdd + 0.2V
Operating ambient temperature (Topr)
SN8P2743K, SN8P2743S, SN8P2742P, SN8P2742S, SN8P27411P, SN8P27411S..... -20°C ~ + 70°C
SN8P2743KD, SN8P2743SD, SN8P2742PD, SN8P2742SD. SN8P27411PD, SN8P27411SD..... –40°C ~ + 85°C
Storage ambient temperature (Tstor) ..... –40°C ~ + 125°C

16.2 ELECTRICAL CHARACTERISTIC

- **DC CHARACTERISTIC**

(All of voltages refer to Vss, Vdd = 5.0V, Fosc = 4MHz,Fcpu=1MHz,ambient temperature is 25℃ unless otherwise note.)

PARAMETER	SYM.	DESCRIPTION		MIN.	TYP.	MAX.	UNIT
Operating voltage	Vdd	Normal mode. Fcpu = 1MHz		2.2	-	5.5	V
		Normal mode. Fcpu = 4MHz		2.4	-	5.5	V
RAM Data Retention voltage	Vdr			1.5	-	-	V
*Vdd rise rate	Vpor	Vdd rise rate to ensure internal power-on reset		0.05	-	-	V/ms
Input Low Voltage	ViL1	All input ports		Vss	-	0.3Vdd	V
	ViL2	Reset pin		Vss	-	0.2Vdd	V
Input High Voltage	ViH1	All input ports		0.7Vdd	-	Vdd	V
	ViH2	Reset pin		0.8Vdd	-	Vdd	V
Reset pin leakage current	Ilekg	Vin = Vdd		-	-	2	uA
I/O port input leakage current	Ilekg	Pull-up resistor disable, Vin = Vdd		-	-	2	uA
I/O port pull-up resistor	Rup	Vin = Vss , Vdd = 3V		100	200	300	KΩ
		Vin = Vss , Vdd = 5V		50	100	150	
I/O output source current	IoH	Vop = Vdd – 0.5V		8	-	-	mA
sink current	IoL	Vop = Vss + 0.5V		8	-	-	
*INTn trigger pulse width	Tint0	INT0 interrupt request pulse width		2/fcpu	-	-	cycle
Supply Current (Disable ADC, OP-amp, Comparator)	Idd1	Run Mode (No loading)	Vdd= 3V, Fcpu = 4MHz	-	2	-	mA
			Vdd= 5V, Fcpu = 4MHz	-	4	-	mA
			Vdd= 3V, Fcpu = 1MHz	-	1.5	-	mA
			Vdd= 5V, Fcpu = 1MHz	-	3	-	mA
			Vdd= 3V, Fcpu = 32KHz	-	20	-	uA
			Vdd= 5V, Fcpu = 32KHz	-	45	-	uA
	Idd2	Slow Mode	Vdd= 3V, ILRC=16KHz	-	3.5	-	uA
			Vdd= 5V, ILRC=32KHz	-	10	-	uA
	Idd3	Sleep Mode	Vdd= 5V/3V	-	1	2	uA
	Idd4	Green Mode (No loading, Watchdog Disable)	Vdd= 3V, IHRC=16MHz	-	0.35	-	mA
			Vdd= 5V, IHRC=16MHz	-	0.55	-	mA
			Vdd= 3V, Ext. 32KHz X'tal	-	6	-	uA
			Vdd= 5V, Ext. 32KHz X'tal	-	18	-	uA
			Vdd= 3V, ILRC=16KHz	-	3	-	uA
			Vdd= 5V, ILRC=32KHz	-	5.5	-	uA
Internal High Oscillator Freq.	Fihrc	Internal High RC (IHRC)	*25℃*, Vdd=2.2V~ 5.5V Fcpu=Fhosc/4~Fhosc/16	15.68	16	16.32	MHz
			-40℃~85℃,Vdd=2.4V~ 5.5V Fcpu=Fhosc/4~Fhosc/16	15.2	16	16.8	MHz
LVD Voltage	Vdet0	Low voltage reset level. *25℃*		1.9	2.0	2.1	V
		Low voltage reset level. *-40℃~85℃*		1.8	2.0	2.3	V
	Vdet1	Low voltage reset/indicator level. *25℃*		2.3	2.4	2.5	V
		Low voltage reset/indicator level. *-40℃~85℃*		2.2	2.4	2.7	V
	Vdet2	Low voltage reset/indicator level. *25℃*		3.5	3.6	3.7	V
		Low voltage reset/indicator level. *-40℃~85℃*		3.3	3.6	3.9	V

" *" These parameters are for design reference, not tested.

ADC CHARACTERISTIC

(All of voltages refer to Vss, Vdd = 5.0V, Fosc = 4MHz,Fcpu=1MHz,ambient temperature is 25℃ unless otherwise note.)

PARAMETER	SYM.	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
AIN0 ~ AIN7 input voltage	Vani	Vdd = 5.0V	0	-	Avrefh	V
ADC reference Voltage	Vref		2	-	-	V
*ADC enable time	Tast	Ready to start convert after set ADENB = "1"	100	-	-	us
*ADC current consumption	I_{ADC}	Vdd=5.0V	-	0.6	-	mA
		Vdd=3.0V	-	0.4	-	mA
ADC Clock Frequency	F_{ADCLK}	VDD=5.0V	-	-	8M	Hz
		VDD=3.0V	-	-	5M	Hz
ADC Conversion Cycle Time	F_{ADCYL}	VDD=2.4V~5.5V	64	-	-	$1/F_{ADCLK}$
ADC Sampling Rate (Set FADS=1 Frequency)	F_{ADSMP}	VDD=5.0V	-	-	125	K/sec
		VDD=3.0V	-	-	80	K/sec
Differential Nonlinearity	DNL	VDD=5.0V , AVREFH=3.2V, F_{ADSMP} =7.8K	±1	-	-	LSB
Integral Nonlinearity	INL	VDD=5.0V , AVREFH=3.2V, F_{ADSMP} =7.8K	±2	-	-	LSB
No Missing Code	NMC	VDD=5.0V , AVREFH=3.2V, F_{ADSMP} =7.8K	10	11	12	Bits
ADC offset Voltage	$V_{ADCoffset}$	Non-trimmed	-10	0	+10	mV
		Trimmed	-2	0	+2	mV

" *" These parameters are for design reference, not tested.

OP AMP CHARACTERISTIC

(All of voltages refer to Vss, Vdd = 5.0V, Slow Mode , High Clock disable,ambient temperature is 25℃ unless otherwise note.)

PARAMETER	SYM.	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
*Supply Current	Iop	Unit Gain Buffer. Vdd=3V. OPP=Vss.	-	130	-	uA
		Unit Gain Buffer. Vdd=5V. OPP=Vss.	-	150	-	uA
Common Mode Input Voltage Range	Vcmr	Vdd=5.0V	Vss-0.3	-	Vdd+0.3	V
Input Offset Voltage	Vos	Vcm=Vss	-3	-	+3	mV
Power Supply Rejection Ratio	PSRR	Vcm=Vss	50	-	70	dB
Common Mode Rejection Ratio	CMRR	Vcm=-0.3V~2.5V. Vdd=5V.	50	-	80	dB
Open-Loop Gain (Large Signal)	Aol	Vout=0.2V~Vdd-0.2V. Vcm=Vss.	90	110	-	dB
Maximum Output Voltage Swing	Vol, Voh	0.5V output overdrive.	Vss+15mv		Vdd-15mv	V
Output Short Current	Isc	Unit Gain Buffer. Vo=Vss, Vdd=VPP=3V.	-17	-	+17	mA
		Unit Gain Buffer. Vo=Vss, Vdd=VPP=5V.	-45	-	+45	mA
Output Slew Rate	Tosr	Vo = Vss to Vdd or Vdd to Vss.	3	-	5	us

" *" These parameters are for design reference, not tested.

COMPARATOR CHARACTERISTIC

(All of voltages refer to Vss, Vdd = 5.0V, Fosc = 4MHz,Fcpu=1MHz,ambient temperature is 25℃ unless otherwise note.)

PARAMETER	SYM.	DESCRIPTION		MIN.	TYP.	MAX.	UNIT
Power Supply Range	Vcmp			2.0		5.5	V
Supply Current	Icm	Vdd=3V. Internal reference disables.				70	uA
		Vdd=5V. Internal reference disables.				70	uA
Quiescent Current	Iq	Iout=0		0.3	0.6	1	uA
Input Offset Voltage	Vos	Vcm=Vss		-5		+5	mV
Response Time	Trs	Positive input voltage = 1/2*Vdd. Negative input voltage transitions from Vss to Vdd.				100	ns
Output Slew Rate	Tosr	Comparator output voltage transitions from Vss to Vdd.	Vdd=3V			100	ns
			Vdd=5V			100	ns
		Comparator output voltage transitions from Vdd to Vss.	Vdd=3V			100	ns
			Vdd=5V			100	ns
Common Mode Input Voltage Range	Vcmr	Vdd=5.0V		Vss+0.5		Vdd-0.5	V

" *" These parameters are for design reference, not tested.

16.3 CHARACTERISTIC GRAPHS

The Graphs in this section are for design guidance, not tested or guaranteed. In some graphs, the data presented are outside specified operating range. This is for information only and devices are guaranteed to operate properly only within the specified range (-40℃~+85℃ curves are for design reference).

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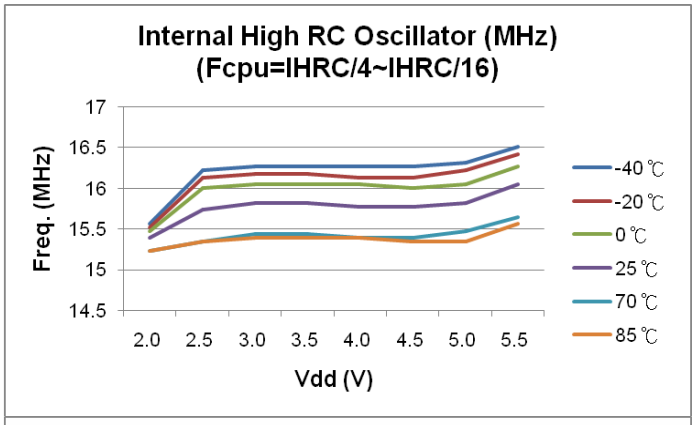
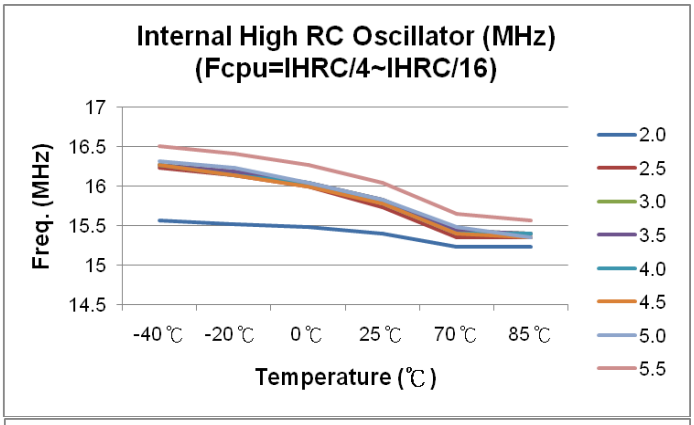
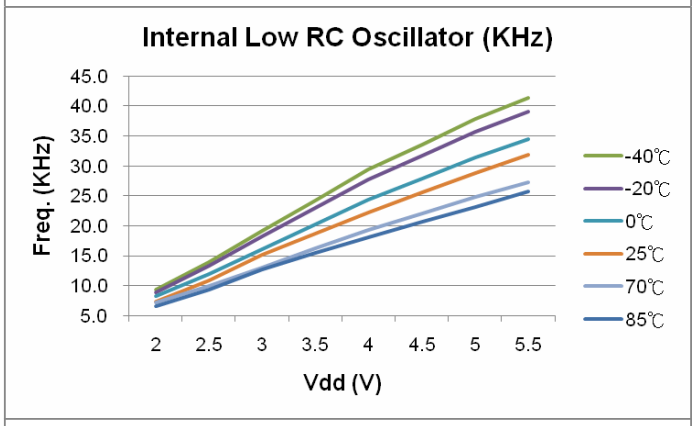
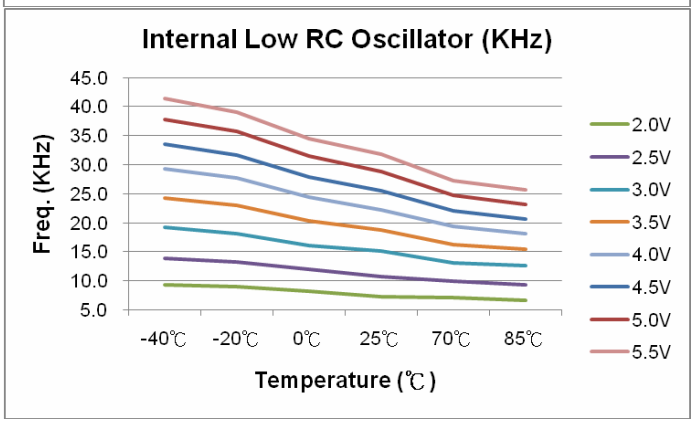
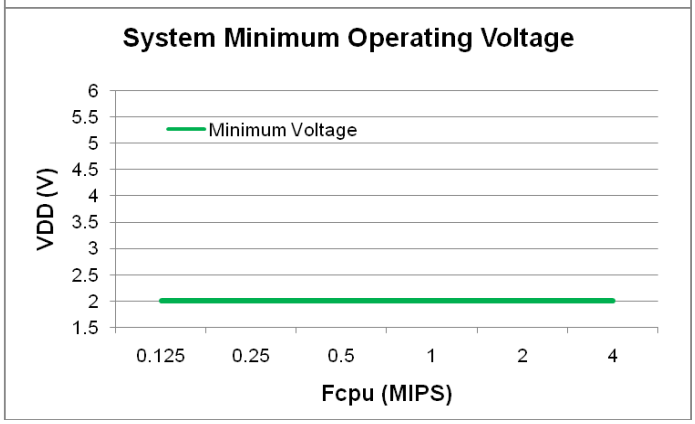










17 DEVELOPMENT TOOL

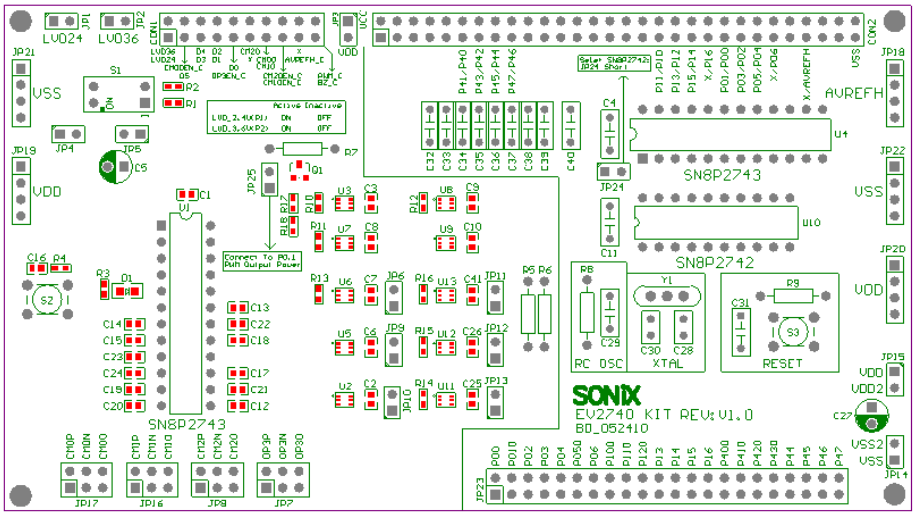
SONIX provides ICE (in circuit emulation), IDE (Integrated Development Environment) and EV-kit for SN8P2740 development. ICE and EV-kit are external hardware devices, and IDE is a friendly user interface for firmware development and emulation. These development tools' version is as following.

- **ICE: SN8ICE2K Plus II. (Please install 16MHz crystal in ICE to implement IHRC emulation.)**
- **ICE emulation speed maximum: 8 MIPS @ 5V (e.g. 16Mhz crystal, Fcpu = Fosc/2).**
- **EV-kit: EV2740 KIT REV: V1.0.**
- **IDE: SONiX IDE M2IDE_V129 and later version.**
- **Writer: MPIII writer.**
- **Writer transition board: SN8P2742 / SN8P2743**

17.1 SN8P2740 EV-KIT

SONIX provides SN8P2740 series MCU which includes PWM, ADC, Comparator and OP analog functions. These functions aren't built in SN8ICE2K Plus 2. To emulate the functions must be through SN8P2743 real chip. The real chip provides an EV-KIT to achieve PWM and the analog functions emulations. For SN8P2743/42 ICE emulation, the EV-Kit includes OP/Comparator/PWM/ADC/LVD2.4V/3.6V and switch circuits.

EV2740 KIT PCB Outline:



- CON1: Connect to SN8ICE2K Plus 2 JP3 (EV-KIT communication bus with ICE, control signal, and the others).
- CON2: Connect to SN8ICE2K Plus 2 CON1 (includes GPIO, EV-KIT control signal, and the others).
- S1: LVD24V/LVD36V control switch. To emulate LVD2.4V flag/reset function and LVD3.6V/flag function

Switch No.	ON	OFF
LVD24 (1)	LVD 2.4V Active	LVD 2.4V Inactive
LVD36 (2)	LVD 3.6V Active	LVD 3.6V Inactive

- S2: SN8P2743 EV-chip reset key. If EV-KIT active fail, press S2 to reset EV-KIT Real Chip (U1).
- JP23: GPIO connector.
- JP18: Using ADC function before, SN8ICE2K Plus 2 AVREFH/VDD jumper pin must be removed. If ADC external reference voltage function enable, JP18 (AVREFH) or P40O pin is external reference voltage input.
- JP17: Observe CMP0 input/output voltage.
- JP16: Observe CMP1 input/output voltage.
- JP8: Observe CMP2 input/output voltage.
- JP7: Observe OP-Amp input/output voltage (OP3P = OPP, OP3N = OPN, OP3O = OPO).
- U1: SN8P2743 EV-chip for analog functions emulation.

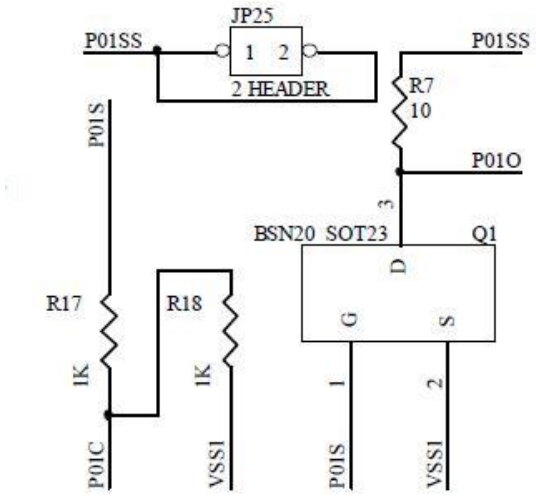
- U4: SN8P2743 DIP form connector for connecting to user's target board.

VSS	1	U	24	VDD
XIN/P0.6	2		23	P4.7/AIN7
XOUT/P0.5/BZ	3		22	P4.6/AIN6
RST/VPP/P0.4	4		21	P4.5/AIN5
P0.0/INT0	5		20	P4.4/AIN4
P0.1/PWM0	6		19	P4.3/AIN3/CM0O
P0.2/CM0P	7		18	P4.2/AIN2/CM1O
P0.3/CM0N	8		17	P4.1/AIN1/CM2O
P1.6/CM1P	9		16	P4.0/AIN0/AVREFH
P1.5/CM1N	10		15	P1.0/OPN
P1.4/CM2P	11		14	P1.1/OPP
P1.3/CM2N	12		13	P1.2/OPO

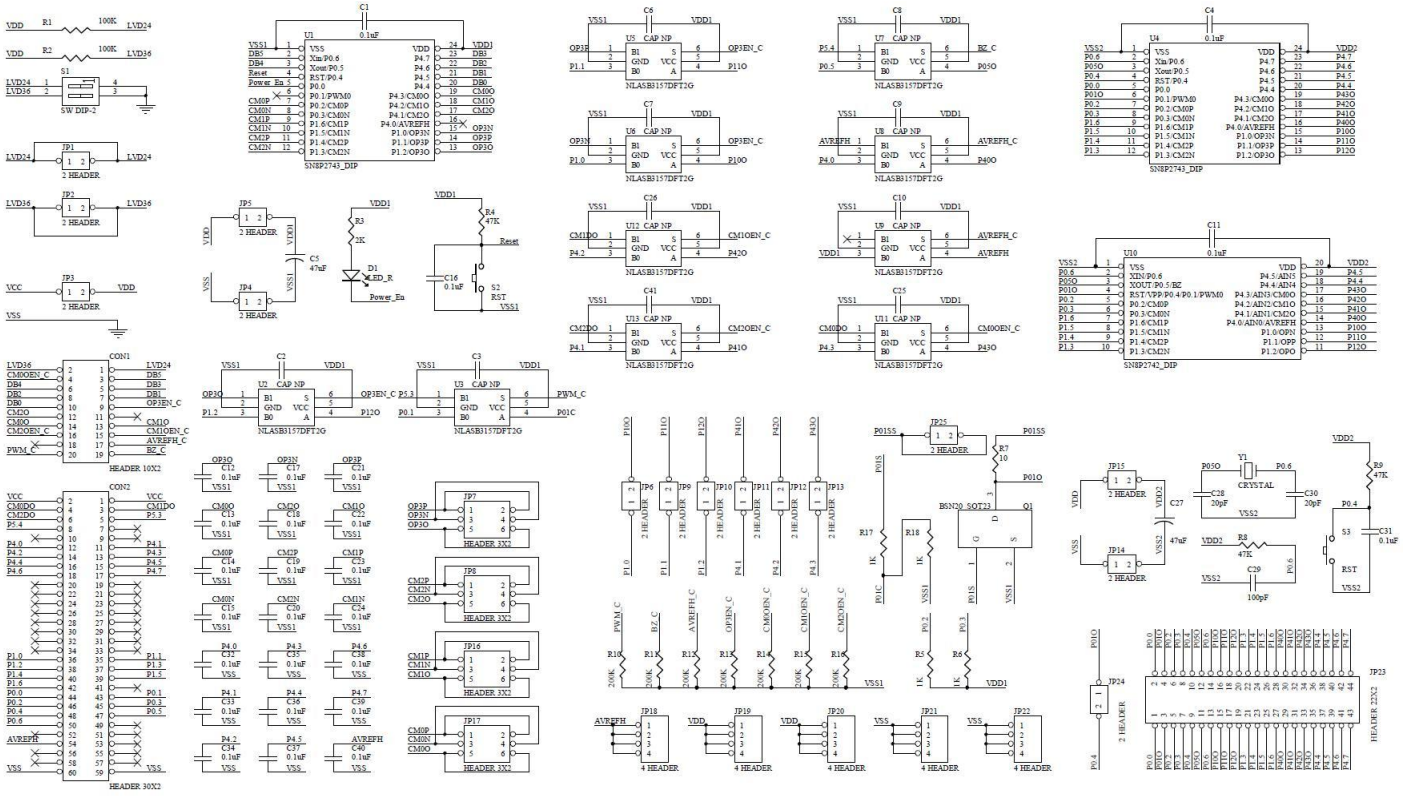
- U10: SN8P2742 DIP form connector for connecting to user's target board.

VSS	1	U	20	VDD
XIN/P0.6	2		19	P4.5/AIN5
XOUT/P0.5/BZ	3		18	P4.4/AIN4
RST/VPP/P0.4/ P0.1/PWM0	4		17	P4.3/AIN3/CM0O
P0.2/CM0P	5		16	P4.2/AIN2/CM1O
P0.3/CM0N	6		15	P4.1/AIN1/CM2O
P1.6/CM1P	7		14	P4.0/AIN0/AVREFH
P1.5/CM1N	8		13	P1.0/OPN
P1.4/CM2P	9		12	P1.1/OPP
P1.3/CM2N	10		11	P1.2/OPO

- C32~C39: Connect 0.1uF capacitors to AIN0~AIN7 input which are ADC channel 0~7 bypass capacitors.
- C40: Connect 0.1uF capacitors to AVREFH input which are ADC reference voltage bypass capacitors.
- C13: CMP0 output pin's 0.1F bypass capacitor.
- C22: CMP1 output pin's 0.1F bypass capacitor.
- C18: CMP2 output pin's 0.1F bypass capacitor.
- C17: OP-Amp negative input pin's 0.1F bypass capacitor.
- C21: OP-Amp positive input pin's 0.1F bypass capacitor.
- C12: OP-Amp output pin's 0.1F bypass capacitor.
- C14: CMP0 positive input pin's 0.1F bypass capacitor.
- C15: CMP0 negative input pin's 0.1F bypass capacitor.
- C23: CMP1 positive input pin's 0.1F bypass capacitor.
- C24: CMP1 negative input pin's 0.1F bypass capacitor.
- C19: CMP2 positive input pin's 0.1F bypass capacitor.
- C20: CMP2 negative input pin's 0.1F bypass capacitor.
- JP24: Chip select (SN8P2742: Jumper short, SN8P2743: Open).
- JP25: P0.1 output MOS circuit power source

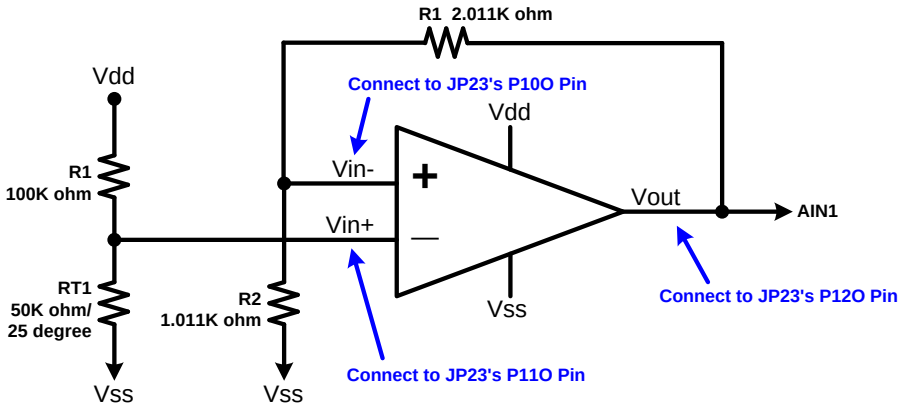


EV2740 KIT schematic:



17.2 ICE AND EV-KIT APPLICATION NOTIC

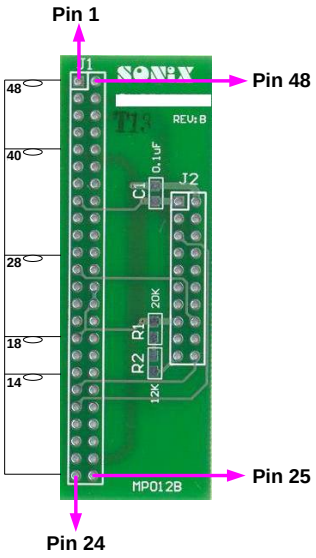
1. SN8ICE2K Plus 2 power switch must be turned off before you connect the EV2740 KIT to SN8ICE2K Plus 2.
2. Connect EV-KIT's CON1/CON2 to ICE's JP3/CON1.
3. SN8ICE2K Plus 2's AVREFH/VDD jumper pin must be removed.
4. Turn on SN8ICE2K Plus power switch after user had finished step 1~3.
5. User observes EV-KIT's power LED (D1) is light after turn on SN8ICE2K Plus power switch. If LED (D1) is not light, that means, user contact to SONIX's agent right now.
6. If user program select chip SN8P2743, JP24 open. Or user program select chip SN8P2742, JP24 short (Jumper).
7. **It is necessary to connect 16MHz crystal in ICE for IHRC_16M mode emulation.**
8. When ADC function enable. The ADM's bit 3 (FAVREFH) is set as High. P40O or JP18 (AVREFH) will be external reference voltage input pin.
9. When ADC function enable. The ADM's bit 3 (FAVREFH) is set as Low. P40O will be analog signal input pin. JP18 (AVREFH) do not connect power device.
10. Observe ADC internal or external reference voltage is JP18(AVREFH).
11. The OP-Amp of SN8P2743 application circuit is as the below figure (OP-AMP connect).



12. When SN8P2743's OP-AMP function enable as the above figure. P12O (JP23) is OP-AMP's output. P11 (JP23) is OP-AMP's non-inverse. P10O (JP23) is OP-AMP's inverse.
13. If user wants to measure OP-AMP V+ / V- / Vo voltage as the above figure, the real OP-AMP's inverse voltage is OP3N (JP7). The real OP-AMP's non-inverse voltage is OP3P (JP7). The real OP-AMP's output voltage is OP3O (JP7).
14. Why OP-AMP connecting is different with measurement, because OP-AMP series connection with analog switch internal resistor (Ron).
15. When CMP0 function enable. The CM0P/CM0N (JP17) will be external analog signal input pin. The P43O (JP23) will be CMP0's output result.
16. When CMP1 function enable. The CM1P/CM1N (JP16) will be external analog signal input pin. The P42O (JP23) will be CMP1's output result.
17. When CMP2 function enable. The CM2P/CM1N (JP8) will be external analog signal input pin. The P41O (JP23) will be CMP2's output result.
18. When user uses CMP0~CMP2's CM0P/CM0N/CM1P/CM1N/CM2P/CM2N analog function, user must be connecting to JP17/JP16/JP8. When user uses CMP0~CMP2's CM0P/CM0N/CM0O/CM1P/CM1N/CM1O/CM2P/CM2N/CM2O logic function, user must be connecting to JP23's P02/P03/P43O/P16/P15/P42O/P14/P13/P41O.
19. When user uses TC0 special function (Pulse generator function and TC0 clock source is Fcpu.) in ICE emulation. If user sets IDE breakpoint, the PWM plus generator output status will be unknown (Fcpu stop).
20. When user uses TC0 special function (Pulse generator function and TC0 clock source is Fhosc.) in ICE emulation. If user sets IDE breakpoint, the PWM plus generator output will be finished (Fhosc still work). And the PWM pulse generator output will be back to idle status.
21. When user uses CMP1 and CMP2's de-bounce time control (CM1D3~CM1D0, CM2D3~CM2D0 and clock source is Fcpu) in ICE emulation. If user sets IDE breakpoint, the CM0O output will be effected (Fcpu stop)
22. When user uses CMP0's de-bounce time control (CM0D3~CM0D0 and clock source is Fhosc) in ICE emulation. If user sets IDE breakpoint, the CM0O output will be not effected (Fhosc still work).

18 OTP PROGRAMMING PIN

18.1 WRITER TRANSITION BOARD SOCKET PIN ASSIGNMENT



JP3 (Mapping to 48-pin text tool)

DIP 1	1	48	DIP48
DIP 2	2	47	DIP47
DIP 3	3	46	DIP46
DIP 4	4	45	DIP45
DIP 5	5	44	DIP44
DIP 6	6	43	DIP43
DIP 7	7	42	DIP42
DIP 8	8	41	DIP41
DIP 9	9	40	DIP40
DIP10	10	39	DIP39
DIP11	11	38	DIP38
DIP12	12	37	DIP37
DIP13	13	36	DIP36
DIP14	14	35	DIP35
DIP15	15	34	DIP34
DIP16	16	33	DIP33
DIP17	17	32	DIP32
DIP18	18	31	DIP31
DIP19	19	30	DIP30
DIP20	20	29	DIP29
DIP21	21	28	DIP28
DIP22	22	27	DIP27
DIP23	23	26	DIP26
DIP24	24	25	DIP25

Writer JP1/JP2

VDD	1	2	VSS
CLK/PGCLK	3	4	CE
PGM/OTPCLK	5	6	OE/ShiftDat
D1	7	8	D0
D3	9	10	D2
D5	11	12	D4
D7	13	14	D6
VDD	15	16	VPP
HLS	17	18	RST
-	19	20	ALSB/PDB

JP1 for Writer transition board
JP2 for dice and >48 pin package

18.2 PROGRAMMING PIN MAPPING:

Programming Pin Information of SN8P2740 Series							
Chip Name		SN8P2743K(SKDIP)/S(SOP)			SN8P2742P(DIP)/S(SOP)		
Writer Connector		IC and JP3 48-pin text tool Pin Assignment					
JP1/JP2 Pin Number	JP1/JP2 Pin Name	IC Pin Number	IC Pin Name	JP3 Pin Number	IC Pin Number	IC Pin Name	JP3 Pin Number
1	VDD	24	VDD	36	20	VDD	34
2	GND	1	VSS	13	1	VSS	15
3	CLK	16	P4.0	28	14	P4.0	28
4	CE	-	-	-	-	-	-
5	PGM	20	P4.4	32	18	P4.4	32
6	OE	17	P4.1	29	15	P4.1	29
7	D1	-	-	-	-	-	-
8	D0	-	-	-	-	-	-
9	D3	-	-	-	-	-	-
10	D2	-	-	-	-	-	-
11	D5	-	-	-	-	-	-
12	D4	-	-	-	-	-	-
13	D7	-	-	-	-	-	-
14	D6	-	-	-	-	-	-
15	VDD	-	-	-	-	-	-
16	VPP	4	RST	16	4	RST	18
17	HLS	-	-	-	-	-	-
18	RST	-	-	-	-	-	-
19	-	-	-	-	-	-	-
20	ALSB/PDB	3	XOUT/P0.5	15	3	XOUT/P0.5	17

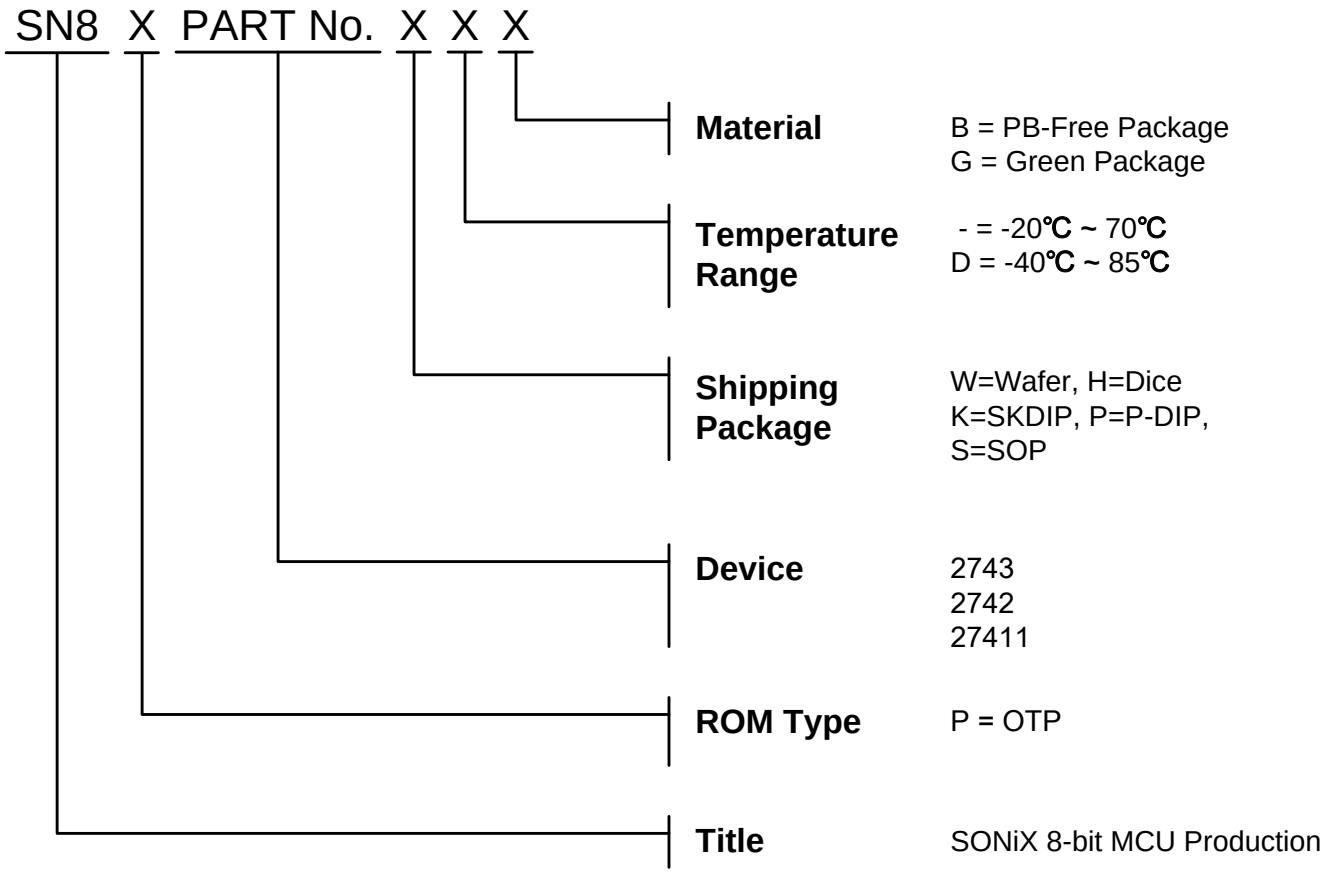
Programming Pin Information of SN8P2740 Series							
Chip Name		SN8P27411P(P-DIP)/S(SOP)					
Writer Connector		IC and JP3 48-pin text tool Pin Assignment					
JP1/JP2 Pin Number	JP1/JP2 Pin Name	IC Pin Number	IC Pin Name	JP3 Pin Number	IC Pin Number	IC Pin Name	JP3 Pin Number
1	VDD	1	VDD	17			
2	GND	13	VSS	29			
3	CLK	10	P4.0	26			
4	CE		-				
5	PGM	14	P4.4	30			
6	OE	11	P4.1	27			
7	D1		-				
8	D0		-				
9	D3		-				
10	D2		-				
11	D5		-				
12	D4		-				
13	D7		-				
14	D6		-				
15	VDD		-				
16	VPP	3	RST	19			
17	HLS		-				
18	RST		-				
19	-		-				
20	ALSB/PDB	2	XOUT/P0.5	18			

19 Marking Definition

19.1 INTRODUCTION

There are many different types in Sonix 8-bit MCU production line. This note listed the production definition of all 8-bit MCU for order or obtain information. This definition is only for Blank OTP MCU.

19.2 MARKING INDETIFICATION SYSTEM



19.3 MARKING EXAMPLE

- **Wafer, Dice:**

Name	ROM Type	Device	Package	Temperature	Material
S8P2743W	OTP	2743	Wafer	-20℃~70℃	-
SN8P2743H	OTP	2743	Dice	-20℃~70℃	-

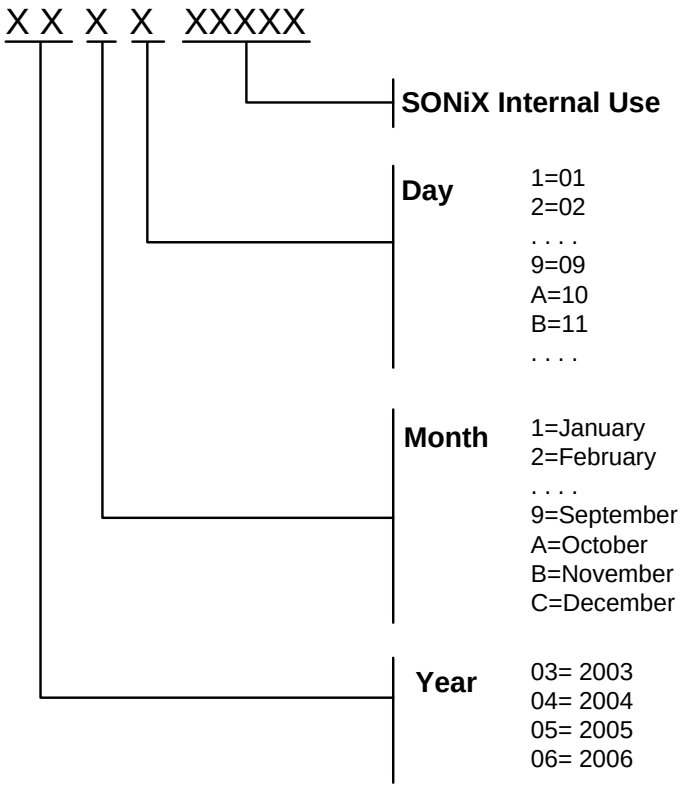
- **Green Package:**

Name	ROM Type	Device	Package	Temperature	Material
SN8P2743KG	OTP	2743	SK-DIP	-20℃~70℃	Green Package
SN8P2743SG	OTP	2743	SOP	-20℃~70℃	Green Package
SN8P2743KDG	OTP	2743	SK-DIP	-40℃~85℃	Green Package
SN8P2743SDG	OTP	2743	SOP	-40℃~85℃	Green Package
SN8P2742PG	OTP	2743	DIP	-20℃~70℃	Green Package
SN8P2742SG	OTP	2743	SOP	-20℃~70℃	Green Package
SN8P2742PDG	OTP	2743	DIP	-40℃~85℃	Green Package
SN8P2742SDG	OTP	2743	SOP	-40℃~85℃	Green Package
SN8P27411PG	OTP	2743	DIP	-20℃~70℃	Green Package
SN8P27411SG	OTP	2743	SOP	-20℃~70℃	Green Package
SN8P27411PDG	OTP	2743	DIP	-40℃~85℃	Green Package
SN8P27411SDG	OTP	2743	SOP	-40℃~85℃	Green Package

- **PB-Free Package:**

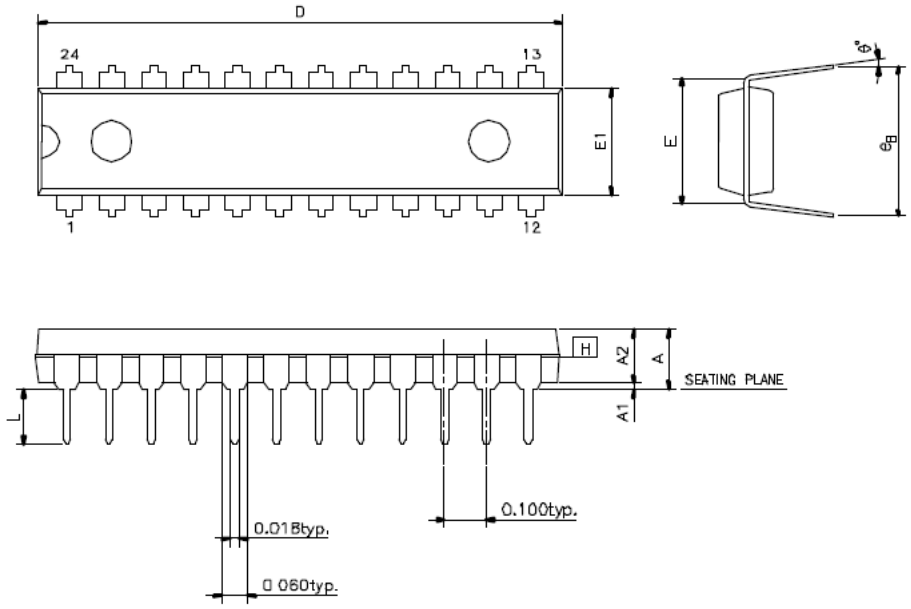
Name	ROM Type	Device	Package	Temperature	Material
SN8P2743KB	OTP	2743	SK-DIP	-20℃~70℃	PB-Free Package
SN8P2743SB	OTP	2743	SOP	-20℃~70℃	PB-Free Package
SN8P2743KDB	OTP	2743	SK-DIP	-40℃~85℃	PB-Free Package
SN8P2743SDB	OTP	2743	SOP	-40℃~85℃	PB-Free Package
SN8P2742PB	OTP	2743	DIP	-20℃~70℃	PB-Free Package
SN8P2742SB	OTP	2743	SOP	-20℃~70℃	PB-Free Package
SN8P2742PDB	OTP	2743	DIP	-40℃~85℃	PB-Free Package
SN8P2742SDB	OTP	2743	SOP	-40℃~85℃	PB-Free Package
SN8P27411PB	OTP	2743	DIP	-20℃~70℃	PB-Free Package
SN8P27411SB	OTP	2743	SOP	-20℃~70℃	PB-Free Package
SN8P27411PDB	OTP	2743	DIP	-40℃~85℃	PB-Free Package
SN8P27411SDB	OTP	2743	SOP	-40℃~85℃	PB-Free Package

19.4 DATECODE SYSTEM



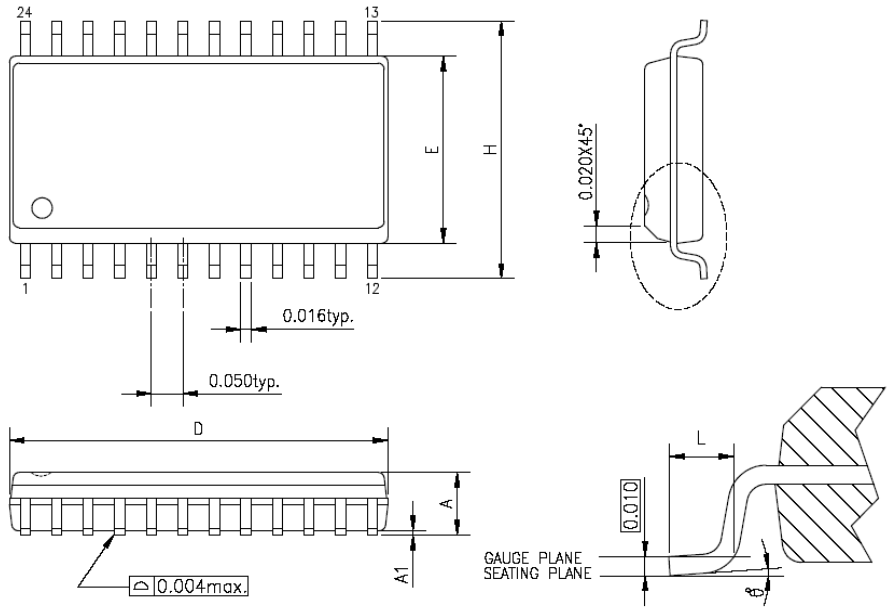
20 PACKAGE INFORMATION

20.1 SK-DIP 24 PIN



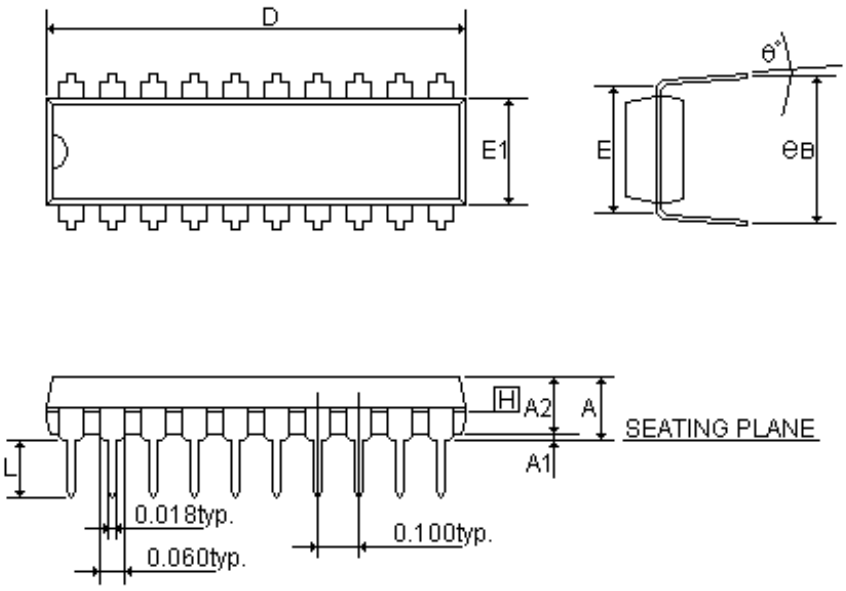
SYMBOLS	MIN	NOR	MAX	MIN	NOR	MAX
	(inch)			(mm)		
A	-	-	0.210	-	-	5.334
A1	0.015	-		0.381	-	-
A2	0.125	0.130	0.135	3.175	3.302	3.429
D	1.230	1.250	1.280	31.242	31.750	32.512
E	0.300 BSC			7.620 BSC		
E1	0.253	0.258	0.263	6.426	6.553	6.680
L	0.115	0.130	0.150	2.921	3.302	3.810
eB	0.335	0.355	0.375	8.509	9.017	9.525
θ°	0°	7°	15°	0°	7°	15°

20.2 SOP 24 PIN



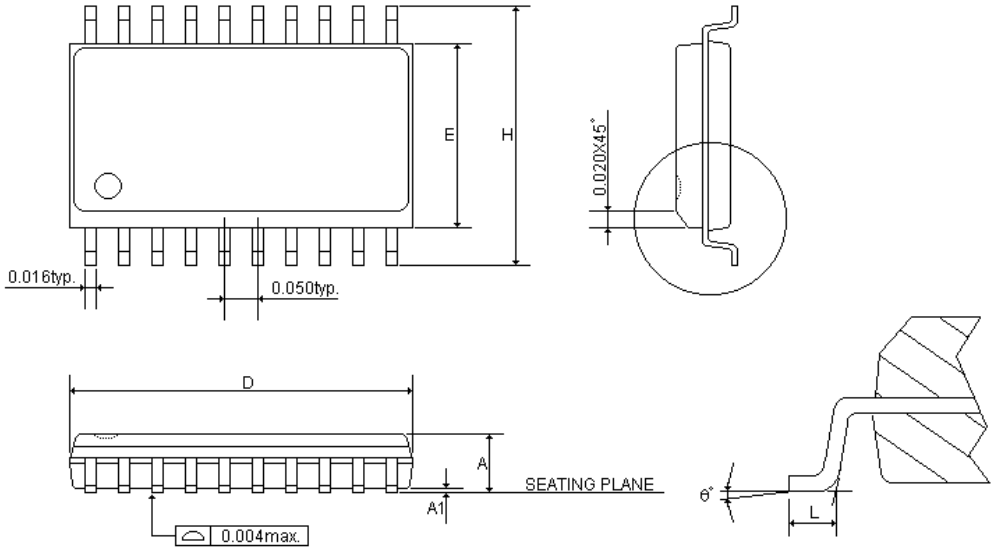
SYMBOLS	MIN	NOR	MAX	MIN	NOR	MAX
	(inch)			(mm)		
A	-	-	0.069	-	-	1.753
A1	0.004	-	0.010	0.102	-	0.254
D	0.612	0.618	0.624	15.545	15.697	15.850
E	0.292	0.296	0.299	7.417	7.518	7.595
H	0.405	0.412	0.419	10.287	10.465	10.643
L	0.021	0.031	0.041	0.533	0.787	1.041
θ°	0°	4°	8°	0°	4°	8°

20.3 P-DIP 20 PIN



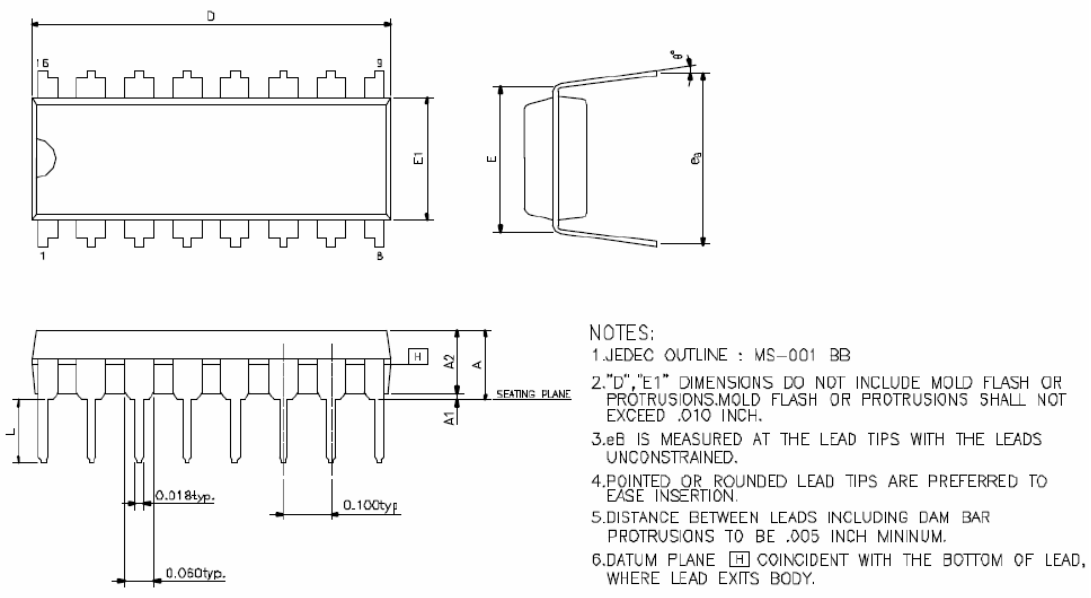
SYMBOLS	MIN	NOR	MAX	MIN	NOR	MAX
	(inch)			(mm)		
A	-	-	0.210	-	-	5.334
A1	0.015	-	-	0.381	-	-
A2	0.125	0.130	0.135	3.175	3.302	3.429
D	0.980	1.030	1.060	24.892	26.162	26.924
E		0.300			7.620	
E1	0.245	0.250	0.255	6.223	6.350	6.477
L	0.115	0.130	0.150	2.921	3.302	3.810
eB	0.335	0.355	0.375	8.509	9.017	9.525
θ°	0°	7°	15°	0°	7°	15°

20.4 SOP 20 PIN



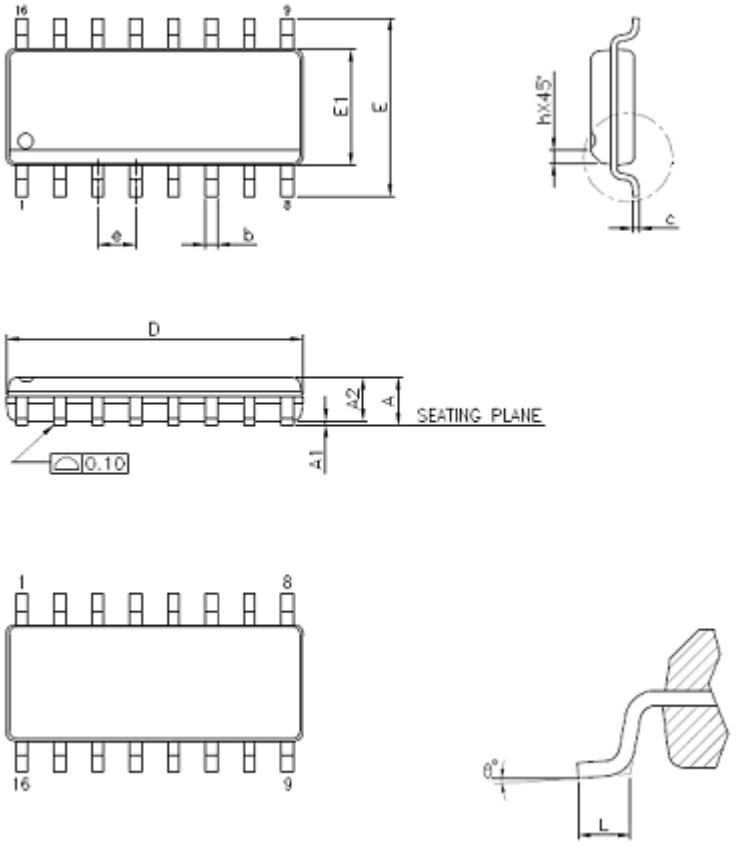
SYMBOLS	MIN	NOR	MAX	MIN	NOR	MAX
	(inch)			(mm)		
A	0.093	0.099	0.104	2.362	2.502	2.642
A1	0.004	0.008	0.012	0.102	0.203	0.305
D	0.496	0.502	0.508	12.598	12.751	12.903
E	0.291	0.295	0.299	7.391	7.493	7.595
H	0.394	0.407	0.419	10.008	10.325	10.643
L	0.016	0.033	0.050	0.406	0.838	1.270
θ°	0°	4°	8°	0°	4°	8°

20.5 P-DIP 16 PIN



SYMBOLS	MIN	NOR	MAX	MIN	NOR	MAX
	(inch)			(mm)		
A	-	-	0.210	-	-	5.334
A1	0.015	-	-	0.381	-	-
A2	0.125	0.130	0.135	3.175	3.302	3.429
D	0.735	0.775	0.775	18.669	19.177	19.685
E	0.300BSC			7.620BSC		
E1	0.245	0.250	0.255	6.223	6.350	6.477
L	0.115	0.130	0.150	2.921	3.302	3.810
eB	0.335	0.355	0.375	8.509	9.017	9.525
θ°	0°	7°	15°	0°	7°	15°

20.6 SOP 16 PIN



SYMBOLS	MIN	NOR	MAX	MIN	NOR	MAX
	(inch)			(mm)		
A	-	-	0.069	-	-	1.75
A1	0.004	-	0.010	0.10	-	0.25
A2	0.049	-		1.25	-	-
b	0.012	-	0.020	0.31	-	0.51
c	0.004	-	0.010	0.10	-	0.25
D	9.90BSC			9.90BSC		
E	6.00BSC			6.00BSC		
E1	3.90BSC			3.90BSC		
e	1.27BSC			1.27BSC		
h	0.016	-	0.050	0.40	-	1.27
L	0.010	-	0.020	0.25	-	0.50
θ°	0°	-	8°	0°	-	8°

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